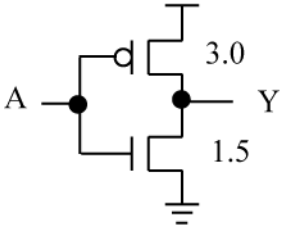
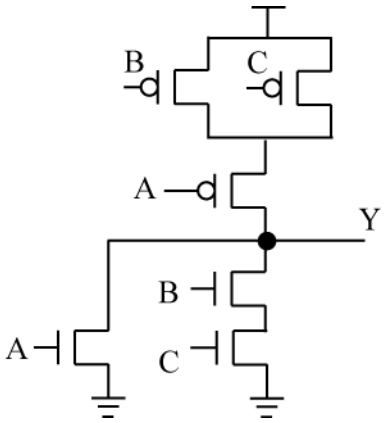
The book is closed book/closed notes, you may use only the provided reference materials. The test is worth 100 pts. You must answer all of the questions from 1-8; you only have to answer 5 questions out of questions 9-16.

1. (8 pts) The 'static_cmos_gate' spectre subcell below implements the complex gate below, but the sizing is incorrect. Modify the spectre description for 'static_cmos_gate' so that the gate is sized correctly to match the inverter template to the left. The value of 'p_mult' is 2.0. The 'invx1' subcell spectre netlist is sized correctly to implement the template inverter.





PMOS sizes = 6.0

A NMOS size = 1.5
B, C NMOS size = 3.0

```
subckt invx1 (a y vddc gndc)
   m2 (y a gndc gndc) n_def ws=1.5 ls=1
   m1 (y a vddc vddc) p_def ws=1.5*p_mult ls=1
ends invx1
```

```
subckt static_cmos_gate (a b c vddc gndc)
   m1 (y a gndc gndc) n_def ws=1 ls=1
   m2 (y b nm2 gndc) n_def ws=1 ls=1
   m3 (nm2 c gndc gndc) n_def ws=1 ls=1
   m4 (y a nm4 vddc) p_def ws=1*p_mult ls=1
   m5 (nm6 b vddc vddc) p_def ws=1*p_mult ls=1
   m6 (nm6 c vddc vddc) p_def ws=1*p_mult ls=1
ends static_cmos_gate
```

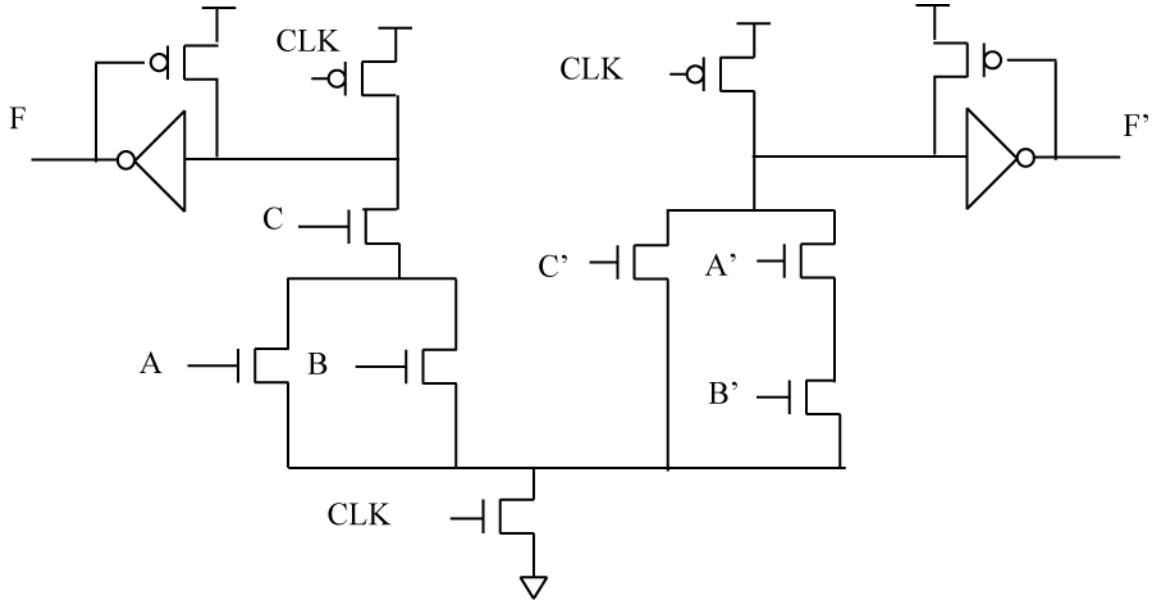
```
subckt static_cmos_gate (a b c vddc gndc)
   m1 (y a gndc gndc) n_def ws=1.5 ls=1
   m2 (y b nm2 gndc) n_def ws=3.0 ls=1
   m3 (nm2 c gndc gndc) n_def ws=3.0 ls=1
   m4 (y a nm4 vddc) p_def ws=3.0*p_mult ls=1
   m5 (nm6 b vddc vddc) p_def ws=3.0*p_mult ls=1
   m6 (nm6 c vddc vddc) p_def ws=3.0*p_mult ls=1
ends static_cmos_gate
```

Note: The PMOS widths are 3.0*p_mult = 3.0*2.0 = 6.0

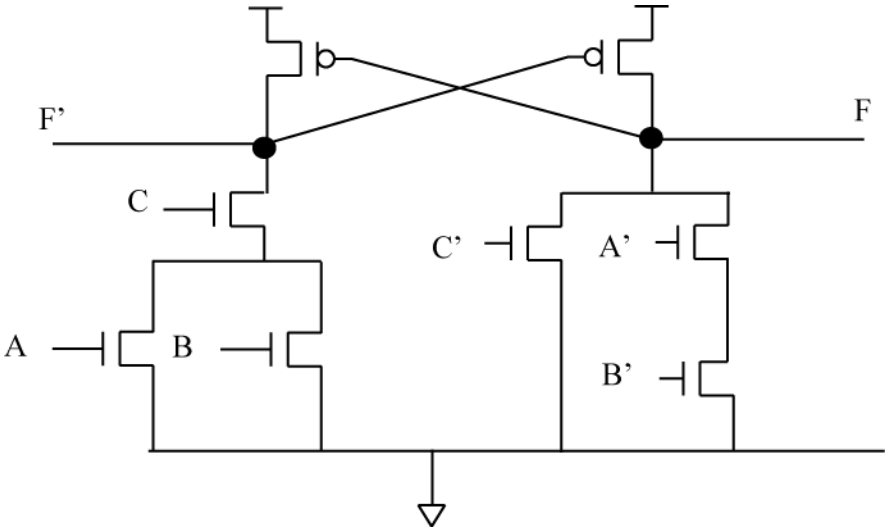
2. (8 pts) Draw a dual rail domino logic gate that implements the logic function

F = (A+B)C

The pulldown trees of F, F’ should share the same evaluation transistor, and the outputs should have **static keeper transistors.**

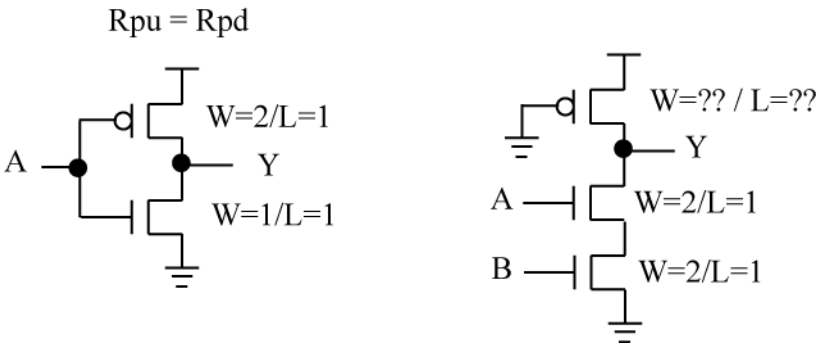


3. (4 pts) Implement the same logic function of problem #1 as a dual-rail DCVSL gate.



4. (10 pts) The template inverter below is sized such that Rpu is equal to Rpd.

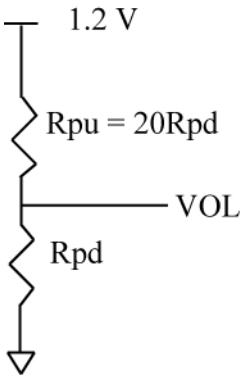
   a. Size the PMOS pullup for the pseudo-NMOS NAND2 gate on the right such that Rpu = 20*Rpd, where Rpd is the same resistance as the transistor template to the left. Assume that transistor resistance varies linearly with width and length (decreases with increasing width, increases with increasing length).
   b. For Vdd = 1.2 V, what is VOL? (the output voltage when both A, B are logic '1', pulling the output to logic 0).



*a. For the inverter on the right, Rpd = Rnmos*Lnmos/Wnmos,*
*Rpu = Rpmos*Lpmos/Wnmos, and are sized such that Rpd = Rpu.*
In the NAND gate, the two NMOS are sized such that Rpd is the same as Rpd of the inverter. So, for the PMOS, we need:
*Rpu new = Rpu old * 20 = Rpmos * (L=1/ W=2) * 20 = Rpmos *(L=10/W=1).*

So, for pullup PMOS, W=1, L = 10.

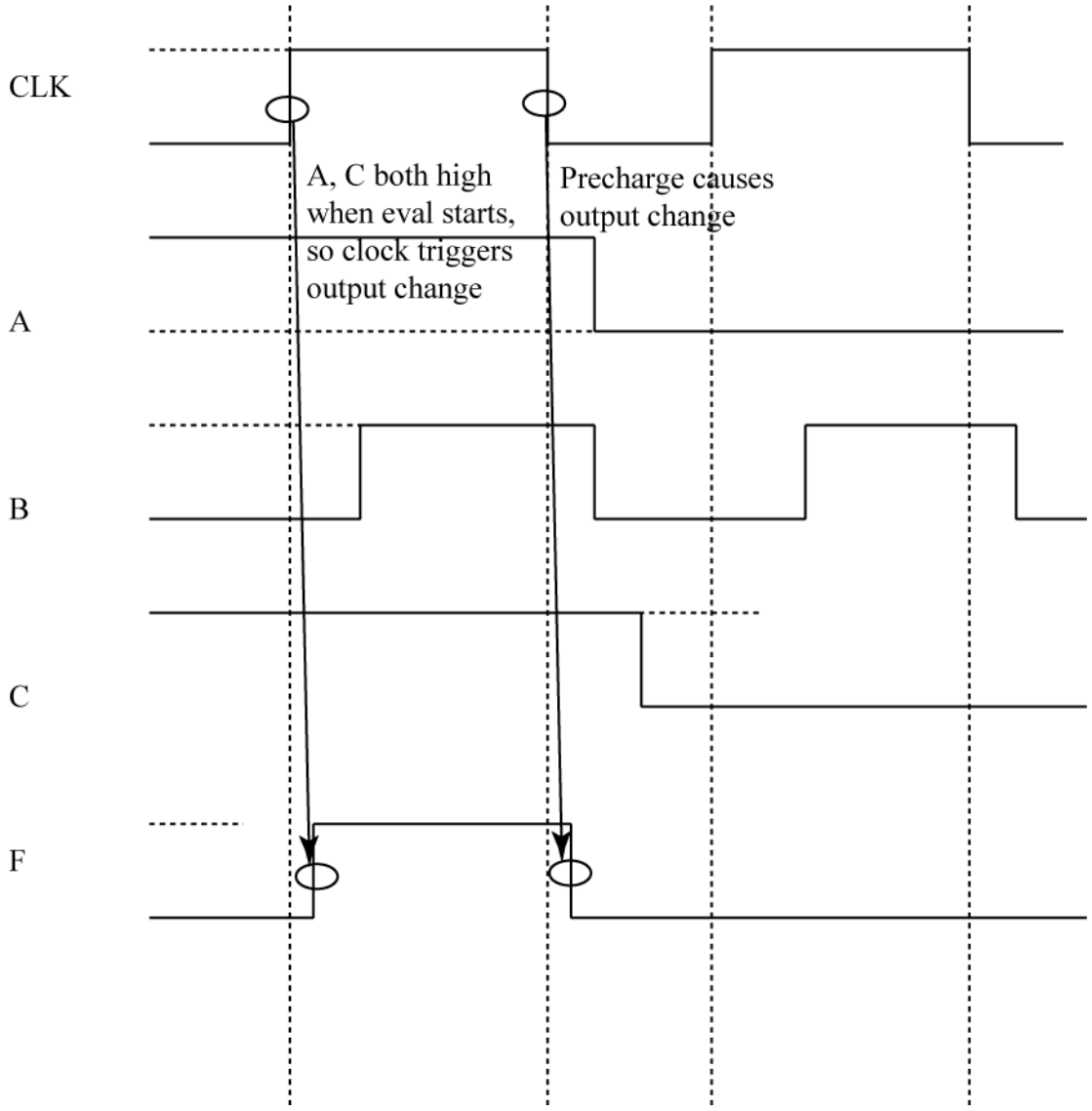
b.



When the NMOS tree is turned on, the device looks like a voltage divider.

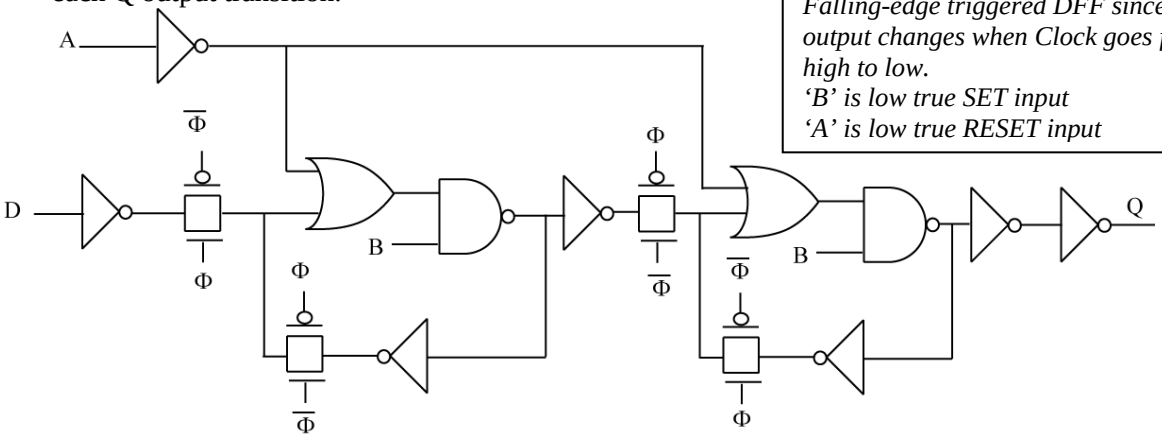
$$VOL = \frac{(Rpd * 1.2\ V)}{(Rpd + 20\ Rpd)} = \frac{1.2\ V}{21} = 0.057\ V$$

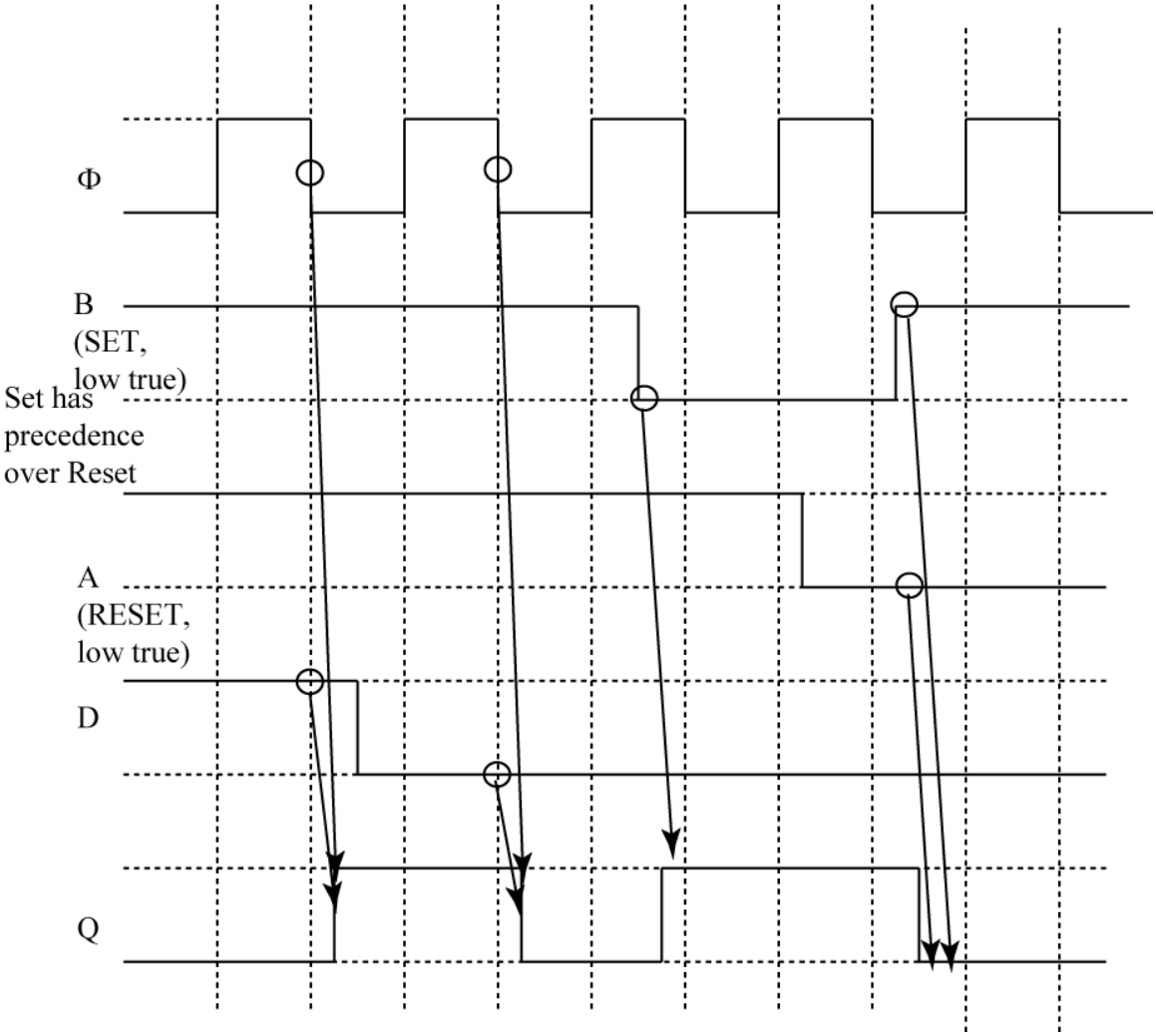
5. (10 pts) Complete the F output waveforms for the dual-rail domino gate of problem #1. For EACH 'F' output transition (low-to-high, or high-to-low), show the input signal transition (CLK, A, B, or C) that causes this transition (draw an arrow from the input transition to the output transition). Assume that the domino logic gate delay is short enough to respond to all input transitions properly.



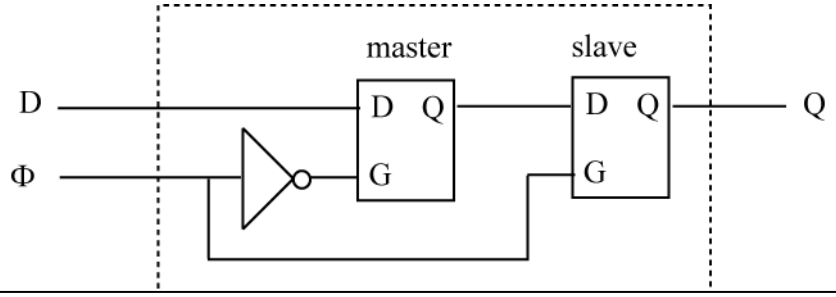
6. (10 pts) Complete the timing diagram for the Q waveform for the storage device and inputs shown below. Draw an arrow from the input signal or signals (clock, D, A, B) that causes each Q output transition.

Falling-edge triggered DFF since Q output changes when Clock goes from high to low.
'B' is low true SET input
'A' is low true RESET input





7. (9 pts) A DFF is built from two transparent-high latches as shown below. Give the equations for Tcq, Tsetup, Thold for the DFF based upon the native Tcq, Tsetup, Thold of the latches, and the Tpd of the inverter.



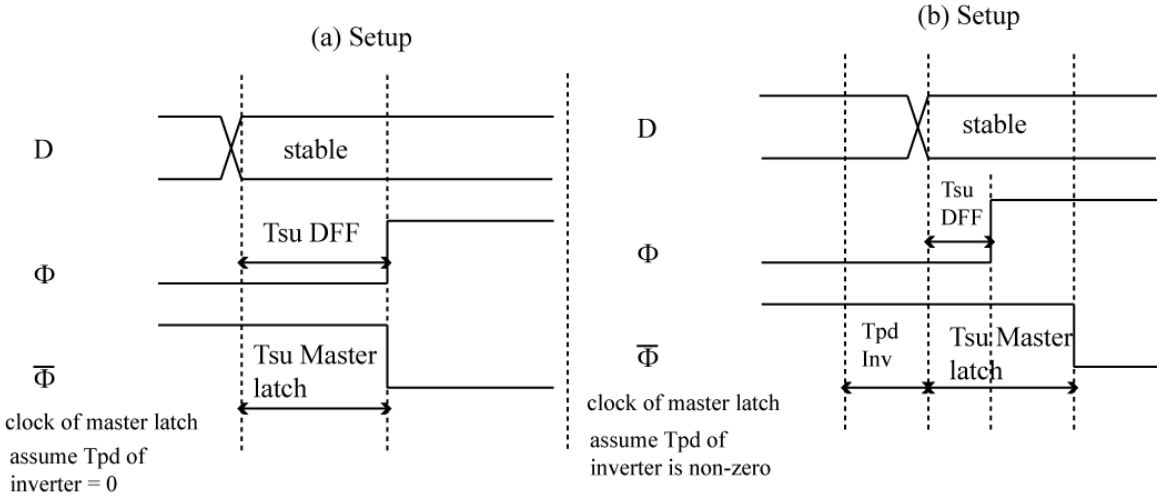
This is a rising edge triggered DFF since the output changes when clock goes from low to high to make the slave transparent

a. Tcq (DFF) = Tcq latch

A rising edge of the clock makes the slave transparent, transferring the Master Q output to the Slave Q output. The clock-to-Q delay of the DFF is just the clock-to-Q delay of the latch.

b. Tsu(DFF) = Tsu latch – Tpd inverter

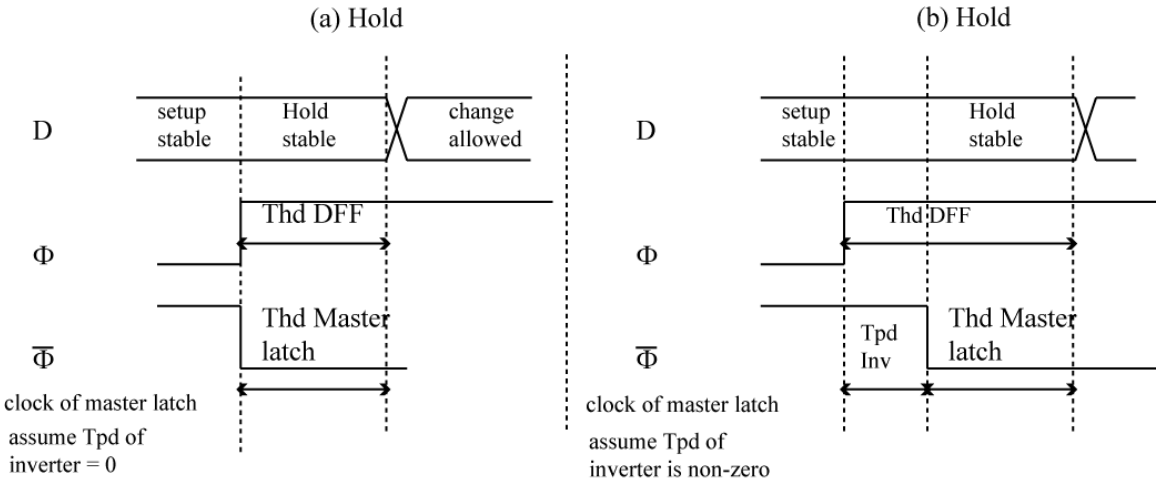
Figure(a) Setup below shows the situation if the inverter if has zero propagation delay; the setup of the DFF (measured from rising edge of the clock) is the setup time of the master latch. Figure (b) Setup below shows what happens if the inverter has non-zero delay; the setup time relative to the DFF clock edge decreases by Tpd, the delay of the inverter, because the clock going to the master latch is delayed by Tpd.
The setup time of the slave latch is no factor at all because when the clock to the slave latch is high, the master latch is closed and no changes are reaching the slave latch.



c. Thd(DFF) = Thd latch + Tpd inverter

Figure(a) Hold below shows the situation if the inverter has zero propagation delay; the hold of the DFF (measured from rising edge of the clock) is the hold time of the master latch. Figure (b) hold below shows what happens if the inverter has non-zero delay; the hold time relative to the DFF clock edge ***increases*** *by Tpd, the delay of the inverter, because the clock going to the master latch is delayed by Tpd.*

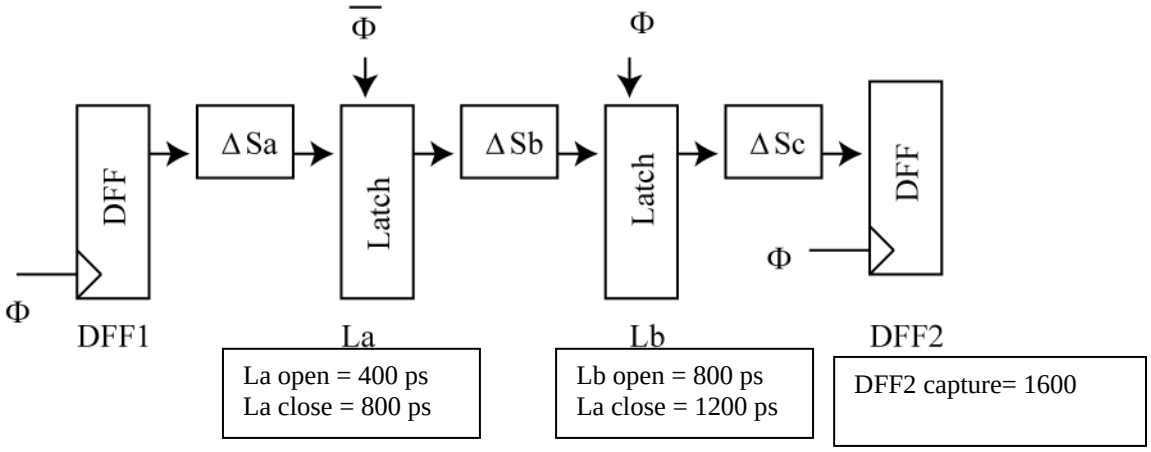
The hold time of the slave latch is not a factor in the hold time of the DFF. However, there is a separate timing constraint that must be satisfied in that the inverter delay plus the master latch Clock-to-Q delay must be greater than the hold time of slave latch. This is commonly true and so is assumed to be true.



8. (16 pts) In the pipeline below, assume Tsetup latch = 20 ps, Tcq latch = Tdq latch = 25 ps, Tcq Dff = 50 ps, Tsetup DFF = 30 ps. The stage delays do not include the latch or DFF delays. Departure time is the time that the latch/DFF output changes.

   ϕ period = 800 ps, ΔSa = 300 ps, ΔSb = 600 ps, ΔSc = 530 ps,

   Define setup time slack as "active clock edge time – setup time – arrival time".



Also assume that ϕ and NOT(ϕ) are perfect inversions of each other without clock skew.

Fill out the following table, show your work

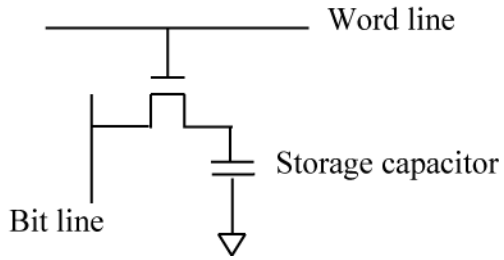
La arrival	DFF1 Tcq + Sa = 300 + 50 = 350 ps
La setup slack	La close – La arrival – Tsetup latch = 800 – 350 – 20 = 430 ps
La departure	Max (La arrival+Tdq latch, La open+Tcq latch) Max(350+25, 400+25) = Max(375, 425) = 425 ps
Lb arrival	La departure + Sb = 425 + 600 = 1025 ps
Lb setup slack	Lb close – Lb arrival – Tsetup latch = 1200 – 1025 – 25 = 155 ps
Lb departure	Max (Lb arrival+Tdq latch, Lb open+Tcq latch) Max(1025+25, 800+25) = Max(1050, 825) = 1050 ps
DFF2 arrival	Lb departure + Sc = 1050 + 530 = 1580 ps
DFF2 setup slack	DFF2 capture – DFF2 arrival – Tsetup DFF = 1600 – 1580 – 30 = -10 ps (setup time violation)

Answer 5 out of the following 7 short answer questions – cross out the TWO questions that you do not want graded. In answering some of the questions, use the symbols Tpd for maximum combinational propagation delay, Tcd for minimum combinational propagation delay (contamination delay), Tcq for maximum DFF clock to q delay, Tccq for minimum DFF clock to q delay (contamination delay), Tsu for DFF setup time, Thd for DFF hold time.

9. (5 pts) Draw a 6-transistor SRAM cell. Label word lines, bit lines.

See notes.

10. (5 pts) Draw a dynamic RAM cell.



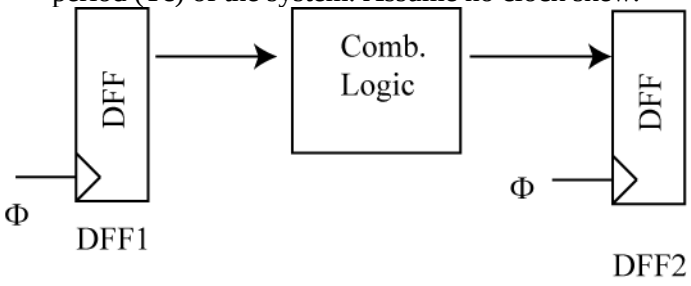
11. (5 pts) For a 1M x 64 bit SRAM, if the bits are arranged in only one square array, how many address bits go to the column decoder? For credit you must show how you arrive at this, don't just write down a guess.

2^{20} x 2^6 = 2^{26} bits, so square array is 2^{13} x 2^{13}. The number of output words from the column decoder are $2^{13}/2^6 = 2^7$, so need 7 address lines for the column decoder.

12. (5 pts) Where are sense amps located in a SRAM and what signals are they connected to?

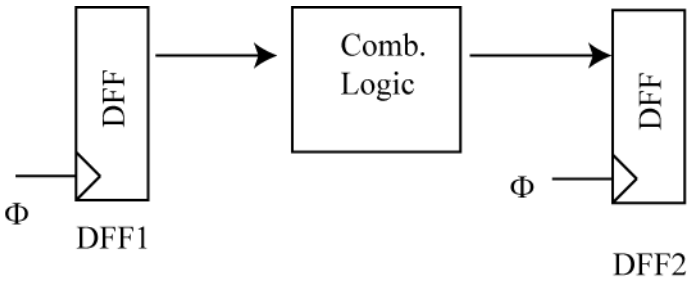
At the bottom of the array, connected to the bit lines.

13. (5 pts) In a system that uses edge-triggered DFFs, give an equation for the maximum clock period (Tc) of the system. Assume no clock skew.



Tc min = Tcq + Tpd + Tsu

14. (5 pts) In a system that uses edge-triggered DFFs, give an equation gives the minimum contamination delay of the combination logic (Tcd) block to avoid a hold time violation on DFF2.



Tcd >= Thd – Tccq (clock to q contamination delay)

15. (5 pts) What is the difference between clock skew and clock delay in a clock distribution network for a digital system? Draw a diagram that illustrates this.

Clock delay is the delay from the clock source to a particular DFF. Typically, a clock distribution network strives to equalize the clock edge arrival times to all DFFs in a particular region by equalizing the delays in the distribution network. However, due to processing variations, the clock buffers and wires used to distribute the clock may have slightly different delays, causing a difference in arrival times. This difference in arrival times is called clock skew.