**ECE 4263**

**Lab-5**

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**Msd153**

1. **Did any stages violate our transition time guidelines**

**after Task 2? Which ones?**

Yes, stage 2 violated the transition guidelines (rise time=492.836 ps > 349 ps (limit)).

1. **In Task 3, were you able to successfully adjust the transistor sizes so that all stages met transition time guidelines? If ‘no’, explain why (a**

**‘no’ answer should be rare, talk to me if you are having problems with this).**

Yes, I was able to successfully adjust the transistor sizes but adjusting the pull-up and pull-down factor

1. **In which task (2 or 3) did you achieve the smallest decoder delay? (results may vary, there is no ‘right’ answer).**

I achieved the smallest decoder delay in task 3 (i.e. 724.7 ps).

1. **How many hours did you spend on this lab?**

I spent around 6-7 hours on this lab. The longest time took to just manipulate the sizes and pull-up factor to get the lowest delay.