ECE 4263

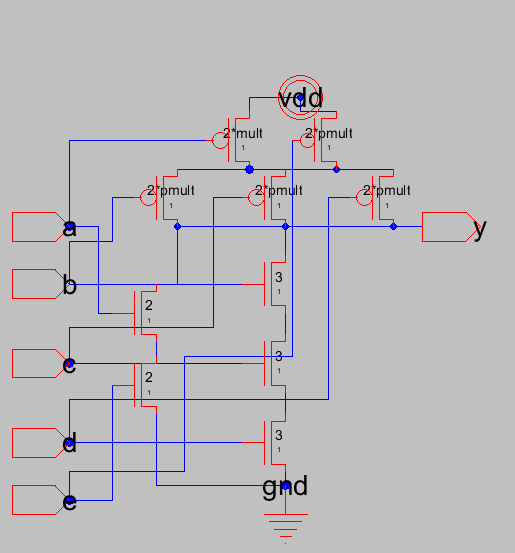
Lab-6(A) Gate Family

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1)Schematics

A) Static\_Cmos



subckt static\_cmos\_gate (a b c d e y vddc gndc)

parameters size=1

m1 (y a net29 gndc) n\_def ws=2\*size ls=1

m2 (net29 e gndc gndc) n\_def ws=2\*size ls=1

m3 (y b net28 gndc) n\_def ws=3\*size ls=1

m4 (net28 c net27 gndc) n\_def ws=3\*size ls=1

m5 (net27 d gndc gndc) n\_def ws=3\*size ls=1

m6 (y b net26 vddc) p\_def ws=2\*p\_mult\*size ls=1

m7 (y c net26 vddc) p\_def ws=2\*p\_mult\*size ls=1

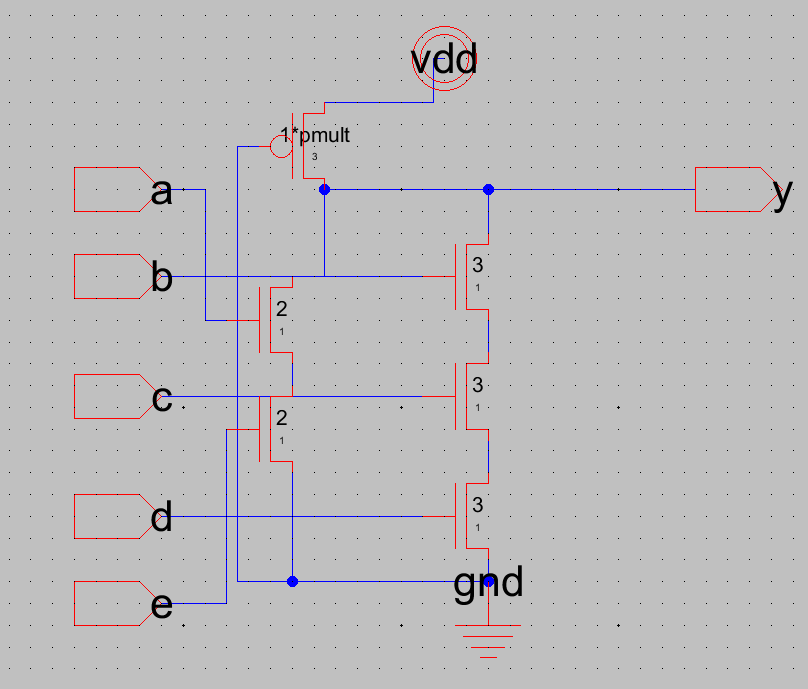
m8 (y d net26 vddc) p\_def ws=2\*p\_mult\*size ls=1

m9 (net26 a vddc vddc) p\_def ws=2\*p\_mult\*size ls=1

m10 (net26 e vddc vddc) p\_def ws=2\*p\_mult\*size ls=1

ends static\_cmos\_gate

B) Pseudo\_nmos



subckt psuedo\_nmos\_gate (a b c d e y vddc gndc)

parameters size=1

m1 (y a net29 gndc) n\_def ws=2\*size ls=1

m2 (net29 e gndc gndc) n\_def ws=2\*size ls=1

m3 (y b net28 gndc) n\_def ws=3\*size ls=1

m4 (net28 c net27 gndc) n\_def ws=3\*size ls=1

m5 (net27 d gndc gndc) n\_def ws=3\*size ls=1

m6 (y gndc vddc vddc) p\_def ws=1\*p\_mult\*size ls=3

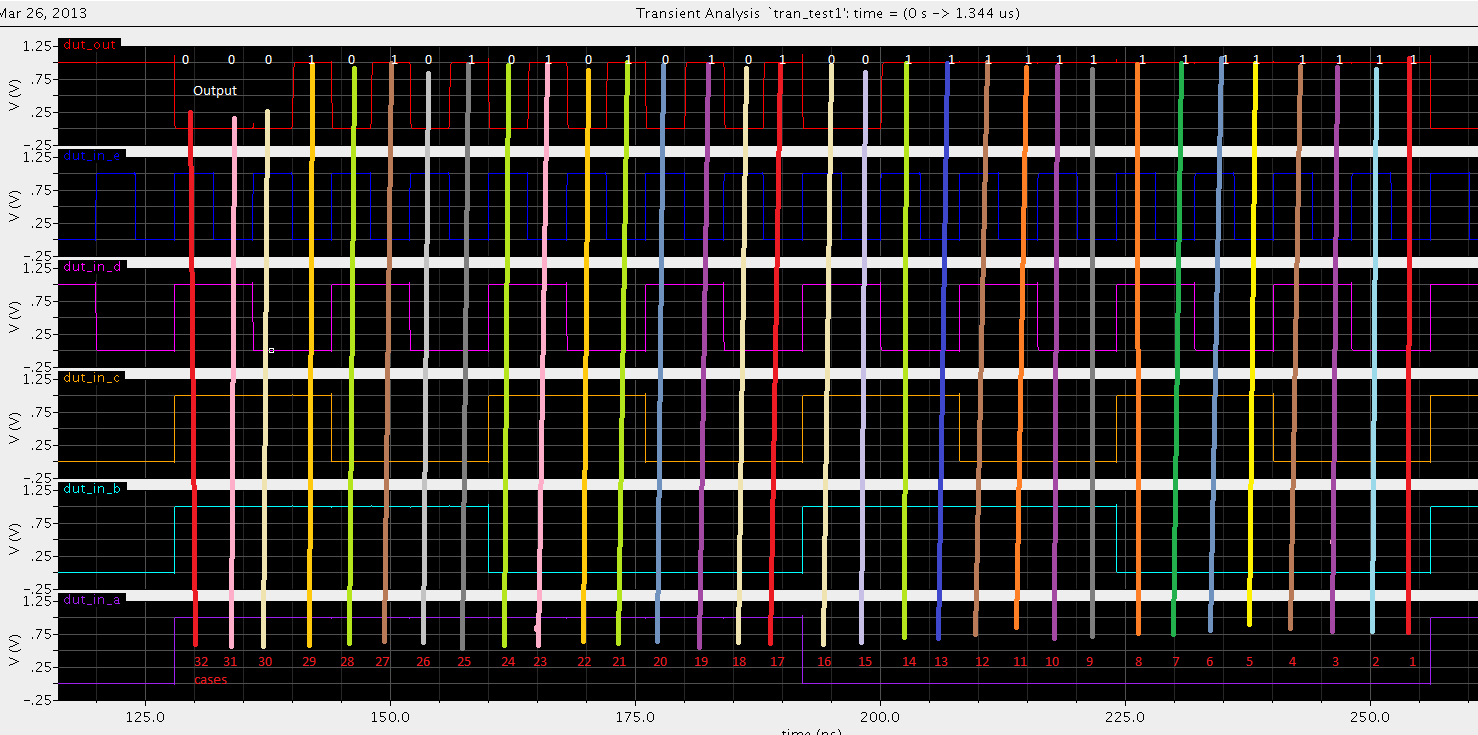
ends psuedo\_nmos\_gate

2) Truth\_table

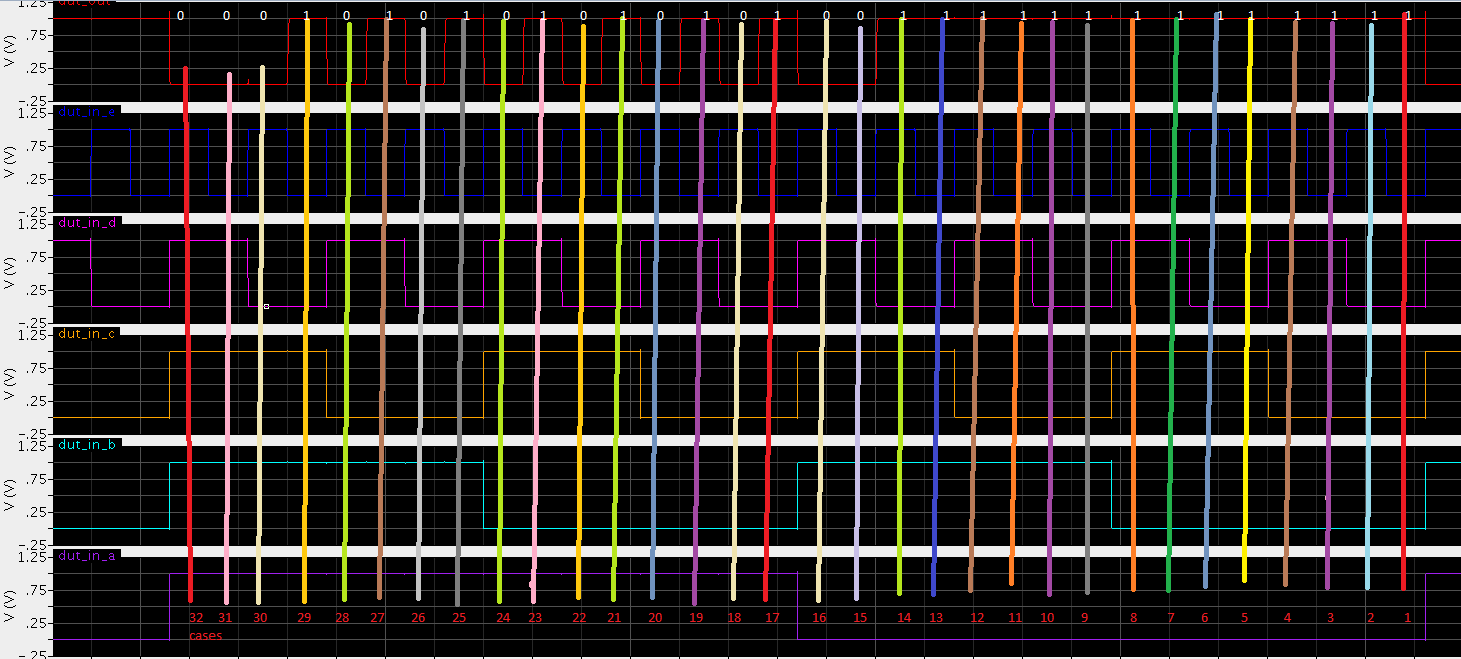
|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Case | A | B | C | D | E | Y=NOT(AE+BCD) |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 0 | 0 | 1 | 1 |
| 3 | 0 | 0 | 0 | 1 | 0 | 1 |
| 4 | 0 | 0 | 0 | 1 | 1 | 1 |
| 5 | 0 | 0 | 1 | 0 | 0 | 1 |
| 6 | 0 | 0 | 1 | 0 | 1 | 1 |
| 7 | 0 | 0 | 1 | 1 | 0 | 1 |
| 8 | 0 | 0 | 1 | 1 | 1 | 1 |
| 9 | 0 | 1 | 0 | 0 | 0 | 1 |
| 10 | 0 | 1 | 0 | 0 | 1 | 1 |
| 11 | 0 | 1 | 0 | 1 | 0 | 1 |
| 12 | 0 | 1 | 0 | 1 | 1 | 1 |
| 13 | 0 | 1 | 1 | 0 | 0 | 1 |
| 14 | 0 | 1 | 1 | 0 | 1 | 1 |
| 15 | 0 | 1 | 1 | 1 | 0 | 0 |
| 16 | 0 | 1 | 1 | 1 | 1 | 0 |
| 17 | 1 | 0 | 0 | 0 | 0 | 1 |
| 18 | 1 | 0 | 0 | 0 | 1 | 0 |
| 19 | 1 | 0 | 0 | 1 | 0 | 1 |
| 20 | 1 | 0 | 0 | 1 | 1 | 0 |
| 21 | 1 | 0 | 1 | 0 | 0 | 1 |
| 22 | 1 | 0 | 1 | 0 | 1 | 0 |
| 23 | 1 | 0 | 1 | 1 | 0 | 1 |
| 24 | 1 | 0 | 1 | 1 | 1 | 0 |
| 25 | 1 | 1 | 0 | 0 | 0 | 1 |
| 26 | 1 | 1 | 0 | 0 | 1 | 0 |
| 27 | 1 | 1 | 0 | 1 | 0 | 1 |
| 28 | 1 | 1 | 0 | 1 | 1 | 0 |
| 29 | 1 | 1 | 1 | 0 | 0 | 1 |
| 30 | 1 | 1 | 1 | 0 | 1 | 0 |
| 31 | 1 | 1 | 1 | 1 | 0 | 0 |
| 32 | 1 | 1 | 1 | 1 | 1 | 0 |

3) waveform

A)Static\_CMOS



B) Psuedo\_NMOS



4) I spent around 19-20 hours on this lab as I had figure out the instructions needed thinking.