ECE 4263

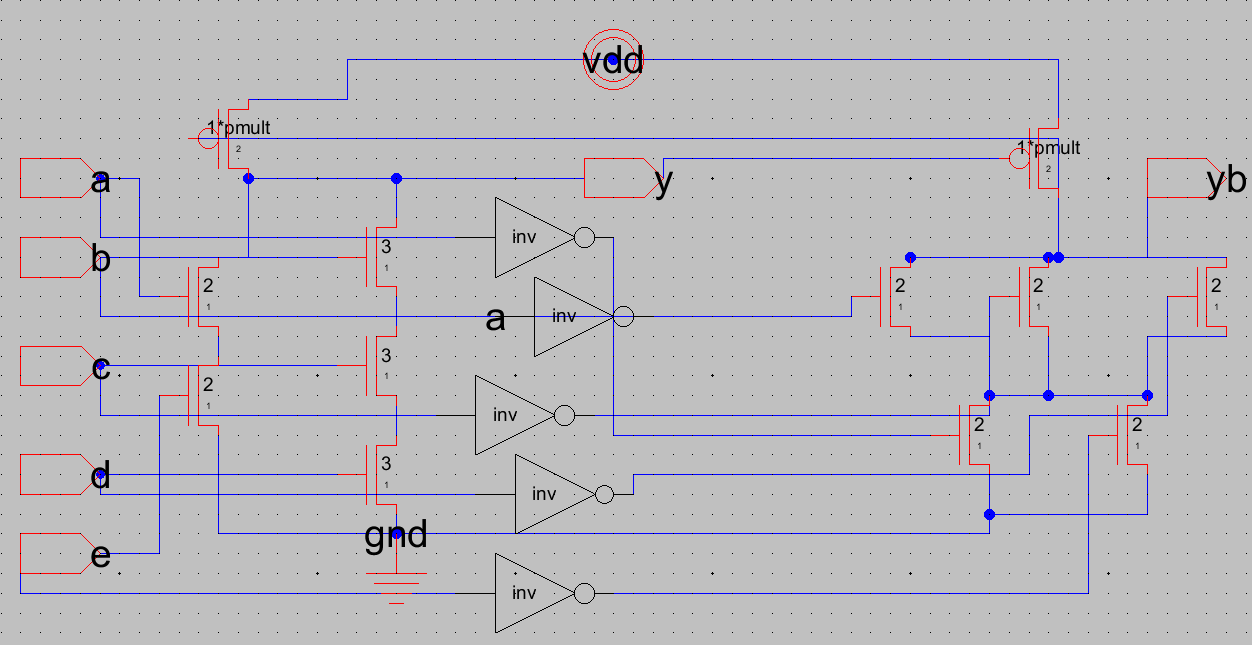
Lab-6(B) Gate Family

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1)Schematics

C) DCVSL



subckt dcvsl\_gate (a b c d e y ab bb cb db eb yb vddc gndc)

parameters size=1

m1 (y a net29 gndc) n\_def ws=2\*size ls=1

m2 (net29 e gndc gndc) n\_def ws=2\*size ls=1

m3 (y b net28 gndc) n\_def ws=3\*size ls=1

m4 (net28 c net27 gndc) n\_def ws=3\*size ls=1

m5 (net27 d gndc gndc) n\_def ws=3\*size ls=1

m6 (y yb vddc vddc) p\_def ws=1\*p\_mult\*size ls=2

m7 (yb bb net26 gndc) n\_def ws=2\*size ls=1

m8 (yb cb net26 gndc) n\_def ws=2\*size ls=1

m9 (yb db net26 gndc) n\_def ws=2\*size ls=1

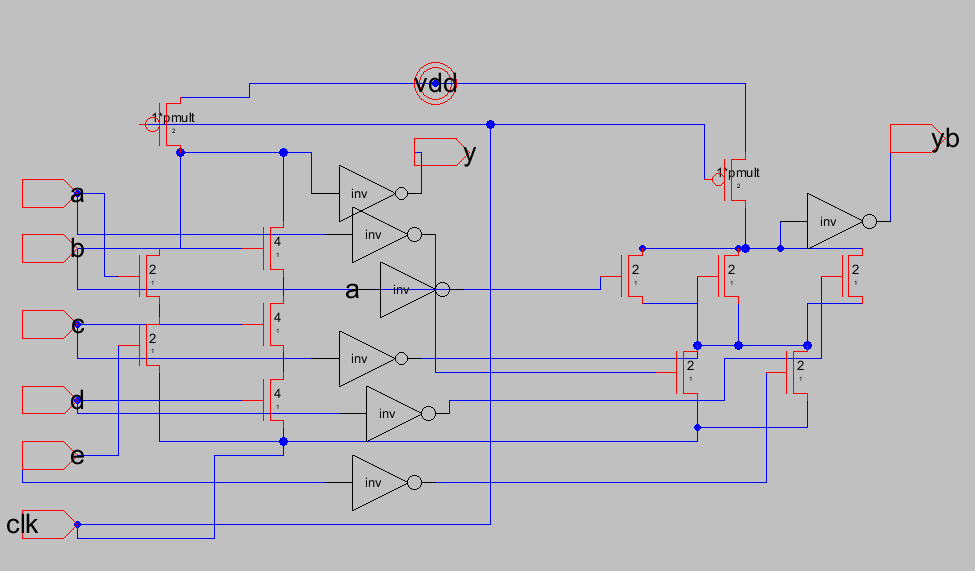
m10 (net26 ab gndc gndc) n\_def ws=2\*size ls=1

m11 (net26 eb gndc gndc) n\_def ws=2\*size ls=1

m12 (yb y vddc vddc) p\_def ws=1\*p\_mult\*size ls=2

ends dcvsl\_gate

D) dual\_rail\_domino



subckt dual\_rail\_domino\_gate (clk a b c d e y ab bb cb db eb yb vddc gndc)

parameters size=1

x1 (net25 y vddc gndc) inv\_gen size=1

m1 (net25 a net29 gndc) n\_def ws=5.35\*size ls=1

m2 (net29 e net24 gndc) n\_def ws=5.35\*size ls=1

m13 (net24 clk gndc gndc) n\_def ws=8\*size ls=1

m3 (net25 b net28 gndc) n\_def ws=8\*size ls=1

m4 (net28 c net27 gndc) n\_def ws=8\*size ls=1

m5 (net27 d net24 gndc) n\_def ws=8\*size ls=1

m6 (net25 clk vddc vddc) p\_def ws=1\*p\_mult\*size ls=1

x2 (net23 yb vddc gndc) inv\_gen size=1

m7 (net23 bb net26 gndc) n\_def ws=5.35\*size ls=1

m8 (net23 cb net26 gndc) n\_def ws=5.35\*size ls=1

m9 (net23 db net26 gndc) n\_def ws=5.35\*size ls=1

m10 (net26 ab net24 gndc) n\_def ws=5.35\*size ls=1

m11 (net26 eb net24 gndc) n\_def ws=5.35\*size ls=1

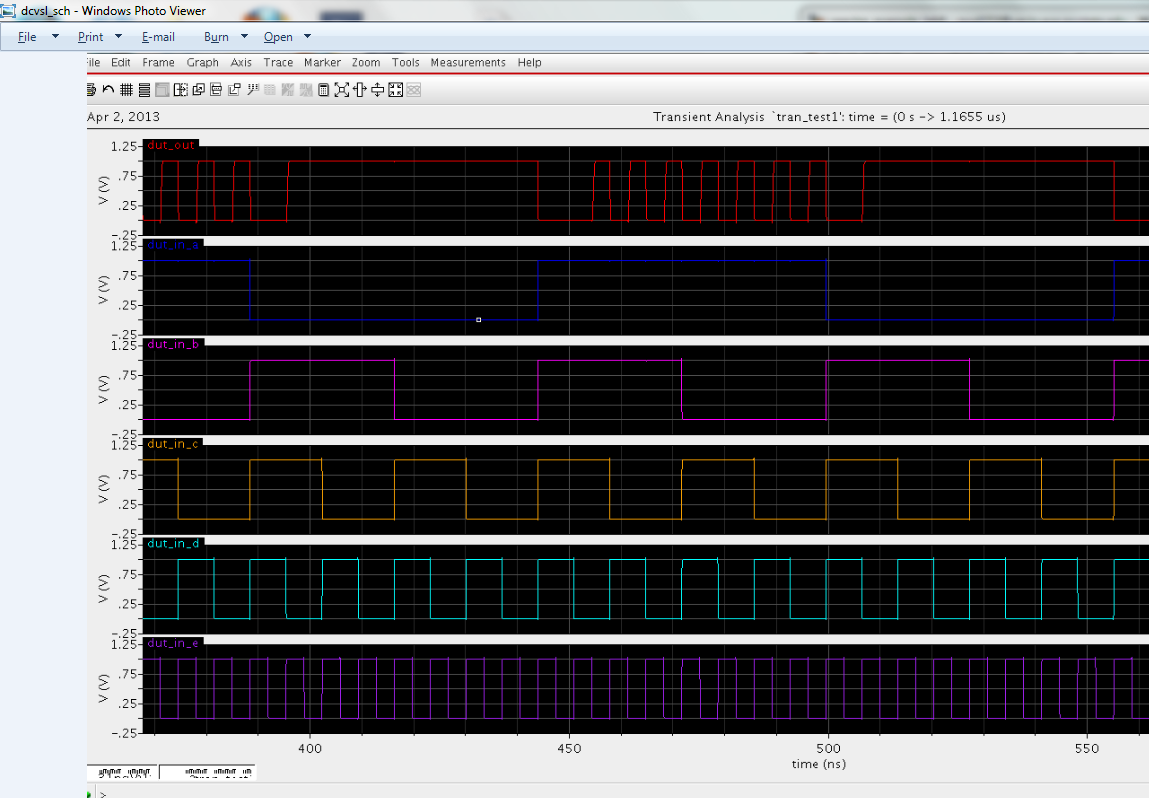
m12 (net23 clk vddc vddc) p\_def ws=1\*p\_mult\*size ls=1

ends dual\_rail\_domino\_gate

2) Truth\_table

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Case | A | B | C | D | E | Y=NOT(AE+BCD) |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 0 | 0 | 1 | 1 |
| 3 | 0 | 0 | 0 | 1 | 0 | 1 |
| 4 | 0 | 0 | 0 | 1 | 1 | 1 |
| 5 | 0 | 0 | 1 | 0 | 0 | 1 |
| 6 | 0 | 0 | 1 | 0 | 1 | 1 |
| 7 | 0 | 0 | 1 | 1 | 0 | 1 |
| 8 | 0 | 0 | 1 | 1 | 1 | 1 |
| 9 | 0 | 1 | 0 | 0 | 0 | 1 |
| 10 | 0 | 1 | 0 | 0 | 1 | 1 |
| 11 | 0 | 1 | 0 | 1 | 0 | 1 |
| 12 | 0 | 1 | 0 | 1 | 1 | 1 |
| 13 | 0 | 1 | 1 | 0 | 0 | 1 |
| 14 | 0 | 1 | 1 | 0 | 1 | 1 |
| 15 | 0 | 1 | 1 | 1 | 0 | 0 |
| 16 | 0 | 1 | 1 | 1 | 1 | 0 |
| 17 | 1 | 0 | 0 | 0 | 0 | 1 |
| 18 | 1 | 0 | 0 | 0 | 1 | 0 |
| 19 | 1 | 0 | 0 | 1 | 0 | 1 |
| 20 | 1 | 0 | 0 | 1 | 1 | 0 |
| 21 | 1 | 0 | 1 | 0 | 0 | 1 |
| 22 | 1 | 0 | 1 | 0 | 1 | 0 |
| 23 | 1 | 0 | 1 | 1 | 0 | 1 |
| 24 | 1 | 0 | 1 | 1 | 1 | 0 |
| 25 | 1 | 1 | 0 | 0 | 0 | 1 |
| 26 | 1 | 1 | 0 | 0 | 1 | 0 |
| 27 | 1 | 1 | 0 | 1 | 0 | 1 |
| 28 | 1 | 1 | 0 | 1 | 1 | 0 |
| 29 | 1 | 1 | 1 | 0 | 0 | 1 |
| 30 | 1 | 1 | 1 | 0 | 1 | 0 |
| 31 | 1 | 1 | 1 | 1 | 0 | 0 |
| 32 | 1 | 1 | 1 | 1 | 1 | 0 |

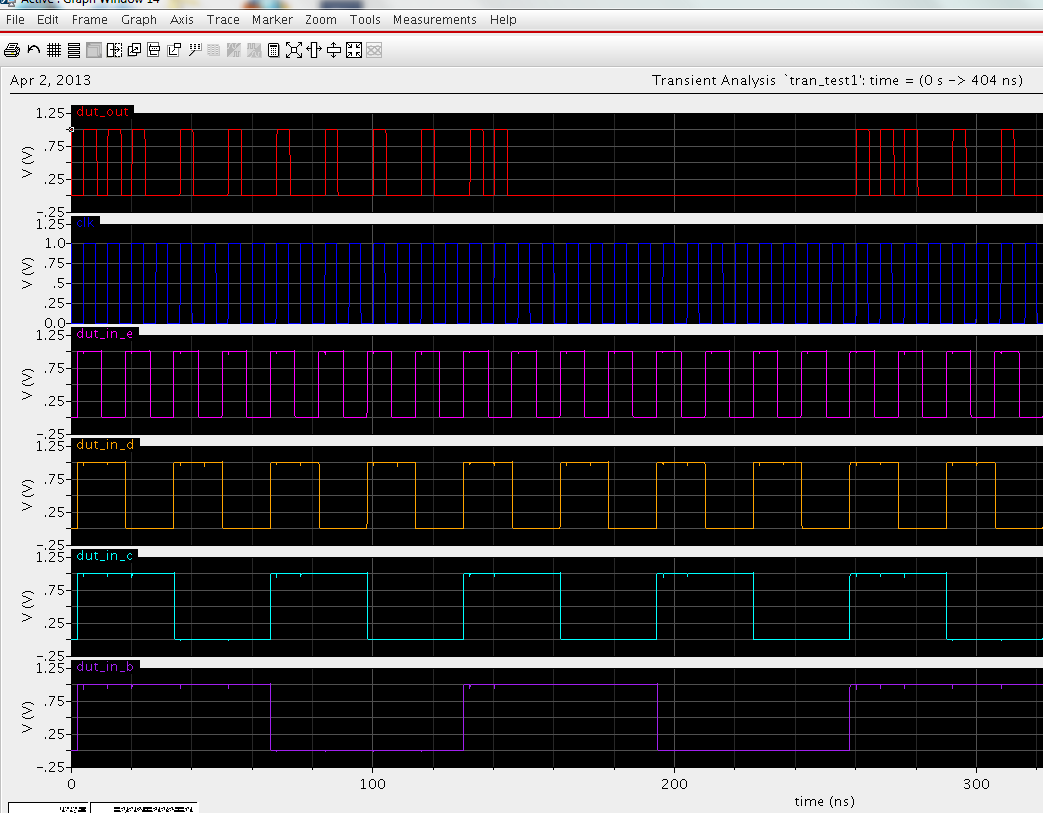
2) Waveforms

C) DCVSL

0 0 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1

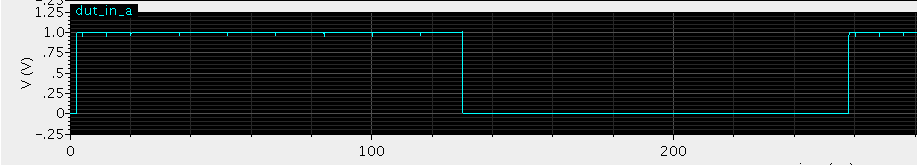
32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

D) Dual rail domino



Transition from Low to high during eval

1 1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0



32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

4) ) I spent around 19-20 hours on this lab.