IV. DELAY ANALYSIS

We have found the total propagation delays of our circuit to verify the operation. For 2GHz frequency of operation, the time period of the clock is 500ps thus the total delay after which each output of the counter is.e. Q3,Q2,Q1,Q0 that are coming must have propagation delays lesser than 0.5 ns or 500 ps. To verify the same we found the propagation delay at each stage and of each component. The detailed analysis for which is presented below:

The propagation delay of each stage is =
$T_{setup} + T_{combinational} + T_{cq,max}$ where,

Tpd of AND found for the worst case is 28.4 ps
Tpd of XOR for the worst case is 29.18 ps

First we'll show the calculation of the combinational path delay of each stage
For Q0 => $(Tpd)_{XOR}$
For Q1 => $(Tpd)_{AND} + (Tpd)_{XOR}$
For Q2 => $2x(Tpd)_{AND} + (Tpd)_{XOR}$
For Q3 => $3x(Tpd)_{AND} + (Tpd)_{XOR}$

Clearly we can see that the combinational path delay for the Q3 is highest, to accommodate the time period we must consider the maximum of all thus $(T_{combinational})_{max}$ will be 3x28.4 + 29.18 = 114.38 ps.

The $T_{cq,max}$ we have calculated is equal to 114.64ps. We are showing the calculation of T_{cq} below in the waveform:

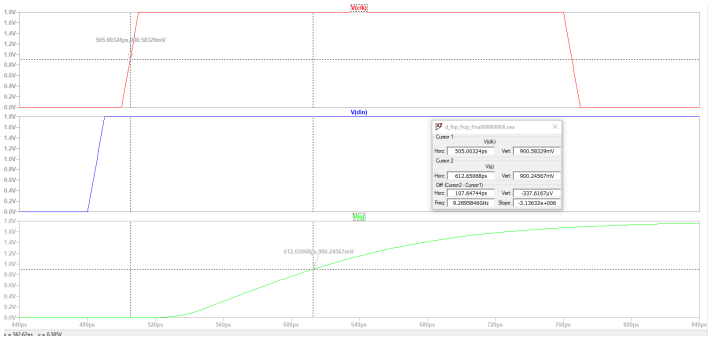

Figure 29: Output waveform observed for measuring clock-Q delay during the rising of the input (107.04ps).

Figure 30: Output waveform observed for measuring clock-Q delay during the falling of the input (121.35ps).

The T_{cq} found is the worst case delay found when the data input is set for the setup time. The average of both output falling from high to low and out rising from low to high is considered while the calculation of $T_{cq,max}$.
From this calculation $T_{cq,max}$ is found to be 114.64 ps.
Similarly the setup time for the D flip flop is calculated as follows, we are depicting this through the waveforms:

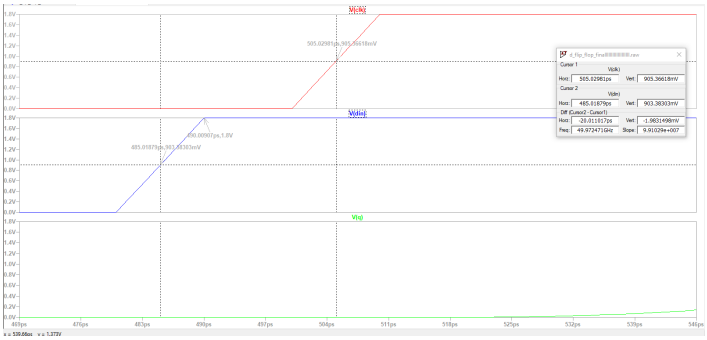

Figure 31: Output waveform observed for measuring setup-time during the rising of the input (20ps).

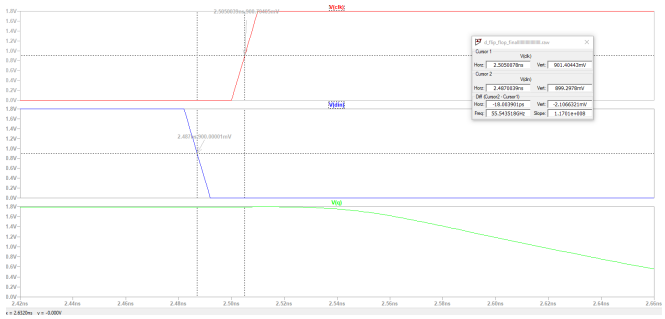

Figure 32: Output waveform observed for measuring setup-time during the falling of the input (18ps).

T_{setup} is found by giving the delays to the data input and observing for which maximum delay the output is missing the clock pulse. We can fix the data input at that delay duration and find the setup time by measuring the 50% levels of Data input and the 50% levels of the clock. The values obtained are 20 ps for the rising input and 18 ps for the falling input, average of which can be taken as 19 ps. Thus the T_{setup} is 19 ps.
Now so far we have all the values to calculate delay for each output, we can perform the final calculation:

Delay of Q0 = $T_{setup} + T_{combinational} + T_{cq,max}$ = 19 + 29.18 + 114.64 = 162.82 ps
Delay of Q1 = $T_{setup} + T_{combinational} + T_{cq,max}$ = 19 + 29.18 + 28.4 + 114.64 = 191.22 ps
Delay of Q2 = $T_{setup} + T_{combinational} + T_{cq,max}$ = 19 + 29.18 + 2x(28.4) + 114.64 = 219.62 ps
Delay of Q3 = $T_{setup} + T_{combinational} + T_{cq,max}$ = 19 + 29.18 + 3x(28.4) + 114.64 = 248.02 ps

As explained earlier, it can be seen that the Q3 is possessing the highest delay. The maximum of all these must be the propagation delay of our counter circuit i.e. 248.02 ps which is far lesser then the 500 ps time period of the clock pulse provided. Hence the circuit operates satisfactorily which is evident from the waveforms.
To verify these results from LTspice we changed the clock period to as minimum as near to the propagation delay of output Q3 i.e. 250 ps and found following waveform:

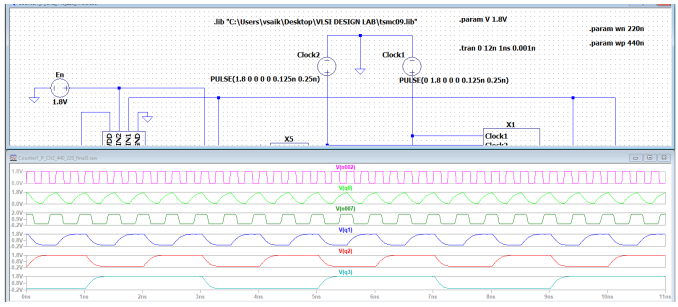

Figure 33: Above observation depicts that the counter is operating correctly at clock time period of (250ps).

We can see that the waveform are just stable, further reducing the time period will distort the waveform of Q3 as seen below:

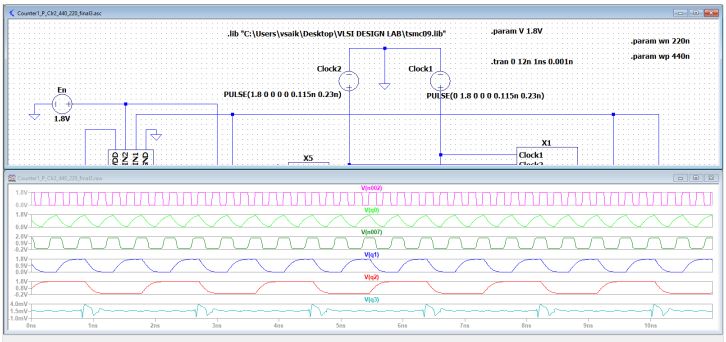

Figure 34: Above observation depicts that the counter output Q3 is distorted at clock time period of (230ps).

The waveforms for Q2,Q1 and Q0 are intact because the clock period still can accommodate the delays for Q2, Q1 and Q0. If we reduce the time period lower than the propagation delay of Q0 i.e. 162.82 ps all the waveforms will get distorted which proves and verifies our calculations for delays. Finally by these calculations we can say this design is working satisfactorily at 2GHz and can even work on frequencies higher than 2 GHz.