Release 14.7 - xst P.20131013 (nt64)

--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.15 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.15 secs

--> Reading design: read_control_top.prj

TABLE OF CONTENTS

===
*   Synthesis Options Summary   *
===
---- Source Parameters
Input File Name   : "read_control_top.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name   : "read_control_top"
Output Format   : NGC
Target Device   : xc6slx9-3-tqg144

---- Source Options
Top Module Name   : read_control_top
Automatic FSM Extraction   : YES
FSM Encoding Algorithm   : Auto
Safe Implementation   : No
FSM Style   : LUT
RAM Extraction   : Yes
RAM Style   : Auto
ROM Extraction   : Yes
Shift Register Extraction   : YES
ROM Style   : Auto

```
Resource Sharing                    : YES
Asynchronous To Synchronous         : NO
Shift Register Minimum Size         : 2
Use DSP Block                       : Auto
Automatic Register Balancing        : No

---- Target Options
LUT Combining                       : Auto
Reduce Control Sets                 : Auto
Add IO Buffers                      : YES
Global Maximum Fanout               : 100000
Add Generic Clock Buffer(BUFG)      : 16
Register Duplication                : YES
Optimize Instantiated Primitives    : NO
Use Clock Enable                    : Auto
Use Synchronous Set                 : Auto
Use Synchronous Reset               : Auto
Pack IO Registers into IOBs         : Auto
Equivalent register Removal         : YES

---- General Options
Optimization Goal                   : Speed
Optimization Effort                 : 1
Power Reduction                     : NO
Keep Hierarchy                      : No
Netlist Hierarchy                   : As_Optimized
RTL Output                          : Yes
Global Optimization                 : AllClockNets
Read Cores                          : YES
Write Timing Constraints            : NO
Cross Clock Analysis                : NO
Hierarchy Separator                 : /
Bus Delimiter                       : <>
Case Specifier                      : Maintain
Slice Utilization Ratio             : 100
BRAM Utilization Ratio              : 100
DSP48 Utilization Ratio             : 100
Auto BRAM Packing                   : NO
Slice Utilization Ratio Delta       : 5

=========================================================================


=========================================================================
*                           HDL Parsing                                 *
=========================================================================
Analyzing Verilog file "G:\FIFO - VLSI Project\RTL
Design\read_control_top_rev_1\binary_up_counter.v" into library work
Parsing module <binary_up_counter>.
Analyzing Verilog file "G:\FIFO - VLSI Project\RTL
Design\read_control_top_rev_1\read_control_top.v" into library work
Parsing module <read_control_top>.

=========================================================================
*                            HDL Elaboration                            *
=========================================================================

Elaborating module <read_control_top>.

Elaborating module <binary_up_counter>.
```

```
=========================================================================
*                            HDL Synthesis                              *
=========================================================================

Synthesizing Unit <read_control_top>.
    Related source file is "G:\FIFO - VLSI Project\RTL
Design\read_control_top_rev_1\read_control_top.v".
        a_length = 3
    Summary:
        no macro.
Unit <read_control_top> synthesized.

Synthesizing Unit <binary_up_counter>.
    Related source file is "G:\FIFO - VLSI Project\RTL
Design\read_control_top_rev_1\binary_up_counter.v".
        a_length = 3
    Found 4-bit register for signal <b_count_ptr>.
    Found 4-bit adder for signal <b_count_ptr[3]_GND_2_o_add_1_OUT> created at line 35.
    Summary:
        inferred   1 Adder/Subtractor(s).
        inferred   4 D-type flip-flop(s).
Unit <binary_up_counter> synthesized.

=========================================================================
HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                                   : 1
 4-bit adder                                           : 1
# Registers                                            : 1
 4-bit register                                        : 1

=========================================================================

=========================================================================
*                        Advanced HDL Synthesis                         *
=========================================================================


Synthesizing (advanced) Unit <binary_up_counter>.
The following registers are absorbed into counter <b_count_ptr>: 1 register on signal
<b_count_ptr>.
Unit <binary_up_counter> synthesized (advanced).

=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Counters                                             : 1
 4-bit up counter                                      : 1

=========================================================================

=========================================================================
*                          Low Level Synthesis                          *
=========================================================================

Optimizing unit <read_control_top> ...

Mapping all equations...
Building and optimizing final netlist ...
```

```
Found area constraint ratio of 100 (+ 5) on block read_control_top, actual ratio is 0.

Final Macro Processing ...

=========================================================================
Final Register Report

Macro Statistics
# Registers                                          : 4
 Flip-Flops                                          : 4

=========================================================================

=========================================================================
*                            Partition Report                           *
=========================================================================

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

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=========================================================================
*                             Design Summary                            *
=========================================================================

Top Level Output File Name         : read_control_top.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 6
#      INV                         : 3
#      LUT2                        : 1
#      LUT3                        : 1
#      LUT4                        : 1
# FlipFlops/Latches                : 4
#      FDCE                        : 4
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 10
#      IBUF                        : 2
#      OBUF                        : 8

Device utilization summary:
---------------------------

Selected Device : 6slx9tqg144-3


Slice Logic Utilization:
 Number of Slice Registers:              4  out of  11440     0%
 Number of Slice LUTs:                   6  out of   5720     0%
    Number used as Logic:                6  out of   5720     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    10
   Number with an unused Flip Flop:      6  out of     10    60%
   Number with an unused LUT:            4  out of     10    40%
   Number of fully used LUT-FF pairs:    0  out of     10     0%
```

```
   Number of unique control sets:         1

IO Utilization:
 Number of IOs:                          11
 Number of bonded IOBs:                  11  out of    102    10%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:                1  out of     16     6%

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Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

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=========================================================================
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
rd_clk                             | BUFGP                  | 4     |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 2.078ns (Maximum Frequency: 481.325MHz)
   Minimum input arrival time before clock: 3.119ns
   Maximum output required time after clock: 3.762ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'rd_clk'
  Clock period: 2.078ns (frequency: 481.325MHz)
  Total number of paths / destination ports: 10 / 4
-------------------------------------------------------------------------
Delay:               2.078ns (Levels of Logic = 1)
  Source:            i/b_count_ptr_0 (FF)
  Destination:       i/b_count_ptr_0 (FF)
  Source Clock:      rd_clk rising
  Destination Clock: rd_clk rising
```

```
  Data Path: i/b_count_ptr_0 to i/b_count_ptr_0
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDCE:C->Q             6   0.447   0.744  i/b_count_ptr_0 (i/b_count_ptr_0)
     INV:I->O              1   0.206   0.579  i/Mcount_b_count_ptr_xor<0>11_INV_0
(Result<0>)
     FDCE:D                    0.102          i/b_count_ptr_0
    ----------------------------------------
    Total                      2.078ns (0.755ns logic, 1.323ns route)
                                       (36.3% logic, 63.7% route)

==============================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'rd_clk'
  Total number of paths / destination ports: 8 / 8
------------------------------------------------------------------------------
Offset:              3.119ns (Levels of Logic = 2)
  Source:            reset_n (PAD)
  Destination:       i/b_count_ptr_0 (FF)
  Destination Clock: rd_clk rising

  Data Path: reset_n to i/b_count_ptr_0
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             1   1.222   0.579  reset_n_IBUF (reset_n_IBUF)
     INV:I->O              4   0.206   0.683  reset_n_inv1_INV_0 (reset_n_inv)
     FDCE:CLR                  0.430          i/b_count_ptr_0
    ----------------------------------------
    Total                      3.119ns (1.858ns logic, 1.261ns route)
                                       (59.6% logic, 40.4% route)

==============================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'rd_clk'
  Total number of paths / destination ports: 8 / 8
------------------------------------------------------------------------------
Offset:              3.762ns (Levels of Logic = 1)
  Source:            i/b_count_ptr_0 (FF)
  Destination:       b_rd_ptr<0> (PAD)
  Source Clock:      rd_clk rising

  Data Path: i/b_count_ptr_0 to b_rd_ptr<0>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDCE:C->Q             6   0.447   0.744  i/b_count_ptr_0 (i/b_count_ptr_0)
     OBUF:I->O                 2.571          b_rd_ptr_0_OBUF (b_rd_ptr<0>)
    ----------------------------------------
    Total                      3.762ns (3.018ns logic, 0.744ns route)
                                       (80.2% logic, 19.8% route)

==============================================================================

Cross Clock Domains Report:
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Clock to Setup on destination clock rd_clk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
```

```
rd_clk          |    2.078|         |         |         |
----------------+---------+---------+---------+---------+

================================================================================


Total REAL time to Xst completion: 7.00 secs
Total CPU time to Xst completion: 6.12 secs

-->

Total memory usage is 4522784 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    0 (   0 filtered)
Number of infos    :    0 (   0 filtered)
```