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Release 14.7 par P.20131013 (nt64)
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ADHRIT::  Thu Oct 10 14:51:08 2019

par -w -intstyle ise -ol high -t 1 fifo_top_1_map.ncd fifo_top_1.ncd
fifo_top_1.pcf


Constraints file: fifo_top_1.pcf.
Loading device for application Rf_Device from file '3s500e.nph' in environment
C:\Xilinx\14.7\ISE_DS\ISE\.
   "fifo_top_1" is an NCD, version 3.2, device xc3s500e, package fg320, speed -5

Initializing temperature to 85.000 Celsius. (default - Range: -40.000 to 100.000 Celsius)
Initializing voltage to 1.140 Volts. (default - Range: 1.140 to 1.320 Volts)

INFO:Par:282 - No user timing constraints were detected or you have set the option to
ignore timing constraints ("par
   -x"). Place and Route will run in "Performance Evaluation Mode" to automatically
improve the performance of all
   internal clocks in this design. Because there are not defined timing requirements, a
timing score will not be
   reported in the PAR report in this mode. The PAR timing summary will list the
performance achieved for each clock.
   Note: For the fastest runtime, set the effort level to "std".  For best performance,
set the effort level to "high".

Device speed data version:  "PRODUCTION 1.27 2013-10-13".


Design Summary Report:

 Number of External IOBs                          25 out of 232    10%

   Number of External Input IOBs                 13

      Number of External Input IBUFs             13

   Number of External Output IOBs                12

      Number of External Output IOBs             12

   Number of External Bidir IOBs                  0


   Number of BUFGMUXs                        2 out of 24      8%
   Number of Slices                         68 out of 4656    1%
      Number of SLICEMs                      8 out of 2328    1%



Overall effort level (-ol):   High
Placer effort level (-pl):    High
Placer cost table entry (-t): 1
Router effort level (-rl):    High

Starting initial Timing Analysis.  REAL time: 4 secs
Finished initial Timing Analysis.  REAL time: 4 secs
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Starting Placer
Total REAL time at the beginning of Placer: 4 secs
Total CPU  time at the beginning of Placer: 1 secs

Phase 1.1  Initial Placement Analysis
Phase 1.1  Initial Placement Analysis (Checksum:1176) REAL time: 15 secs

Phase 2.7  Design Feasibility Check
Phase 2.7  Design Feasibility Check (Checksum:1176) REAL time: 15 secs

Phase 3.31  Local Placement Optimization
Phase 3.31  Local Placement Optimization (Checksum:1176) REAL time: 15 secs

Phase 4.2  Initial Clock and IO Placement
...........
Phase 4.2  Initial Clock and IO Placement (Checksum:b3b4b011) REAL time: 17 secs

Phase 5.30  Global Clock Region Assignment
Phase 5.30  Global Clock Region Assignment (Checksum:b3b4b011) REAL time: 17 secs

Phase 6.36  Local Placement Optimization
Phase 6.36  Local Placement Optimization (Checksum:b3b4b011) REAL time: 17 secs

Phase 7.3  Local Placement Optimization
..........
Phase 7.3  Local Placement Optimization (Checksum:5acd653f) REAL time: 17 secs

Phase 8.5  Local Placement Optimization
Phase 8.5  Local Placement Optimization (Checksum:5acd653f) REAL time: 17 secs

Phase 9.8  Global Placement
..............
Phase 9.8  Global Placement (Checksum:b0b63344) REAL time: 17 secs

Phase 10.5  Local Placement Optimization
Phase 10.5  Local Placement Optimization (Checksum:b0b63344) REAL time: 17 secs

Phase 11.18  Placement Optimization
Phase 11.18  Placement Optimization (Checksum:353d421d) REAL time: 17 secs

Phase 12.5  Local Placement Optimization
Phase 12.5  Local Placement Optimization (Checksum:353d421d) REAL time: 17 secs

Total REAL time to Placer completion: 17 secs
Total CPU  time to Placer completion: 3 secs
Writing design to file fifo_top_1.ncd



Starting Router


Phase  1  : 538 unrouted;      REAL time: 20 secs

Phase  2  : 487 unrouted;      REAL time: 20 secs

Phase  3  : 92 unrouted;      REAL time: 21 secs

Phase  4  : 115 unrouted; (Par is working to improve performance)     REAL time: 21 secs

Phase  5  : 0 unrouted; (Par is working to improve performance)     REAL time: 21 secs
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Updating file: fifo_top_1.ncd with current fully routed design.

Phase  6  : 0 unrouted; (Par is working to improve performance)     REAL time: 22 secs

Phase  7  : 0 unrouted; (Par is working to improve performance)     REAL time: 24 secs

Updating file: fifo_top_1.ncd with current fully routed design.

Phase  8  : 0 unrouted; (Par is working to improve performance)     REAL time: 26 secs

Phase  9  : 0 unrouted; (Par is working to improve performance)     REAL time: 26 secs

Phase 10  : 0 unrouted; (Par is working to improve performance)     REAL time: 26 secs

Phase 11  : 0 unrouted; (Par is working to improve performance)     REAL time: 26 secs

Phase 12  : 0 unrouted; (Par is working to improve performance)     REAL time: 26 secs

Total REAL time to Router completion: 26 secs
Total CPU time to Router completion: 9 secs

Partition Implementation Status
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  No Partitions were found in this design.

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Generating "PAR" statistics.

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Generating Clock Report
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+----------------------+--------------+------+------+------------+-------------+
|        Clock Net     |   Resource   |Locked|Fanout|Net Skew(ns)|Max Delay(ns)|
+----------------------+--------------+------+------+------------+-------------+
|        wr_clk_BUFGP | BUFGMUX_X2Y10| No   |   16 |  0.049     |  0.166      |
+----------------------+--------------+------+------+------------+-------------+
|        rd_clk_BUFGP |  BUFGMUX_X1Y0| No   |   17 |  0.046     |  0.167      |
+----------------------+--------------+------+------+------------+-------------+

* Net Skew is the difference between the minimum and maximum routing
only delays for the net. Note this is different from Clock Skew which
is reported in TRCE timing report. Clock Skew is the difference between
the minimum and maximum path delays which includes logic delays.

* The fanout is the number of component pins not the individual BEL loads,
for example SLICE loads not FF loads.

Timing Score: 0 (Setup: 0, Hold: 0)

Asterisk (*) preceding a constraint indicates it was not met.
   This may be due to a setup or hold violation.

----------------------------------------------------------------------------------------------------
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  Constraint                                |    Check    | Worst Case |  Best Case |
Timing |   Timing
                                            |             |    Slack   | Achievable |
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Errors |    Score
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--------------
  Autotimespec constraint for clock net wr_ | SETUP       |         N/A|     6.658ns|
N/A|           0
  clk_BUFGP                                 | HOLD        |     0.845ns|
|       0|           0
-------------------------------------------------------------------------------------------------
--------------
  Autotimespec constraint for clock net rd_ | SETUP       |         N/A|     6.377ns|
N/A|           0
  clk_BUFGP                                 | HOLD        |     0.871ns|
|       0|           0
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All constraints were met.
INFO:Timing:2761 - N/A entries in the Constraints List may indicate that the
   constraint is not analyzed due to the following: No paths covered by this
   constraint; Other constraints intersect with this constraint; or This
   constraint was disabled by a Path Tracing Control. Please run the Timespec
   Interaction Report (TSI) via command line (trce tsi) or Timing Analyzer GUI.


Generating Pad Report.

All signals are completely routed.

Total REAL time to PAR completion: 28 secs
Total CPU time to PAR completion: 10 secs

Peak Memory Usage:  4465 MB

Placement: Completed - No errors found.
Routing: Completed - No errors found.

Number of error messages: 0
Number of warning messages: 0
Number of info messages: 1

Writing design to file fifo_top_1.ncd



PAR done!
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