Release 14.7 Map P.20131013 (nt64)
Xilinx Mapping Report File for Design 'fifo_top_1'

Design Information

Command Line   : map -intstyle ise -p xc3s500e-fg320-5 -cm area -ir off -pr off
-c 100 -o fifo_top_1_map.ncd fifo_top_1.ngd fifo_top_1.pcf
Target Device : xc3s500e
Target Package : fg320
Target Speed   : -5
Mapper Version : spartan3e -- $Revision: 1.55 $
Mapped Date   : Thu Oct 10 14:50:38 2019

Design Summary

Number of errors: 0
Number of warnings: 0
Logic Utilization:
  Number of Slice Flip Flops: 29 out of   9,312   1%
  Number of 4 input LUTs: 120 out of   9,312   1%
Logic Distribution:
  Number of occupied Slices: 68 out of   4,656   1%
    Number of Slices containing only related logic: 68 out of   68 100%
    Number of Slices containing unrelated logic: 0 out of   68   0%
      *See NOTES below for an explanation of the effects of unrelated logic.
  Total Number of 4 input LUTs: 120 out of   9,312   1%
    Number used as logic: 104
    Number used for Dual Port RAMs: 16
      (Two LUTs used per Dual Port RAM)

  The Slice Logic Distribution report is not meaningful if the design is
  over-mapped for a non-slice resource or if Placement fails.

  Number of bonded IOBs: 25 out of   232   10%
  Number of BUFGMUXs: 2 out of   24   8%

Average Fanout of Non-Clock Nets: 3.76

Peak Memory Usage: 4444 MB
Total REAL time to MAP completion: 23 secs
Total CPU time to MAP completion: 1 secs

NOTES:

   Related logic is defined as being logic that shares connectivity - e.g. two
   LUTs are "related" if they share common inputs. When assembling slices,
   Map gives priority to combine logic that is related. Doing so results in
   the best timing performance.

   Unrelated logic shares no connectivity. Map will only begin packing
   unrelated logic into a slice once 99% of the slices are occupied through
   related logic packing.

   Note that once logic distribution reaches the 99% level through related
   logic packing, this does not mean the device is completely utilized.
   Unrelated logic packing will then begin, continuing until all usable LUTs
   and FFs are occupied. Depending on your timing budget, increased levels of
   unrelated logic packing may adversely affect the overall timing performance
   of your design.

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Section 1 - Errors
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Section 2 - Warnings
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Section 3 - Informational
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INFO:LIT:243 - Logical network sram_top/memory/Mram_mem8/SPO has no load.
INFO:LIT:395 - The above info message is repeated 7 more times for the following
   (max. 5 shown):
   sram_top/memory/Mram_mem7/SPO,
   sram_top/memory/Mram_mem6/SPO,
   sram_top/memory/Mram_mem5/SPO,
   sram_top/memory/Mram_mem4/SPO,
   sram_top/memory/Mram_mem3/SPO
   To see the details of these info messages, please use the -detail switch.
INFO:MapLib:562 - No environment variables are currently set.
INFO:LIT:244 - All of the single ended outputs in this design are using slew
   rate limited output drivers. The delay on speed critical single ended outputs
   can be dramatically reduced by designating them as fast outputs.

Section 4 - Removed Logic Summary
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   1 block(s) optimized away

Section 5 - Removed Logic
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Optimized Block(s):
TYPE            BLOCK
GND             XST_GND

To enable printing of redundant blocks removed and signals merged, set the
detailed map report option and rerun map.

Section 6 - IOB Properties
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+-----------------------------------------------------------------------------------------------
-------------------------------------------------------------+
| IOB Name                          | Type             | Direction | IO Standard
| Diff  | Drive    | Slew | Reg (s)      | Resistor | IOB      |
|                                   |                  |           |
| Term  | Strength | Rate |              |          | Delay    |
+-----------------------------------------------------------------------------------------------
```

data_in<0>			IBUF		INPUT	LVCMOS25
				0 / 0		
data_in<1>			IBUF		INPUT	LVCMOS25
				0 / 0		
data_in<2>			IBUF		INPUT	LVCMOS25
				0 / 0		
data_in<3>			IBUF		INPUT	LVCMOS25
				0 / 0		
data_in<4>			IBUF		INPUT	LVCMOS25
				0 / 0		
data_in<5>			IBUF		INPUT	LVCMOS25
				0 / 0		
data_in<6>			IBUF		INPUT	LVCMOS25
				0 / 0		
data_in<7>			IBUF		INPUT	LVCMOS25
				0 / 0		
data_out<0>			IOB		OUTPUT	LVCMOS25
	12	SLOW		0 / 0		
data_out<1>			IOB		OUTPUT	LVCMOS25
	12	SLOW		0 / 0		
data_out<2>			IOB		OUTPUT	LVCMOS25
	12	SLOW		0 / 0		
data_out<3>			IOB		OUTPUT	LVCMOS25
	12	SLOW		0 / 0		
data_out<4>			IOB		OUTPUT	LVCMOS25
	12	SLOW		0 / 0		
data_out<5>			IOB		OUTPUT	LVCMOS25
	12	SLOW		0 / 0		
data_out<6>			IOB		OUTPUT	LVCMOS25
	12	SLOW		0 / 0		
data_out<7>			IOB		OUTPUT	LVCMOS25
	12	SLOW		0 / 0		
enable_rd			IBUF		INPUT	LVCMOS25
				0 / 0		
enable_wr			IBUF		INPUT	LVCMOS25
				0 / 0		
f_almost_empty			IOB		OUTPUT	LVCMOS25
	12	SLOW		0 / 0		
f_almost_full			IOB		OUTPUT	LVCMOS25
	12	SLOW		0 / 0		
f_empty			IOB		OUTPUT	LVCMOS25
	12	SLOW		0 / 0		
f_full			IOB		OUTPUT	LVCMOS25
	12	SLOW		0 / 0		
rd_clk			IBUF		INPUT	LVCMOS25
				0 / 0		
reset_n			IBUF		INPUT	LVCMOS25
				0 / 0		
wr_clk			IBUF		INPUT	LVCMOS25
				0 / 0		

Section 7 - RPMs

Section 8 - Guide Report

Guide not run on this design.

Section 9 - Area Group and Partition Summary

Partition Implementation Status

No Partitions were found in this design.

Area Group Information

No area groups were found in this design.

Section 10 - Timing Report

This design was not run using timing mode.

Section 11 - Configuration String Details

Use the "-detail" map option to print out Configuration Strings

Section 12 - Control Set Information

No control set information for this architecture.

Section 13 - Utilization by Hierarchy

Use the "-detail" map option to print out the Utilization by Hierarchy section.