

data_out_port1[7:0]
data_out_port2[7:0]
clk_port1
clk_port2
en_port1
en_port2
ctrl_port1
ctrl_port2
addr_in_port1[2:0]
addr_in_port2[2:0]
data_in_port1[7:0]
data_in_port2[7:0]

