```
Release 14.7 par P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc.  All rights reserved.

ADHRIT::  Wed Oct 09 23:01:20 2019

par -w -intstyle ise -ol high -t 1 test_sigals_map.ncd test_sigals.ncd
test_sigals.pcf


Constraints file: test_sigals.pcf.
Loading device for application Rf_Device from file '3s500e.nph' in environment
C:\Xilinx\14.7\ISE_DS\ISE\.
   "test_sigals" is an NCD, version 3.2, device xc3s500e, package fg320, speed -5

Initializing temperature to 85.000 Celsius. (default - Range: -40.000 to 100.000 Celsius)
Initializing voltage to 1.140 Volts. (default - Range: 1.140 to 1.320 Volts)

INFO:Par:282 - No user timing constraints were detected or you have set the option to
ignore timing constraints ("par
   -x"). Place and Route will run in "Performance Evaluation Mode" to automatically
improve the performance of all
   internal clocks in this design. Because there are not defined timing requirements, a
timing score will not be
   reported in the PAR report in this mode. The PAR timing summary will list the
performance achieved for each clock.
   Note: For the fastest runtime, set the effort level to "std".  For best performance,
set the effort level to "high".

Device speed data version:  "PRODUCTION 1.27 2013-10-13".


Design Summary Report:

 Number of External IOBs                          17 out of 232     7%

   Number of External Input IOBs                   5

      Number of External Input IBUFs               5
        Number of LOCed External Input IBUFs       5 out of 5     100%


   Number of External Output IOBs                 12

      Number of External Output IOBs              12
        Number of LOCed External Output IOBs       5 out of 12     41%


   Number of External Bidir IOBs                   0


   Number of BUFGMUXs                        1 out of 24      4%
   Number of Slices                         67 out of 4656    1%
      Number of SLICEMs                      3 out of 2328    1%



Overall effort level (-ol):   High
Placer effort level (-pl):    High
Placer cost table entry (-t): 1
Router effort level (-rl):    High
```

```
Starting initial Timing Analysis.  REAL time: 1 secs
Finished initial Timing Analysis.  REAL time: 1 secs


Starting Placer
Total REAL time at the beginning of Placer: 1 secs
Total CPU  time at the beginning of Placer: 1 secs

Phase 1.1  Initial Placement Analysis
Phase 1.1  Initial Placement Analysis (Checksum:99984ae7) REAL time: 1 secs

Phase 2.7  Design Feasibility Check
INFO:Place:834 - Only a subset of IOs are locked. Out of 12 IOs, 5 are locked and 7 are
not locked. If you would like to
   print the names of these IOs, please set the environment variable
XIL_PAR_DESIGN_CHECK_VERBOSE to 1.
Phase 2.7  Design Feasibility Check (Checksum:99984ae7) REAL time: 1 secs

Phase 3.31  Local Placement Optimization
Phase 3.31  Local Placement Optimization (Checksum:99984ae7) REAL time: 1 secs

Phase 4.2  Initial Clock and IO Placement
........
Phase 4.2  Initial Clock and IO Placement (Checksum:b701ca0f) REAL time: 2 secs

Phase 5.30  Global Clock Region Assignment
Phase 5.30  Global Clock Region Assignment (Checksum:b701ca0f) REAL time: 2 secs

Phase 6.36  Local Placement Optimization
Phase 6.36  Local Placement Optimization (Checksum:b701ca0f) REAL time: 2 secs

Phase 7.3  Local Placement Optimization
.......
Phase 7.3  Local Placement Optimization (Checksum:70b8b548) REAL time: 2 secs

Phase 8.5  Local Placement Optimization
Phase 8.5  Local Placement Optimization (Checksum:70b8b548) REAL time: 2 secs

Phase 9.8  Global Placement
........
........
Phase 9.8  Global Placement (Checksum:b7d8afe8) REAL time: 2 secs

Phase 10.5  Local Placement Optimization
Phase 10.5  Local Placement Optimization (Checksum:b7d8afe8) REAL time: 2 secs

Phase 11.18  Placement Optimization
Phase 11.18  Placement Optimization (Checksum:18104c1b) REAL time: 3 secs

Phase 12.5  Local Placement Optimization
Phase 12.5  Local Placement Optimization (Checksum:18104c1b) REAL time: 3 secs

Total REAL time to Placer completion: 3 secs
Total CPU  time to Placer completion: 3 secs
Writing design to file test_sigals.ncd



Starting Router
```

```
Phase  1  : 475 unrouted;      REAL time: 6 secs

Phase  2  : 430 unrouted;      REAL time: 6 secs

Phase  3  : 83 unrouted;      REAL time: 6 secs

Phase  4  : 105 unrouted; (Par is working to improve performance)     REAL time: 6 secs

Phase  5  : 0 unrouted; (Par is working to improve performance)     REAL time: 6 secs

Updating file: test_sigals.ncd with current fully routed design.

Phase  6  : 0 unrouted; (Par is working to improve performance)     REAL time: 6 secs

Phase  7  : 0 unrouted; (Par is working to improve performance)     REAL time: 7 secs

Updating file: test_sigals.ncd with current fully routed design.

Phase  8  : 0 unrouted; (Par is working to improve performance)     REAL time: 7 secs

Phase  9  : 0 unrouted; (Par is working to improve performance)     REAL time: 7 secs

Phase 10  : 0 unrouted; (Par is working to improve performance)     REAL time: 7 secs

Phase 11  : 0 unrouted; (Par is working to improve performance)     REAL time: 7 secs
WARNING:Route:455 - CLK Net:clk_tmp<23> may have excessive skew because
      0 CLK pins and 1 NON_CLK pins failed to route using a CLK template.
WARNING:Route:455 - CLK Net:q_out_4 may have excessive skew because
      0 CLK pins and 2 NON_CLK pins failed to route using a CLK template.
WARNING:Route:455 - CLK Net:q_out_0 may have excessive skew because
      0 CLK pins and 6 NON_CLK pins failed to route using a CLK template.

Total REAL time to Router completion: 7 secs
Total CPU time to Router completion: 7 secs

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

-------------------------------

Generating "PAR" statistics.

**************************
Generating Clock Report
**************************

+---------------------+--------------+------+------+------------+-------------+
|        Clock Net    |   Resource   |Locked|Fanout|Net Skew(ns)|Max Delay(ns)|
+---------------------+--------------+------+------+------------+-------------+
|        clk_in_BUFGP | BUFGMUX_X1Y11| No   |   12 |  0.019     |  0.129      |
+---------------------+--------------+------+------+------------+-------------+
|         clk_tmp<23> |         Local|      |    4 |  0.003     |  1.433      |
+---------------------+--------------+------+------+------------+-------------+
|             q_out_0 |         Local|      |   17 |  0.280     |  1.913      |
+---------------------+--------------+------+------+------------+-------------+
|             q_out_4 |         Local|      |   13 |  0.241     |  1.850      |
+---------------------+--------------+------+------+------------+-------------+

* Net Skew is the difference between the minimum and maximum routing
```

only delays for the net. Note this is different from Clock Skew which
is reported in TRCE timing report. Clock Skew is the difference between
the minimum and maximum path delays which includes logic delays.

* The fanout is the number of component pins not the individual BEL loads,
for example SLICE loads not FF loads.

Timing Score: 0 (Setup: 0, Hold: 0)

Asterisk (*) preceding a constraint indicates it was not met.
   This may be due to a setup or hold violation.

Constraint	Check	Worst Case Slack	Best Case Achievable	Timing Errors	Timing Score
Autotimespec constraint for clock net clk	SETUP	N/A	3.744ns	N/A	0
_in_BUFGP	HOLD	1.360ns		0	0
Autotimespec constraint for clock net clk	SETUP	N/A	2.583ns	N/A	0
_tmp<23>	HOLD	1.156ns		0	0
Autotimespec constraint for clock net q_o	SETUP	N/A	6.219ns	N/A	0
ut_0	HOLD	0.598ns		0	0
Autotimespec constraint for clock net q_o	SETUP	N/A	6.370ns	N/A	0
ut_4	HOLD	0.834ns		0	0

All constraints were met.
INFO:Timing:2761 - N/A entries in the Constraints List may indicate that the
   constraint is not analyzed due to the following: No paths covered by this
   constraint; Other constraints intersect with this constraint; or This
   constraint was disabled by a Path Tracing Control. Please run the Timespec
   Interaction Report (TSI) via command line (trce tsi) or Timing Analyzer GUI.

Generating Pad Report.

All signals are completely routed.

Total REAL time to PAR completion: 8 secs
Total CPU time to PAR completion: 8 secs

```
Peak Memory Usage:  4446 MB

Placement: Completed - No errors found.
Routing: Completed - No errors found.

Number of error messages: 0
Number of warning messages: 3
Number of info messages: 2

Writing design to file test_sigals.ncd



PAR done!
```