Release 14.7 - xst P.20131013 (nt64)

--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.09 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.09 secs

--> Reading design: dp_sram_top_1.prj

TABLE OF CONTENTS

===
*   Synthesis Options Summary   *
===
---- Source Parameters
Input File Name   : "dp_sram_top_1.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name   : "dp_sram_top_1"
Output Format   : NGC
Target Device   : xc6slx9-3-tqg144

---- Source Options
Top Module Name   : dp_sram_top_1
Automatic FSM Extraction   : YES
FSM Encoding Algorithm   : Auto
Safe Implementation   : No
FSM Style   : LUT
RAM Extraction   : Yes
RAM Style   : Auto
ROM Extraction   : Yes
Shift Register Extraction   : YES
ROM Style   : Auto

```
Resource Sharing                    : YES
Asynchronous To Synchronous         : NO
Shift Register Minimum Size         : 2
Use DSP Block                       : Auto
Automatic Register Balancing        : No

---- Target Options
LUT Combining                       : Auto
Reduce Control Sets                 : Auto
Add IO Buffers                      : YES
Global Maximum Fanout               : 100000
Add Generic Clock Buffer(BUFG)      : 16
Register Duplication                : YES
Optimize Instantiated Primitives    : NO
Use Clock Enable                    : Auto
Use Synchronous Set                 : Auto
Use Synchronous Reset               : Auto
Pack IO Registers into IOBs         : Auto
Equivalent register Removal         : YES

---- General Options
Optimization Goal                   : Speed
Optimization Effort                 : 1
Power Reduction                     : NO
Keep Hierarchy                      : No
Netlist Hierarchy                   : As_Optimized
RTL Output                          : Yes
Global Optimization                 : AllClockNets
Read Cores                          : YES
Write Timing Constraints            : NO
Cross Clock Analysis                : NO
Hierarchy Separator                 : /
Bus Delimiter                       : <>
Case Specifier                      : Maintain
Slice Utilization Ratio             : 100
BRAM Utilization Ratio              : 100
DSP48 Utilization Ratio             : 100
Auto BRAM Packing                   : NO
Slice Utilization Ratio Delta       : 5

=========================================================================


=========================================================================
*                            HDL Parsing                                *
=========================================================================
Analyzing Verilog file "I:\RTL_Codes_Dual_Port_SRAM_For_FIFO\dp_sram\dp_sram_basic.v" into
library work
Parsing module <dp_sram_basic>.
Analyzing Verilog file "I:\RTL_Codes_Dual_Port_SRAM_For_FIFO\dp_sram\dp_sram_top_1.v" into
library work
Parsing module <dp_sram_top_1>.

=========================================================================
*                             HDL Elaboration                           *
=========================================================================

Elaborating module <dp_sram_top_1>.

Elaborating module <dp_sram_basic>.
WARNING:HDLCompiler:1127 - "I:\RTL_Codes_Dual_Port_SRAM_For_FIFO\dp_sram\dp_sram_basic.v"
```

```
Line 58: Assignment to ctrl_port1_reg ignored, since the identifier is never used

=========================================================================
*                            HDL Synthesis                              *
=========================================================================

Synthesizing Unit <dp_sram_top_1>.
    Related source file is "I:\RTL_Codes_Dual_Port_SRAM_For_FIFO\dp_sram\dp_sram_top_1.v".
        a_length = 3
        d_length = 8
INFO:Xst:3210 - "I:\RTL_Codes_Dual_Port_SRAM_For_FIFO\dp_sram\dp_sram_top_1.v" line 36:
Output port <data_out_port1> of the instance <memory> is unconnected or connected to
loadless signal.
    Found 1-bit tristate buffer for signal <idle_pin_2<7>> created at line 34
    Found 1-bit tristate buffer for signal <idle_pin_2<6>> created at line 34
    Found 1-bit tristate buffer for signal <idle_pin_2<5>> created at line 34
    Found 1-bit tristate buffer for signal <idle_pin_2<4>> created at line 34
    Found 1-bit tristate buffer for signal <idle_pin_2<3>> created at line 34
    Found 1-bit tristate buffer for signal <idle_pin_2<2>> created at line 34
    Found 1-bit tristate buffer for signal <idle_pin_2<1>> created at line 34
    Found 1-bit tristate buffer for signal <idle_pin_2<0>> created at line 34
    Summary:
        inferred   8 Tristate(s).
Unit <dp_sram_top_1> synthesized.

Synthesizing Unit <dp_sram_basic>.
    Related source file is "I:\RTL_Codes_Dual_Port_SRAM_For_FIFO\dp_sram\dp_sram_basic.v".
        a_length = 3
        d_length = 8
        depth_fifo = 8
    Found 8x8-bit dual-port RAM <Mram_mem> for signal <mem>.
    Found 8-bit register for signal <data_out_port2>.
    Found 8-bit register for signal <data_out_port1>.
    Summary:
        inferred   1 RAM(s).
        inferred  16 D-type flip-flop(s).
Unit <dp_sram_basic> synthesized.

=========================================================================
HDL Synthesis Report

Macro Statistics
# RAMs                                                 : 1
 8x8-bit dual-port RAM                                 : 1
# Registers                                            : 2
 8-bit register                                        : 2
# Tristates                                            : 8
 1-bit tristate buffer                                 : 8

=========================================================================

=========================================================================
*                       Advanced HDL Synthesis                          *
=========================================================================


Synthesizing (advanced) Unit <dp_sram_basic>.
INFO:Xst:3226 - The RAM <Mram_mem> will be implemented as a BLOCK RAM, absorbing the
following register(s): <data_out_port2>
    ----------------------------------------------------------------------
    | ram_type           | Block                                 |          |
```

```
    -----------------------------------------------------------------------
    | Port A                                                              |
    |     aspect ratio   | 8-word x 8-bit                       |          |
    |     mode           | write-first                          |          |
    |     clkA           | connected to signal <clk_port1>      | rise     |
    |     weA            | connected to signal <ctrl_port1_0>   | high     |
    |     addrA          | connected to signal <addr_in_port1>  |          |
    |     diA            | connected to signal <data_in_port1>  |          |
    -----------------------------------------------------------------------
    | optimization       | speed                                |          |
    -----------------------------------------------------------------------
    | Port B                                                              |
    |     aspect ratio   | 8-word x 8-bit                       |          |
    |     mode           | write-first                          |          |
    |     clkB           | connected to signal <clk_port2>      | rise     |
    |     enB            | connected to signal <en_port2>       | high     |
    |     weB            | connected to signal <GND>            | high     |
    |     addrB          | connected to signal <addr_in_port2>  |          |
    |     diB            | connected to signal <data_in_port2>  |          |
    |     doB            | connected to signal <data_out_port2> |          |
    -----------------------------------------------------------------------
    | optimization       | speed                                |          |
    -----------------------------------------------------------------------
Unit <dp_sram_basic> synthesized (advanced).

=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# RAMs                                                 : 1
 8x8-bit dual-port block RAM                           : 1
# Registers                                            : 8
 Flip-Flops                                            : 8

=========================================================================

=========================================================================
*                        Low Level Synthesis                            *
=========================================================================
WARNING:Xst:1710 - FF/Latch <data_out_port1_0> (without init value) has a constant value
of 0 in block <dp_sram_basic>. This FF/Latch will be trimmed during the optimization
process.
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <data_out_port1_1> (without
init value) has a constant value of 0 in block <dp_sram_basic>. This FF/Latch will be
trimmed during the optimization process.
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <data_out_port1_2> (without
init value) has a constant value of 0 in block <dp_sram_basic>. This FF/Latch will be
trimmed during the optimization process.
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <data_out_port1_3> (without
init value) has a constant value of 0 in block <dp_sram_basic>. This FF/Latch will be
trimmed during the optimization process.
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <data_out_port1_4> (without
init value) has a constant value of 0 in block <dp_sram_basic>. This FF/Latch will be
trimmed during the optimization process.
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <data_out_port1_5> (without
init value) has a constant value of 0 in block <dp_sram_basic>. This FF/Latch will be
trimmed during the optimization process.
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <data_out_port1_6> (without
init value) has a constant value of 0 in block <dp_sram_basic>. This FF/Latch will be
trimmed during the optimization process.
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <data_out_port1_7> (without
```

```
init value) has a constant value of 0 in block <dp_sram_basic>. This FF/Latch will be
trimmed during the optimization process.

Optimizing unit <dp_sram_top_1> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block dp_sram_top_1, actual ratio is 0.

Final Macro Processing ...

=========================================================================
Final Register Report

Found no macro
=========================================================================

=========================================================================
*                            Partition Report                           *
=========================================================================

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

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=========================================================================
*                             Design Summary                            *
=========================================================================

Top Level Output File Name         : dp_sram_top_1.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 2
#      GND                         : 1
#      VCC                         : 1
# RAMS                             : 1
#      RAMB8BWER                   : 1
# Clock Buffers                    : 2
#      BUFGP                       : 2
# IO Buffers                       : 24
#      IBUF                        : 16
#      OBUF                        : 8

Device utilization summary:
---------------------------

Selected Device : 6slx9tqg144-3


Slice Logic Utilization:

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:      0
   Number with an unused Flip Flop:       0  out of      0
   Number with an unused LUT:             0  out of      0
   Number of fully used LUT-FF pairs:     0  out of      0
   Number of unique control sets:         0
```

```
IO Utilization:
 Number of IOs:                          26
 Number of bonded IOBs:                  26  out of    102    25%

Specific Feature Utilization:
 Number of Block RAM/FIFO:                1  out of     32     3%
    Number using Block RAM only:          1
 Number of BUFG/BUFGCTRLs:                2  out of     16    12%

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Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

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=========================================================================
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
rd_clk                             | BUFGP                  | 1     |
wr_clk                             | BUFGP                  | 1     |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: No path found
   Minimum input arrival time before clock: 2.151ns
   Maximum output required time after clock: 5.000ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'rd_clk'
  Total number of paths / destination ports: 4 / 4
-------------------------------------------------------------------------
Offset:              2.151ns (Levels of Logic = 1)
  Source:            b_rd_ptr<2> (PAD)
  Destination:       memory/Mram_mem (RAM)
  Destination Clock: rd_clk rising
```

```
  Data Path: b_rd_ptr<2> to memory/Mram_mem
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             1   1.222   0.579  b_rd_ptr_2_IBUF (b_rd_ptr_2_IBUF)
     RAMB8BWER:ADDRBRDADDR5        0.350          memory/Mram_mem
    ----------------------------------------
    Total                       2.151ns (1.572ns logic, 0.579ns route)
                                        (73.1% logic, 26.9% route)

=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'wr_clk'
  Total number of paths / destination ports: 13 / 13
-------------------------------------------------------------------------
Offset:              2.151ns (Levels of Logic = 1)
  Source:            b_wr_ptr<2> (PAD)
  Destination:       memory/Mram_mem (RAM)
  Destination Clock: wr_clk rising

  Data Path: b_wr_ptr<2> to memory/Mram_mem
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             1   1.222   0.579  b_wr_ptr_2_IBUF (b_wr_ptr_2_IBUF)
     RAMB8BWER:ADDRAWRADDR5        0.350          memory/Mram_mem
    ----------------------------------------
    Total                       2.151ns (1.572ns logic, 0.579ns route)
                                        (73.1% logic, 26.9% route)

=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'rd_clk'
  Total number of paths / destination ports: 8 / 8
-------------------------------------------------------------------------
Offset:              5.000ns (Levels of Logic = 1)
  Source:            memory/Mram_mem (RAM)
  Destination:       rd_data_out<7> (PAD)
  Source Clock:      rd_clk rising

  Data Path: memory/Mram_mem to rd_data_out<7>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     RAMB8BWER:CLKBRDCLK->DOBDO7    1   1.850   0.579  memory/Mram_mem (rd_data_out_7_OBUF)
     OBUF:I->O                 2.571          rd_data_out_7_OBUF (rd_data_out<7>)
    ----------------------------------------
    Total                       5.000ns (4.421ns logic, 0.579ns route)
                                        (88.4% logic, 11.6% route)

=========================================================================

Cross Clock Domains Report:
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=========================================================================


Total REAL time to Xst completion: 5.00 secs
Total CPU time to Xst completion: 4.80 secs

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```

```
Total memory usage is 4509240 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    9 (   0 filtered)
Number of infos    :    2 (   0 filtered)
```