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Release 14.7 - xst P.20131013 (nt64)
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--> Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.32 secs

--> Parameter xsthdpdir set to xst


Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.33 secs

--> Reading design: flag_logic_top_1.prj

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=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "flag_logic_top_1.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "flag_logic_top_1"
Output Format                      : NGC
Target Device                      : xc6slx9-3-tqg144

---- Source Options
Top Module Name                    : flag_logic_top_1
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
```

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Resource Sharing                    : YES
Asynchronous To Synchronous         : NO
Shift Register Minimum Size         : 2
Use DSP Block                       : Auto
Automatic Register Balancing        : No

---- Target Options
LUT Combining                       : Auto
Reduce Control Sets                 : Auto
Add IO Buffers                      : YES
Global Maximum Fanout               : 100000
Add Generic Clock Buffer(BUFG)      : 16
Register Duplication                : YES
Optimize Instantiated Primitives    : NO
Use Clock Enable                    : Auto
Use Synchronous Set                 : Auto
Use Synchronous Reset               : Auto
Pack IO Registers into IOBs         : Auto
Equivalent register Removal         : YES

---- General Options
Optimization Goal                   : Speed
Optimization Effort                 : 1
Power Reduction                     : NO
Keep Hierarchy                      : No
Netlist Hierarchy                   : As_Optimized
RTL Output                          : Yes
Global Optimization                 : AllClockNets
Read Cores                          : YES
Write Timing Constraints            : NO
Cross Clock Analysis                : NO
Hierarchy Separator                 : /
Bus Delimiter                       : <>
Case Specifier                      : Maintain
Slice Utilization Ratio             : 100
BRAM Utilization Ratio              : 100
DSP48 Utilization Ratio             : 100
Auto BRAM Packing                   : NO
Slice Utilization Ratio Delta       : 5

=========================================================================


=========================================================================
*                           HDL Parsing                                 *
=========================================================================
Analyzing Verilog file "I:\FIFO - VLSI Project\RTL
Design\flag_logic\flag_logic_8\wr_ptr_diff.v" into library work
Parsing module <wr_ptr_diff>.
Analyzing Verilog file "I:\FIFO - VLSI Project\RTL
Design\flag_logic\flag_logic_8\flag_logic_wr.v" into library work
Parsing module <flag_logic_wr>.
Analyzing Verilog file "I:\FIFO - VLSI Project\RTL
Design\flag_logic\flag_logic_7\rd_ptr_diff.v" into library work
Parsing module <rd_ptr_diff>.
Analyzing Verilog file "I:\FIFO - VLSI Project\RTL
Design\flag_logic\flag_logic_7\rd_flag_logic.v" into library work
Parsing module <rd_flag_logic>.
Analyzing Verilog file "I:\FIFO - VLSI Project\RTL
Design\flag_logic\flag_logic_8\flag_top_wr.v" into library work
Parsing module <flag_top_wr>.
```

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Analyzing Verilog file "I:\FIFO - VLSI Project\RTL
Design\flag_logic\flag_logic_7\flag_logic_top_rd.v" into library work
Parsing module <flag_logic_top_rd>.
Analyzing Verilog file "I:\FIFO - VLSI Project\RTL Design\flag_logic\flag_logic_top_1.v"
into library work
Parsing module <flag_logic_top_1>.

=========================================================================
*                            HDL Elaboration                            *
=========================================================================

Elaborating module <flag_logic_top_1>.

Elaborating module <flag_logic_top_rd>.

Elaborating module <rd_ptr_diff>.

Elaborating module <rd_flag_logic>.

Elaborating module <flag_top_wr>.

Elaborating module <wr_ptr_diff>.

Elaborating module <flag_logic_wr>.

=========================================================================
*                           HDL Synthesis                               *
=========================================================================

Synthesizing Unit <flag_logic_top_1>.
    Related source file is "I:\FIFO - VLSI Project\RTL
Design\flag_logic\flag_logic_top_1.v".
    Summary:
        no macro.
Unit <flag_logic_top_1> synthesized.

Synthesizing Unit <flag_logic_top_rd>.
    Related source file is "I:\FIFO - VLSI Project\RTL
Design\flag_logic\flag_logic_7\flag_logic_top_rd.v".
        a_length = 3
    Summary:
        no macro.
Unit <flag_logic_top_rd> synthesized.

Synthesizing Unit <rd_ptr_diff>.
    Related source file is "I:\FIFO - VLSI Project\RTL
Design\flag_logic\flag_logic_7\rd_ptr_diff.v".
        config_depth = 3'b111
        a_length = 3
    Found 3-bit subtractor for signal <b_wr_ptr_sync[2]_b_rd_ptr[2]_sub_2_OUT> created at
line 36.
    Found 3-bit subtractor for signal <n0015> created at line 38.
    Found 3-bit adder for signal <PWR_3_o_b_wr_ptr_sync[2]_add_3_OUT> created at line 38.
    Found 3-bit comparator lessequal for signal <n0001> created at line 35
    Summary:
        inferred   2 Adder/Subtractor(s).
        inferred   1 Comparator(s).
        inferred   2 Multiplexer(s).
Unit <rd_ptr_diff> synthesized.

Synthesizing Unit <rd_flag_logic>.
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```
    Related source file is "I:\FIFO - VLSI Project\RTL
Design\flag_logic\flag_logic_7\rd_flag_logic.v".
        f_a_empty = 2
        a_length = 3
    Summary:
Unit <rd_flag_logic> synthesized.

Synthesizing Unit <flag_top_wr>.
    Related source file is "I:\FIFO - VLSI Project\RTL
Design\flag_logic\flag_logic_8\flag_top_wr.v".
        a_length = 3
    Summary:
        no macro.
Unit <flag_top_wr> synthesized.

Synthesizing Unit <wr_ptr_diff>.
    Related source file is "I:\FIFO - VLSI Project\RTL
Design\flag_logic\flag_logic_8\wr_ptr_diff.v".
        config_depth = 3'b111
        a_length = 3
    Found 3-bit subtractor for signal <b_wr_ptr[2]_b_rd_ptr_sync[2]_sub_2_OUT> created at
line 37.
    Found 3-bit subtractor for signal <n0015> created at line 40.
    Found 3-bit adder for signal <PWR_7_o_b_wr_ptr[2]_add_3_OUT> created at line 40.
    Found 3-bit comparator lessequal for signal <n0001> created at line 36
    Summary:
        inferred   2 Adder/Subtractor(s).
        inferred   1 Comparator(s).
        inferred   2 Multiplexer(s).
Unit <wr_ptr_diff> synthesized.

Synthesizing Unit <flag_logic_wr>.
    Related source file is "I:\FIFO - VLSI Project\RTL
Design\flag_logic\flag_logic_8\flag_logic_wr.v".
        f_a_full = 6
        a_length = 3
    Summary:
Unit <flag_logic_wr> synthesized.

=========================================================================
HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                                   : 4
 3-bit addsub                                         : 2
 3-bit subtractor                                     : 2
# Comparators                                          : 2
 3-bit comparator lessequal                           : 2
# Multiplexers                                         : 4
 3-bit 2-to-1 multiplexer                             : 4
# Xors                                                 : 2
 1-bit xor2                                           : 2

=========================================================================
INFO:Xst:1767 - HDL ADVISOR - Resource sharing has identified that some arithmetic
operations in this design can share the same physical resources for reduced device
utilization. For improved clock frequency you may try to disable resource sharing.

=========================================================================
*                      Advanced HDL Synthesis                           *
=========================================================================
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=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                                   : 4
 3-bit addsub                                         : 2
 3-bit subtractor                                     : 2
# Comparators                                          : 2
 3-bit comparator lessequal                           : 2
# Multiplexers                                         : 4
 3-bit 2-to-1 multiplexer                             : 4
# Xors                                                 : 2
 1-bit xor2                                           : 2

=========================================================================

=========================================================================
*                            Low Level Synthesis                        *
=========================================================================

Optimizing unit <flag_logic_top_1> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block flag_logic_top_1, actual ratio is 0.

Final Macro Processing ...

=========================================================================
Final Register Report

Found no macro
=========================================================================

=========================================================================
*                             Partition Report                          *
=========================================================================

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

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=========================================================================
*                             Design Summary                            *
=========================================================================

Top Level Output File Name         : flag_logic_top_1.ngc

Primitive and Black Box Usage:
-------------------------------
# BELS                             : 9
#      LUT2                        : 2
#      LUT6                        : 7
# IO Buffers                       : 13
#      IBUF                        : 9
#      OBUF                        : 4
```

Device utilization summary:

Selected Device : 6slx9tqg144-3

Slice Logic Utilization:

Number of Slice LUTs:	9	out of	5720	0%
Number used as Logic:	9	out of	5720	0%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used:	9			
Number with an unused Flip Flop:	9	out of	9	100%
Number with an unused LUT:	0	out of	9	0%
Number of fully used LUT-FF pairs:	0	out of	9	0%
Number of unique control sets:	0			

IO Utilization:

Number of IOs:	13			
Number of bonded IOBs:	13	out of	102	12%

Specific Feature Utilization:

Partition Resource Summary:

No Partitions were found in this design.

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Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 6.841ns

Timing Details:

All values displayed in nanoseconds (ns)

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================================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 88 / 4
--------------------------------------------------------------------------------
Delay:               6.841ns (Levels of Logic = 4)
  Source:            b_wr_ptr<0> (PAD)
  Destination:       f_full (PAD)

  Data Path: b_wr_ptr<0> to f_full
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             3   1.222   1.015  b_wr_ptr_0_IBUF (b_wr_ptr_0_IBUF)
     LUT6:I0->O            4   0.203   1.048
empty/U1/PWR_3_o_b_wr_ptr_sync[2]_mux_4_OUT<0>1
(empty/U1/PWR_3_o_b_wr_ptr_sync[2]_mux_4_OUT<0>)
     LUT6:I0->O            1   0.203   0.579  full/U2/f_full1 (f_full_OBUF)
     OBUF:I->O                 2.571          f_full_OBUF (f_full)
    ----------------------------------------
    Total                      6.841ns (4.199ns logic, 2.642ns route)
                                       (61.4% logic, 38.6% route)

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Cross Clock Domains Report:
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Total REAL time to Xst completion: 7.00 secs
Total CPU time to Xst completion: 6.47 secs

-->

Total memory usage is 4522800 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    0 (   0 filtered)
Number of infos    :    1 (   0 filtered)
```