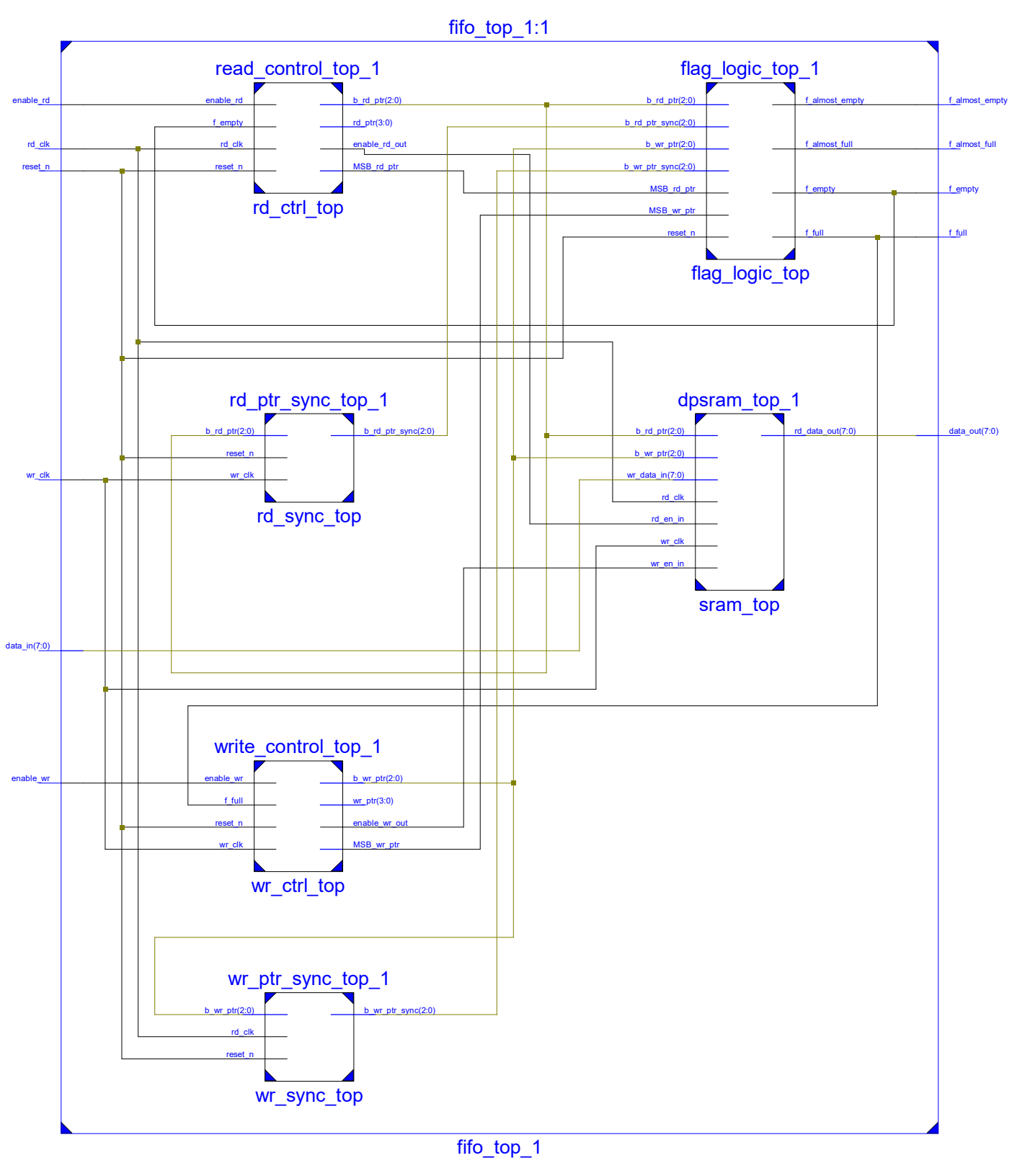
fifo_top_1:1
read_control_top_1
enable_rd
rd_clk
reset_n
enable_rd
f_empty
rd_clk
reset_n
b_rd_ptr(2:0)
rd_ptr(3:0)
enable_rd_out
MSB_rd_ptr
rd_ctrl_top
flag_logic_top_1
b_rd_ptr(2:0)
b_rd_ptr_sync(2:0)
b_wr_ptr(2:0)
b_wr_ptr_sync(2:0)
MSB_rd_ptr
MSB_wr_ptr
reset_n
f_almost_empty
f_almost_full
f_empty
f_full
flag_logic_top
f_almost_empty
f_almost_full
f_empty
f_full
rd_ptr_sync_top_1
b_rd_ptr(2:0)
reset_n
wr_clk
b_rd_ptr_sync(2:0)
rd_sync_top
wr_clk
dpsram_top_1
b_rd_ptr(2:0)
b_wr_ptr(2:0)
wr_data_in(7:0)
rd_clk
rd_en_in
wr_clk
wr_en_in
rd_data_out(7:0)
sram_top
data_out(7:0)
data_in(7:0)
write_control_top_1
enable_wr
f_full
reset_n
wr_clk
b_wr_ptr(2:0)
wr_ptr(3:0)
enable_wr_out
MSB_wr_ptr
wr_ctrl_top
enable_wr
wr_ptr_sync_top_1
b_wr_ptr(2:0)
rd_clk
reset_n
b_wr_ptr_sync(2:0)
wr_sync_top
fifo_top_1