# FIFO Implementation Using FPGA Micro-Architecture

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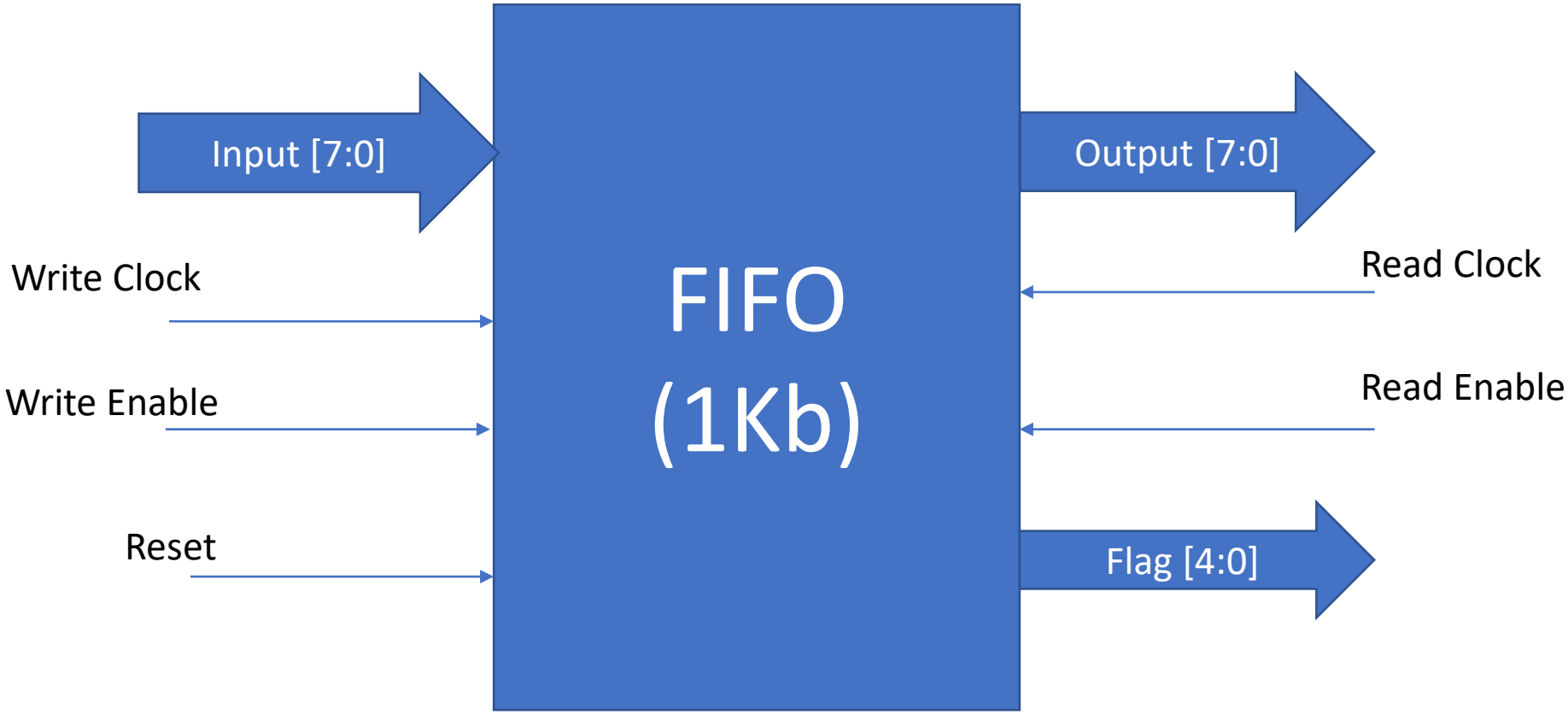
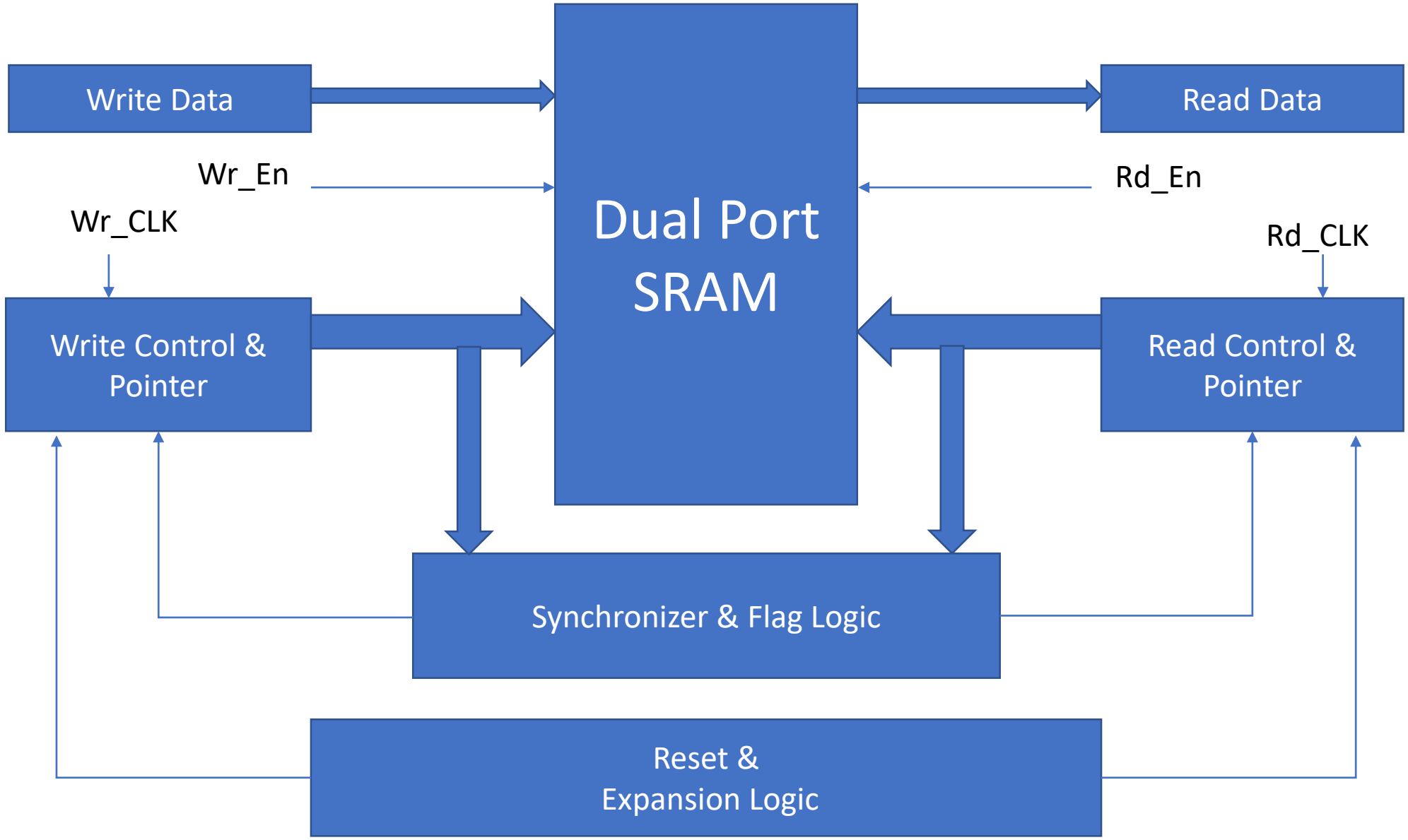
# SPECIFICATIONS

- BURST Size : 1.5K bytes
- FIFO Size : 1 K bytes
- Input Data Pins: 8
- Input Pins: 2 (R/W enable)
- Output Data Pins: 8
- Write Pointer Pins: 10
- Read Pointer Pins: 10
- Flag Pins: 5 ( EMPTY, FULL, HALF FULL / EMPTY, ALMOST FULL, ALMOST EMPTY)
- Reset: 1
- Write Clock (100MHz)
- Read Clock (33MHz)

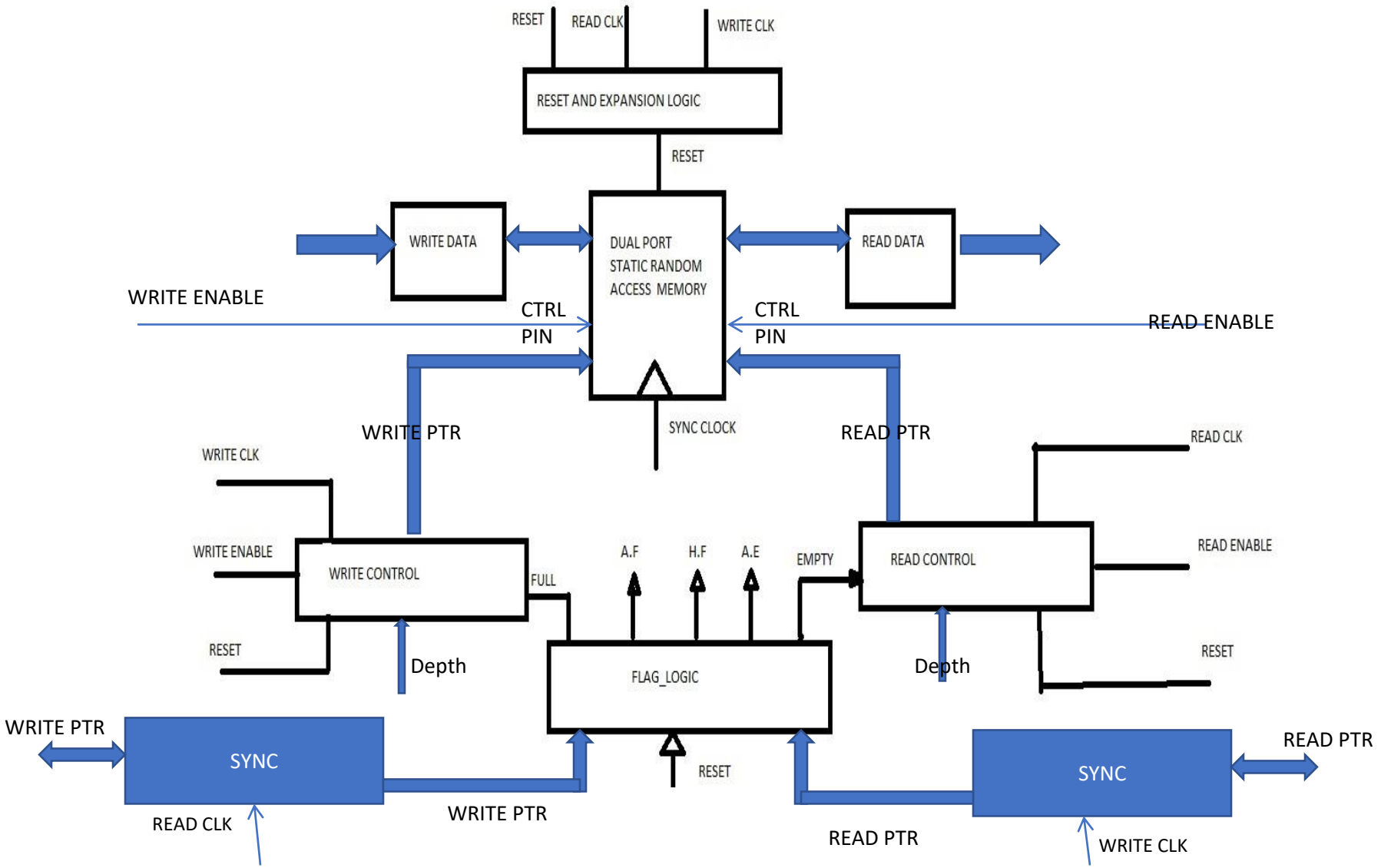
# PIN Diagram:


Input [7:0]
Write Clock
Write Enable
Reset
FIFO
(1Kb)
Output [7:0]
Read Clock
Read Enable
Flag [4:0]

# Top Level Diagram:



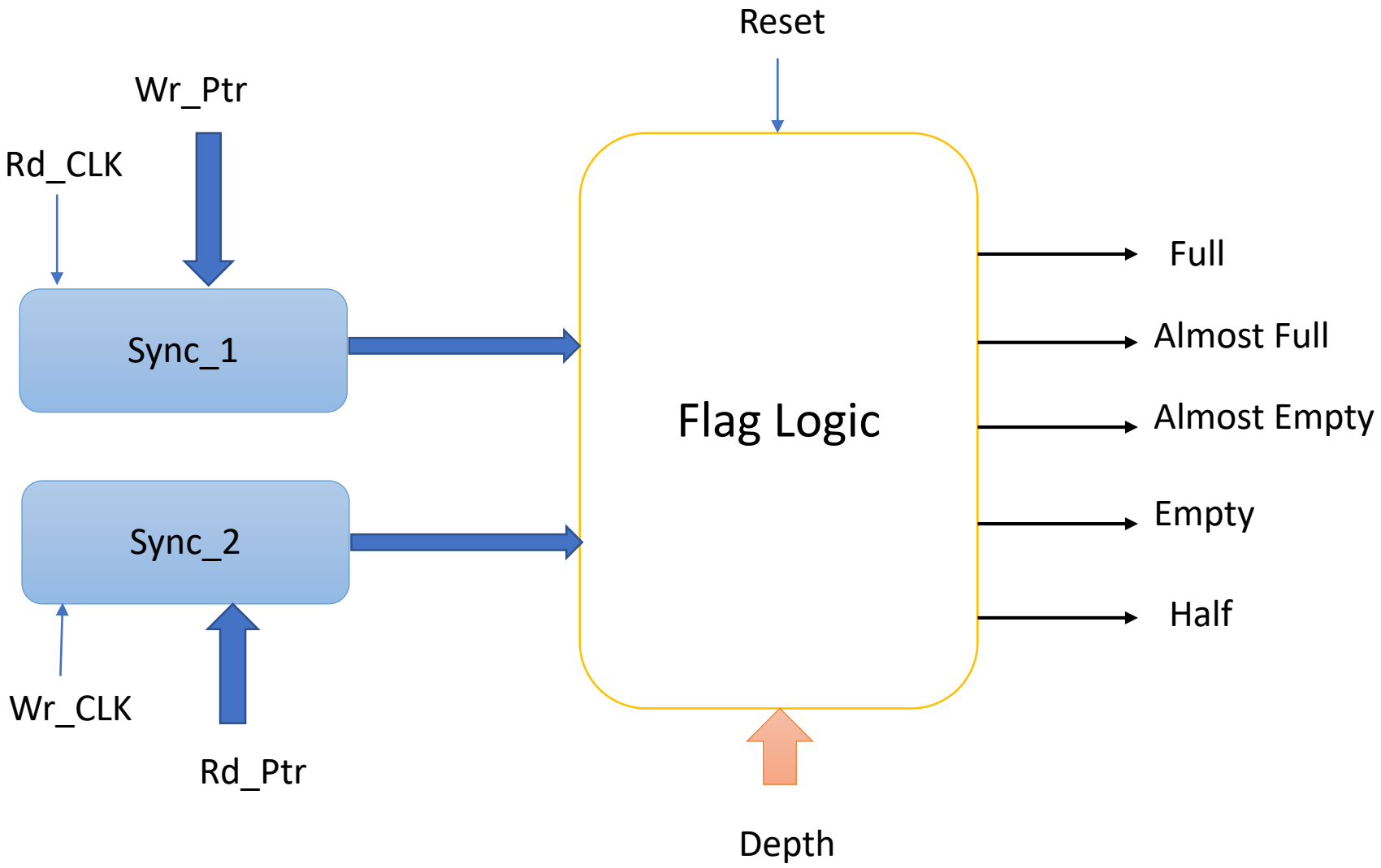
# Micro Architecture



# Pin Description – Top Level

| No. | Name of Pin | No. of Pins | Direction | Description |
|---|---|---|---|---|
| 1. | Write Data | 8 | Input | Input data to SRAM |
| 2. | Read Data | 8 | Output | Output data from SRAM |
| 3. | Write Enable | 1 | Input | Enable write operation |
| 4. | Read Enable | 1 | Input | Enable read operation |
| 5. | Write Clock | 1 | Input | Clock for write operation |
| 6. | Read Clock | 1 | Input | Clock for read operation |
| 7. | Reset | 1 | Input | To reset FIFO memory |
| 8. | Flag Logic | 4 | Output | Show status of FIFO |

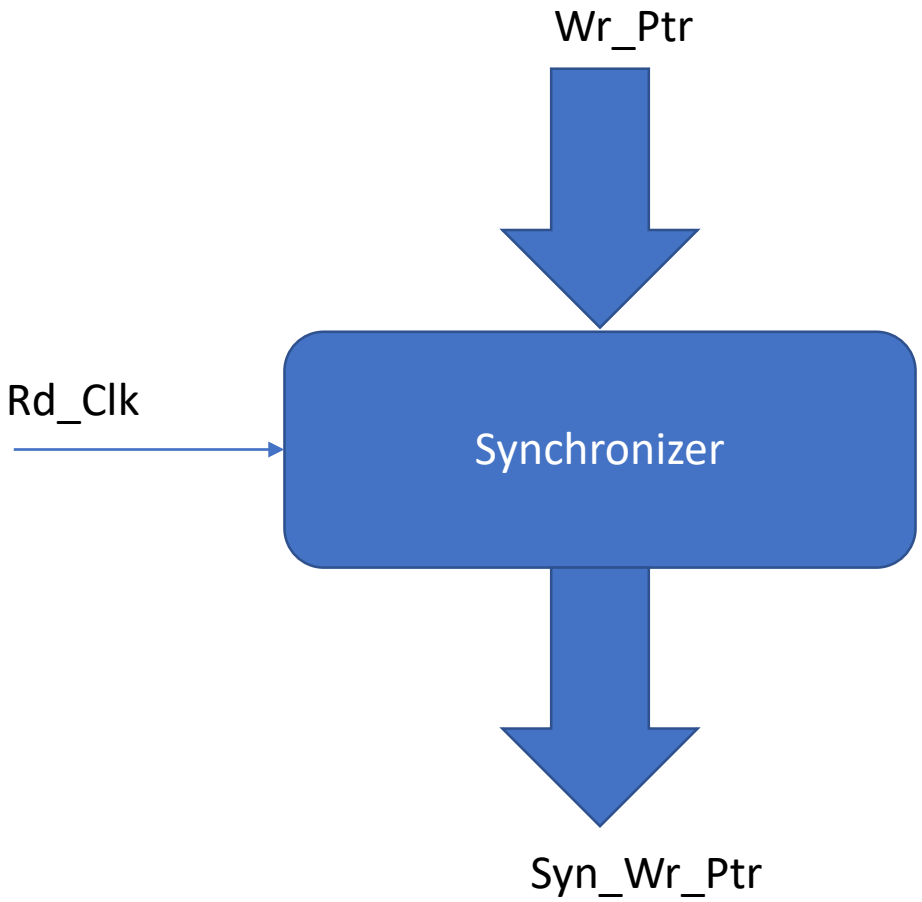
# Flag Logic

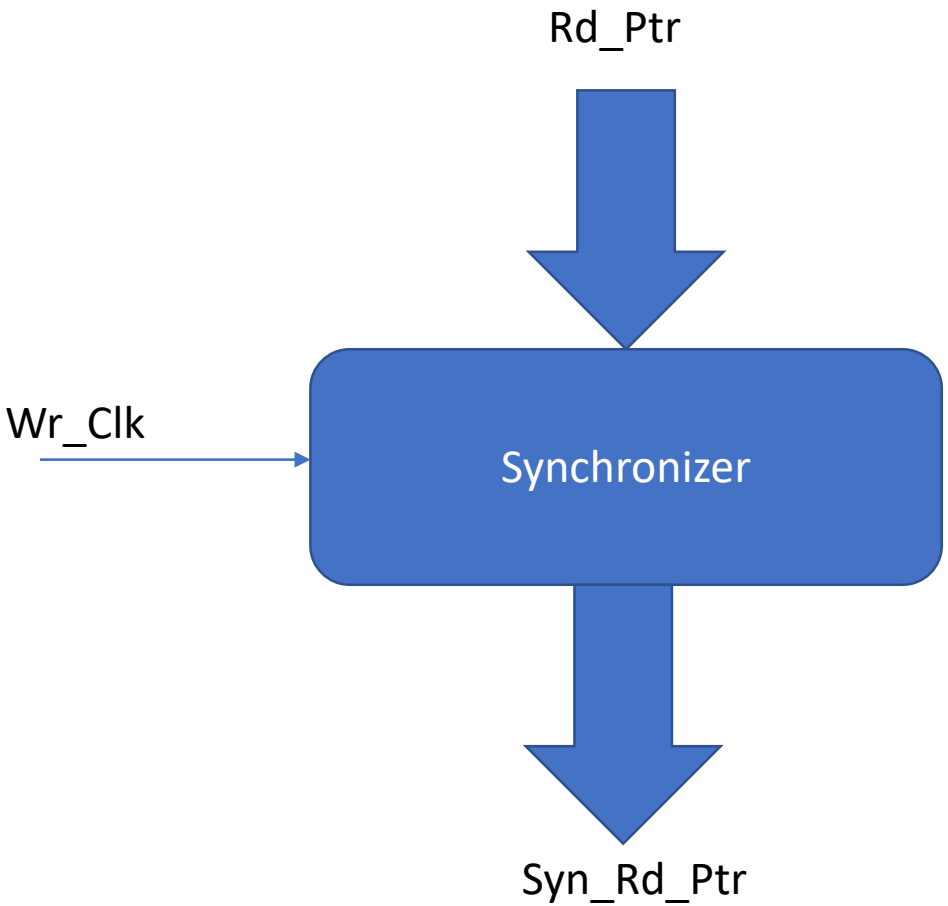

Reset
Wr_Ptr
Rd_CLK
Sync_1
Sync_2
Flag Logic
Full
Almost Full
Almost Empty
Empty
Half
Wr_CLK
Rd_Ptr
Depth

# Pin Functions – Flag Logic

| No. | Name of Pin | No. of Pins | Direction | Function |
|---|---|---|---|---|
| 1. | Write Pointer | 10 | Input | Address input to comparator |
| 2. | Read Pointer | 10 | Input | Address input to comparator |
| 3. | Depth | 10 | Input | Limiting value of memory location |
| 4. | Reset | 1 | Input | To set empty flag |
| 5. | Write Clock | 1 | Input | To synchronize Read pointer |
| 6. | Read Clock | 1 | Input | To synchronize Write pointer |
| 7. | Full | 1 | Output | Show status as FIFO is Full |
| 8. | Empty | 1 | Output | Show status as FIFO is empty |
| 9. | Almost Full | 1 | Output | FIFO is Almost empty |
| 10. | Almost Empty | 1 | Output | FIFO is Almost empty |
| 11. | Half | 1 | Output | Show status as FIFO is half |

# Synchronizers

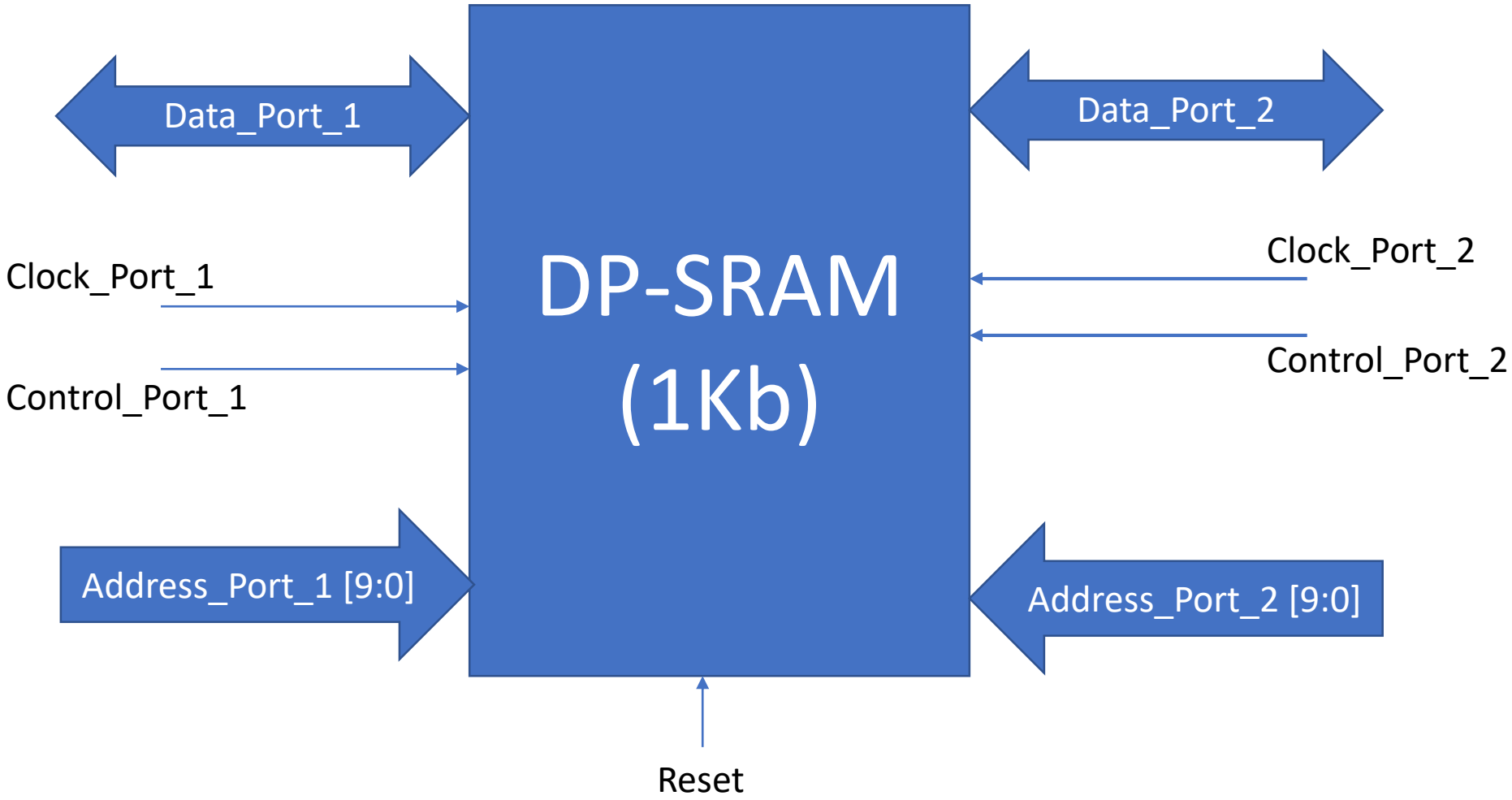


# Pin Functions – Synchronizers

| No. | Name of Pin | No. of Pins | Direction | Function |
|---|---|---|---|---|
| 1. | Write Pointer | 10 | Input | Address to be synchronized |
| 2 | Read Pointer | 10 | Input | Address to be synchronized |
| 3 | Write Clock | 1 | Input | Synchronizing clock |
| 4 | Read Clock | 1 | Input | Synchronizing clock |
| 5 | Synchronized Write Pointer | 10 | Output | Synchronized address |
| 6 | Synchronized Read Pointer | 10 | Output | Synchronized address |

# Dual Port SRAM

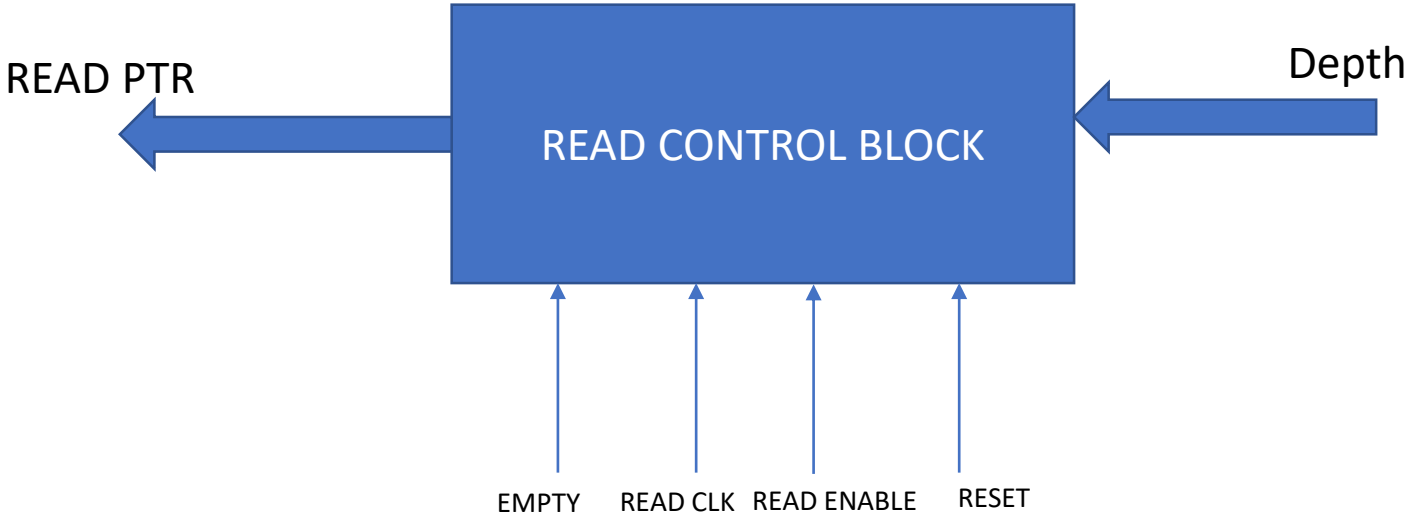


# Pin Description – Dual Port SRAM

| No. | Name of Pin | No. of Pins | Direction | Function |
|---|---|---|---|---|
| 1 | Data Port x | 8 | Bidirectional | Data to or from the memory |
| 2 | Address Port x | 10 | Input | Specifies memory location for W/R |
| 3 | Clock Port x | 1 | Input | Clock signal for operation |
| 4 | Control Port x | 1 | Input | Specifies operation to be performed W/R |
| 5 | Reset | 1 | Input | Resets the SRAM and memory locations |

Here x can be 1 or 2.

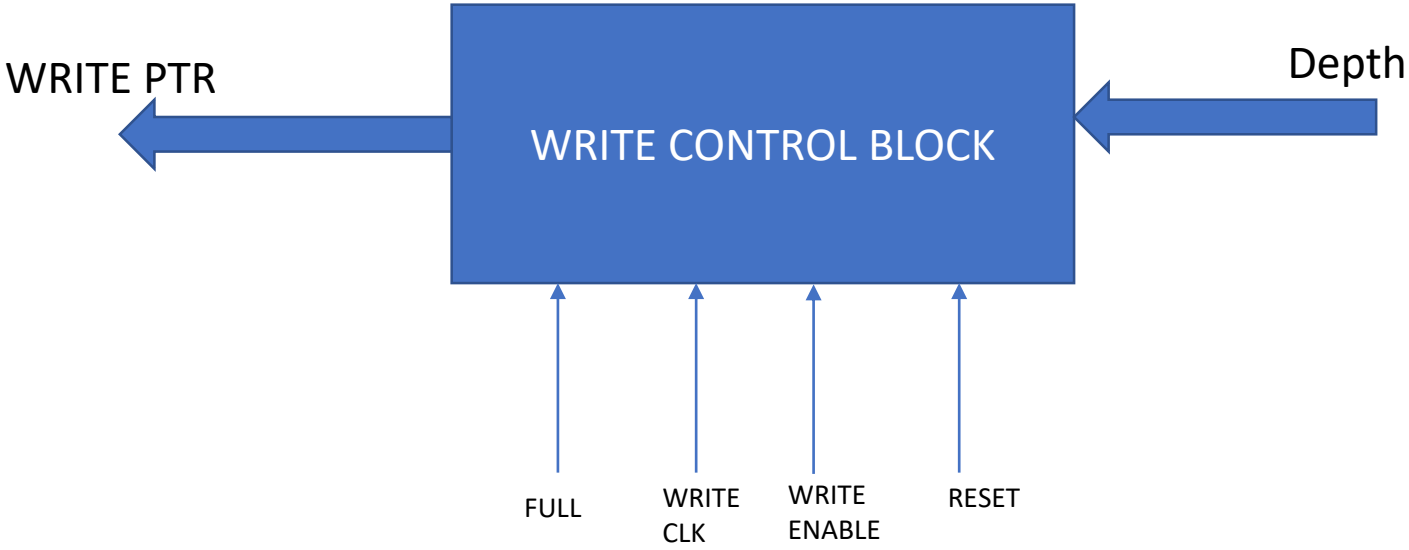
# Read Control Block



# Pin Functions – Read Control Block

| No. | Name of Pin | No. of Pins | Direction | Function |
|---|---|---|---|---|
| 1. | Read Pointer | 10 | Output | Output address to SRAM |
| 2. | Read Enable | 1 | Input | Enable read operation |
| 3. | Read Clock | 1 | Input | Clock for read operation |
| 4. | Reset | 1 | Input | To reset Read Pointer |
| 5. | Empty | 1 | Input | Show status of FIFO as empty |
| 6. | Depth | 10 | Input | Indicate FIFO size |

# Write Control Block



# Pin Functions – Write Control Block

| No. | Name of Pin | No. of Pins | Direction | Function |
|---|---|---|---|---|
| 1. | Write Pointer | 10 | Output | Output address to SRAM |
| 2. | Write Enable | 1 | Input | Enable write operation |
| 3. | Write Clock | 1 | Input | Clock for write operation |
| 4. | Reset | 1 | Input | To reset write Pointer |
| 5. | Full | 1 | Input | Show status of FIFO as full |
| 6. | Depth | 10 | Input | Indicate FIFO size |