A HIGH THROUGHPUT, ASYNCHRONOUS, DUAL PORT FIFO MEMORY IMPLEMENTED IN ASIC TECHNOLOGY

Giao N. Pham, P.E.

NCR Corporation
1635 Aeroplaza Drive
Colorado Springs, CO 80916
(719) 596-5795
FAX (719) 570-6045

Kenneth C. Schmitt, P.E.

NCR Corporation
1635 Aeroplaza Drive
Colorado Springs, CO 80916
(719) 596-5795
FAX (719) 570-6045

ABSTRACT

This paper describes an ASIC first-in first-out (FIFO) memory circuit which has the capability of interfacing two data processing units operating at different speeds. The memory is implemented using a circular queue structure, which permits writing and reading of data indefinitely as long as the boundary flag conditions are not met. This memory also has the capability to retransmit only bad data words, not whole memory blocks as most standard FIFOs do. Another feature is dual port memory operation which allows bidirectional data transfers through the FIFO. All of the circuit implementations are done using NCR standard cells. This allows the use of automatic routing and test program generation tools provided by NCR VISYS.*

INTRODUCTION

Microprocessors and I/O devices often have different operating capabilities usually related to data throughput or operating frequency. Therefore, the need arises to be able to transfer data between two devices operating at different speeds with minimal impact on data throughput [2]. Because speed of operation is important, we used a RAM for the memory storage element, thus data can be accessed directly from it. The read and write address pointers for the RAM are controlled by the system requesting the read or write function and can therefore operate independent of each other. This allows reading and writing of the RAM to occur simultaneously. Because the read and write cycles are asynchronous and independent of each other, it becomes necessary to provide control circuitry which can accurately determine the status of the RAM. The control circuitry must be able to determine when the memory is full or empty to prevent corrupting the RAM data by writing over data which has not been read yet. Since a read or write can occur at any time, determining the exact status of the RAM becomes a non-trivial effort. This FIFO was designed to solve these problems.

*NCR VISYS is a trademark of NCR Corp.

CH1234-5/89/0000-P3-1.1$01.00 © 1989 IEEE

OBJECTIVES

A number of design objectives were specified concerning the different aspects of this FIFO architecture.

1. Technology:
   Implementation must be in the NCR standard cell library and completely compatible with NCR VISYS tools. This allows rapid changes to different memory sizes and the FIFO can be treated as a macrocell. Macrocells are built from several lower complexity function blocks and are stored within the CAD system. These cells can be modified by adding or deleting functions and changing layout configurations [4]. It also enables the logic to migrate to smaller technologies with the cell library.

2. Speed considerations:
   Because the FIFO interfaces devices of different speeds, circuits had to be designed which handled two asynchronous inputs (WRITE & READ). These asynchronous signals are then used to keep track of the free memory space in the FIFO. This gives the user the ability to continuously and simultaneously write and read the FIFO. The FIFO also had to operate at a minimum of 20 Mhz.

3. Functional considerations:
   A dual port memory configuration was needed to allow bidirectional data transfers. To further enhance speed, the retransmit feature must allow partial memory blocks to be resent upon request. The FIFO status can be examined by the state of the Empty, Almost Empty, Half Full, Almost Full, and Full flags. The user needs to observe these flags to avoid the condition of over writing a full memory or over reading an empty memory.

ARCHITECTURE

The FIFO architecture [3] as shown in figure 1 consists of:

- Two memory pointers
  (READ and WRITE counters)
  Generate the current addresses for the Dual port RAM from the WRITE/READ signals.

- DATA GOOD Counter
  To keep track of the last successfully read data location.

- Two asynchronous Up/Down counters (FLAG counter, RETRANSMIT counter, and CLOCKCND)
  These up/down counters and the clock conditioning circuit handle fully asynchronous clock signals. The FLAG counter indicates the current memory space available in the FIFO while the RETRANSMIT counter indicates the memory space available if a retransmit occurs.

- Flag logic (FLAGDEC)
  Generates the signals to indicate the predefined memory space available in the FIFO. These signals can be changed to accommodate different memory sizes. The flags are: "almost empty", "half full", "almost full", "full" and "empty".

- One Dual Port RAM (DPRAM)
  Fully static and operates at frequencies up to 30 Mhz, can be written and read on either port.

- DIR Signal
  Input signal which indicates which ports of the dual port RAM are being written or read.

- INH Signal
  This input signal, when active, will allow the FIFO to automatically stop writing when full and stop reading when empty.

- Configurable memory size
  The layout and circuit implementation allows the memory to be expanded or shrunk to different sizes very easily.

DESIGN CONSIDERATIONS

Due to the need for fast transfer rates in the system, a FIFO needed to be designed which could write and read indefinitely as long as the boundary conditions were not met. Most standard FIFOs retransmit whole memory blocks of data if a bad word is detected [1]. This will not allow the user to wrap around and begin rewriting the memory until they have successfully read all the data in the FIFO. Therefore, it slows down the throughput as shown in Figures 2 and 3. Assume f is the frequency of the data to be transferred and a bad word is at location X in the memory. The retransmit time of a standard FIFO is X/f and that of the high throughput FIFO is Td (time to validate a data word), because this FIFO only retransmits a bad word, not the whole memory block. If S is the total memory locations, the average retransmit time of a standard FIFO is S/2f while the high throughput FIFO takes a constant Td time to retransmit. Many available FIFOs do not allow asynchronous operation which means the user cannot do simultaneous read and writes. In this high throughput FIFO, the combination of asynchronous operation and the ability to fill the memory space of words that have been successfully transmitted allow maximum transfer rate.

In the current design, when a system reads a valid data word from the FIFO it will send a signal, DATA_GD, to indicate that the word was successfully received. This in turn, will update the DATA GOOD counter. If a bad word was received, a retransmit (RETRAN) signal will be sent to the FIFO. The RETRAN signal will load the current value of the DATA GOOD counter

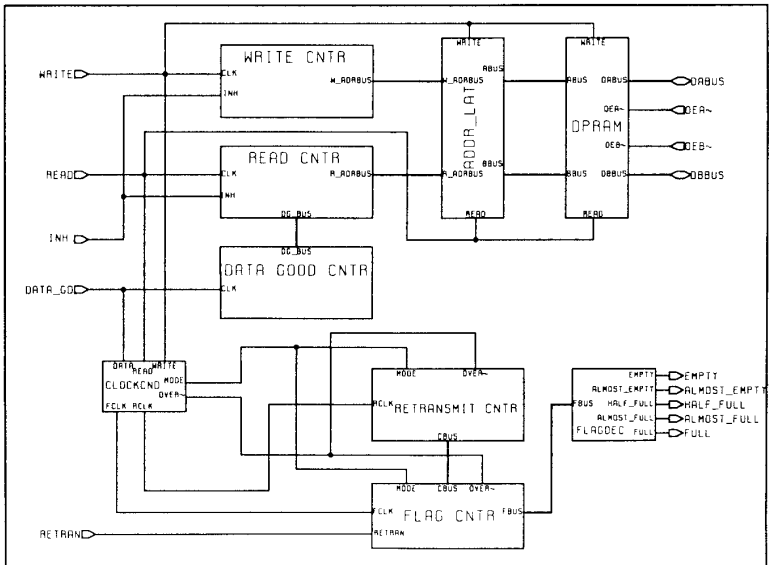


Figure 1: HIGH THROUGHPUT FIFO ARCHITECTURE

note: detailed connection is not shown on this schematic

into the READ counter. It will also load the RETRANSMIT counter value into the FLAG counter.

The asynchronous operation is handled by the clock conditioning circuit which directly controls the operation of the FLAG and RETRANSMIT counters. If a WRITE signal occurs when the READ or DATA_GD signal is inactive, the clock conditioning circuit will generate a FCLK or RCLK output signal to clock the counter and the MODE signal will go low to indicate the count up mode. Similarly, if the READ or DATA_GD signal occurs when the WRITE signal is inactive, a clock output is generated and the MODE signal goes high to indicate the count down mode. In the case when both WRITE and READ signals occur at the same time or any overlap between these two signals exist, FCLK or RCLK signal is generated but the overlap (OVER_)signal will go active before this clock pulse and disable the FLAG or RETRANSMIT counters.

The FIFO status flags are used to indicate the following memory conditions:

EMPTY - used to indicate that all the written data has been read.

ALMOST EMPTY - used to indicate that only three more locations are left to be read.

HALF FULL - used to indicate that the memory is half full.

ALMOST FULL - used to indicate that only three more locations are left to be written.

FULL - used to indicate that all the available memory in the FIFO has been written.

During data transfers, the user must pay very close attention to these status flags to avoid the over writing or over reading of the memory. One feature in the current design is the inhibit mode. When the user activates the INH signal, the FIFO will automatically stop reading or writing when the empty or full status flags occur. The EMPTY signal will not be released until a write cycle is completed thus preventing a read of a memory location that has not yet been written. The read location will always lag the write location, therefore the contention between read and write operations cannot happen. This design also features dual port transfers of data. The user can select either ports to be written or read by using the DIR pin.

APPLICATIONS

This high throughput FIFO can be used in many applications. One of the immediate uses will be to handle bi-directional data transfers in an NCR minicomputer. The interface is between the Multibus II and a host computer which run at 10 Mhz and 20 Mhz, respectively. This system will fully utilize the asynchronous dual port capabilities of this FIFO memory. It can also be used to fetch data or instructions in microprocessor designs.

CONCLUSIONS

The architecture presented here allows the use of a FIFO memory with the advantages of:

- fast data rate
  The described FIFO allows the user to write or read data continuously without stopping unless the status flags indicate Full or Empty.
- bidirectional data transfer
  Due to the storage elements being implemented using a dual port RAM, the present FIFO can be written or read on either port depending upon the DIR signal.
- fully asynchronous operation
  The clock conditioning and the flag decode circuits of the FIFO are implemented so the FIFO can handle the write and read operations asynchronously.
- READ and WRITE signals can be at different clock frequencies.

By implementing this FIFO in NCR Standard Cell methodology, time is saved in circuit implementation, layout, and verification. It also allows users to configure the FIFO memory to meet their particular applications in an efficient and error free manner.

ACKNOWLEDGEMENTS

The authors are grateful for the assistance of Dan Hackney and Janice Reed, and the encouragement from Gail Walters.

REFERENCES

[1] Integrated Device Technology, "High Performance CMOS Data Book", 1988.

[2] A. K. Hargrove et al., "FIFO Register with Independent Clocking Means", US Patent 4,423,482, December 1983.

[3] G. N. Pham, K. C. Schmitt, "Asynchronous FIFO Architectures", Patent Pending, Docket No. 4374, February, 1989.

[4] NCR Corporation, "NCR ASIC Data Book", 1989.

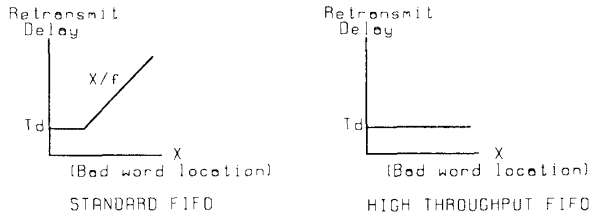


Figure 2: Retransmit Time vs. Bad Word Location

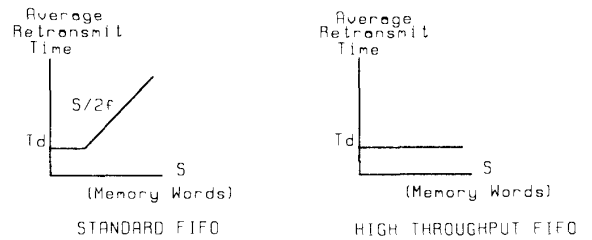
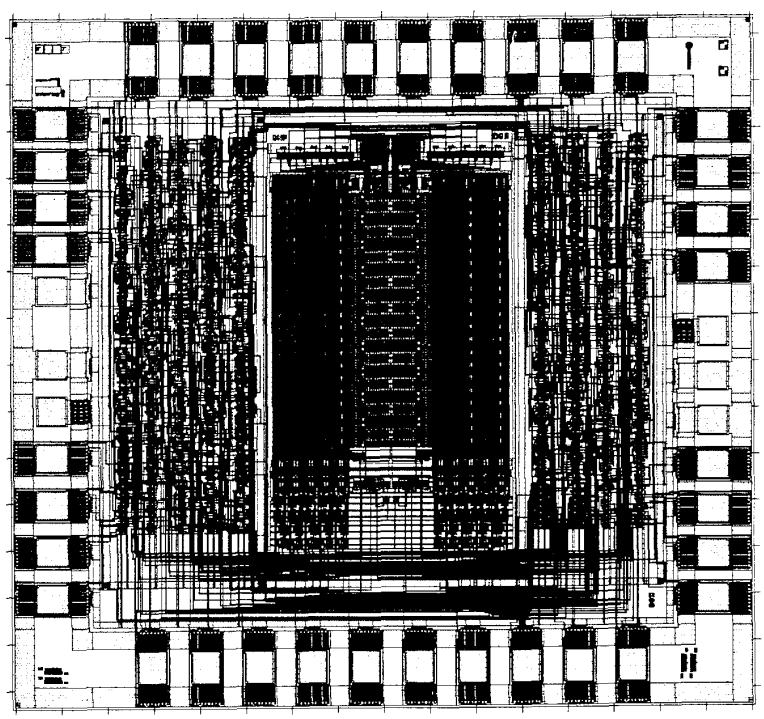


Figure 3: Average Retransmit Time vs. Memory Words

note: Td is the time to validate a data word
f is the data transfer rate



FIFO Chip Layout