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Release 14.7 Map P.20131013 (nt64)
Xilinx Mapping Report File for Design 'test_sigals'

Design Information
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Command Line   : map -intstyle ise -p xc3s500e-fg320-5 -cm area -ir off -pr off
-c 100 -o test_sigals_map.ncd test_sigals.ngd test_sigals.pcf
Target Device  : xc3s500e
Target Package : fg320
Target Speed   : -5
Mapper Version : spartan3e -- $Revision: 1.55 $
Mapped Date    : Wed Oct 09 23:01:16 2019

Design Summary
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Number of errors:      0
Number of warnings:    0
Logic Utilization:
  Number of Slice Flip Flops:            52 out of   9,312    1%
  Number of 4 input LUTs:                96 out of   9,312    1%
Logic Distribution:
  Number of occupied Slices:             67 out of   4,656    1%
    Number of Slices containing only related logic:      67 out of      67 100%
    Number of Slices containing unrelated logic:          0 out of      67   0%
      *See NOTES below for an explanation of the effects of unrelated logic.
  Total Number of 4 input LUTs:         119 out of   9,312    1%
    Number used as logic:                90
    Number used as a route-thru:         23
    Number used for Dual Port RAMs:       6
      (Two LUTs used per Dual Port RAM)

  The Slice Logic Distribution report is not meaningful if the design is
  over-mapped for a non-slice resource or if Placement fails.

  Number of bonded IOBs:                 17 out of     232    7%
  Number of BUFGMUXs:                     1 out of      24    4%

Average Fanout of Non-Clock Nets:                3.30

Peak Memory Usage:  4444 MB
Total REAL time to MAP completion:  1 secs
Total CPU time to MAP completion:   1 secs

NOTES:

   Related logic is defined as being logic that shares connectivity - e.g. two
   LUTs are "related" if they share common inputs.  When assembling slices,
   Map gives priority to combine logic that is related.  Doing so results in
   the best timing performance.

   Unrelated logic shares no connectivity.  Map will only begin packing
   unrelated logic into a slice once 99% of the slices are occupied through
   related logic packing.

   Note that once logic distribution reaches the 99% level through related
   logic packing, this does not mean the device is completely utilized.
   Unrelated logic packing will then begin, continuing until all usable LUTs
   and FFs are occupied.  Depending on your timing budget, increased levels of
   unrelated logic packing may adversely affect the overall timing performance
   of your design.
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Table of Contents

Section 1 - Errors

Section 2 - Warnings

Section 3 - Informational

INFO:LIT:243 - Logical network top/sram_top/memory/Mram_mem3/SPO has no load.
INFO:LIT:395 - The above info message is repeated 2 more times for the following
   (max. 5 shown):
   top/sram_top/memory/Mram_mem1/SPO,
   top/sram_top/memory/Mram_mem2/SPO
   To see the details of these info messages, please use the -detail switch.
INFO:MapLib:562 - No environment variables are currently set.
INFO:LIT:244 - All of the single ended outputs in this design are using slew
   rate limited output drivers. The delay on speed critical single ended outputs
   can be dramatically reduced by designating them as fast outputs.

Section 4 - Removed Logic Summary
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   2 block(s) optimized away

Section 5 - Removed Logic

Optimized Block(s):
TYPE   BLOCK
GND   XST_GND
VCC   XST_VCC

To enable printing of redundant blocks removed and signals merged, set the
detailed map report option and rerun map.

Section 6 - IOB Properties

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| IOB Name | Type | Direction | IO Standard | Diff | Drive | Slew | Reg (s) | Resistor | IOB | |
| Term | Strength | Rate | | | Delay |
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clk_in	IBUF	INPUT	LVCMOS25
		0 / 0	
data_out<0>	IOB	OUTPUT	LVCMOS25
12	SLOW		
		0 / 0	
data_out<1>	IOB	OUTPUT	LVCMOS25
12	SLOW		
		0 / 0	
data_out<2>	IOB	OUTPUT	LVCMOS25
12	SLOW		
		0 / 0	
enable_rd	IBUF	INPUT	LVCMOS25
		0 / 0	
enable_wr	IBUF	INPUT	LVCMOS25
		0 / 0	
f_almost_empty	IOB	OUTPUT	LVCMOS25
12	SLOW		
		0 / 0	
f_almost_full	IOB	OUTPUT	LVCMOS25
12	SLOW		
		0 / 0	
f_empty	IOB	OUTPUT	LVCMOS25
12	SLOW		
		0 / 0	
f_full	IOB	OUTPUT	LVCMOS25
12	SLOW		
		0 / 0	
q_out<0>	IOB	OUTPUT	LVCMOS25
12	SLOW		
		0 / 0	
q_out<1>	IOB	OUTPUT	LVCMOS25
12	SLOW		
		0 / 0	
q_out<2>	IOB	OUTPUT	LVCMOS25
12	SLOW		
		0 / 0	
q_out<3>	IOB	OUTPUT	LVCMOS25
12	SLOW		
		0 / 0	
q_out<4>	IOB	OUTPUT	LVCMOS25
12	SLOW		
		0 / 0	
reset_in	IBUF	INPUT	LVCMOS25
		0 / 0	
reset_n	IBUF	INPUT	LVCMOS25
		0 / 0	

Section 7 - RPMs

Section 8 - Guide Report

Guide not run on this design.

Section 9 - Area Group and Partition Summary

Partition Implementation Status

No Partitions were found in this design.

Area Group Information

No area groups were found in this design.

Section 10 - Timing Report

This design was not run using timing mode.

Section 11 - Configuration String Details

Use the "-detail" map option to print out Configuration Strings

Section 12 - Control Set Information

No control set information for this architecture.

Section 13 - Utilization by Hierarchy

Use the "-detail" map option to print out the Utilization by Hierarchy section.