```
Release 14.7 - xst P.20131013 (nt64)
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--> Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.19 secs

--> Parameter xsthdpdir set to xst


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.20 secs

--> Reading design: test_sigals.prj

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=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "test_sigals.prj"
Input Format                       : mixed
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "test_sigals"
Output Format                      : NGC
Target Device                      : xc3s500e-5-fg320

---- Source Options
Top Module Name                    : test_sigals
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Mux Style                          : Auto
Decoder Extraction                 : YES
Priority Encoder Extraction        : Yes
Shift Register Extraction          : YES
Logical Shifter Extraction         : YES
XOR Collapsing                     : YES
```

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ROM Style                          : Auto
Mux Extraction                     : Yes
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Multiplier Style                   : Auto
Automatic Register Balancing       : No

---- Target Options
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 16
Register Duplication               : YES
Slice Packing                      : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Auto
Use Synchronous Set                : Auto
Use Synchronous Reset              : Auto
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES

---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
Verilog 2001                       : YES
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5

=========================================================================


=========================================================================
*                           HDL Compilation                             *
=========================================================================
Compiling verilog file "../flag_logic/flag_logic_8/wr_ptr_diff.v" in library work
Compiling verilog file "../flag_logic/flag_logic_8/flag_logic_wr.v" in library work
Module <wr_ptr_diff> compiled
Compiling verilog file "../flag_logic/flag_logic_7/rd_ptr_diff.v" in library work
Module <flag_logic_wr> compiled
Compiling verilog file "../flag_logic/flag_logic_7/rd_flag_logic.v" in library work
Module <rd_ptr_diff> compiled
Compiling verilog file "../flag_logic/flag_logic_8/flag_top_wr.v" in library work
Module <rd_flag_logic> compiled
Compiling verilog file "../flag_logic/flag_logic_7/flag_logic_top_rd.v" in library work
Compiling verilog include file "para.h"
Module <flag_top_wr> compiled
Compiling verilog file "sync_basic_top_1.v" in library work
Compiling verilog include file "para.h"
Module <flag_logic_top_rd> compiled
Compiling verilog file "gray_to_bin_top_1.v" in library work
```

```
Compiling verilog include file "para.h"
Module <sync_basic_top_1> compiled
Compiling verilog file "dpsram_basic_top_1.v" in library work
Compiling verilog include file "para.h"
Module <gray_to_bin_top_1> compiled
Compiling verilog file "bin_to_gray_top_1.v" in library work
Compiling verilog include file "para.h"
Module <dpsram_basic_top_1> compiled
Compiling verilog file "binary_up_counter.v" in library work
Compiling verilog include file "para.h"
Module <bin_to_gray_top_1> compiled
Compiling verilog file "../flag_logic/flag_logic_top_1.v" in library work
Compiling verilog include file "para.h"
Module <binary_up_counter> compiled
Compiling verilog file "wr_ptr_sync_top_1.v" in library work
Compiling verilog include file "para.h"
Module <flag_logic_top_1> compiled
Compiling verilog file "write_control_top_1.v" in library work
Compiling verilog include file "para.h"
Module <wr_ptr_sync_top_1> compiled
Compiling verilog file "read_control_top_1.v" in library work
Compiling verilog include file "para.h"
Module <write_control_top_1> compiled
Compiling verilog file "rd_ptr_sync_top_1.v" in library work
Compiling verilog include file "para.h"
Module <read_control_top_1> compiled
Compiling verilog file "dpsram_top_1.v" in library work
Compiling verilog include file "para.h"
Module <rd_ptr_sync_top_1> compiled
Compiling verilog file "fifo_top_1.v" in library work
Compiling verilog include file "para.h"
Module <dpsram_top_1> compiled
Compiling verilog file "test_sigals.v" in library work
Module <fifo_top_1> compiled
Module <test_sigals> compiled
No errors in compilation
Analysis of file <"test_sigals.prj"> succeeded.


=========================================================================
*                     Design Hierarchy Analysis                         *
=========================================================================
Analyzing hierarchy for module <test_sigals> in library <work>.

Analyzing hierarchy for module <fifo_top_1> in library <work>.

Analyzing hierarchy for module <dpsram_top_1> in library <work>.

Analyzing hierarchy for module <read_control_top_1> in library <work>.

Analyzing hierarchy for module <write_control_top_1> in library <work>.

Analyzing hierarchy for module <wr_ptr_sync_top_1> in library <work>.

Analyzing hierarchy for module <rd_ptr_sync_top_1> in library <work>.

Analyzing hierarchy for module <flag_logic_top_1> in library <work>.

Analyzing hierarchy for module <dpsram_basic_top_1> in library <work>.

Analyzing hierarchy for module <binary_up_counter> in library <work>.
```

```
Analyzing hierarchy for module <bin_to_gray_top_1> in library <work>.

Analyzing hierarchy for module <sync_basic_top_1> in library <work>.

Analyzing hierarchy for module <gray_to_bin_top_1> in library <work> with parameters.
        a_length = "00000000000000000000000000000011"

Analyzing hierarchy for module <flag_logic_top_rd> in library <work>.

Analyzing hierarchy for module <flag_top_wr> in library <work> with parameters.
        a_length = "00000000000000000000000000000011"

Analyzing hierarchy for module <rd_ptr_diff> in library <work> with parameters.
        a_length = "00000000000000000000000000000011"
        config_depth = "111"

Analyzing hierarchy for module <rd_flag_logic> in library <work> with parameters.
        a_length = "00000000000000000000000000000011"
        f_a_empty = "00000000000000000000000000000010"

Analyzing hierarchy for module <wr_ptr_diff> in library <work> with parameters.
        a_length = "00000000000000000000000000000011"
        config_depth = "111"

Analyzing hierarchy for module <flag_logic_wr> in library <work> with parameters.
        a_length = "00000000000000000000000000000011"
        f_a_full = "00000000000000000000000000000110"


=========================================================================
*                            HDL Analysis                               *
=========================================================================
Analyzing top module <test_sigals>.
Module <test_sigals> is correct for synthesis.

Analyzing module <fifo_top_1> in library <work>.
Module <fifo_top_1> is correct for synthesis.

Analyzing module <dpsram_top_1> in library <work>.
Module <dpsram_top_1> is correct for synthesis.

Analyzing module <dpsram_basic_top_1> in library <work>.
Module <dpsram_basic_top_1> is correct for synthesis.

Analyzing module <read_control_top_1> in library <work>.
Module <read_control_top_1> is correct for synthesis.

Analyzing module <binary_up_counter> in library <work>.
Module <binary_up_counter> is correct for synthesis.

Analyzing module <write_control_top_1> in library <work>.
Module <write_control_top_1> is correct for synthesis.

Analyzing module <wr_ptr_sync_top_1> in library <work>.
Module <wr_ptr_sync_top_1> is correct for synthesis.

Analyzing module <bin_to_gray_top_1> in library <work>.
Module <bin_to_gray_top_1> is correct for synthesis.

Analyzing module <sync_basic_top_1> in library <work>.
```

```
Module <sync_basic_top_1> is correct for synthesis.

Analyzing module <gray_to_bin_top_1> in library <work>.
        a_length = 32'sb00000000000000000000000000000011
Module <gray_to_bin_top_1> is correct for synthesis.

Analyzing module <rd_ptr_sync_top_1> in library <work>.
Module <rd_ptr_sync_top_1> is correct for synthesis.

Analyzing module <flag_logic_top_1> in library <work>.
Module <flag_logic_top_1> is correct for synthesis.

Analyzing module <flag_logic_top_rd> in library <work>.
Module <flag_logic_top_rd> is correct for synthesis.

Analyzing module <rd_ptr_diff> in library <work>.
        a_length = 32'sb00000000000000000000000000000011
        config_depth = 3'b111
Module <rd_ptr_diff> is correct for synthesis.

Analyzing module <rd_flag_logic> in library <work>.
        a_length = 32'sb00000000000000000000000000000011
        f_a_empty = 32'sb00000000000000000000000000000010
Module <rd_flag_logic> is correct for synthesis.

Analyzing module <flag_top_wr> in library <work>.
        a_length = 32'sb00000000000000000000000000000011
Module <flag_top_wr> is correct for synthesis.

Analyzing module <wr_ptr_diff> in library <work>.
        a_length = 32'sb00000000000000000000000000000011
        config_depth = 3'b111
Module <wr_ptr_diff> is correct for synthesis.

Analyzing module <flag_logic_wr> in library <work>.
        a_length = 32'sb00000000000000000000000000000011
        f_a_full = 32'sb00000000000000000000000000000110
Module <flag_logic_wr> is correct for synthesis.


=========================================================================
*                            HDL Synthesis                              *
=========================================================================

Performing bidirectional port resolution...

Synthesizing Unit <dpsram_basic_top_1>.
    Related source file is "dpsram_basic_top_1.v".
    Found 8x3-bit dual-port RAM <Mram_mem> for signal <mem>.
    Found 3-bit register for signal <data_out_port1>.
    Found 3-bit register for signal <data_out_port2>.
    Summary:
        inferred   1 RAM(s).
        inferred   6 D-type flip-flop(s).
Unit <dpsram_basic_top_1> synthesized.


Synthesizing Unit <binary_up_counter>.
    Related source file is "binary_up_counter.v".
    Found 4-bit up counter for signal <b_count_ptr>.
    Summary:
```

```
        inferred   1 Counter(s).
Unit <binary_up_counter> synthesized.


Synthesizing Unit <bin_to_gray_top_1>.
    Related source file is "bin_to_gray_top_1.v".
    Found 2-bit xor2 for signal <data_out<1:0>>.
Unit <bin_to_gray_top_1> synthesized.


Synthesizing Unit <sync_basic_top_1>.
    Related source file is "sync_basic_top_1.v".
    Found 3-bit register for signal <data_out>.
    Found 3-bit register for signal <dff_1>.
    Summary:
        inferred   6 D-type flip-flop(s).
Unit <sync_basic_top_1> synthesized.


Synthesizing Unit <gray_to_bin_top_1>.
    Related source file is "gray_to_bin_top_1.v".
    Found 1-bit xor2 for signal <data_out<0>>.
    Found 1-bit xor2 for signal <data_out_0$xor0000> created at line 22.
Unit <gray_to_bin_top_1> synthesized.


Synthesizing Unit <rd_ptr_diff>.
    Related source file is "../flag_logic/flag_logic_7/rd_ptr_diff.v".
    Found 3-bit addsub for signal <ptr_diff_rd$addsub0000>.
    Found 3-bit adder for signal <ptr_diff_rd$addsub0001> created at line 37.
    Found 3-bit comparator greatequal for signal <ptr_diff_rd$cmp_ge0000> created at line
34.
    Summary:
        inferred   2 Adder/Subtractor(s).
        inferred   1 Comparator(s).
Unit <rd_ptr_diff> synthesized.


Synthesizing Unit <rd_flag_logic>.
    Related source file is "../flag_logic/flag_logic_7/rd_flag_logic.v".
    Found 1-bit xor2 for signal <w1>.
Unit <rd_flag_logic> synthesized.


Synthesizing Unit <wr_ptr_diff>.
    Related source file is "../flag_logic/flag_logic_8/wr_ptr_diff.v".
    Found 3-bit addsub for signal <ptr_diff_wr$addsub0000>.
    Found 3-bit adder for signal <ptr_diff_wr$addsub0001> created at line 40.
    Found 3-bit comparator greatequal for signal <ptr_diff_wr$cmp_ge0000> created at line
36.
    Summary:
        inferred   2 Adder/Subtractor(s).
        inferred   1 Comparator(s).
Unit <wr_ptr_diff> synthesized.


Synthesizing Unit <flag_logic_wr>.
    Related source file is "../flag_logic/flag_logic_8/flag_logic_wr.v".
    Found 1-bit xor2 for signal <w1>.
Unit <flag_logic_wr> synthesized.
```

```
Synthesizing Unit <dpsram_top_1>.
    Related source file is "dpsram_top_1.v".
    Found 3-bit tristate buffer for signal <idle_pin_2>.
    Summary:
        inferred   3 Tristate(s).
Unit <dpsram_top_1> synthesized.


Synthesizing Unit <read_control_top_1>.
    Related source file is "read_control_top_1.v".
Unit <read_control_top_1> synthesized.


Synthesizing Unit <write_control_top_1>.
    Related source file is "write_control_top_1.v".
Unit <write_control_top_1> synthesized.


Synthesizing Unit <wr_ptr_sync_top_1>.
    Related source file is "wr_ptr_sync_top_1.v".
Unit <wr_ptr_sync_top_1> synthesized.


Synthesizing Unit <rd_ptr_sync_top_1>.
    Related source file is "rd_ptr_sync_top_1.v".
Unit <rd_ptr_sync_top_1> synthesized.


Synthesizing Unit <flag_logic_top_rd>.
    Related source file is "../flag_logic/flag_logic_7/flag_logic_top_rd.v".
Unit <flag_logic_top_rd> synthesized.


Synthesizing Unit <flag_top_wr>.
    Related source file is "../flag_logic/flag_logic_8/flag_top_wr.v".
Unit <flag_top_wr> synthesized.


Synthesizing Unit <flag_logic_top_1>.
    Related source file is "../flag_logic/flag_logic_top_1.v".
Unit <flag_logic_top_1> synthesized.


Synthesizing Unit <fifo_top_1>.
    Related source file is "fifo_top_1.v".
Unit <fifo_top_1> synthesized.


Synthesizing Unit <test_sigals>.
    Related source file is "test_sigals.v".
    Found 5-bit up counter for signal <q_out>.
    Found 24-bit up counter for signal <clk_tmp>.
    Summary:
        inferred   2 Counter(s).
Unit <test_sigals> synthesized.

INFO:Xst:1767 - HDL ADVISOR - Resource sharing has identified that some arithmetic
operations in this design can share the same physical resources for reduced device
utilization. For improved clock frequency you may try to disable resource sharing.
```

```
=========================================================================
HDL Synthesis Report

Macro Statistics
# RAMs                                                  : 1
 8x3-bit dual-port RAM                                  : 1
# Adders/Subtractors                                    : 4
 3-bit adder                                            : 2
 3-bit addsub                                           : 2
# Counters                                              : 4
 24-bit up counter                                      : 1
 4-bit up counter                                       : 2
 5-bit up counter                                       : 1
# Registers                                             : 6
 3-bit register                                         : 6
# Comparators                                           : 2
 3-bit comparator greatequal                            : 2
# Tristates                                             : 3
 1-bit tristate buffer                                  : 3
# Xors                                                  : 10
 1-bit xor2                                             : 10

=========================================================================

=========================================================================
*                        Advanced HDL Synthesis                         *
=========================================================================

WARNING:Xst:2404 -  FFs/Latches <data_out_port1<2:0>> (without init value) have a constant
value of 0 in block <dpsram_basic_top_1>.

Synthesizing (advanced) Unit <dpsram_basic_top_1>.
INFO:Xst:3231 - The small RAM <Mram_mem> will be implemented on LUTs in order to maximize
performance and save block RAM resources. If you want to force its implementation on
block, use option/constraint ram_style.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                         |          |
    -----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 8-word x 3-bit                      |          |
    |     clkA           | connected to signal <clk_port1>     | rise     |
    |     weA            | connected to signal <en_port1>      | high     |
    |     addrA          | connected to signal <addr_in_port1> |          |
    |     diA            | connected to signal <data_in_port1> |          |
    -----------------------------------------------------------------------
    | Port B                                                               |
    |     aspect ratio   | 8-word x 3-bit                      |          |
    |     addrB          | connected to signal <addr_in_port2> |          |
    |     doB            | connected to internal node          |          |
    -----------------------------------------------------------------------
Unit <dpsram_basic_top_1> synthesized (advanced).

=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# RAMs                                                  : 1
 8x3-bit dual-port distributed RAM                      : 1
# Adders/Subtractors                                    : 4
 3-bit adder                                            : 2
 3-bit addsub                                           : 2
```

```
# Counters                                              : 4
 24-bit up counter                                     : 1
 4-bit up counter                                      : 2
 5-bit up counter                                      : 1
# Registers                                             : 15
 Flip-Flops                                            : 15
# Comparators                                           : 2
 3-bit comparator greatequal                           : 2
# Xors                                                  : 10
 1-bit xor2                                            : 10

=========================================================================

=========================================================================
*                          Low Level Synthesis                          *
=========================================================================

Optimizing unit <test_sigals> ...

Optimizing unit <rd_ptr_diff> ...

Optimizing unit <wr_ptr_diff> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block test_sigals, actual ratio is 0.

Final Macro Processing ...

=========================================================================
Final Register Report

Macro Statistics
# Registers                                             : 52
 Flip-Flops                                            : 52

=========================================================================

=========================================================================
*                           Partition Report                            *
=========================================================================

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

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=========================================================================
*                            Final Report                               *
=========================================================================
Final Results
RTL Top Level Output File Name     : test_sigals.ngr
Top Level Output File Name         : test_sigals
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 17
```

```
Cell Usage :
# BELS                          : 169
#      GND                     : 1
#      INV                     : 5
#      LUT1                    : 23
#      LUT2                    : 8
#      LUT2_D                  : 2
#      LUT2_L                  : 1
#      LUT3                    : 11
#      LUT4                    : 49
#      LUT4_D                  : 5
#      LUT4_L                  : 11
#      MUXCY                   : 23
#      MUXF5                   : 5
#      VCC                     : 1
#      XORCY                   : 24
# FlipFlops/Latches            : 52
#      FD                      : 3
#      FDC                     : 44
#      FDR                     : 5
# RAMS                         : 3
#      RAM16X1D                : 3
# Clock Buffers                : 1
#      BUFGP                   : 1
# IO Buffers                   : 16
#      IBUF                    : 4
#      OBUF                    : 12
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s500efg320-5

 Number of Slices:                       61  out of   4656     1%
 Number of Slice Flip Flops:             52  out of   9312     0%
 Number of 4 input LUTs:                121  out of   9312     1%
    Number used as logic:               115
    Number used as RAMs:                  6
 Number of IOs:                          17
 Number of bonded IOBs:                  17  out of    232     7%
 Number of GCLKs:                         1  out of     24     4%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

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=========================================================================
TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
```

```
------------------
-----------------------------------+-----------------------------------------+-------+
Clock Signal                       | Clock buffer(FF name)                   | Load  |
-----------------------------------+-----------------------------------------+-------+
q_out_0                            | NONE(top/rd_sync_top/sync_2/data_out_2)| 13    |
q_out_4                            | NONE(top/wr_sync_top/sync_1/data_out_2)| 13    |
clk_in                             | BUFGP                                   | 24    |
clk_tmp_23                         | NONE(q_out_0)                           | 5     |
-----------------------------------+-----------------------------------------+-------+
INFO:Xst:2169 - HDL ADVISOR - Some clock signals were not automatically buffered by XST
with BUFG/BUFR resources. Please use the buffer_type constraint in order to insert these
buffers to the clock signals to help prevent skew problems.

Asynchronous Control Signals Information:
----------------------------------------
-----------------------------------+-----------------------------------------+-------+
Control Signal                     | Buffer(FF name)                         | Load  |
-----------------------------------+-----------------------------------------+-------+
reset_in_inv(reset_in_inv1_INV_0:O)| NONE(clk_tmp_0)                         | 24    |
reset_n_inv(reset_n_inv1_INV_0:O)  | NONE(top/rd_ctrl_top/i_2/b_count_ptr_0)| 20    |
-----------------------------------+-----------------------------------------+-------+

Timing Summary:
---------------
Speed Grade: -5

   Minimum period: 7.231ns (Maximum Frequency: 138.303MHz)
   Minimum input arrival time before clock: 6.066ns
   Maximum output required time after clock: 11.488ns
   Maximum combinational path delay: 8.866ns

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'q_out_0'
  Clock period: 6.713ns (frequency: 148.958MHz)
  Total number of paths / destination ports: 450 / 19
-------------------------------------------------------------------------
Delay:               6.713ns (Levels of Logic = 5)
  Source:            top/wr_ctrl_top/i_1/b_count_ptr_0 (FF)
  Destination:       top/wr_ctrl_top/i_1/b_count_ptr_2 (FF)
  Source Clock:      q_out_0 rising
  Destination Clock: q_out_0 rising

  Data Path: top/wr_ctrl_top/i_1/b_count_ptr_0 to top/wr_ctrl_top/i_1/b_count_ptr_2
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDC:C->Q             23   0.514   1.025  top/wr_ctrl_top/i_1/b_count_ptr_0
(top/wr_ctrl_top/i_1/b_count_ptr_0)
     LUT4:I3->O            1   0.612   0.387
top/flag_logic_top/full/ptr_diff_wr/ptr_diff_wr_cmp_ge00001_SW0 (N73)
     LUT4:I2->O            6   0.612   0.572
top/flag_logic_top/full/ptr_diff_wr/ptr_diff_wr_cmp_ge00001
(top/flag_logic_top/full/ptr_diff_wr/ptr_diff_wr_cmp_ge00002)
     LUT4:I3->O            4   0.612   0.499  top/wr_ctrl_top/enable_wr_out_SW0_SW0 (N26)
     MUXF5:S->O            1   0.641   0.360  top/wr_ctrl_top/enable_wr_out_SW4 (N82)
     LUT4:I3->O            1   0.612   0.000  top/wr_ctrl_top/i_1/b_count_ptr_2_rstpot
(top/wr_ctrl_top/i_1/b_count_ptr_2_rstpot)
```

```
     FDC:D                     0.268          top/wr_ctrl_top/i_1/b_count_ptr_2
    ----------------------------------------
    Total                      6.713ns (3.871ns logic, 2.842ns route)
                                       (57.7% logic, 42.3% route)

=========================================================================
Timing constraint: Default period analysis for Clock 'q_out_4'
  Clock period: 7.231ns (frequency: 138.303MHz)
  Total number of paths / destination ports: 490 / 10
-------------------------------------------------------------------------
Delay:               7.231ns (Levels of Logic = 6)
  Source:            top/rd_ctrl_top/i_2/b_count_ptr_0 (FF)
  Destination:       top/rd_ctrl_top/i_2/b_count_ptr_0 (FF)
  Source Clock:      q_out_4 rising
  Destination Clock: q_out_4 rising

  Data Path: top/rd_ctrl_top/i_2/b_count_ptr_0 to top/rd_ctrl_top/i_2/b_count_ptr_0
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDC:C->Q             15   0.514   0.894  top/rd_ctrl_top/i_2/b_count_ptr_0
(top/rd_ctrl_top/i_2/b_count_ptr_0)
     LUT4:I2->O            1   0.612   0.360
top/flag_logic_top/empty/ptr_diff_rd/ptr_diff_rd_cmp_ge00001_SW1 (N43)
     LUT4:I3->O           11   0.612   0.796
top/flag_logic_top/empty/ptr_diff_rd/ptr_diff_rd_cmp_ge00001
(top/flag_logic_top/empty/ptr_diff_rd/ptr_diff_rd_cmp_ge00002)
     LUT4:I3->O            1   0.612   0.000
top/flag_logic_top/empty/ptr_diff_rd/ptr_diff_rd<2>_SW0_G (N128)
     MUXF5:I1->O           1   0.278   0.360
top/flag_logic_top/empty/ptr_diff_rd/ptr_diff_rd<2>_SW0 (N16)
     LUT4:I3->O            9   0.612   0.700
top/flag_logic_top/empty/ptr_diff_rd/ptr_diff_rd<2>
(top/flag_logic_top/empty/temp_ptr_diff_rd<2>)
     LUT4:I3->O            1   0.612   0.000  top/sram_top/memory/data_out_port2_2_rstpot
(top/sram_top/memory/data_out_port2_2_rstpot)
     FD:D                      0.268          top/sram_top/memory/data_out_port2_2
    ----------------------------------------
    Total                      7.231ns (4.120ns logic, 3.111ns route)
                                       (57.0% logic, 43.0% route)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk_in'
  Clock period: 4.088ns (frequency: 244.648MHz)
  Total number of paths / destination ports: 300 / 24
-------------------------------------------------------------------------
Delay:               4.088ns (Levels of Logic = 24)
  Source:            clk_tmp_1 (FF)
  Destination:       clk_tmp_23 (FF)
  Source Clock:      clk_in rising
  Destination Clock: clk_in rising

  Data Path: clk_tmp_1 to clk_tmp_23
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDC:C->Q              1   0.514   0.509  clk_tmp_1 (clk_tmp_1)
     LUT1:I0->O            1   0.612   0.000  Mcount_clk_tmp_cy<1>_rt
(Mcount_clk_tmp_cy<1>_rt)
     MUXCY:S->O            1   0.404   0.000  Mcount_clk_tmp_cy<1> (Mcount_clk_tmp_cy<1>)
     MUXCY:CI->O           1   0.052   0.000  Mcount_clk_tmp_cy<2> (Mcount_clk_tmp_cy<2>)
```

```
     MUXCY:CI->O           1   0.051   0.000  Mcount_clk_tmp_cy<3> (Mcount_clk_tmp_cy<3>)
     MUXCY:CI->O           1   0.051   0.000  Mcount_clk_tmp_cy<4> (Mcount_clk_tmp_cy<4>)
     MUXCY:CI->O           1   0.051   0.000  Mcount_clk_tmp_cy<5> (Mcount_clk_tmp_cy<5>)
     MUXCY:CI->O           1   0.051   0.000  Mcount_clk_tmp_cy<6> (Mcount_clk_tmp_cy<6>)
     MUXCY:CI->O           1   0.051   0.000  Mcount_clk_tmp_cy<7> (Mcount_clk_tmp_cy<7>)
     MUXCY:CI->O           1   0.051   0.000  Mcount_clk_tmp_cy<8> (Mcount_clk_tmp_cy<8>)
     MUXCY:CI->O           1   0.051   0.000  Mcount_clk_tmp_cy<9> (Mcount_clk_tmp_cy<9>)
     MUXCY:CI->O           1   0.051   0.000  Mcount_clk_tmp_cy<10> (Mcount_clk_tmp_cy<10>)
     MUXCY:CI->O           1   0.051   0.000  Mcount_clk_tmp_cy<11> (Mcount_clk_tmp_cy<11>)
     MUXCY:CI->O           1   0.051   0.000  Mcount_clk_tmp_cy<12> (Mcount_clk_tmp_cy<12>)
     MUXCY:CI->O           1   0.051   0.000  Mcount_clk_tmp_cy<13> (Mcount_clk_tmp_cy<13>)
     MUXCY:CI->O           1   0.051   0.000  Mcount_clk_tmp_cy<14> (Mcount_clk_tmp_cy<14>)
     MUXCY:CI->O           1   0.051   0.000  Mcount_clk_tmp_cy<15> (Mcount_clk_tmp_cy<15>)
     MUXCY:CI->O           1   0.051   0.000  Mcount_clk_tmp_cy<16> (Mcount_clk_tmp_cy<16>)
     MUXCY:CI->O           1   0.051   0.000  Mcount_clk_tmp_cy<17> (Mcount_clk_tmp_cy<17>)
     MUXCY:CI->O           1   0.051   0.000  Mcount_clk_tmp_cy<18> (Mcount_clk_tmp_cy<18>)
     MUXCY:CI->O           1   0.051   0.000  Mcount_clk_tmp_cy<19> (Mcount_clk_tmp_cy<19>)
     MUXCY:CI->O           1   0.051   0.000  Mcount_clk_tmp_cy<20> (Mcount_clk_tmp_cy<20>)
     MUXCY:CI->O           1   0.051   0.000  Mcount_clk_tmp_cy<21> (Mcount_clk_tmp_cy<21>)
     MUXCY:CI->O           0   0.051   0.000  Mcount_clk_tmp_cy<22> (Mcount_clk_tmp_cy<22>)
     XORCY:CI->O           1   0.699   0.000  Mcount_clk_tmp_xor<23> (Result<23>)
     FDC:D                     0.268          clk_tmp_23
    ----------------------------------------
    Total                      4.088ns (3.579ns logic, 0.509ns route)
                                       (87.5% logic, 12.5% route)

==========================================================================
Timing constraint: Default period analysis for Clock 'clk_tmp_23'
  Clock period: 3.345ns (frequency: 298.931MHz)
  Total number of paths / destination ports: 15 / 5
--------------------------------------------------------------------------
Delay:               3.345ns (Levels of Logic = 2)
  Source:            q_out_0 (FF)
  Destination:       q_out_4 (FF)
  Source Clock:      clk_tmp_23 rising
  Destination Clock: clk_tmp_23 rising

  Data Path: q_out_0 to q_out_4
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDR:C->Q             19   0.514   0.952  q_out_0 (q_out_0)
     LUT3:I2->O            1   0.612   0.387  Mcount_q_out_xor<3>111 (N5)
     LUT3:I2->O            1   0.612   0.000  Mcount_q_out_xor<4>11 (Result<4>1)
     FDR:D                     0.268          q_out_4
    ----------------------------------------
    Total                      3.345ns (2.006ns logic, 1.339ns route)
                                       (60.0% logic, 40.0% route)

==========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'q_out_0'
  Total number of paths / destination ports: 40 / 7
--------------------------------------------------------------------------
Offset:              5.187ns (Levels of Logic = 4)
  Source:            reset_n (PAD)
  Destination:       top/wr_ctrl_top/i_1/b_count_ptr_2 (FF)
  Destination Clock: q_out_0 rising

  Data Path: reset_n to top/wr_ctrl_top/i_1/b_count_ptr_2
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
```

```
    ----------------------------------------  ------------
     IBUF:I->O            20   1.106   1.089  reset_n_IBUF (reset_n_IBUF)
     LUT4:I0->O            4   0.612   0.499  top/wr_ctrl_top/enable_wr_out_SW0_SW0 (N26)
     MUXF5:S->O            1   0.641   0.360  top/wr_ctrl_top/enable_wr_out_SW4 (N82)
     LUT4:I3->O            1   0.612   0.000  top/wr_ctrl_top/i_1/b_count_ptr_2_rstpot
(top/wr_ctrl_top/i_1/b_count_ptr_2_rstpot)
     FDC:D                     0.268          top/wr_ctrl_top/i_1/b_count_ptr_2
    ----------------------------------------
    Total                      5.187ns (3.239ns logic, 1.948ns route)
                                       (62.4% logic, 37.6% route)

==========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk_tmp_23'
  Total number of paths / destination ports: 5 / 5
--------------------------------------------------------------------------
Offset:              3.942ns (Levels of Logic = 2)
  Source:            reset_in (PAD)
  Destination:       q_out_0 (FF)
  Destination Clock: clk_tmp_23 rising

  Data Path: reset_in to q_out_0
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             1   1.106   0.357  reset_in_IBUF (reset_in_IBUF)
     INV:I->O             29   0.612   1.072  reset_in_inv1_INV_0 (reset_in_inv)
     FDR:R                     0.795          q_out_0
    ----------------------------------------
    Total                      3.942ns (2.513ns logic, 1.429ns route)
                                       (63.7% logic, 36.3% route)

==========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'q_out_4'
  Total number of paths / destination ports: 58 / 7
--------------------------------------------------------------------------
Offset:              6.066ns (Levels of Logic = 5)
  Source:            reset_n (PAD)
  Destination:       top/rd_ctrl_top/i_2/b_count_ptr_2 (FF)
  Destination Clock: q_out_4 rising

  Data Path: reset_n to top/rd_ctrl_top/i_2/b_count_ptr_2
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            20   1.106   1.089  reset_n_IBUF (reset_n_IBUF)
     LUT2:I0->O            3   0.612   0.454  top/rd_ctrl_top/enable_rd_out_SW0_SW0_SW1
(N37)
     LUT4:I3->O            2   0.612   0.532  top/rd_ctrl_top/enable_rd_out_SW11 (N69)
     LUT4_L:I0->LO         1   0.612   0.169  top/rd_ctrl_top/enable_rd_out_SW10 (N68)
     LUT4:I1->O            1   0.612   0.000  top/rd_ctrl_top/i_2/b_count_ptr_2_rstpot
(top/rd_ctrl_top/i_2/b_count_ptr_2_rstpot)
     FDC:D                     0.268          top/rd_ctrl_top/i_2/b_count_ptr_2
    ----------------------------------------
    Total                      6.066ns (3.822ns logic, 2.244ns route)
                                       (63.0% logic, 37.0% route)

==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'q_out_4'
  Total number of paths / destination ports: 123 / 6
--------------------------------------------------------------------------
Offset:              11.488ns (Levels of Logic = 8)
```

```
  Source:            top/rd_ctrl_top/i_2/b_count_ptr_0 (FF)
  Destination:       f_empty (PAD)
  Source Clock:      q_out_4 rising

  Data Path: top/rd_ctrl_top/i_2/b_count_ptr_0 to f_empty
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDC:C->Q             15   0.514   0.894  top/rd_ctrl_top/i_2/b_count_ptr_0
(top/rd_ctrl_top/i_2/b_count_ptr_0)
     LUT4:I2->O            1   0.612   0.360
top/flag_logic_top/empty/ptr_diff_rd/ptr_diff_rd_cmp_ge00001_SW1 (N43)
     LUT4:I3->O           11   0.612   0.796
top/flag_logic_top/empty/ptr_diff_rd/ptr_diff_rd_cmp_ge00001
(top/flag_logic_top/empty/ptr_diff_rd/ptr_diff_rd_cmp_ge00002)
     LUT4:I3->O            1   0.612   0.000
top/flag_logic_top/empty/ptr_diff_rd/ptr_diff_rd<2>_SW0_G (N128)
     MUXF5:I1->O           1   0.278   0.360
top/flag_logic_top/empty/ptr_diff_rd/ptr_diff_rd<2>_SW0 (N16)
     LUT4:I3->O            9   0.612   0.700
top/flag_logic_top/empty/ptr_diff_rd/ptr_diff_rd<2>
(top/flag_logic_top/empty/temp_ptr_diff_rd<2>)
     LUT4:I3->O            1   0.612   0.387  top/flag_logic_top/empty/flag_rd/f_empty_SW1
(N125)
     LUT4:I2->O            1   0.612   0.357  top/flag_logic_top/empty/flag_rd/f_empty
(f_empty_OBUF)
     OBUF:I->O                 3.169          f_empty_OBUF (f_empty)
    ----------------------------------------
    Total                     11.488ns (7.633ns logic, 3.855ns route)
                                       (66.4% logic, 33.6% route)

==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'q_out_0'
  Total number of paths / destination ports: 118 / 3
--------------------------------------------------------------------------
Offset:              10.164ns (Levels of Logic = 6)
  Source:            top/wr_ctrl_top/i_1/b_count_ptr_0 (FF)
  Destination:       f_full (PAD)
  Source Clock:      q_out_0 rising

  Data Path: top/wr_ctrl_top/i_1/b_count_ptr_0 to f_full
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDC:C->Q             23   0.514   1.025  top/wr_ctrl_top/i_1/b_count_ptr_0
(top/wr_ctrl_top/i_1/b_count_ptr_0)
     LUT4:I3->O            1   0.612   0.387
top/flag_logic_top/full/ptr_diff_wr/ptr_diff_wr_cmp_ge00001_SW0 (N73)
     LUT4:I2->O            6   0.612   0.572
top/flag_logic_top/full/ptr_diff_wr/ptr_diff_wr_cmp_ge00001
(top/flag_logic_top/full/ptr_diff_wr/ptr_diff_wr_cmp_ge00002)
     LUT4_D:I3->O          6   0.612   0.721
top/flag_logic_top/full/ptr_diff_wr/ptr_diff_wr<1>1
(top/flag_logic_top/full/temp_ptr_diff_wr<1>)
     LUT4:I0->O            1   0.612   0.360  top/flag_logic_top/full/flag_wr/f_full_SW1
(N123)
     LUT4:I3->O            1   0.612   0.357  top/flag_logic_top/full/flag_wr/f_full
(f_full_OBUF)
     OBUF:I->O                 3.169          f_full_OBUF (f_full)
    ----------------------------------------
    Total                     10.164ns (6.743ns logic, 3.421ns route)
```

```
                                        (66.3% logic, 33.7% route)

=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk_tmp_23'
  Total number of paths / destination ports: 5 / 5
-------------------------------------------------------------------------
Offset:              4.605ns (Levels of Logic = 1)
  Source:            q_out_0 (FF)
  Destination:       q_out<0> (PAD)
  Source Clock:      clk_tmp_23 rising

  Data Path: q_out_0 to q_out<0>
                               Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDR:C->Q             19   0.514   0.922  q_out_0 (q_out_0)
     OBUF:I->O                 3.169          q_out_0_OBUF (q_out<0>)
    ----------------------------------------
    Total                      4.605ns (3.683ns logic, 0.922ns route)
                                       (80.0% logic, 20.0% route)

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 14 / 4
-------------------------------------------------------------------------
Delay:               8.866ns (Levels of Logic = 6)
  Source:            reset_n (PAD)
  Destination:       f_full (PAD)

  Data Path: reset_n to f_full
                               Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            20   1.106   1.089  reset_n_IBUF (reset_n_IBUF)
     LUT4:I0->O            1   0.612   0.000
top/flag_logic_top/full/ptr_diff_wr/ptr_diff_wr<2>_F (N129)
     MUXF5:I0->O           7   0.278   0.671
top/flag_logic_top/full/ptr_diff_wr/ptr_diff_wr<2>
(top/flag_logic_top/full/temp_ptr_diff_wr<2>)
     LUT4:I1->O            1   0.612   0.360  top/flag_logic_top/full/flag_wr/f_full_SW1
(N123)
     LUT4:I3->O            1   0.612   0.357  top/flag_logic_top/full/flag_wr/f_full
(f_full_OBUF)
     OBUF:I->O                 3.169          f_full_OBUF (f_full)
    ----------------------------------------
    Total                      8.866ns (6.389ns logic, 2.477ns route)
                                       (72.1% logic, 27.9% route)

=========================================================================


Total REAL time to Xst completion: 5.00 secs
Total CPU time to Xst completion: 4.97 secs

-->

Total memory usage is 4537252 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    1 (   0 filtered)
Number of infos    :    3 (   0 filtered)
```