**FIFO Implementation on FPGA**

**PIN Description-**

The table given below provides all the pins which are mentioned in the micro-architecture.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Sr. No. | PIN Name | Initialization as Name | Width | I/O | PIN Description |
| 1 | Input Data | data\_in | 8 | I | Data to be written on FIFO. |
| 2 | Output Data | data\_out | 8 | O | Data to be read on FIFO. |
| 3 | Write Clock | wr\_clk | 1 | I | Clock signal of the write (input) domain. |
| 4 | Read Clock | rd\_clk | 1 | I | Clock signal of the read (output) domain. |
| 5 | Reset | rst\_in | 1 | I | Pin to clear the FIFO and starting from initial. |
| 6 | Write Enable | wr\_en | 1 | I | To enable FIFO for the write operation. |
| 7 | Read Enable | rd\_en | 1 | I | To enable FIFO for the read operation. |
| 8 | Write Pointer | wr\_ptr | 10 | I | To store the address of the location where the next write will store the data. |
| 9 | Read Pointer | rd\_ptr | 10 | I | To store the address of the location from where the next read will extract the data. |
| 10 | Empty | fifo\_empty | 1 | O | To indicate that the FIFO is empty. |
| 11 | Full | fifo\_full | 1 | O | To indicate that the FIFO is full. |
| 12 | Almost Full | fifo\_nr\_full | 1 | O | To indicate that the FIFO is almost full. |
| 13 | Almost Empty | fifo\_nr\_empty | 1 | O | To indicate that the FIFO is almost empty. |
| 14 | Half | fifo\_half | 1 | O | To indicate that the FIFO is half full or half empty. |
| 15 | Depth | dep\_sel | 10 | - | To show how much space is required for given requirements. |