
STM32
CubeMX

1. Description

1.1. Project

Project Name	NEW_COFIG
Board Name	NUCLEO-H743ZI2
Generated with:	STM32CubeMX 6.0.1
Date	09/24/2020

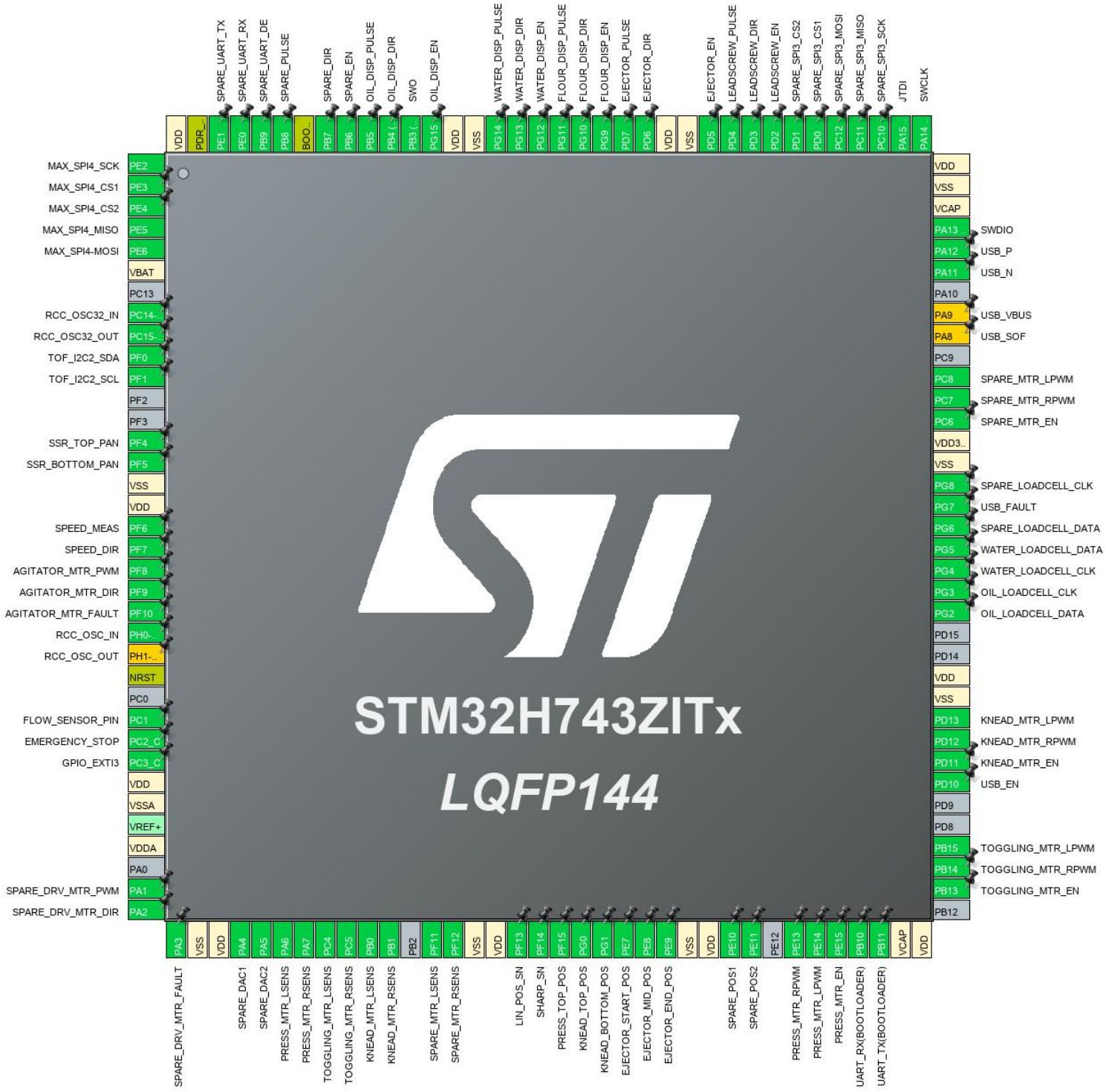
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H743/753
MCU name	STM32H743ZITx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	ARM Cortex-M7

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	SPI4_SCK	MAX_SPI4_SCK
2	PE3 *	I/O	GPIO_Output	MAX_SPI4_CS1
3	PE4 *	I/O	GPIO_Output	MAX_SPI4_CS2
4	PE5	I/O	SPI4_MISO	MAX_SPI4_MISO
5	PE6	I/O	SPI4_MOSI	MAX_SPI4-MOSI
6	VBAT	Power		
8	PC14-OSC32_IN (OSC32_IN)	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT (OSC32_OUT)	I/O	RCC_OSC32_OUT	
10	PF0	I/O	I2C2_SDA	TOF_I2C2_SDA
11	PF1	I/O	I2C2_SCL	TOF_I2C2_SCL
14	PF4 *	I/O	GPIO_Output	SSR_TOP_PAN
15	PF5 *	I/O	GPIO_Output	SSR_BOTTOM_PAN
16	VSS	Power		
17	VDD	Power		
18	PF6	I/O	TIM16_CH1	SPEED_MEAS
19	PF7 *	I/O	GPIO_Input	SPEED_DIR
20	PF8	I/O	TIM13_CH1	AGITATOR_MTR_PWM
21	PF9 *	I/O	GPIO_Output	AGITATOR_MTR_DIR
22	PF10 *	I/O	GPIO_Input	AGITATOR_MTR_FAULT
23	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
24	PH1-OSC_OUT (PH1) **	I/O	RCC_OSC_OUT	
25	NRST	Reset		
27	PC1	I/O	GPIO_EXTI1	FLOW_SENSOR_PIN
28	PC2_C	I/O	GPIO_EXTI2	EMERGENCY_STOP
29	PC3_C	I/O	GPIO_EXTI3	
30	VDD	Power		
31	VSSA	Power		
33	VDDA	Power		
35	PA1	I/O	TIM5_CH2	SPARE_DRV_MTR_PWM
36	PA2 *	I/O	GPIO_Output	SPARE_DRV_MTR_DIR
37	PA3 *	I/O	GPIO_Input	SPARE_DRV_MTR_FAULT
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	DAC1_OUT1	SPARE_DAC1

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
41	PA5	I/O	DAC1_OUT2	SPARE_DAC2
42	PA6	I/O	ADC1_INP3	PRESS_MTR_LSENS
43	PA7	I/O	ADC1_INP7	PRESS_MTR_RSENS
44	PC4	I/O	ADC1_INP4	TOGGLING_MTR_LSENS
45	PC5	I/O	ADC1_INP8	TOGGLING_MTR_RSENS
46	PB0	I/O	ADC1_INP9	KNEAD_MTR_LSENS
47	PB1	I/O	ADC1_INP5	KNEAD_MTR_RSENS
49	PF11	I/O	ADC1_INP2	SPARE_MTR_LSENS
50	PF12	I/O	ADC1_INP6	SPARE_MTR_RSENS
51	VSS	Power		
52	VDD	Power		
53	PF13	I/O	ADC2_INP2	LIN_POS_SN
54	PF14	I/O	ADC2_INP6	SHARP_SN
55	PF15 *	I/O	GPIO_Input	PRESS_TOP_POS
56	PG0 *	I/O	GPIO_Input	KNEAD_TOP_POS
57	PG1 *	I/O	GPIO_Input	KNEAD_BOTTOM_POS
58	PE7 *	I/O	GPIO_Input	EJECTOR_START_POS
59	PE8 *	I/O	GPIO_Input	EJECTOR_MID_POS
60	PE9 *	I/O	GPIO_Input	EJECTOR_END_POS
61	VSS	Power		
62	VDD	Power		
63	PE10 *	I/O	GPIO_Input	SPARE_POS1
64	PE11 *	I/O	GPIO_Input	SPARE_POS2
66	PE13	I/O	TIM1_CH3	PRESS_MTR_RPWM
67	PE14	I/O	TIM1_CH4	PRESS_MTR_LPWM
68	PE15 *	I/O	GPIO_Output	PRESS_MTR_EN
69	PB10	I/O	USART3_TX	UART_RX(BOOTLOADER)
70	PB11	I/O	USART3_RX	UART_TX(BOOTLOADER)
71	VCAP	Power		
72	VDD	Power		
74	PB13 *	I/O	GPIO_Output	TOGGLING_MTR_EN
75	PB14	I/O	TIM12_CH1	TOGGLING_MTR_RPWM
76	PB15	I/O	TIM12_CH2	TOGGLING_MTR_LPWM
79	PD10 *	I/O	GPIO_Output	USB_EN
80	PD11 *	I/O	GPIO_Output	KNEAD_MTR_EN
81	PD12	I/O	TIM4_CH1	KNEAD_MTR_RPWM
82	PD13	I/O	TIM4_CH2	KNEAD_MTR_LPWM
83	VSS	Power		
84	VDD	Power		

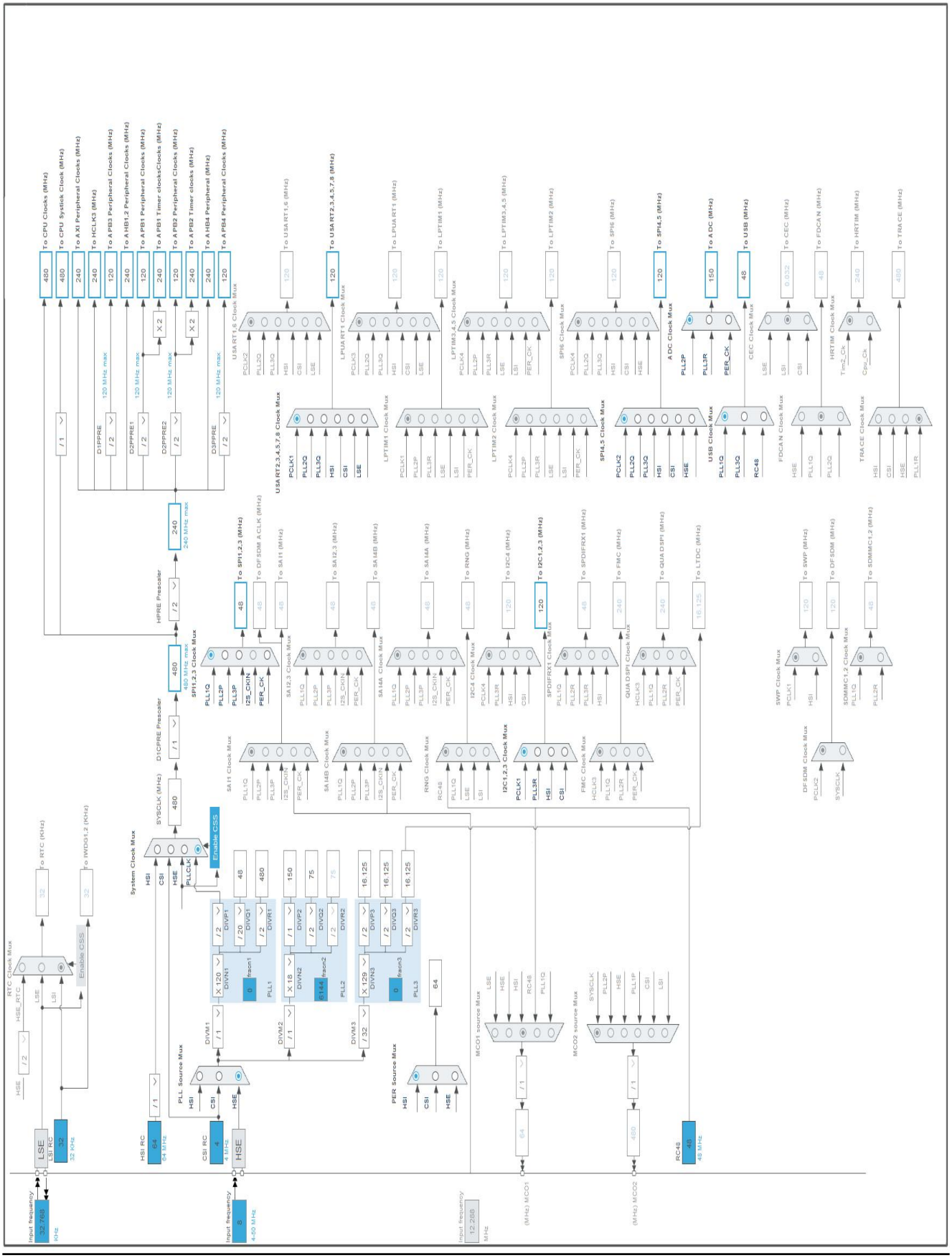
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
87	PG2 *	I/O	GPIO_Input	OIL_LOADCELL_DATA
88	PG3 *	I/O	GPIO_Output	OIL_LOADCELL_CLK
89	PG4 *	I/O	GPIO_Output	WATER_LOADCELL_CLK
90	PG5 *	I/O	GPIO_Input	WATER_LOADCELL_DATA
91	PG6 *	I/O	GPIO_Input	SPARE_LOADCELL_DATA
92	PG7 *	I/O	GPIO_Input	USB_FAULT
93	PG8 *	I/O	GPIO_Output	SPARE_LOADCELL_CLK
94	VSS	Power		
95	VDD33_USB	Power		
96	PC6 *	I/O	GPIO_Output	SPARE_MTR_EN
97	PC7	I/O	TIM3_CH2	SPARE_MTR_RPWM
98	PC8	I/O	TIM3_CH3	SPARE_MTR_LPWM
100	PA8 **	I/O	USB_OTG_FS_SOF	USB_SOF
101	PA9 **	I/O	USB_OTG_FS_VBUS	USB_VBUS
103	PA11	I/O	USB_OTG_FS_DM	USB_N
104	PA12	I/O	USB_OTG_FS_DP	USB_P
105	PA13 (JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	SWDIO
106	VCAP	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14 (JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	SWCLK
110	PA15 (JTDI)	I/O	DEBUG_JTDI	JTDI
111	PC10	I/O	SPI3_SCK	SPARE_SPI3_SCK
112	PC11	I/O	SPI3_MISO	SPARE_SPI3_MISO
113	PC12	I/O	SPI3_MOSI	SPARE_SPI3_MOSI
114	PD0 *	I/O	GPIO_Output	SPARE_SPI3_CS1
115	PD1 *	I/O	GPIO_Output	SPARE_SPI3_CS2
116	PD2 *	I/O	GPIO_Output	LEADSCREW_EN
117	PD3 *	I/O	GPIO_Output	LEADSCREW_DIR
118	PD4 *	I/O	GPIO_Output	LEADSCREW_PULSE
119	PD5 *	I/O	GPIO_Output	EJECTOR_EN
120	VSS	Power		
121	VDD	Power		
122	PD6 *	I/O	GPIO_Output	EJECTOR_DIR
123	PD7 *	I/O	GPIO_Output	EJECTOR_PULSE
124	PG9 *	I/O	GPIO_Output	FLOUR_DISP_EN
125	PG10 *	I/O	GPIO_Output	FLOUR_DISP_DIR
126	PG11 *	I/O	GPIO_Output	FLOUR_DISP_PULSE
127	PG12 *	I/O	GPIO_Output	WATER_DISP_EN

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
128	PG13 *	I/O	GPIO_Output	WATER_DISP_DIR
129	PG14 *	I/O	GPIO_Output	WATER_DISP_PULSE
130	VSS	Power		
131	VDD	Power		
132	PG15 *	I/O	GPIO_Output	OIL_DISP_EN
133	PB3 (JTDO/TRACESWO)	I/O	DEBUG_JTDO-SWO	SWO
134	PB4 (NJTRST) *	I/O	GPIO_Output	OIL_DISP_DIR
135	PB5 *	I/O	GPIO_Output	OIL_DISP_PULSE
136	PB6 *	I/O	GPIO_Output	SPARE_EN
137	PB7 *	I/O	GPIO_Output	SPARE_DIR
138	BOOT0	Boot		
139	PB8 *	I/O	GPIO_Output	SPARE_PULSE
140	PB9 *	I/O	GPIO_Output	SPARE_UART_DE
141	PE0	I/O	UART8_RX	SPARE_UART_RX
142	PE1	I/O	UART8_TX	SPARE_UART_TX
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	NEW_COFIG
Project Folder	C:\Users\Admin\Desktop\Pizza\Kneading Flow Check\NEW_COFIG
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.8.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	IP Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_USART3_UART_Init	USART3
4	MX_ADC1_Init	ADC1
5	MX_ADC2_Init	ADC2
6	MX_DAC1_Init	DAC1
7	MX_I2C2_Init	I2C2
8	MX_SPI3_Init	SPI3
9	MX_SPI4_Init	SPI4
10	MX_TIM1_Init	TIM1
11	MX_TIM3_Init	TIM3

Rank	Function Name	IP Instance Name
12	MX_TIM4_Init	TIM4
13	MX_TIM5_Init	TIM5
14	MX_TIM12_Init	TIM12
15	MX_TIM13_Init	TIM13
16	MX_TIM16_Init	TIM16
17	MX_UART8_Init	UART8
18	MX_TIM17_Init	TIM17
19	MX_USB_DEVICE_Init	USB_DEVICE
0	MX_CORTEX_M7_Init	CORTEX_M7

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H743/753
MCU	STM32H743ZITx
Datasheet	DS12110_Rev5

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

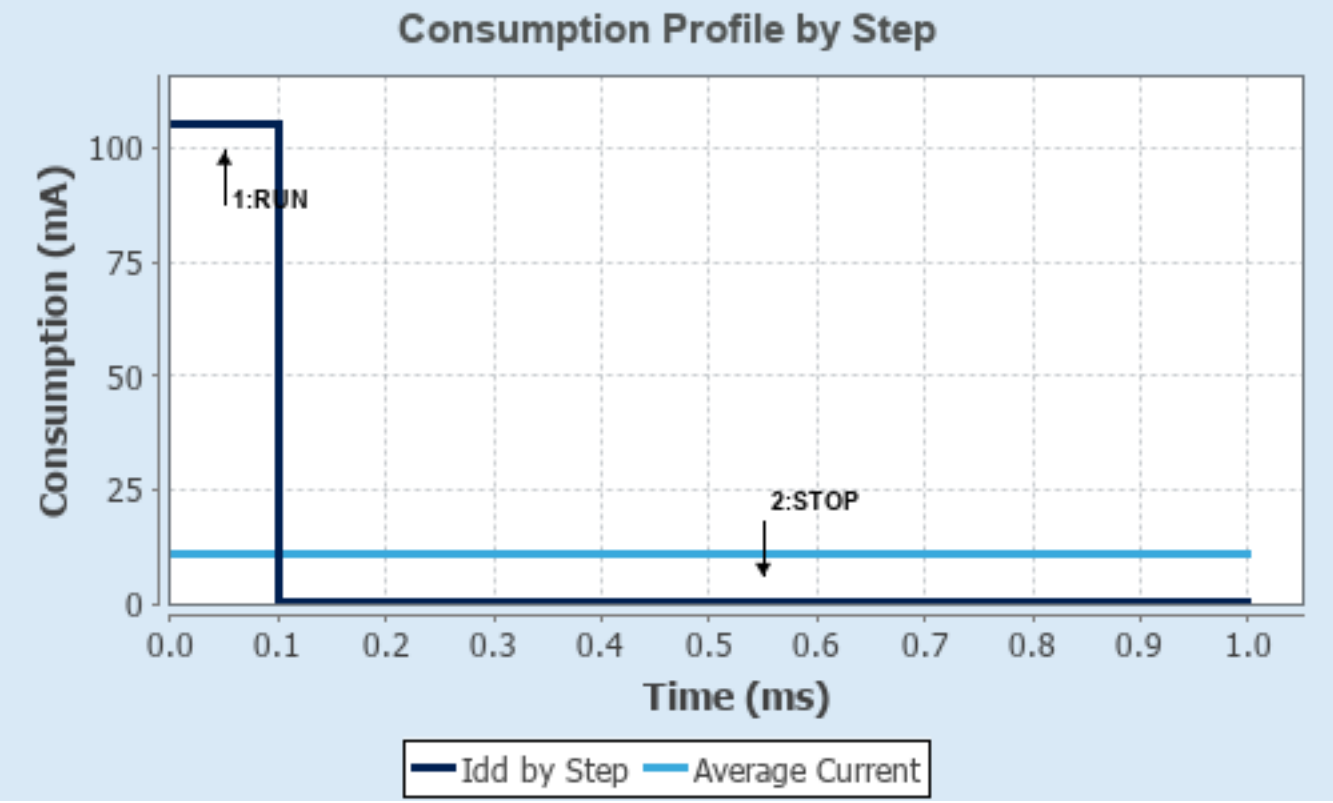
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS1: Scale1-High	SVOS5: System-Scale5
D1 Mode	DRUN/CRUN	DSTANDBY
D2 Mode	DSTANDBY	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	FLASH_A	NA
CPU Frequency	400 MHz	0 Hz
Clock Configuration	HSE BYP PLL Flash-ON Cache-ON	Flash-LP
Clock Source Frequency	25 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	105 mA	170 µA
Duration	0.1 ms	0.9 ms
DMIPS	856.0	0.0
Ta Max	111.14	124.98
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	10.65 mA
Battery Life	2 days, 10 hours	Average DMIPS	856.00006 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
100
75
50
25
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. IPs and Middleware Configuration

7.1. ADC1

IN2: IN2 Single-ended

IN3: IN3 Single-ended

IN4: IN4 Single-ended

IN5: IN5 Single-ended

mode: IN6

mode: IN7

mode: IN8

mode: IN9

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Left Bit Shift	No bit shift
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	**Channel 3 ***
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset Signed Saturation	Disable

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. ADC2

IN2: IN2 Single-ended

mode: IN6

7.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Left Bit Shift	No bit shift
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	**Channel 6 ***
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset Signed Saturation	Disable

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.3. DAC1

OUT1 mode: Connected to external pin only

OUT2 mode: Connected to external pin only

7.3.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
Trigger	None
User Trimming	Factory trimming
Sample And Hold	Sampleandhold Disable

DAC Out2 Settings:

Output Buffer	Enable
Trigger	None
User Trimming	Factory trimming
Sample And Hold	Sampleandhold Disable

7.4. DEBUG

Debug: JTAG (4 pins)

7.5. GPIO

7.6. I2C2

I2C: I2C

7.6.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0

Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x307075B1 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.7. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.7.1. Parameter Settings:

SupplySource	PWR_LDO_SUPPLY

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	32

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	4 WS (5 CPU cycle)

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 0

PLL range Parameters:

PLL1 clock Input range	Between 8 and 16 MHz
PLL2 input frequency range	Between 8 and 16 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	MEDIUM VCO range

7.8. SPI3

Mode: Full-Duplex Master

7.8.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**24.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.9. SPI4

Mode: Full-Duplex Master

7.9.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**60.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled

NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.10. SYS

Timebase Source: TIM2

7.11. TIM1

Clock Source : Internal Clock

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**120-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**100-1 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable

- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.12. TIM3

Clock Source : Internal Clock

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

7.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**120-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**100-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.13. TIM4

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

7.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**120-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**100-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.14. TIM5

Clock Source : Internal Clock

Channel2: PWM Generation CH2

7.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**120-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**100-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.15. TIM12

mode: Clock Source

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

7.15.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**120-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**100-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.16. TIM13

mode: Activated

Channel1: PWM Generation CH1

7.16.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**120-1 ***
Counter Mode	Up

Counter Period (AutoReload Register - 16 bits value)	**100-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.17. TIM16

mode: Activated

Channel1: Input Capture direct mode

7.17.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**240-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

7.18. TIM17

mode: Activated

7.18.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**249 ***
Counter Mode	Up

Counter Period (AutoReload Register - 16 bits value)	**0xfffe ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

7.19. UART8

Mode: Asynchronous

7.19.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.20. USART3

Mode: Asynchronous

7.20.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200

Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.21. USB_OTG_FS

Mode: Device_Only

7.21.1. Parameter Settings:

Speed	Full Speed 12MBit/s
Enable internal IP DMA	Disabled
Low power	Disabled
Battery charging	Disabled
Link Power Management	Disabled
Use dedicated end point 1 interrupt	Disabled
VBUS sensing	Disabled
Signal start of frame	Disabled

7.22. FREERTOS

Interface: CMSIS_V2

7.22.1. Config parameters:

API:

FreeRTOS API	CMSIS v2

Versions:

FreeRTOS version	10.2.1
CMSIS-RTOS version	2.00

MPU/FPU:

ENABLE_MPU	Disabled
ENABLE_FPU	Disabled

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	56
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Enabled
USE_COUNTING_SEMAPHORES	Enabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Disabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Enabled

USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Enabled
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10
TIMER_TASK_STACK_DEPTH	256

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

7.22.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Enabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Enabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Enabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Enabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Enabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

7.22.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT	Disabled

Project settings (see parameter description first):

Use FW pack heap file	Enabled

7.23. USB_DEVICE

Class For FS IP: Communication Device Class (Virtual Port Com)

7.23.1. Parameter Settings:

Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SELF_POWERED (Enabled self power)	Enabled
USBD_DEBUG_LEVEL (USBD Debug Level)	0: No debug message

Class Parameters:

USB CDC Rx Buffer Size	2048
USB CDC Tx Buffer Size	2048

7.23.2. Device Descriptor:

Device Descriptor:

VID (Vendor IDentifier)	1155
LANGID_STRING (Language Identifier)	English(United States)
MANUFACTURER_STRING (Manufacturer Identifier)	STMicroelectronics

Device Descriptor FS:

PID (Product IDentifier)	22336
PRODUCT_STRING (Product Identifier)	STM32 Virtual ComPort
CONFIGURATION_STRING (Configuration Identifier)	CDC Config
INTERFACE_STRING (Interface Identifier)	CDC Interface

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA6	ADC1_INP3	Analog mode	No pull-up and no pull-down	n/a	PRESS_MTR_LSENS
	PA7	ADC1_INP7	Analog mode	No pull-up and no pull-down	n/a	PRESS_MTR_RSENS
	PC4	ADC1_INP4	Analog mode	No pull-up and no pull-down	n/a	TOGGLING_MTR_LSENS
	PC5	ADC1_INP8	Analog mode	No pull-up and no pull-down	n/a	TOGGLING_MTR_RSENS
	PB0	ADC1_INP9	Analog mode	No pull-up and no pull-down	n/a	KNEAD_MTR_LSENS
	PB1	ADC1_INP5	Analog mode	No pull-up and no pull-down	n/a	KNEAD_MTR_RSENS
	PF11	ADC1_INP2	Analog mode	No pull-up and no pull-down	n/a	SPARE_MTR_LSENS
	PF12	ADC1_INP6	Analog mode	No pull-up and no pull-down	n/a	SPARE_MTR_RSENS
ADC2	PF13	ADC2_INP2	Analog mode	No pull-up and no pull-down	n/a	LIN_POS_SN
	PF14	ADC2_INP6	Analog mode	No pull-up and no pull-down	n/a	SHARP_SN
DAC1	PA4	DAC1_OUT1	Analog mode	No pull-up and no pull-down	n/a	SPARE_DAC1
	PA5	DAC1_OUT2	Analog mode	No pull-up and no pull-down	n/a	SPARE_DAC2
DEBUG	PA13 (JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	SWDIO
	PA14 (JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	SWCLK
	PA15 (JTDI)	DEBUG_JTDI	n/a	n/a	n/a	JTDI
	PB3 (JTDO/TRACESWO)	DEBUG_JTDO-SWO	n/a	n/a	n/a	SWO
I2C2	PF0	I2C2_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	TOF_I2C2_SDA
	PF1	I2C2_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	TOF_I2C2_SCL
RCC	PC14-OSC32_IN (OSC32_IN)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
SPI3	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	SPARE_SPI3_SCK
	PC11	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	SPARE_SPI3_MISO
	PC12	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	SPARE_SPI3_MOSI
SPI4	PE2	SPI4_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	MAX_SPI4_SCK

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PE5	SPI4_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	MAX_SPI4_MISO
	PE6	SPI4_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	MAX_SPI4-MOSI
TIM1	PE13	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	PRESS_MTR_RPWM
	PE14	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	PRESS_MTR_LPWM
TIM3	PC7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	SPARE_MTR_RPWM
	PC8	TIM3_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	SPARE_MTR_LPWM
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	KNEAD_MTR_RPWM
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	KNEAD_MTR_LPWM
TIM5	PA1	TIM5_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	SPARE_DRV_MTR_PWM
TIM12	PB14	TIM12_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	TOGGLING_MTR_RPWM
	PB15	TIM12_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	TOGGLING_MTR_LPWM
TIM13	PF8	TIM13_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	AGITATOR_MTR_PWM
TIM16	PF6	TIM16_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	SPEED_MEAS
UART8	PE0	UART8_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	SPARE_UART_RX
	PE1	UART8_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	SPARE_UART_TX
USART3	PB10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	UART_RX(BOOTLOADER)
	PB11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	UART_TX(BOOTLOADER)
USB_OTG_FS	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	Low	USB_N
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	Low	USB_P
Single Mapped Signals	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
	PA8	USB_OTG_FS_SOF	Alternate Function Push Pull	No pull-up and no pull-down	Low	USB_SOF
	PA9	USB_OTG_FS_VBUS	n/a	n/a	n/a	USB_VBUS
GPIO	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MAX_SPI4_CS1
	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MAX_SPI4_CS2
	PF4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SSR_TOP_PAN
	PF5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SSR_BOTTOM_PAN
	PF7	GPIO_Input	Input mode	**Pull-up ***	n/a	SPEED_DIR
	PF9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	AGITATOR_MTR_DIR
	PF10	GPIO_Input	Input mode	**Pull-up ***	n/a	AGITATOR_MTR_FAULT
	PC1	GPIO_EXTI1	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	FLOW_SENSOR_PIN
	PC2_C	GPIO_EXTI2	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	EMERGENCY_STOP
	PC3_C	GPIO_EXTI3	External Interrupt Mode with	No pull-up and no pull-down	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
			Rising edge trigger detection			
	PA2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPARE_DRV_MTR_DIR
	PA3	GPIO_Input	Input mode	**Pull-up ***	n/a	SPARE_DRV_MTR_FAULT
	PF15	GPIO_Input	Input mode	**Pull-up ***	n/a	PRESS_TOP_POS
	PG0	GPIO_Input	Input mode	**Pull-up ***	n/a	KNEAD_TOP_POS
	PG1	GPIO_Input	Input mode	**Pull-up ***	n/a	KNEAD_BOTTOM_POS
	PE7	GPIO_Input	Input mode	**Pull-up ***	n/a	EJECTOR_START_POS
	PE8	GPIO_Input	Input mode	**Pull-down ***	n/a	EJECTOR_MID_POS
	PE9	GPIO_Input	Input mode	**Pull-up ***	n/a	EJECTOR_END_POS
	PE10	GPIO_Input	Input mode	**Pull-up ***	n/a	SPARE_POS1
	PE11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SPARE_POS2
	PE15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PRESS_MTR_EN
	PB13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TOGGLING_MTR_EN
	PD10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_EN
	PD11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	KNEAD_MTR_EN
	PG2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	OIL_LOADCELL_DATA
	PG3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OIL_LOADCELL_CLK
	PG4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	WATER_LOADCELL_CLK
	PG5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	WATER_LOADCELL_DATA
	PG6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SPARE_LOADCELL_DATA
	PG7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USB_FAULT
	PG8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPARE_LOADCELL_CLK
	PC6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPARE_MTR_EN
	PD0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPARE_SPI3_CS1
	PD1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPARE_SPI3_CS2
	PD2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LEADSCREW_EN
	PD3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LEADSCREW_DIR
	PD4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	LEADSCREW_PULSE
	PD5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	EJECTOR_EN
	PD6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	EJECTOR_DIR
	PD7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	EJECTOR_PULSE
	PG9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	FLOUR_DISP_EN
	PG10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	FLOUR_DISP_DIR
	PG11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High**	FLOUR_DISP_PULSE

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
	PG12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	WATER_DISP_EN
	PG13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	WATER_DISP_DIR
	PG14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High** *	WATER_DISP_PULSE
	PG15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OIL_DISP_EN
	PB4 (NJTRST)	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OIL_DISP_DIR
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High** *	OIL_DISP_PULSE
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPARE_EN
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPARE_DIR
	PB8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High** *	SPARE_PULSE
	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPARE_UART_DE

8.2. DMA configuration

nothing configured in DMA service

8.3. BDMA configuration

nothing configured in DMA service

8.4. MDMA configuration

nothing configured in DMA service

8.5. NVIC configuration

8.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
EXTI line1 interrupt	true	0	0
EXTI line2 interrupt	true	0	0
EXTI line3 interrupt	true	0	0
TIM2 global interrupt	true	0	0
TIM3 global interrupt	true	0	0
TIM4 global interrupt	true	0	0
TIM8 break interrupt and TIM12 global interrupt	true	0	0
TIM8 update interrupt and TIM13 global interrupt	true	0	0
USB On The Go FS global interrupt	true	0	0
TIM16 global interrupt	true	0	0
TIM17 global interrupt	true	0	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
USART3 global interrupt	unused		
TIM5 global interrupt	unused		
SPI3 global interrupt	unused		
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts	unused		
FPU global interrupt	unused		
UART8 global interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
SPI4 global interrupt	unused		
USB On The Go FS End Point 1 Out global interrupt	unused		
USB On The Go FS End Point 1 In global interrupt	unused		
HSEM1 global interrupt	unused		

8.5.2. NVIC Code generation

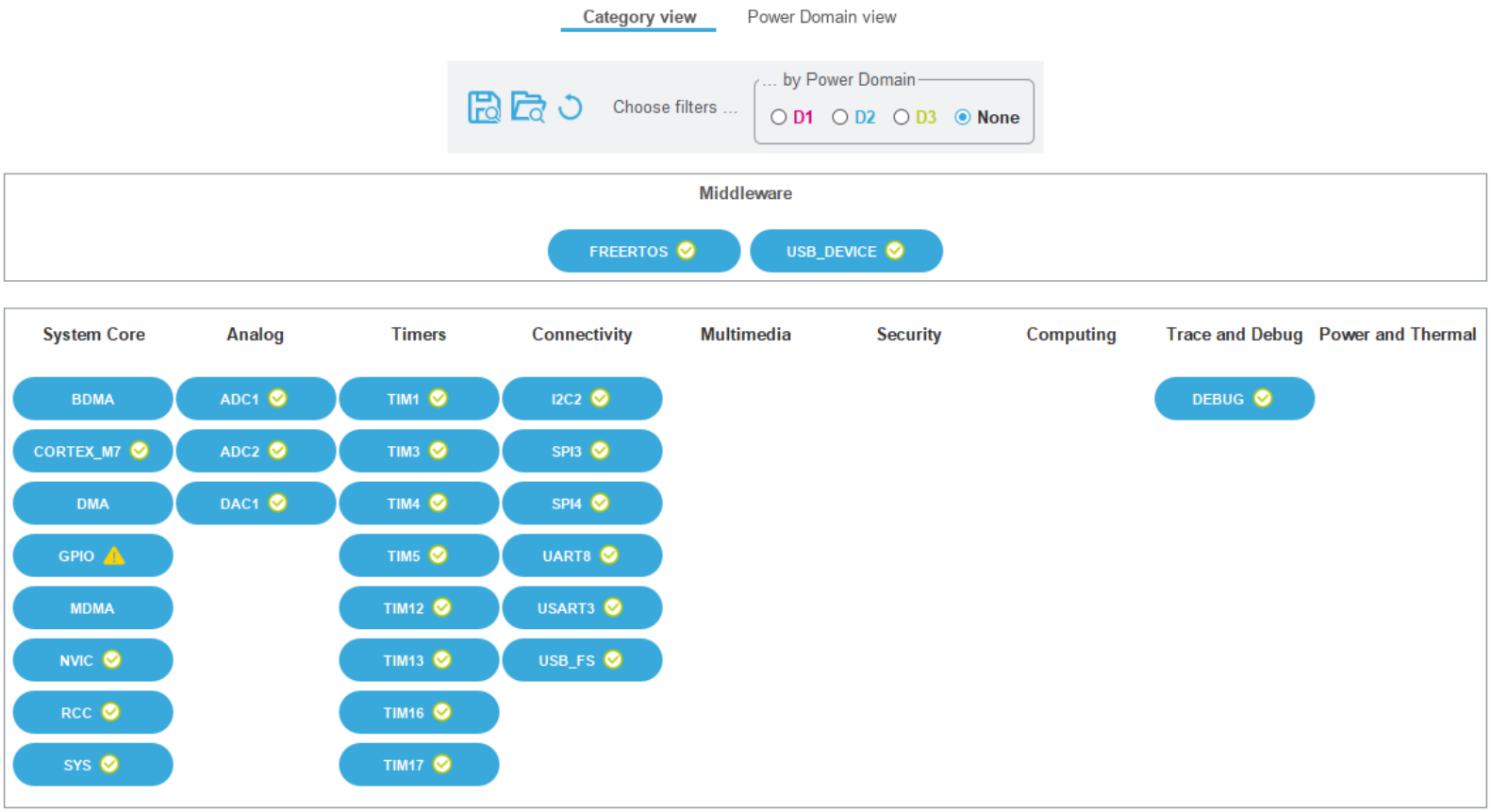
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	true	true	false
Hard fault interrupt	true	true	false
Memory management fault	true	true	false
Pre-fetch fault, memory access fault	true	true	false
Undefined instruction or illegal state	true	true	false
System service call via SWI instruction	true	false	false
Debug monitor	true	true	false
Pendable request for system service	true	false	false
System tick timer	true	false	false
EXTI line1 interrupt	true	true	true
EXTI line2 interrupt	true	true	true
EXTI line3 interrupt	true	true	true
TIM2 global interrupt	true	true	true
TIM3 global interrupt	true	true	true
TIM4 global interrupt	true	true	true
TIM8 break interrupt and TIM12 global interrupt	true	true	true
TIM8 update interrupt and TIM13 global interrupt	true	true	true
USB On The Go FS global interrupt	true	true	true
TIM16 global interrupt	true	true	true
TIM17 global interrupt	true	true	true

*** User modified value**

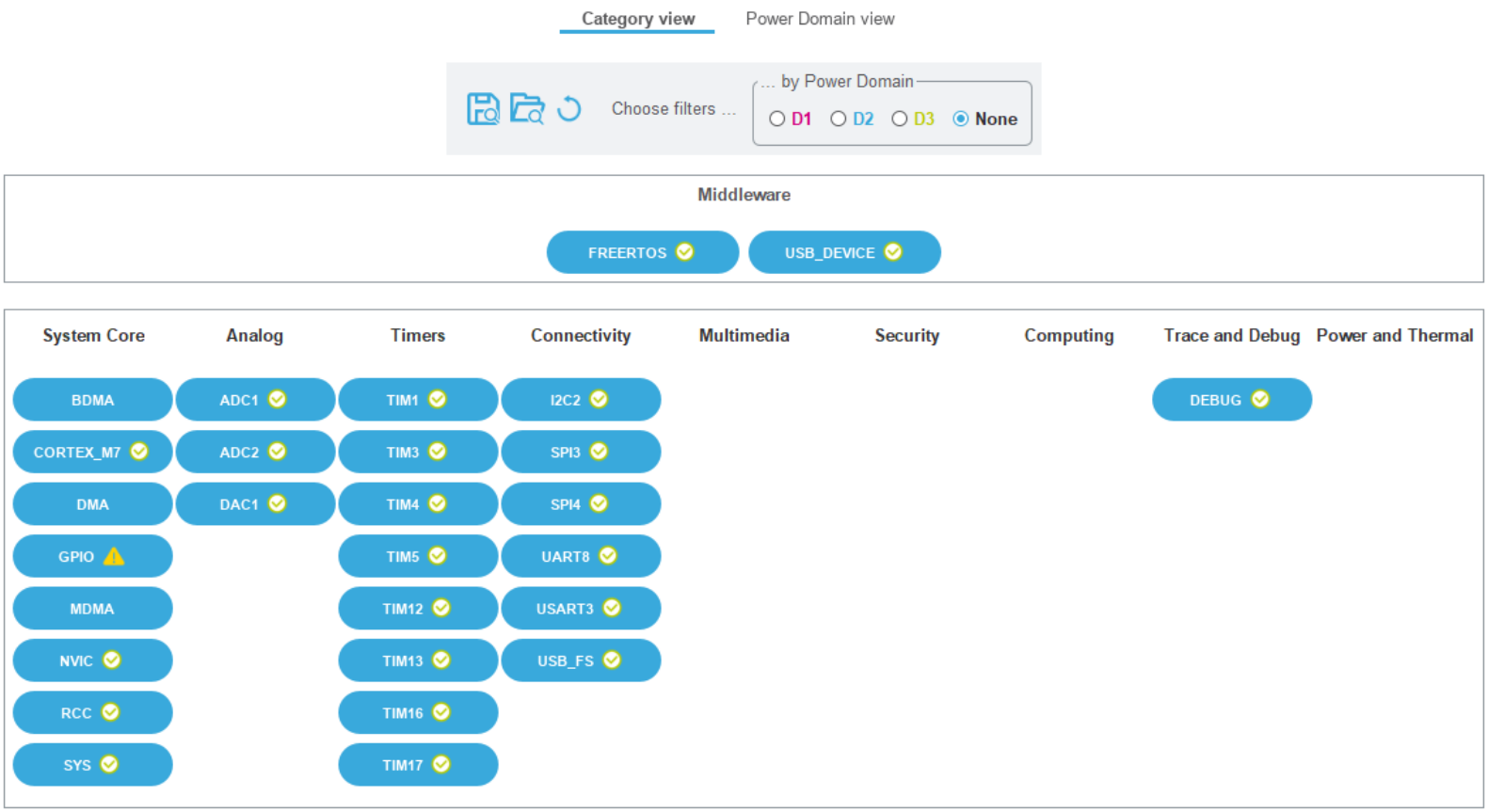
9. System Views

9.1. Category view

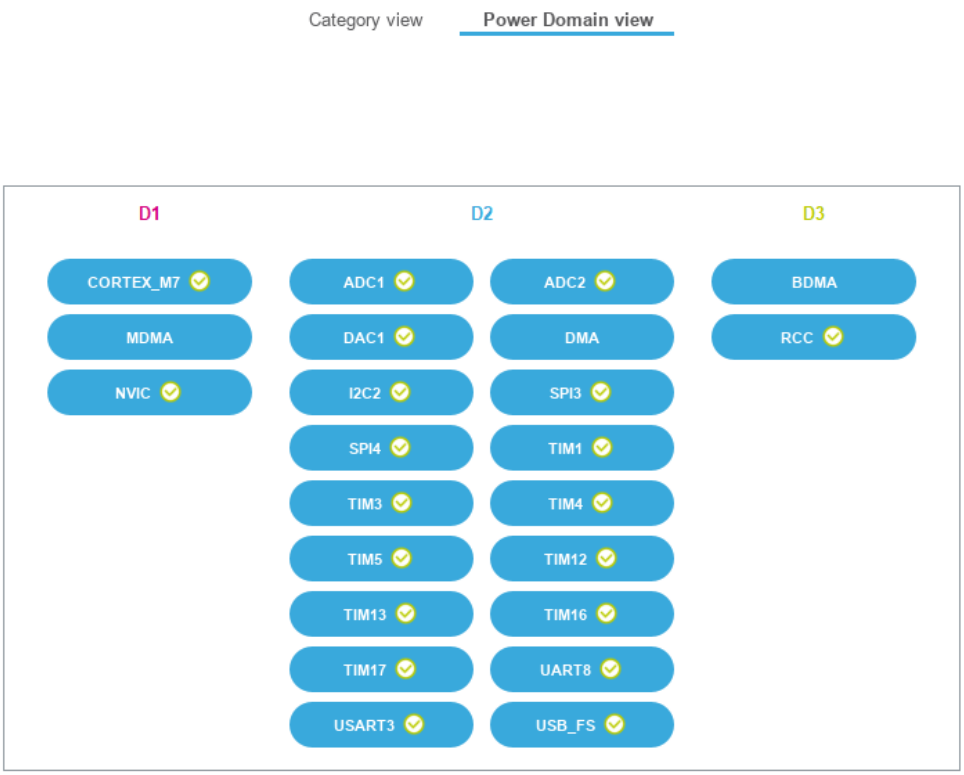
9.1.1. Current



9.1.2. Without filters



9.2. Power Domain view



10. Software Pack Report

10.1. Software Pack selected

Vendor	Name	Version	Component
STMicroelectronics	FreeRTOS	0.0.1	Class : CMSIS Group : RTOS2 SubGroup : FreeRTOS Version : 10.2.0 Class : RTOS Group : Core Version : 10.2.0
STMicroelectronics	USB_DEVICE	1.0.0	Class : USB Group : USB Device SubGroup : CDC FS Version : 1.0

11. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00387108.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00314099.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00237416.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00368411.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00121475.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00151811.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00227538.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272913.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf

Application note	http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00337702.pdf
Application note	http://www.st.com/resource/en/application_note/DM00393275.pdf
Application note	http://www.st.com/resource/en/application_note/DM00337873.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00373474.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00356635.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354333.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00431633.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00535045.pdf
Application note	http://www.st.com/resource/en/application_note/DM00525510.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00609692.pdf
Application note	http://www.st.com/resource/en/application_note/DM00622045.pdf
Application note	http://www.st.com/resource/en/application_note/DM00623136.pdf
Application note	http://www.st.com/resource/en/application_note/DM00625700.pdf
Application note	http://www.st.com/resource/en/application_note/DM00660346.pdf
Application note	http://www.st.com/resource/en/application_note/DM00600614.pdf
Application note	http://www.st.com/resource/en/application_note/DM00628458.pdf