EE 2511- 0A1

Logic Design Open Ended Project

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Lab Group: 07

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Course Description:

Introduction to digital design techniques and hardware. Implementation of combinational circuits, registers, flip-flops, sequential circuits, and state-machine.

Report Description:

Implementation of multiple state machine elements arranged in a “master/slave” scheme.

- Overview of the design.
- Detailed description of our approach; how we process it.
- Truth table and K-maps.
- Schematics and Timing Diagram.
- Electronic devices containing digital logic.

Project Overview/Description:

The design project proposal herein describes the implementation of multiple state machine elements arranged in a "master/slave" scheme. The main goal of the design focuses on cascade protection typically seen in electrical power distribution controls, and more specifically -breaker failure protection.

The sequence of operation begins with a fault introduced to the system in zone one. Before engaging a trip command, the surge monitor incorporated in the circuit allows a preset delay to elapse for the purpose of mitigating nuisance tripping in the scheme. The process then passes to the trip command of zone one, and an opportunity is given to clear the fault locally before zone two is employed as an overarching response. If the fault is cleared in zone one, the sequence is stopped, zone one is driven to lockout, and the system must be manually reset before being placed back in service. However, if the system continues to sustain a condition where zone one has declared a trip and the fault persists, zone two is engaged upon a predetermined delay after which zone one has been given ample time to extinguish the fault. As zone two is called to action, it is also mitigated by the surge monitor before issuing a trip command. Zone two tripping then elicits a similar response as that of zone one by driving the system to lockout and requiring a manual reset before the scheme may be placed back in service.

Now that we have an overview for the concept of the scheme's operation, greater detail may be introduced for the inner workings of the state machine arrangement used to implement this sequence of controls. Our basic design kicks off with the creation of a state diagram and graph for the procession of events slated to take place. State and truth tables with given inputs and desired outputs were developed, from which we later create K-maps. K-maps helped us finding the minterms to create the logic gates. Upon arriving at K-map solutions, a circuit could be generated to emulate the design.

We wanted to simulate a cascading power failure. There will be several inputs including a clock, Surge monitor, Fault, as well as a Master Reset.

In the logic circuit, we used 4 J-K flip flops to simulate our two different states within Zone 1 and Zone 2. We take a surge monitor input as well as the fault input to determine if the initial fault is going to be detrimental to our electrical system. If the fault is determined to only be noise and not of any real danger, Zone 1 will not fault. If however Zone 1 does fault, we need to check to see if Zone 2 is at risk of being harmed as well. As such we use an AND gate with surge monitor to determine if Zone 2 should trip as well. If Zone 1 and Zone 2 both trip our system is in lockdown. Once the fault has been addressed we can clear the trips with a master reset.

State Table:

Z1-Trip	Br	MR	Z1 I	Z1 F	Z2 I	Z2 F	Z1 I'	Z1 F'	Z2 I'	Z2 F'
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	0	1	0	0	0	1	1	0	0
1	1	0	1	0	0	0	0	0	0	0
1	0	0	1	1	0	0	1	1	1	0
1	0	0	1	1	1	0	1	1	1	1
1	1	0	1	1	1	0	1	1	0	0
1	X	1	1	1	1	1	0	0	0	0

K-maps:

AB / C	00	01	11	10
0	0	0	0	1
1	1	1	0	1

Z1 F' : A'C + AB'

AB / C	00	01	11	10
0	0	0	0	0
1	0	1	0	0

Z2 F' : A'BC

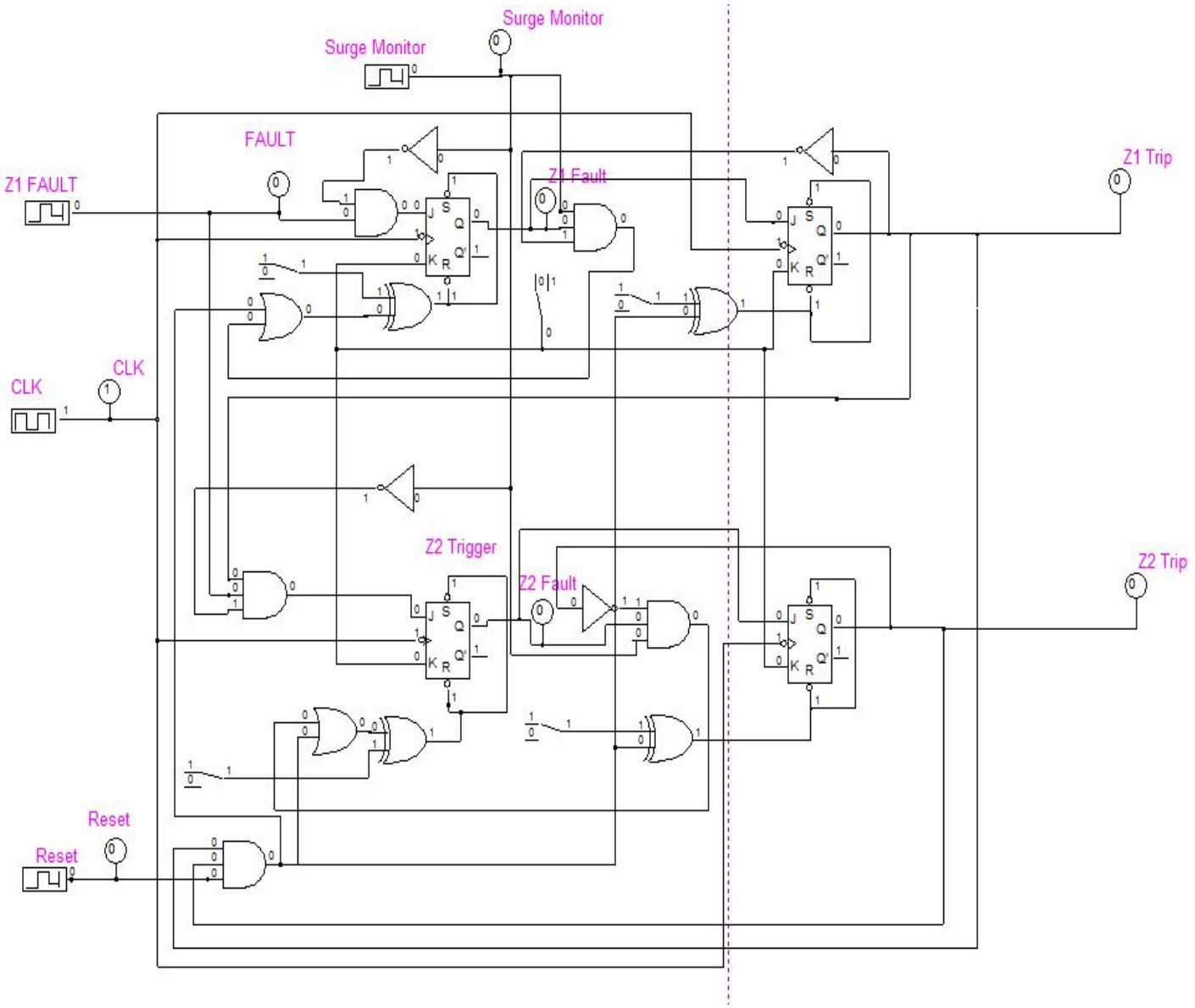
AB / C	00	01	11	10
0	0	1	0	1
1	1	1	0	1

Z1 I' : A'B+AB'+B'C

AB / C	00	01	11	10
0	0	0	0	0
1	1	1	0	0

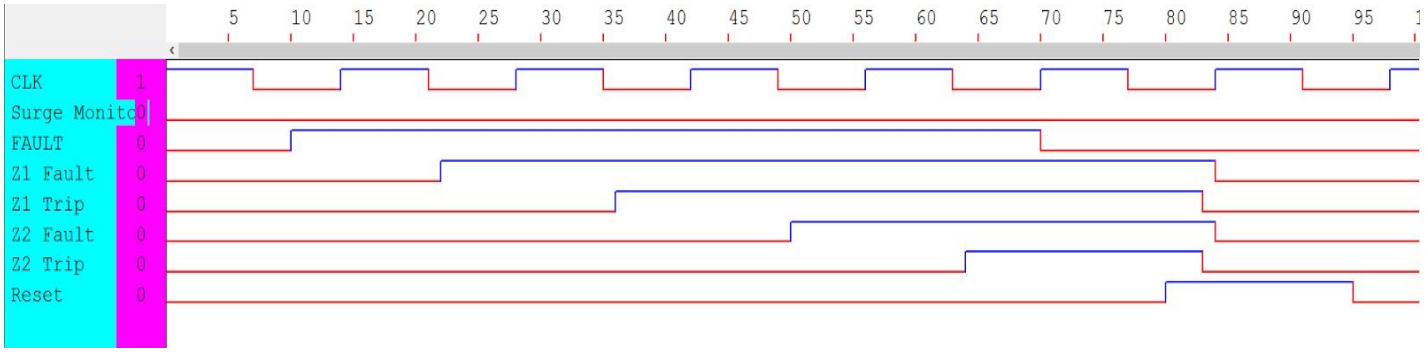
Z2I' : A'C

Circuit Diagram:

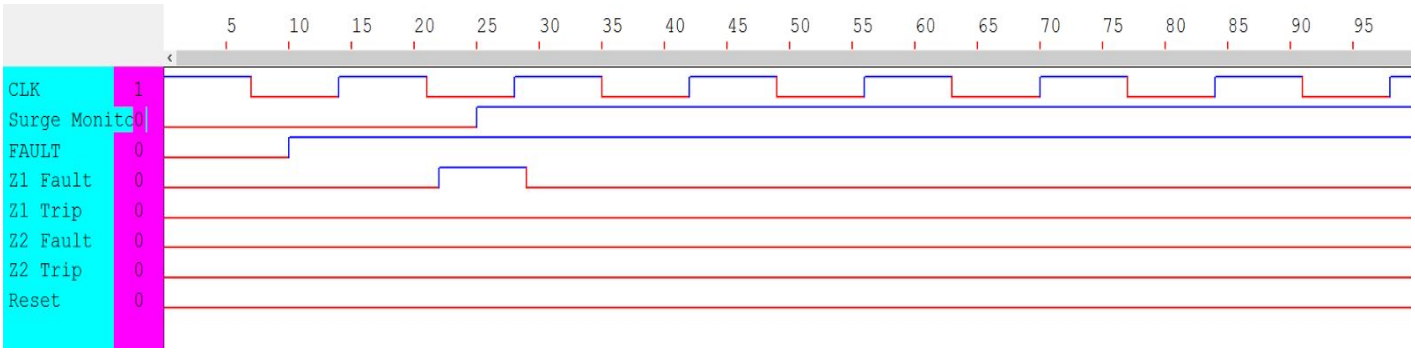


Timing Diagram:

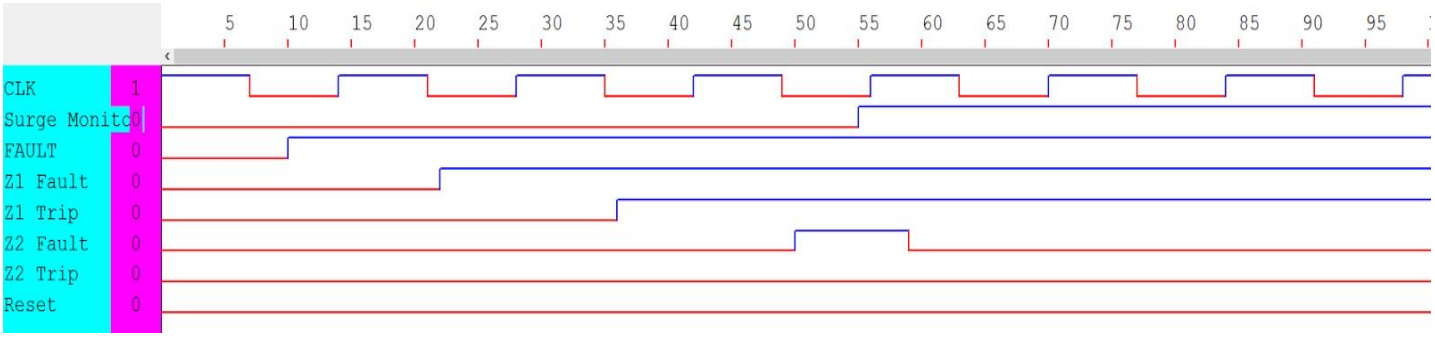
Z1 and Z2 trip with master reset.



Z1 Fault with Surge Monitor reset.



Z2 Fault with Surge Monitor reset.



Electronic devices containing digital logic, variables:

Inputs:

Clock, Fault, Surge Monitor, Master Reset

Outputs:

Zone 1 Fault, Zone 1 Trip, Zone 2 Fault, Zone 2 Trip

Participation:

James Willoughby : 25 %

Mukunda Subedi : 25 %

Adam West : 25 %

John Helmy : 25 %