MUKUT DEBNATH

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Third Year Undergraduate Student
Electrical Engineering, Indian Institute of Technology Kharagpur

RESEARCH INTERESTS

Mixed Signal Circuit Design, Digital Logic Design, Digital VLSI Circuits and Systems

EDUCATION

Indian Institute of Technology Kharagpur, India 2020 – present
5 Years Dual Degree, Department of Electrical Engineering *CGPA: 9.39/10.00*

Sri Sri Ravishankar Vidyamandir Agartala, India 2018 – 2020
Central Board of Secondary Education (AISSCE) *Percentage: 95.8*

Sri Sri Ravishankar Vidyamandir Agartala, India 2016 – 2018
Central Board of Secondary Education (AISSE) *Percentage: 97.6*

PUBLICATIONS

M Debnath, P Maji, M Sharad, **"Area and Power Efficient Word Alignment and 32b/40b Encoding Scheme for High-Speed SERDES."**
–under review

KEY PROJECTS

- **16b/20b Encoder-Decoder Design** *July 2022 – August 2022*
  Advisor: Prof. Mrigank Sharad, IIT Kharagpur *[Report]*
  - RTL Design, Synthesis, and Place Route of standard 8b/10b encoder and decoder using Synopsis Design tools, required for maintaining DC balancing and higher data transitions in the serialized data stream
  - Performed integration of encoder/decoder module with full-chip layout of SERDES in Cadence with verification
  - Explored and designed schemes to extend standard 8b/10b encoding decoding to 16b/20b and 32b/40b versions for use in higher speed SERDES interfaces

- **Comma Detection & Word Alignment for high-speed SERDES interface** *July 2022 – August 2022*
  Advisor: Prof. Mrigank Sharad, IIT Kharagpur *[Report]*
  - Explored and compared different schemes for comma detection and word alignment in the SERDES interface
  - Successfully designed a new scheme that has lower area requirements as well as lower power consumption for word alignment in the SERDES interface. Work involved rigorous timing analysis for high-speed data and clock paths, layout integration, and post-layout simulation with the full SERDES system

- **High-speed SERDES design for radiation hardened IC, ISRO** *June 2022 – July 2022*
  Advisor: Prof. Mrigank Sharad, IIT Kharagpur *[Report]*
  - The project involves the design of a high-speed (2 GPS) SERDES using 180nm SCL technology
  - The architecture involved high speed Serial-In Parallel Out Shift Registers along with Synthesizer and CDR followed by deserializer on the transmitter and receiver side respectively
  - Half-rate architecture was chosen to allow a clock frequency that was half of the data rate
  - The work involved custom circuit design, and rigorous timing analysis, followed by custom layout and post layout verification in Cadence

INTERNSHIPS & TRAINING

- **Internship at ISRO Space Applications Centre, Ahmedabad** *July 2022*
  - Visited Advanced VLSI Design Lab of ISRO SAC Ahmedabad, for collaborative work, as a part of the ISRO project. Worked in team to complete the integration of digital modules with mixed signal blocks using Cadence and Synopsys tools

- **Summer VLSI Course 2022** *May 2022 - June 2022*
  - Participated in a 6 week-long Summer Workshop/Course where we learned and applied the various important concepts of analog and mixed-signal circuit design and applied the concepts in designing and optimizing circuits such as two-stage Opamp, Operational Transconductance Amplifier, Low Dropout Regulator (LDO), etc in LTspice

COURSEWORK

Electronics and Electrical Courses: Analog Electronic Circuits*, Digital Electronic Circuits*, Power Electronics*, Signals and Systems, Network Analysis, Signals and Networks Lab, Digital Signal Processing*, Control Systems Engineering, Industrial Instrumentation, Control and Instrumentation Lab, Measurements and Electronic Instruments*, Embedded Systems**, Computer Architecture and Operating Systems**, Control and Electronic System Design**, Fundamentals of Embedded Control and Software, Power Systems**, Electrical Machines*, Electrical Technology

Programming & Mathematics: Programming and Data Structures*, Artificial Intelligence: Foundations and Applications, Advanced Calculus, Linear Algebra, Numerical and Complex Analysis, Probability and Statistics, Applied Computational Methods

**Indicates the course had a lab component as well, **To be taken next semester*

TECHNICAL SKILLS

Programming: Verilog HDL, MATLAB, C/C++, Python
Software Tools: Cadence Virtuoso, Synopsys, MATLAB/Simulink, LTspice, Tina-TI, Latex

ACHIEVEMENTS & RECOGNITION

- Enrolled as an UG researcher in ISRO Sponsored Project
- Department Rank 2 among 170 students
- Recognized as top 5 performers among 50 students enrolled in VLSI Summer School 2022 at IIT Kharagpur
- Amongst top 200 in more than 1850 first-year students to secure a branch change at the end of the first year with CGPA 9.59 in IIT Kharagpur
- Secured All India Rank 3767 (GE) in JEE Advanced 2020 among more than 1,50,000 shortlisted candidates across India
- Secured All India Rank 4864 (GE) in JEE Main 2020 among more than 10,00,000 candidates across India

EXTRA-CURRICULAR ACTIVITIES

- Got bronze in Inter Hall Data Analytics 2022
- Got bronze in Intra Hall Math Olympiad organized by LLR Hall of Residence, IIT Kharagpur
- Participated in Open IIT Product Design 2022 and secured 4th position
- UC Council Mentor for the academic year 2021-22
- NSS volunteer for NSS Unit-11, IIT Kharagpur