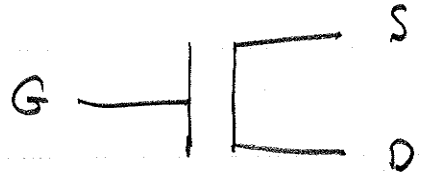
Rm 148
2:10 - 3:00 pm

Review of FETs

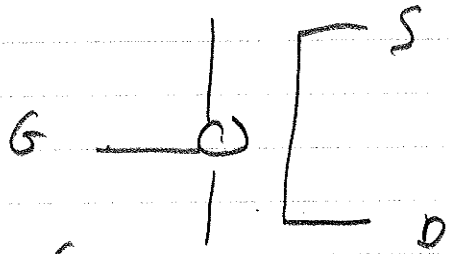
FET



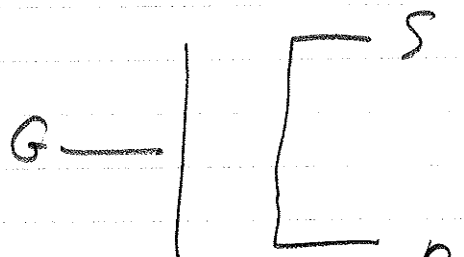
⇒ High input impedance at gate

⇒ Uses electric field (not current) to manipulate conduction band between Source and Drain

Concerned with two polarities:

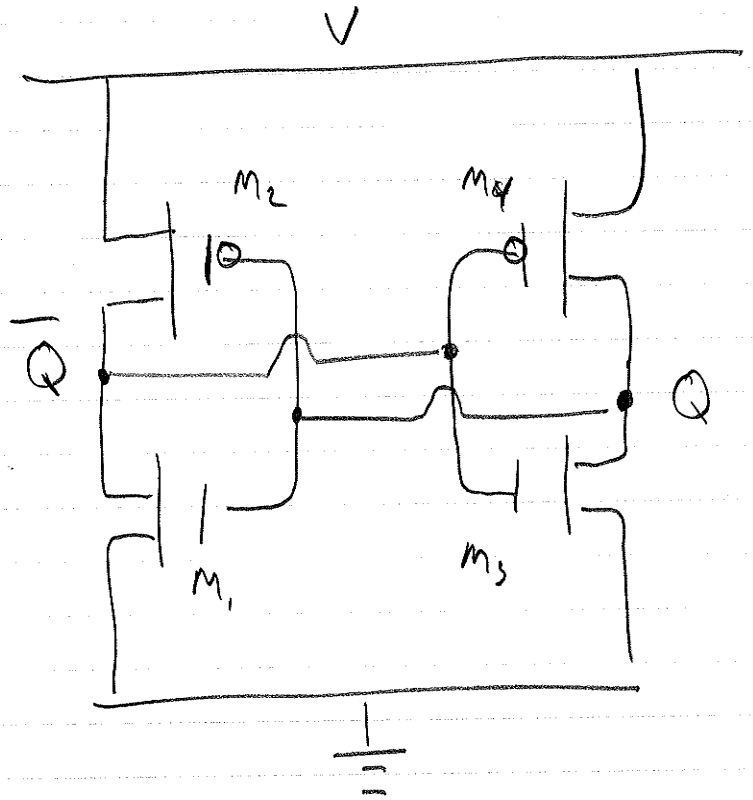


(p-channel)



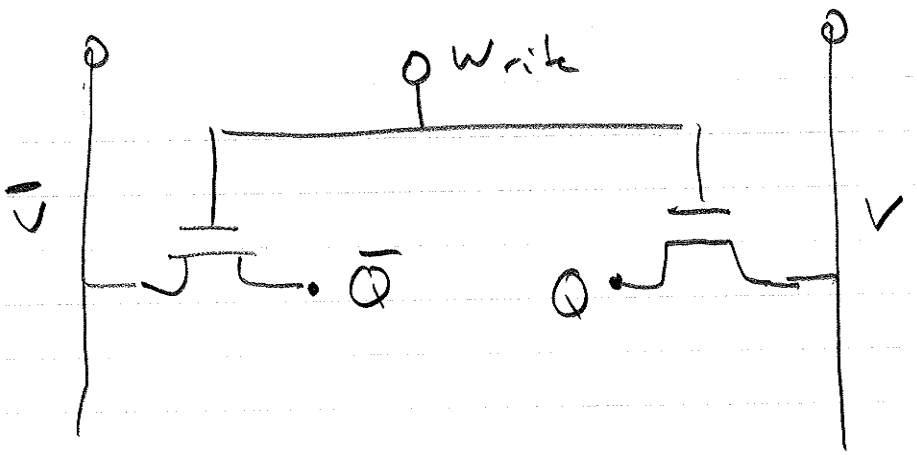
(n-channel)

SRAM (static ram)



Q high ⇒ M_1 open, M_2 closed, so $\overline{Q}$ low

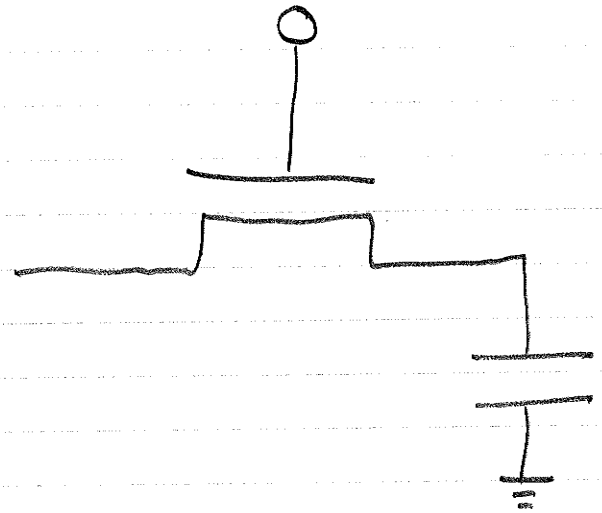
⇒ M_4 open, M_3 closed, so Q high.



To write, over-power previous state

* "static": no need to refresh
→ self reinforcing

DRAM Dynamic RAM



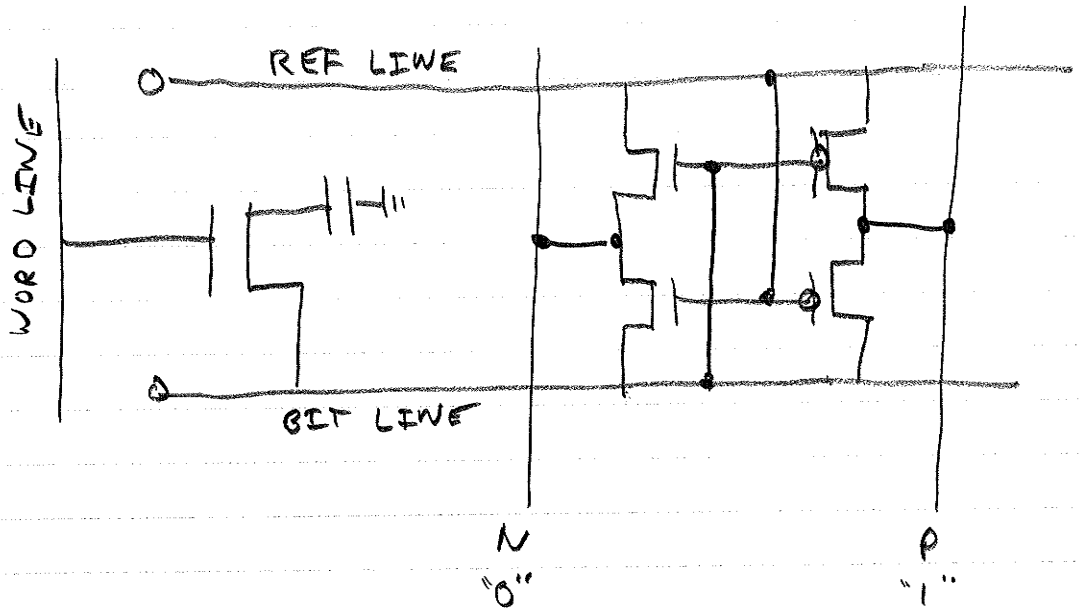
+

Bit stored on capacitor ... leaks!

→ "dynamic" requires constant refresh.

⇒ Also requires

"Differential Sense Amplification"

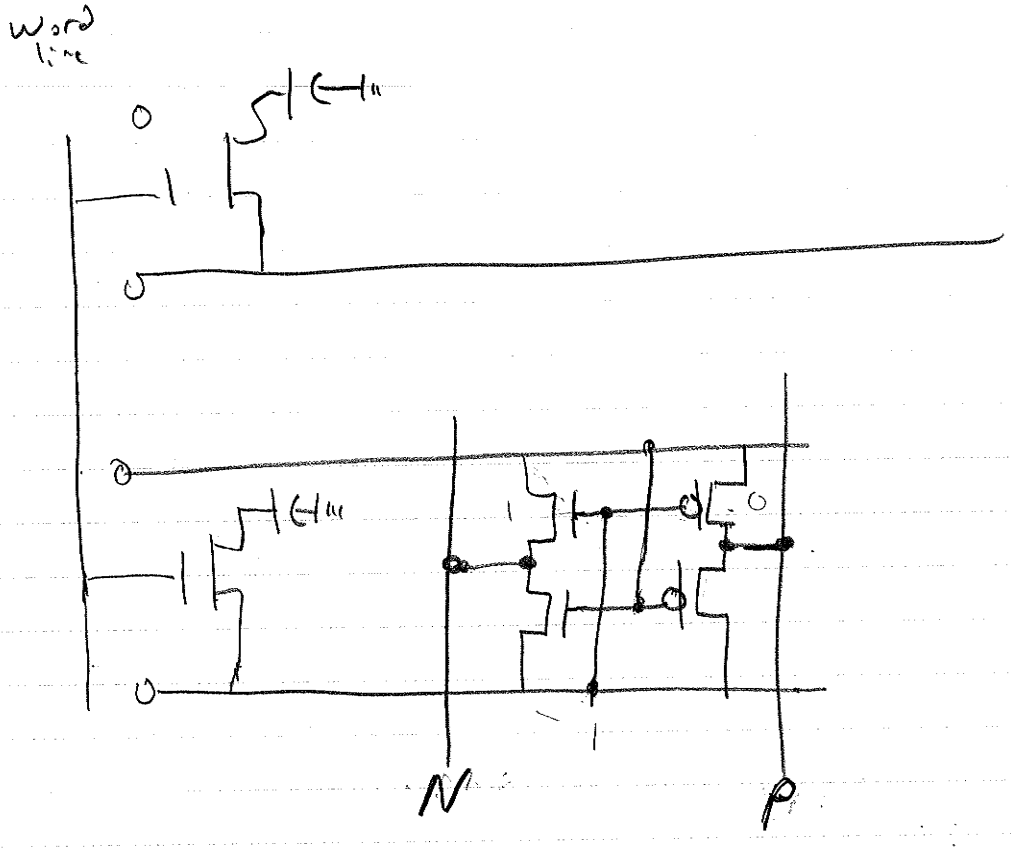


Now the beauty : read also refreshes.

Q: This requires 5 Transistors, but SRAm uses 4 ...

Why bother ?

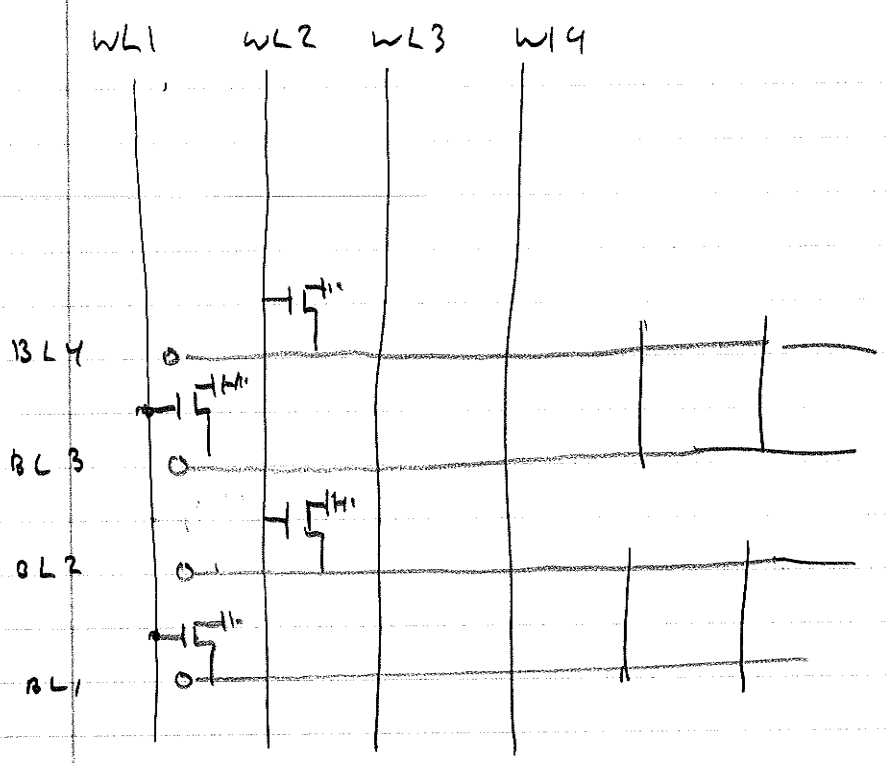
A: Multiplexing.



Heres beauty

→ Recharges cap

→ Buffers output



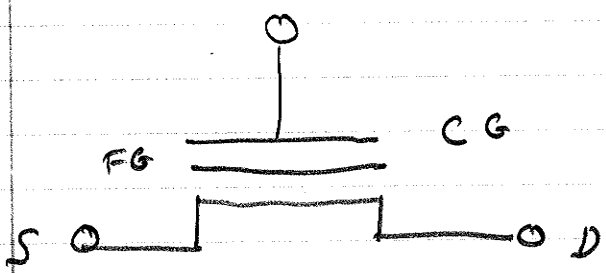
→ Reuse read / refresh transistors many times by multiplexing.

→ Each read circuit also acts as a buffer

Flash Memory

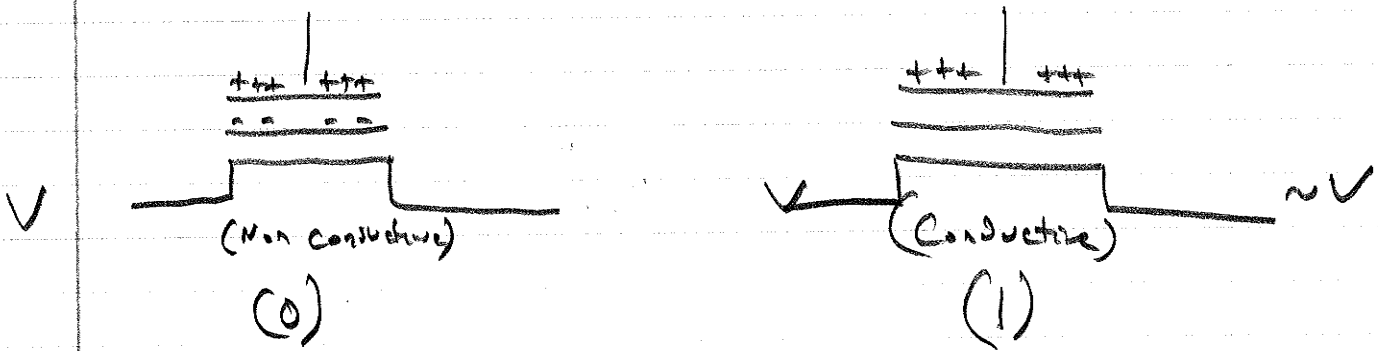
"Flash" of a camera to erase

Floating Gate Transistor

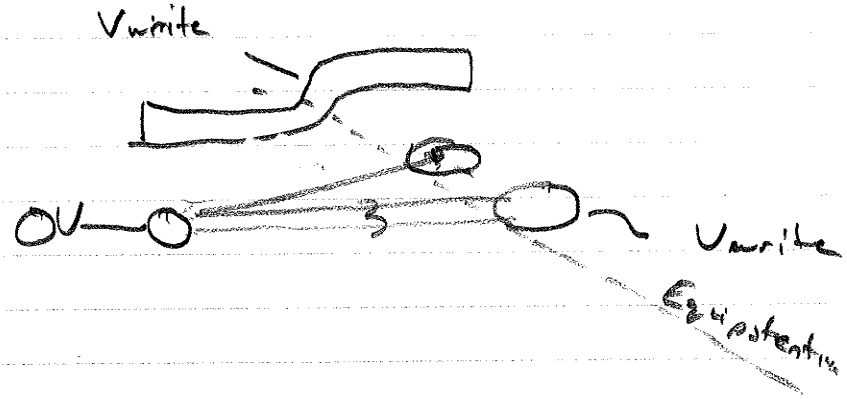


bit is stored on F.G as amount of charge.

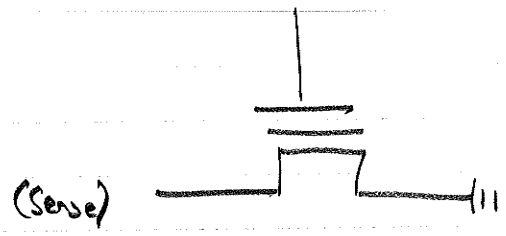
Save by applying positive voltage to CG



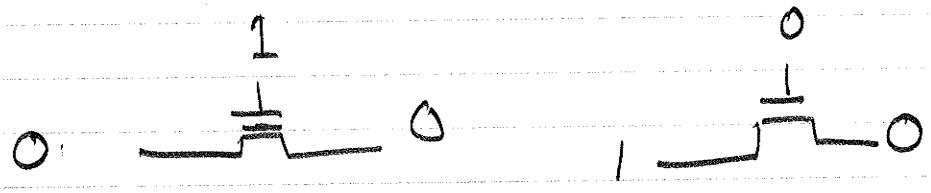
Inject Electrons (1 → 0)



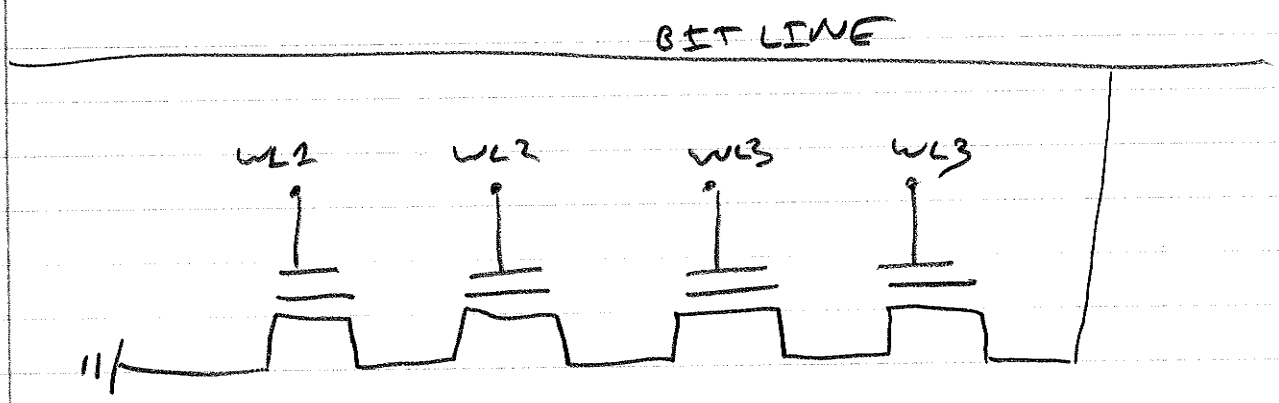
NOR / NAND flash



Acts like a NOR gate



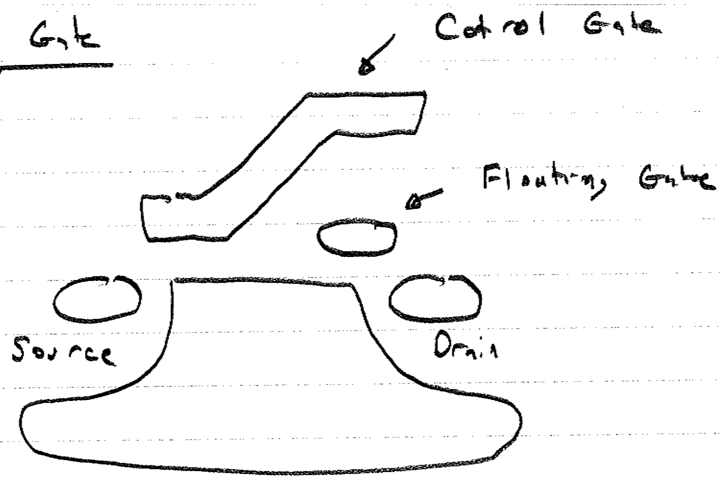
NAND



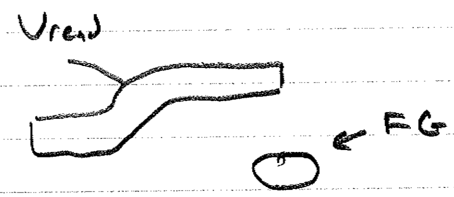
Set all but one WL high enough to ensure conductivity.

Set probe WL to "Vread" ...
Bit line pulled high or low depending on

Floating Gate



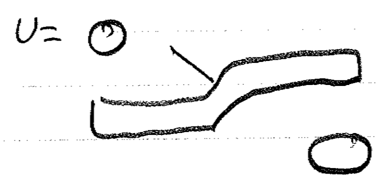
Sense



V_{read} O O — (sense) —|||

Current Flows depending on whether
FG screens (w/ −'s) or not.

Strip Electrons Off (0 → 1) "Erasing."



(V_{write} ~12V
> V_{read})

Open — O ⊂⊃ ⌐ |V_{write}

Any electrons jump resistive barrier
via quantum tunneling.