Review of Cold Electronics

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March 1, 2019

1 Survey of Relevant Devices

Device	Technology	Institution	Reference
DUNE Front-end ASIC	180 nm CMOS	BNL	[2]
SCT Front-end ASIC	250 nm CMOS	BNL	[3]
MicroBooNE Front-End ASIC	180 nm CMOS	BNL	

2 Transistor Modelling

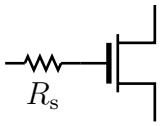

Figure 1: Model for intrinsic thermal noise as Johnson-Nyquist noise from an equivalent series resistance R_S.

For a well-designed amplifier based on a field-effect transistor, the noise will be dominated by the intrinsic thermal noise in the conducting channel, so that the drain current spectral density is given by

$$\langle i_D^2 \rangle = 4kTa_n g_m$$

where a_n is a dimensionless constant. Because the drain current and gate voltage are related by the transconductance:

$$i_D = g_m v_G$$

we can interpret the spectral density as if it were due to Johnson-Nyquist noise of an equivalent resistance R_s in series with the gate terminal:

$$\langle v_G^2 \rangle = 4kTR_s$$

with

$$R_s = a_n/g_m$$

For field effect devices $a_n \sim 2/3$.

The equivalent noise charge is the voltage spectral density multiplied by an effective bandwidth $1/t_{\mathrm{m}}$ from the impulse response of the amplifier, and scaled by the input capacitance C_{in}:

$$ENC^2 = 4kTR_{\mathrm{s}}C_{\mathrm{in}}^2\frac{1}{t_m}$$

The explicit temperature dependence is favorable to operation of a front-end amplifier under cryogenic conditions, but for precise modeling, the temperature dependence of the transistor parameters must also be understood.

3 Lifetime Reliability

The lifetime reliability of CMOS devices is degraded by four major effects: electromigration (EM), stress migration, thermal cycling (TC), and hot-carrier effects.

Electromigration (EM) is the movement of the conductor atoms from collisions with conducting electrons, which results in degradation of interconnects. The mean time to failure (MTTF) is:

$$\mathrm{MTTF}_{\mathrm{EM}} \propto J^{-n}\,\exp\left(\frac{E_{\mathrm{EM}}}{k_{\mathrm{b}}T}\right)$$

where J is the current density in the interconnect, E_{EM} is the activation energy for electromigration, and n is a constant for the conductor material. For copper $E_{\mathrm{EM}} = 1.1$ eV and $n = 0.9$.

Stress migration (SM) is the movement of conductor ions under thermo-mechanical stress resulting from mismatched thermal expansion rates, which results in degradation of interconnects. The mean time to failure is:

$$\mathrm{MTTF}_{\mathrm{SM}} \propto |T_0 - T|^{-m}\,\exp\left(\frac{E_{\mathrm{SM}}}{k_{\mathrm{b}}T}\right)$$

where T_0 is the metal deposition temperature, and m and E_{SM} are material properties. For copper, $E_{\mathrm{SM}} = 0.9$ eV and $n = 2.5$.

Thermal cycling (TC) is alternating heating and cooling of the device causing the accumulation of permanent mechanical damage.

$$\mathrm{MTTF}_{\mathrm{TC}} \propto \left(\frac{1}{\Delta T}\right)^q$$

Where ΔT is the change in temperature during one thermal cycle and q is an empirical constant for the material.

Under cryogenic conditions, the exponential dependence on temperature ensures that the effect of electromigration and stress migration on lifetime becomes neglible. Likewise, if held under constant cryogenic conditions, $\Delta T \to 0$ and so the effect of thermal cycling is likewise negligible.

That leaves hot-carrier effects, which we consider in the lucky-electron model. To reach sufficient energy $\phi_i \sim 1.3$ eV to create an electron-hole pair, an electron accelerated by an electric field E_{m} must travel at least a distance:

$$d = \frac{\phi_i}{qE_{\mathrm{m}}}$$

If the mean free path of the electron is λ, than the probability of an electron creating an electron-hole pair is:

$$\exp\left(-\frac{\phi_i}{q\lambda E}\right)$$

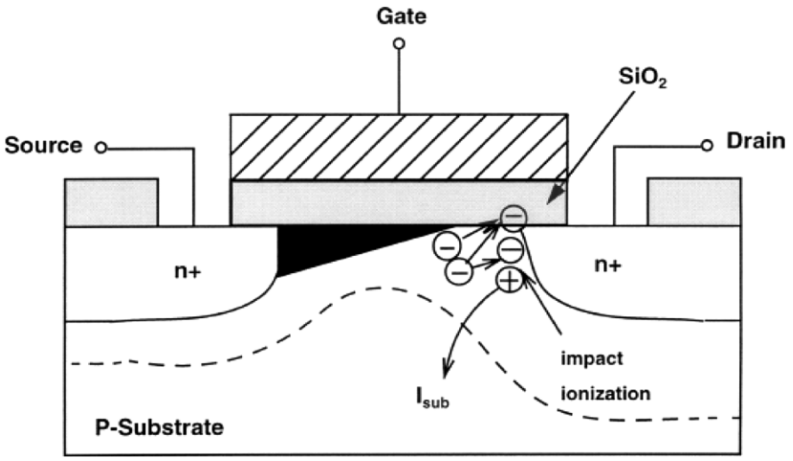

Figure 2: Schematic for interface state creation by hot-electrons, from [6].

Such an electron is called hot by analogy to a thermodynamic Boltzman factor.

In the context of a MOSFET, E_m is the difference between the applied voltage $V_{\rm ds}$ and the pinch off voltage. Hot electrons, and the electron hole pairs they produce, will be produced predominantly near the drain. The electrons will simply contribute to $I_{\rm ds}$, but the holes drift into the substrate, producing a substrate current:

$$I_{\rm sub} = C_1 I_{\rm ds} \exp\left(-\frac{\phi_i}{q\lambda E}\right) \tag{1}$$

The substrate current is proportional to the rate of hot-carrier creation and is therefore serves as a monitor for all hot-carrier effects.

Hot-carriers that reach sufficient energy $\phi_{\rm it} \sim 3.7$ eVcan create an interface state (acceptor-like trap) in the $\rm Si-SiO_2$ interface. This degrade transistor parameters such as transconductance, input resistance, and threshold voltage. Such hot-carriers are produced at a rate per channel width W proportional to:

$$\frac{I_{\rm ds}}{W} \exp\left(-\frac{\phi_{\rm it}}{q\lambda E}\right)$$

and so we can expect the lifetime (defined as some well-defined degradation in a particular parameter) to be:

$$\tau = C_2 \frac{W}{I_{\rm ds}} \exp\left(\frac{\phi_{\rm it}}{q\lambda E}\right) \tag{2}$$

From which we notice:

$$\log(\tau) \propto \frac{1}{\lambda E_{\rm m}}$$

Since the mean free path increases as the temperature decreases, hot-carrier effects can significantly reduce the lifetime of CMOS sensors in cryogenic conditions, and therefore must be estimated for each CMOS technology. Since E_m is related to the applied voltage, a popular approach is to raise $V_{\rm ds}$ until the lifetime is short enough to conveniently measure, then extrapolate back to the intended value for $V_{\rm ds}$. An example is shown in Fig. 4.

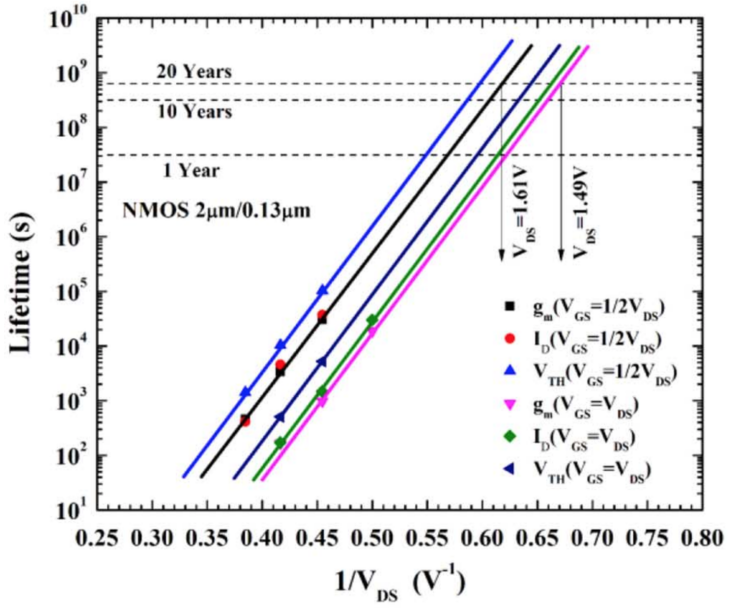

Figure 3: Example of over-voltage stress-testing to determine lifetime from [6].

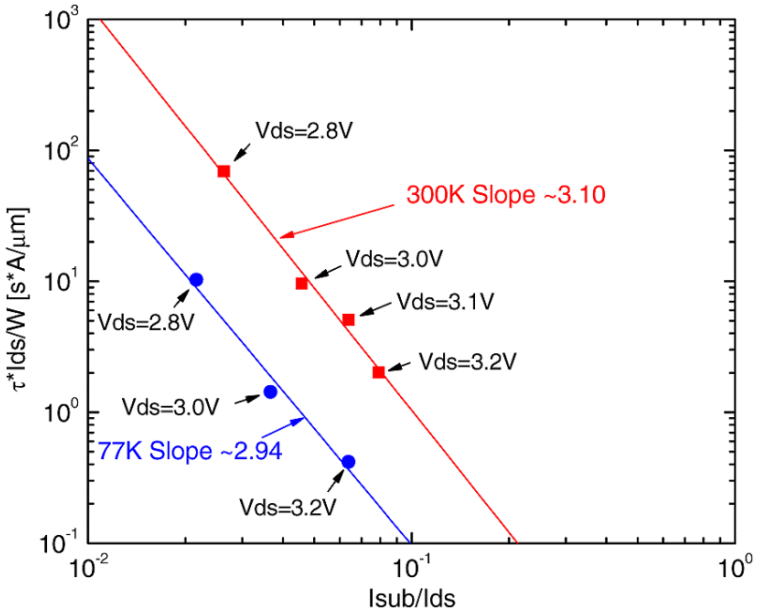

Figure 4: Example showing expected power-law relationship between $I_{rmsum}/I_{\rm ds}$ and $\tau I_{\rm ds}/W$, with slope $\phi_{\rm it}/\phi_i \sim 3$. From [6].

Another approach comes from Combining Equations 1 and 2 to eliminate the factor $q\lambda E$ to obtain:

$$\tau \propto \frac{W}{I_{\rm ds}} \left(\frac{I_{\rm ds}}{I_{\rm sub}} \right)^{(\phi_{\rm it}/\phi_{\rm i})} .$$

With $\phi_{\rm it}/\phi_i \sim 3$, the lifetime is seen to be sharply dependent on $I_{\rm ds}$. Operating at lower $V_{\rm ds}$ offers significant margin to the lifetime. This relation offers a second approach to estimating the lifetime that does not rely on over-voltage stressing, by simply monitoring the $I_{\rm sub}$ and I_{rmds}. (I suspect monitoring $I_{\rm sub}$ is useful for radiation hardness too?)

In explanation for how electrons to reach energies higher than the drain source potential difference is understood to be due to electron-electron scattering[[6]]. Commercial off-the-shelf ADCs, designed for room-temperature operation, where evaluated using these techniques and a candidate ADC was determined [7].

References

[1] Overview of the design considerations which support the choice of cold over warm electronics for large liquid argon TPCs. Describes TPC detector design, Equivalent Noise Charge for the initial MOSFET transistor, thermal noise in the sense wire, performance of MOS transistors at low temperature, lifetime

- V. Radeka *et al.*, "Cold electronics for 'Giant' Liquid Argon Time Projection Chambers," J. Phys. Conf. Ser. **308**, 012021 (2011). doi:10.1088/1742-6596/308/1/012021

[2] The Front-End ASIC design for the DUNE liquid Argon TDC, based on CMOS 180 nm technology, detailed introduction to noise model for MOSFET devices and comparisons between simulation and measured quantities. Highly useful references. One article:

- G. De Geronimo *et al.*, "Front-end ASIC for a Liquid Argon TPC," IEEE Trans. Nucl. Sci. **58**, 1376 (2011). doi:10.1109/TNS.2011.2127487

[3] Initial R&D which demonstrates that CMOS is better suited than JFET technology for cryogenic conditions. BNL developed a 250 nm CMOS ASIC for room temperature operation in the Silicon Compton Telescope. The equivalent noice charge (ENC) of the device was later characterized at cryogenic temperatures. In JFET devices, after initially decreasing and reaching a pedestal, freeze-out phenomena causes the ENC to increase again at very low temperatures in JFET devices. The CMOS device was shown to be free from freeze-out down to 40 K. Two articles:

- G. De Geronimo *et al.*, "Front-End ASIC for a Silicon Compton Telescope" IEEE Trans. Nucl. Sci. **55**, 4 (2008).

- H. Chen. *et al.*, "Cryogenic readout electronics R&D for MicroBooNE and beyond" IEEE Trans. Nucl. Sci. **55**, 4 (2008).

[4] Superb review of theory and techniques for reducing and characterizing noise in particle detectors and analog front-ends. Particularly important to us are Equations 52 and 53 on page 247. One article:

- V. Radeka, "Low-Noise Techniques in Detectors", Ann. Rev. Nucl. Part. Sci. **38**, 217 (1988). https://www.annualreviews.org/doi/pdf/10.1146/annurev.ns.38.120188.001245

[5] Summary of how CMOS technology scaling affects lifetime reliability. Scaling would tend to improve reliability, if voltage were reduced to keep power density constant. Instead, power density is increasing and therefore the temperature increases. The temperature dependence of the main sources of intrinsic hard failures: electromigration, stress migration, time-dependent dielectric breakdown, and thermal cycling. See Equations 1,2,3, and 4 and Table 1. One Article:

- J. Srinivasan, S. Adve, P. Bose, and J. Rivers, "The Impact of Technology Scaling on Lifetime Reliability" Proceedings of the 2004 International Conference on Dependable Systems and Networks. doi:10.1109/DSN.2004.1311888

[6] Lifetime measurements of CMOS. The first article has a very good overview of the model for hot-carrier effects and techniques for measuring lifetime, and presents results for 180 nm CMOS. Further references (see p. 4738) describe the role of electron-electron scattering. The second, more recent article, presents the lifetime results for 130 nm and 75 nm CMOS. The third article is a dated and somewhat difficult read original application of the "lucky-electron" model to describe Hot-electron effects in MOSFETs. The last, more recent article, provides much more detail.

- S. Li and others, "LAr TPC Electronics CMOS Lifetime at 300 K and 77 K and Reliability Under Thermal Cycling", IEEE Trans. Nucl. Sci. 60(6):4737-4743 (2013).
- J. Hoff and others, "Cryogenic Lifetime Studies of 130 nm and 65 nm nMOS Transistors for High-Energy Physics Experiments", IEEE Trans. Nucl. Sci. 62(3):1255-1261 (2015). doi:10.1109/TNS.2015.2433793
- C. Hu and others, "Hot-Electron-Induced MOSFET Degradation–Model, Monitor, and Improvement", IEEE Trans. Electron Devices, 32(2):375 (1985).
- P. Heremans and others, "Temperature Dependence of the Channel Hot-Carrier Degradation of n-Channel MOSFET's", IEEE Trans. Electron Devices, 37(4):980 (1990).

[7] Reports on techniques and preliminary measurements of the lifetime of commercial-off-the-shelf (COTS) ADCs under cryogenic conditions.

- H. Chen and others, "Lifetime Study of COTS ADC for SBND LAr TPC Readout Electronics", arXiv:1806.09226 [physics.ins-det].