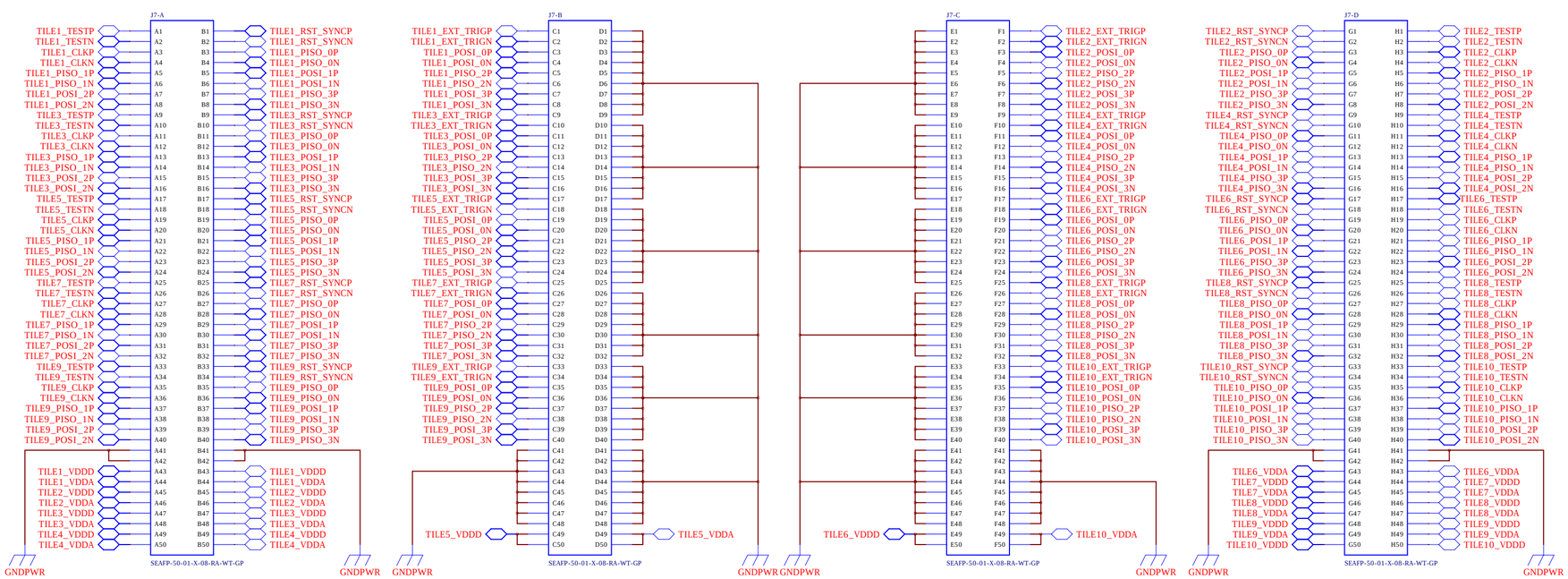
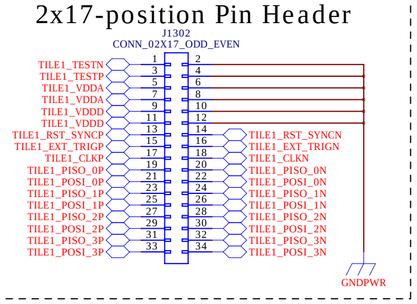
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

SAMTEC 400-position High-Density Connector



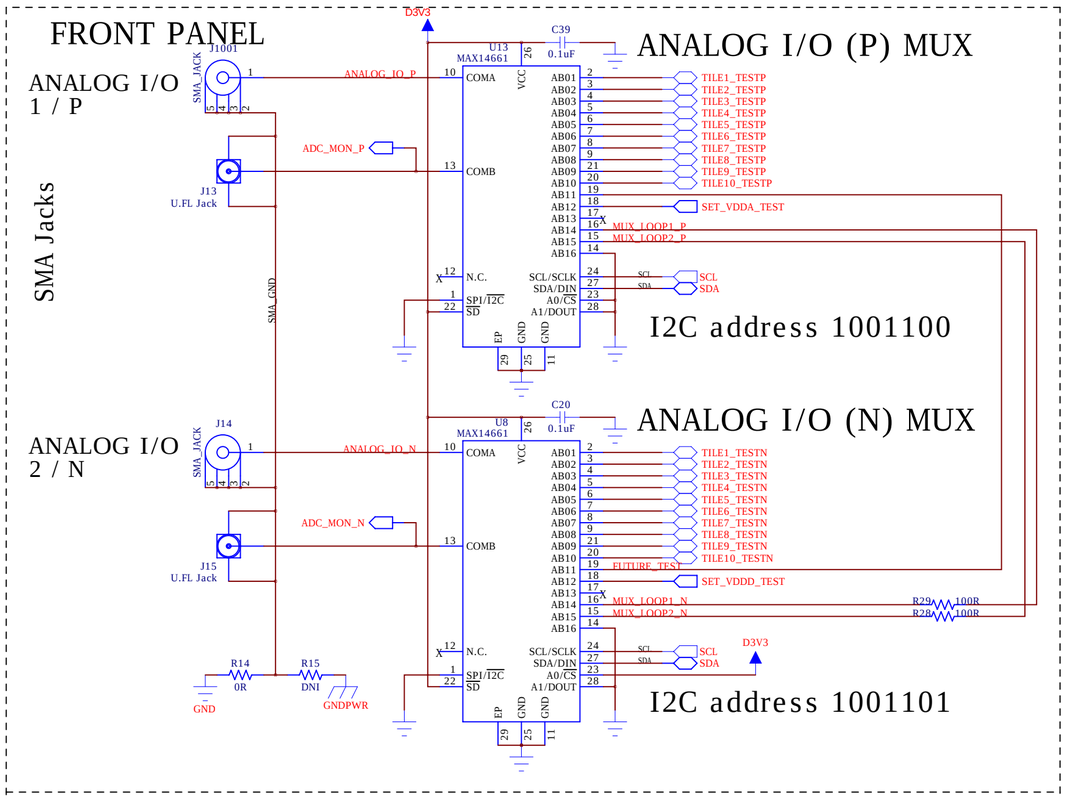
2x17-position Pin Header

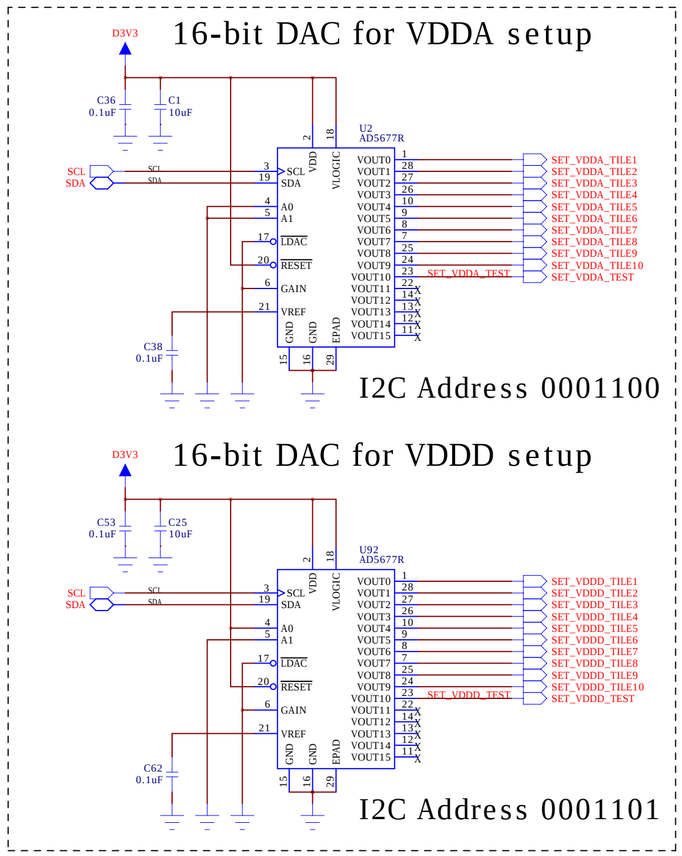


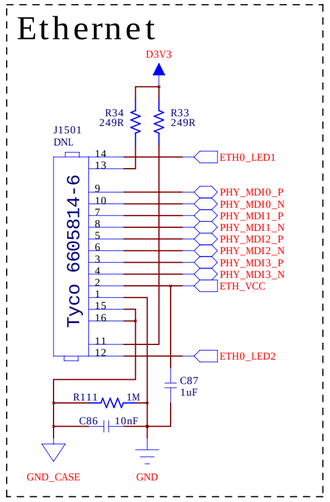
CONNECTOR

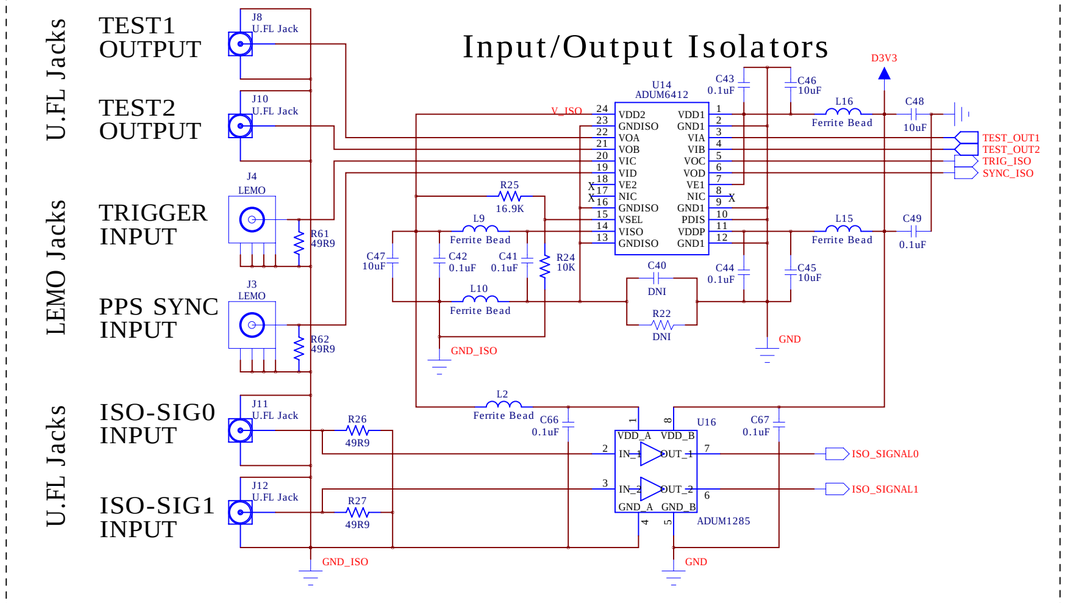
DRAWN: H.G.Berns	DATED: 05/15/2024	COMPANY: University of California Davis	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: LarPix PACMAN Version 5	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code> / SIZE: C	DRAWING NO: PacMan_V5.sch / REV: 5
RELEASED: H.G.Berns	DATED: 05/15/2024	SCALE: <Scale>	SHEET: 1 OF 16

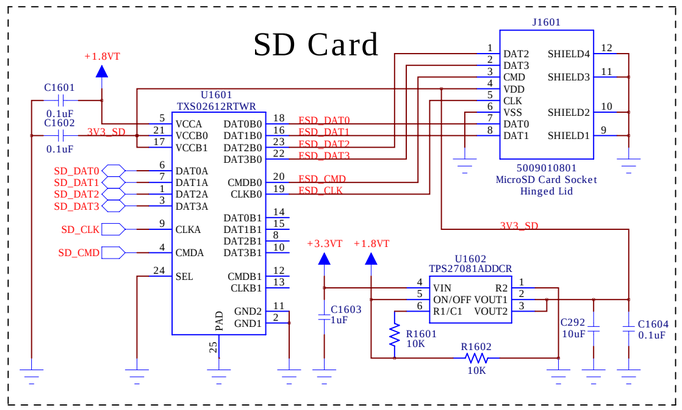
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

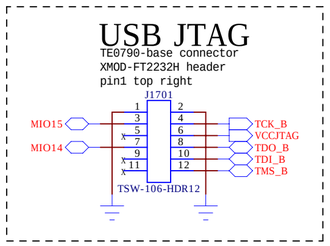


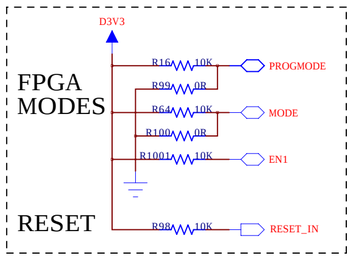


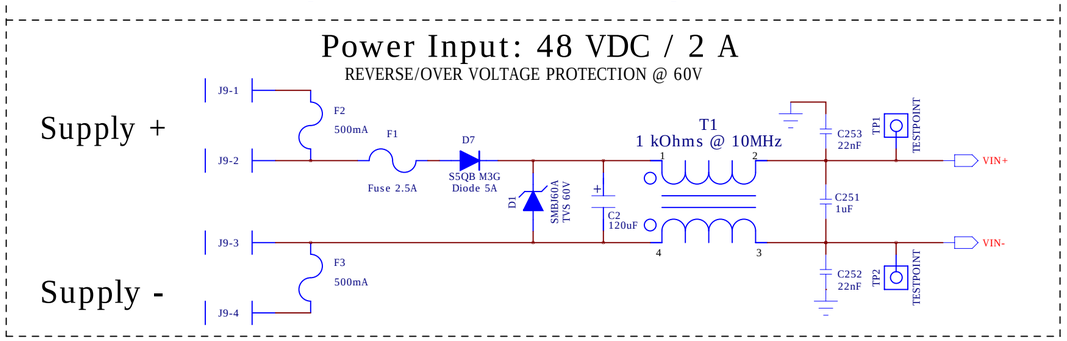








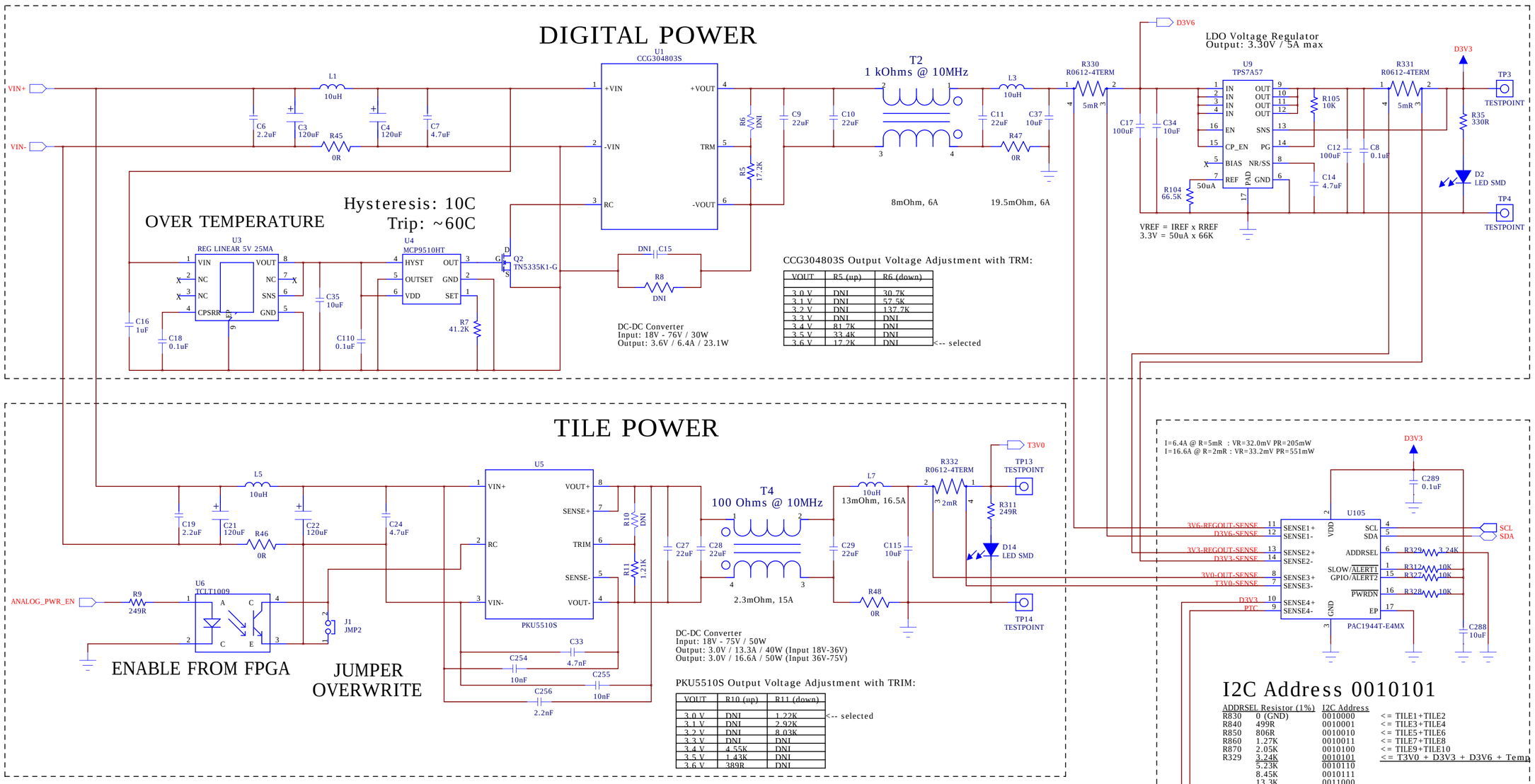


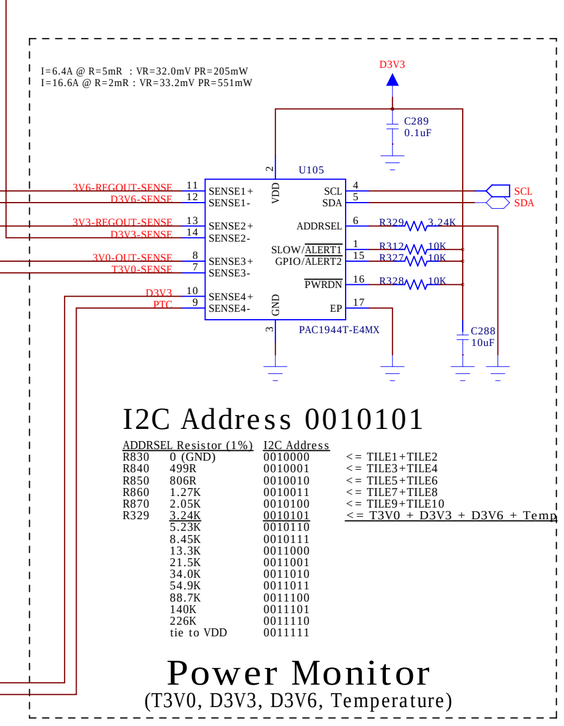


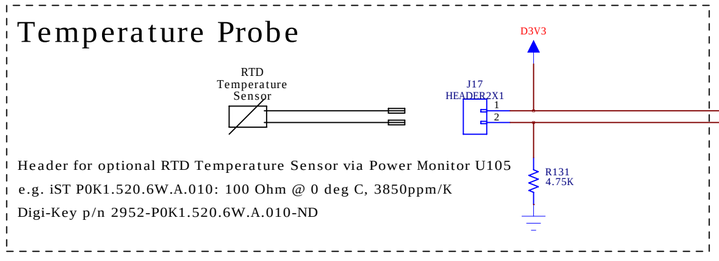
FRONT PANEL & PERIPHERALS

COMPANY: University of California Davis			
TITLE: LarPix PACMAN Version 5			
DRAWN: H.G.Berns	DATED: 05/15/2024	CODE: <Code>	SIZE: C
CHECKED: <Checked By>	DATED: <Checked Date>	DRAWING NO: PacMan_V5.sch	REV: 5
QUALITY CONTROL: <QC By>	DATED: <QC Date>		
RELEASED: H.G.Berns	DATED: 05/15/2024	SCALE: <Scale>	SHEET: 1 OF 16

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:





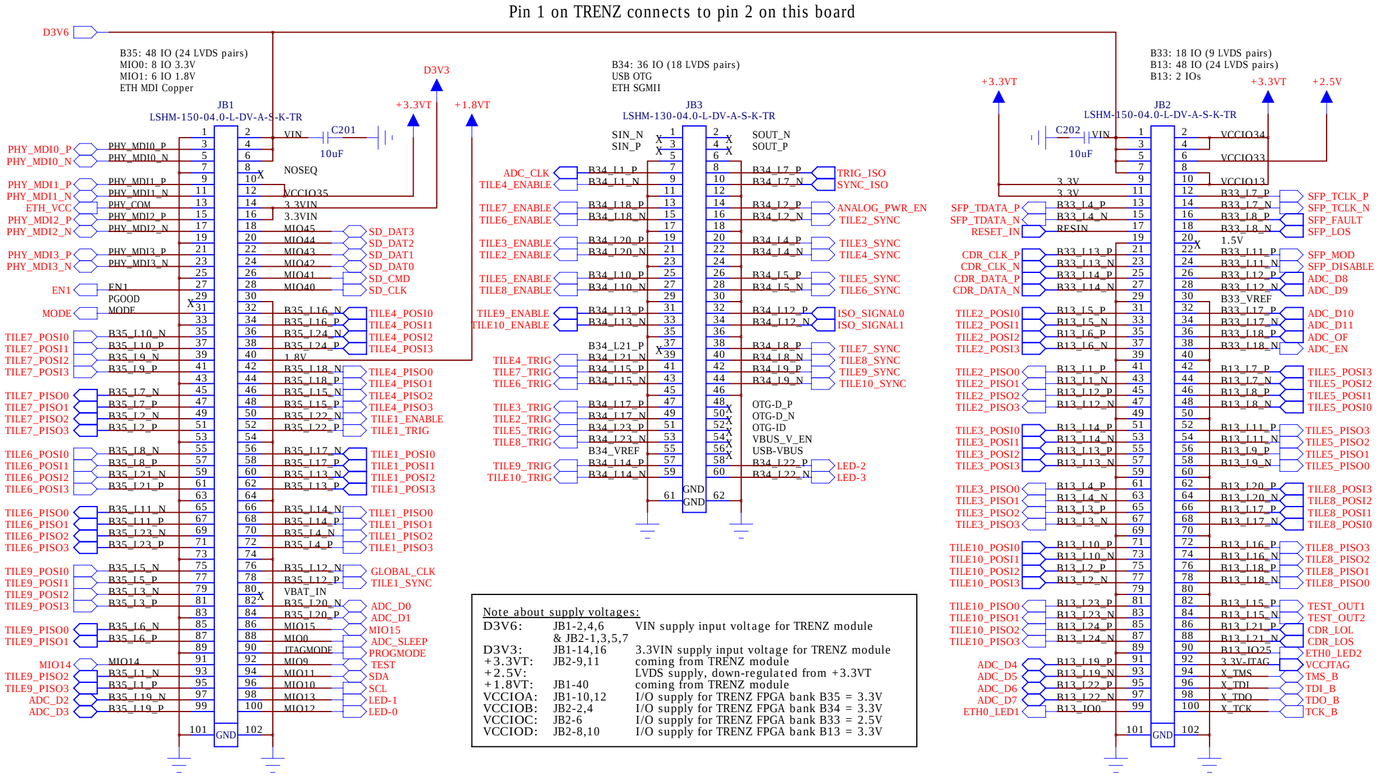


POWER

DRAWN: H.G.Berns	DATED: 05/15/2024	COMPANY: University of California Davis	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: LarPix PACMAN Version 5	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: C
RELEASED: H.G.Berns	DATED: 05/15/2024	DRAWING NO: PacMan_V5.sch	REV: 5
		SCALE: <Scale>	SHEET: 01 OF 16

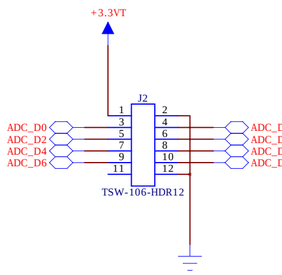
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

Pin numbers are mirrored on TRENZ board
Pin 1 on TRENZ connects to pin 2 on this board

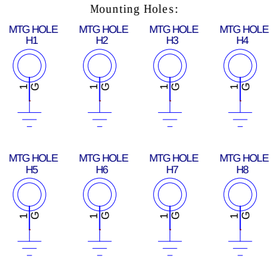


Note about supply voltages:

D3V6:	JB1-2,4,6 & JB2-1,3,5,7	VIN supply input voltage for TRENZ module
D3V3:	JB1-14,16	3.3VIN supply input voltage for TRENZ module
+3.3VT:	JB2-9,11	coming from TRENZ module
+2.5V:		LVDS supply, down-regulated from +3.3VT
+1.8VT:	JB1-40	coming from TRENZ module
VCCIOA:	JB1-10,12	I/O supply for TRENZ FPGA bank B35 = 3.3V
VCCIOB:	JB2-2,4	I/O supply for TRENZ FPGA bank B34 = 3.3V
VCCIOC:	JB2-6	I/O supply for TRENZ FPGA bank B33 = 2.5V
VCCIOD:	JB2-8,10	I/O supply for TRENZ FPGA bank B13 = 3.3V

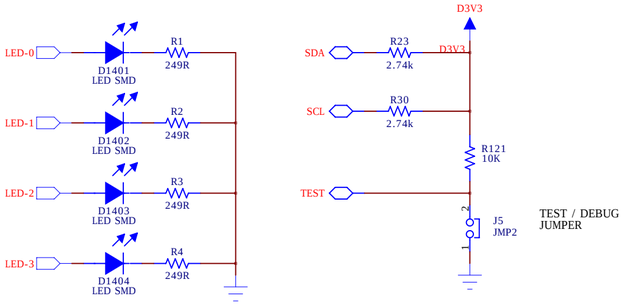


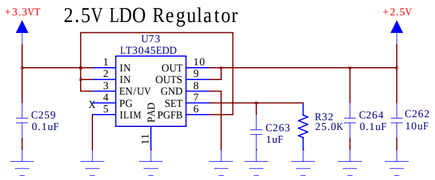
Mounting Holes:



I2C Addresses used in this version:

Address	RefDes	Device	Function
0001100	U2	AD5677	16-chan. 16-bit DAC for VDDA setup
0001101	U92	AD5677	16-chan. 16-bit DAC for VDDD setup
0010000	U11	PAC1944	4-chan. Power Monitor VDDA+VDDD Tile1 + Tile2
0010001	U20	PAC1944	4-chan. Power Monitor VDDA+VDDD Tile3 + Tile4
0010010	U21	PAC1944	4-chan. Power Monitor VDDA+VDDD Tile5 + Tile6
0010011	U23	PAC1944	4-chan. Power Monitor VDDA+VDDD Tile7 + Tile8
0010100	U94	PAC1944	4-chan. Power Monitor VDDA+VDDD Tile9 + Tile10
0010101	U105	PAC1944	4-chan. Power Monitor T3V0 + D3V6 + D3V3
1001100	U13	MAX14661	16:2 Analog Monitor MUX
1001101	U8	MAX14661	16:2 DAC Test MUX
1010000	J6	SFP	SFP Module for Timing (primary addr.)
1010001	J6	SFP	SFP Module for Timing (secondary addr.)
1100000	U63	ADN2814	Clock & Data Recovery (CDR) for Timing



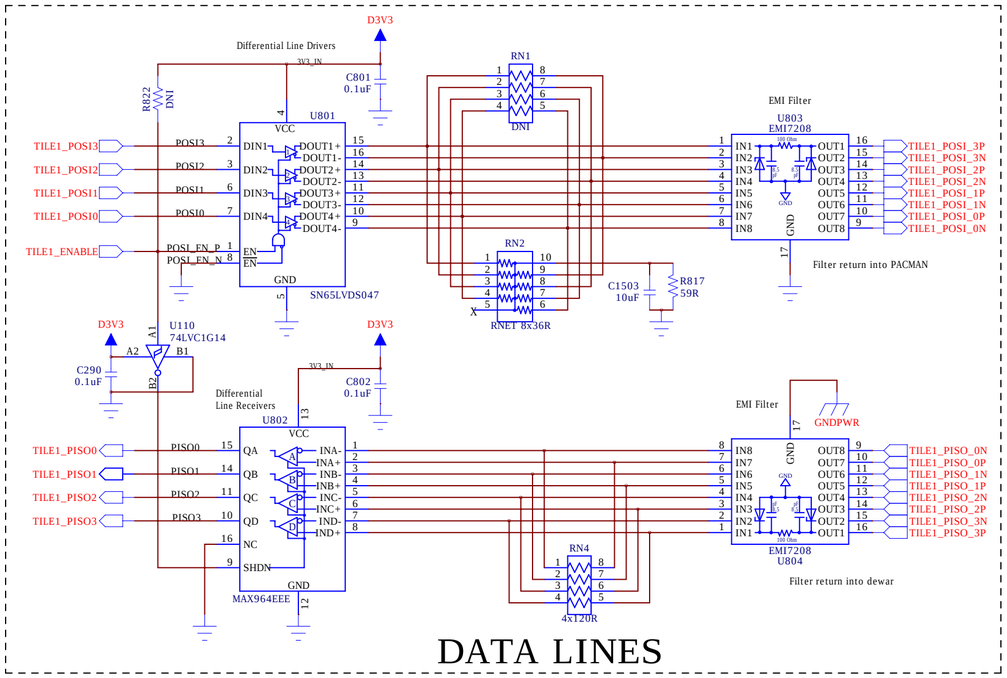


TRENZ

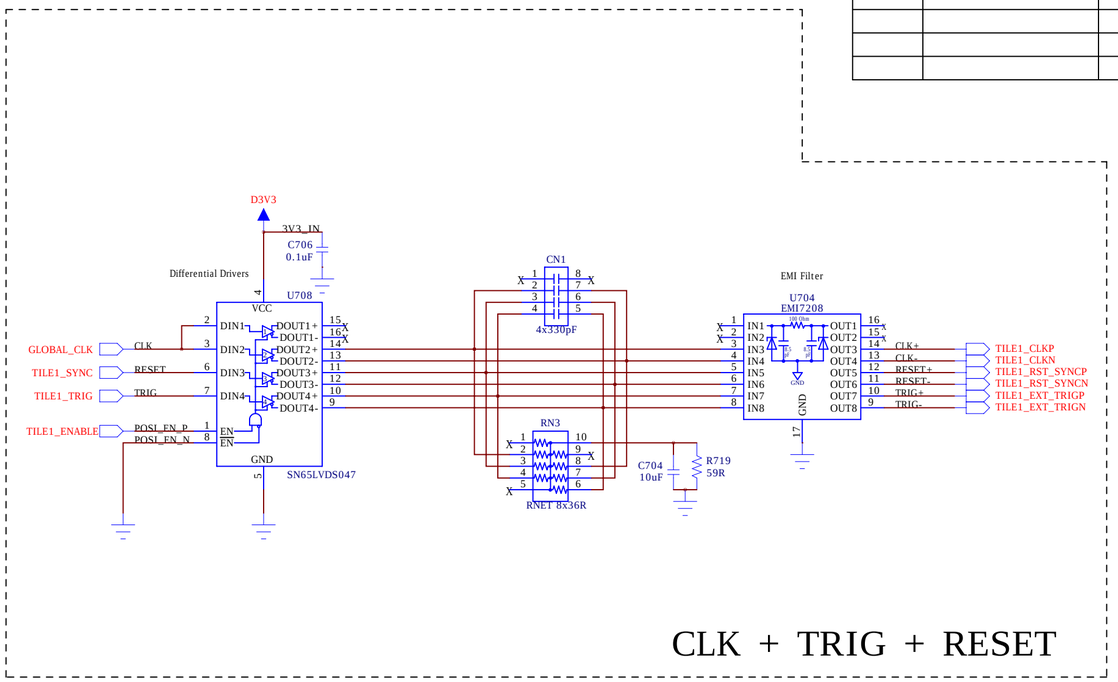
DRAWN: H.G.Berns	DATED: 05/15/2024	COMPANY: University of California Davis	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: LarPix PACMAN Version 5	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code> / SIZE: C / DRAWING NO: PacMan_V5.sch	REV: 5
RELEASED: H.G.Berns	DATED: 05/15/2024	SCALE: <Scale>	SHEET: 1 OF 16

$$$21078
$$$21078

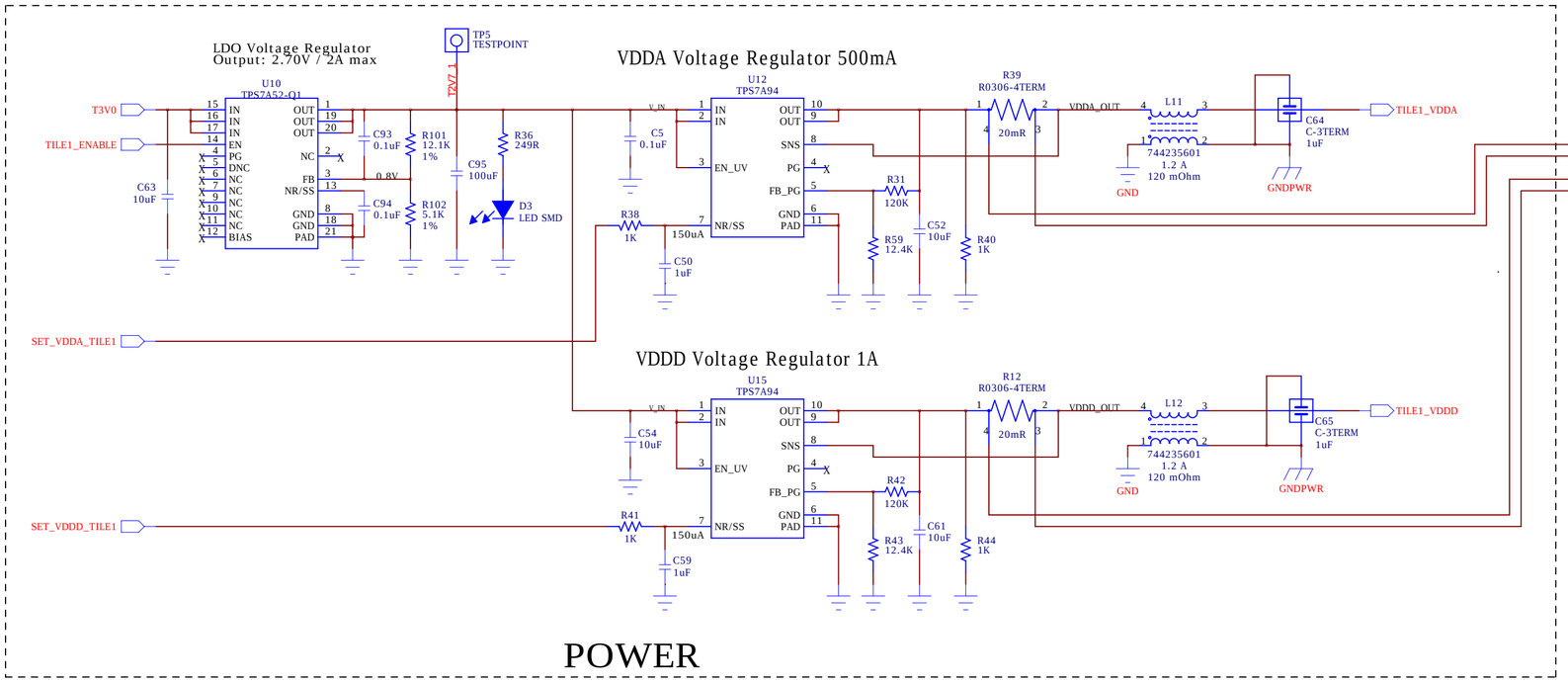
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



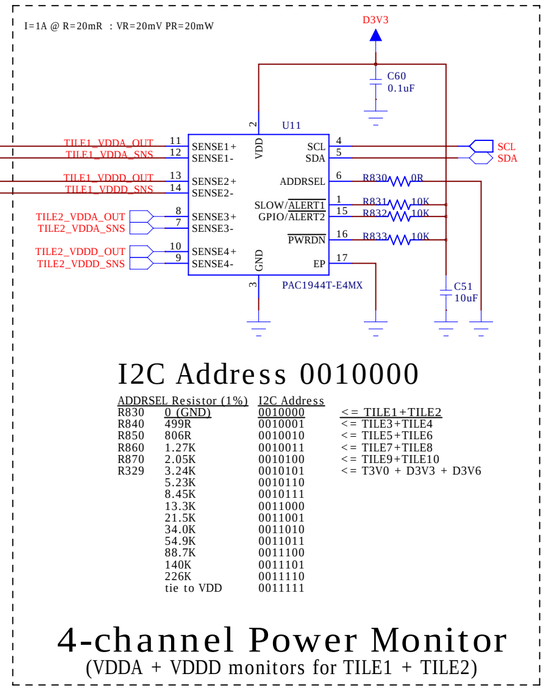
DATA LINES



CLK + TRIG + RESET



POWER



I2C Address 0010000

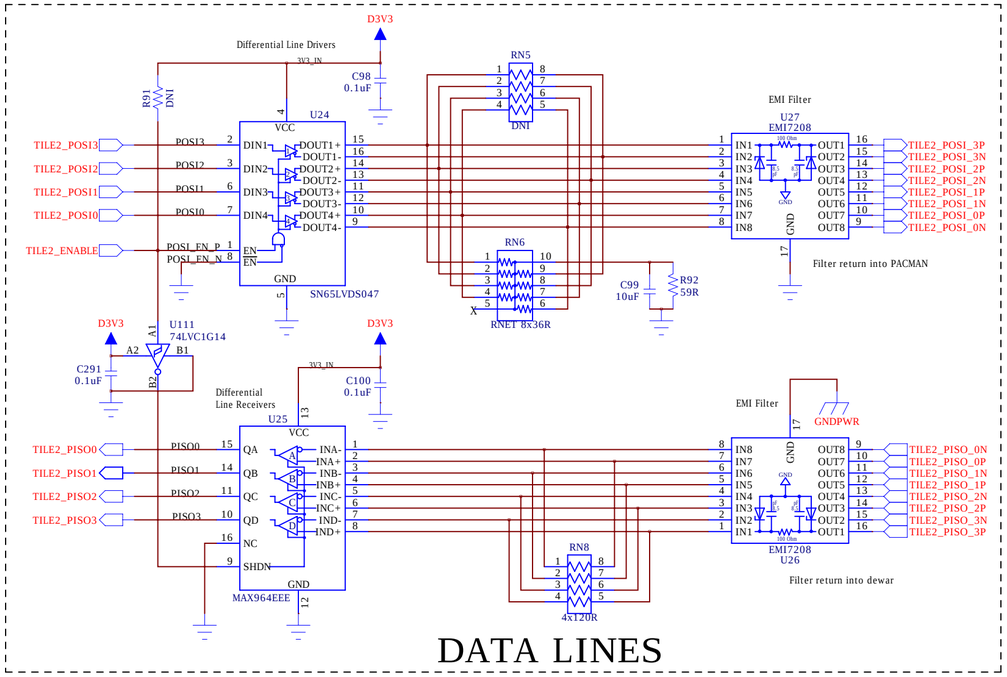
ADDRSEL	Resistor (1%)	I2C Address	
R830	0 (GND)	0010000	<= TILE1+TILE2
R840	499R	0010001	<= TILE3+TILE4
R850	806R	0010010	<= TILE5+TILE6
R860	1.27K	0010011	<= TILE7+TILE8
R870	2.05K	0010100	<= TILE9+TILE10
R329	3.24K	0010101	<= T3V0 + D3V3 + D3V6
	5.23K	0010110	
	8.45K	0010111	
	13.3K	0011000	
	21.5K	0011001	
	34.0K	0011010	
	54.9K	0011011	
	88.7K	0011100	
	140K	0011101	
	226K	0011110	
	tie to VDD	0011111	

4-channel Power Monitor
(VDDA + VDDD monitors for TILE1 + TILE2)

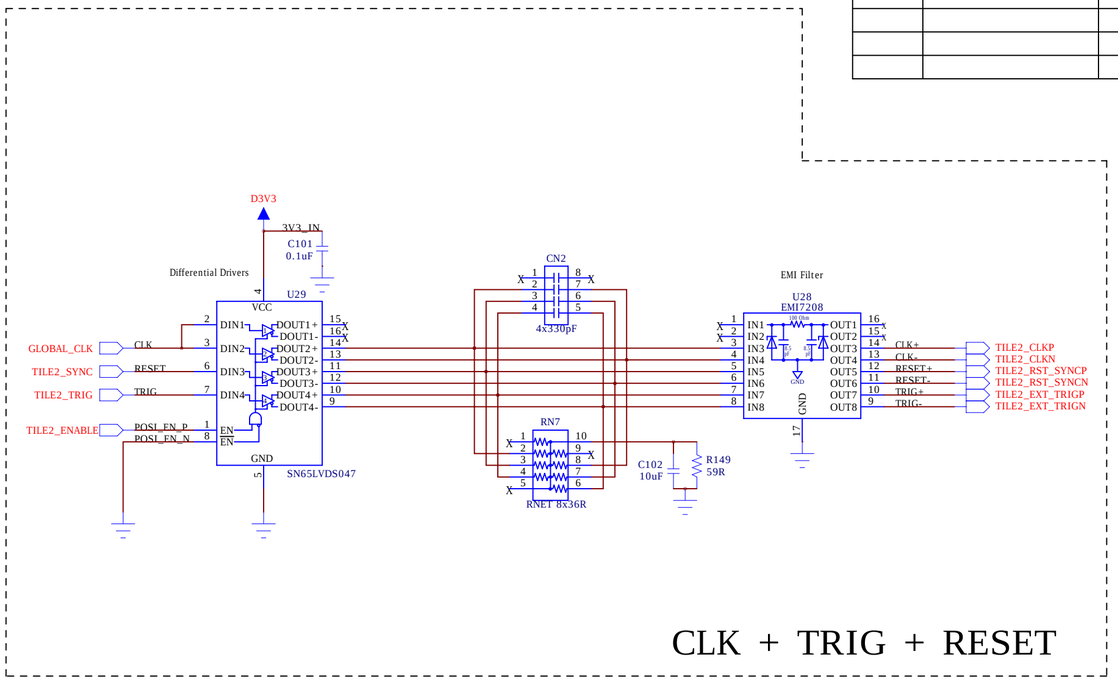
TILE1

DRAWN: H.G.Berns	DATED: 05/15/2024	COMPANY: University of California Davis	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: LarPix PACMAN Version 5	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: C
RELEASED: H.G.Berns	DATED: 05/15/2024	DRAWING NO: PacMan_V5.sch	REV: 5
		SCALE: <Scale>	SHEET: 5 OF 16

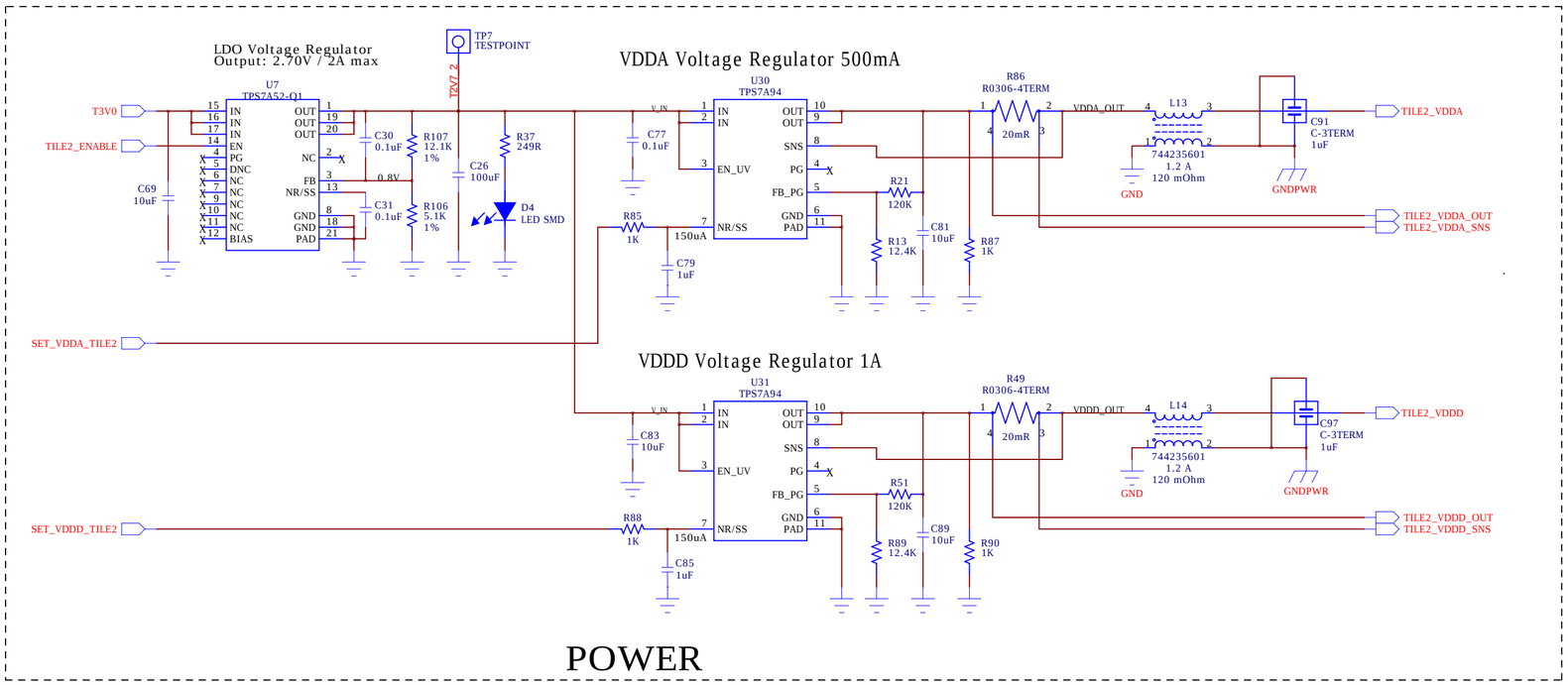
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



DATA LINES



CLK + TRIG + RESET

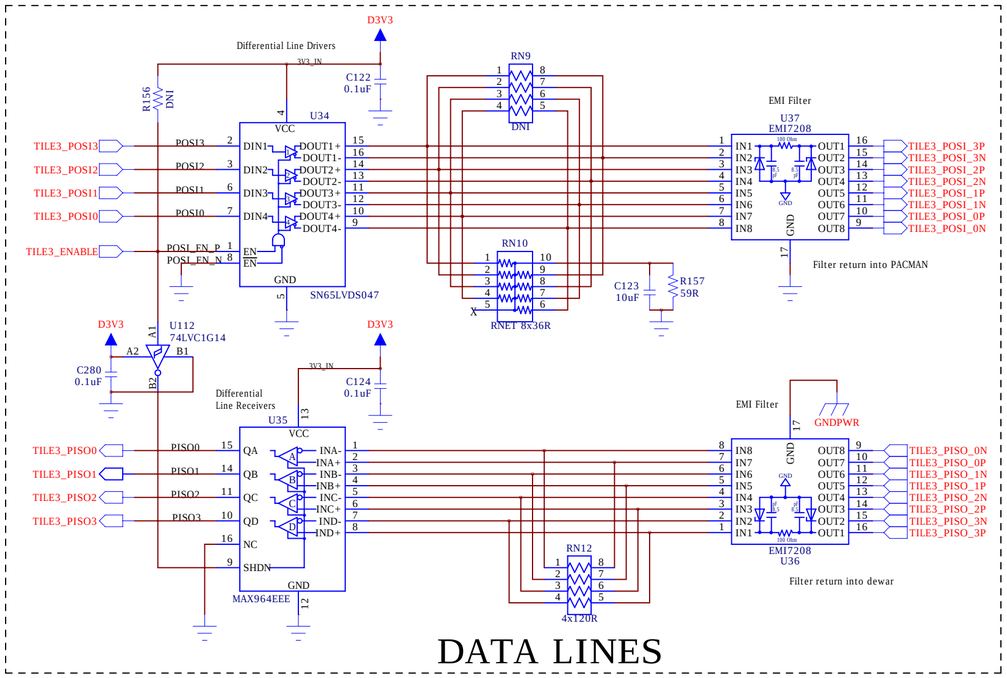


POWER

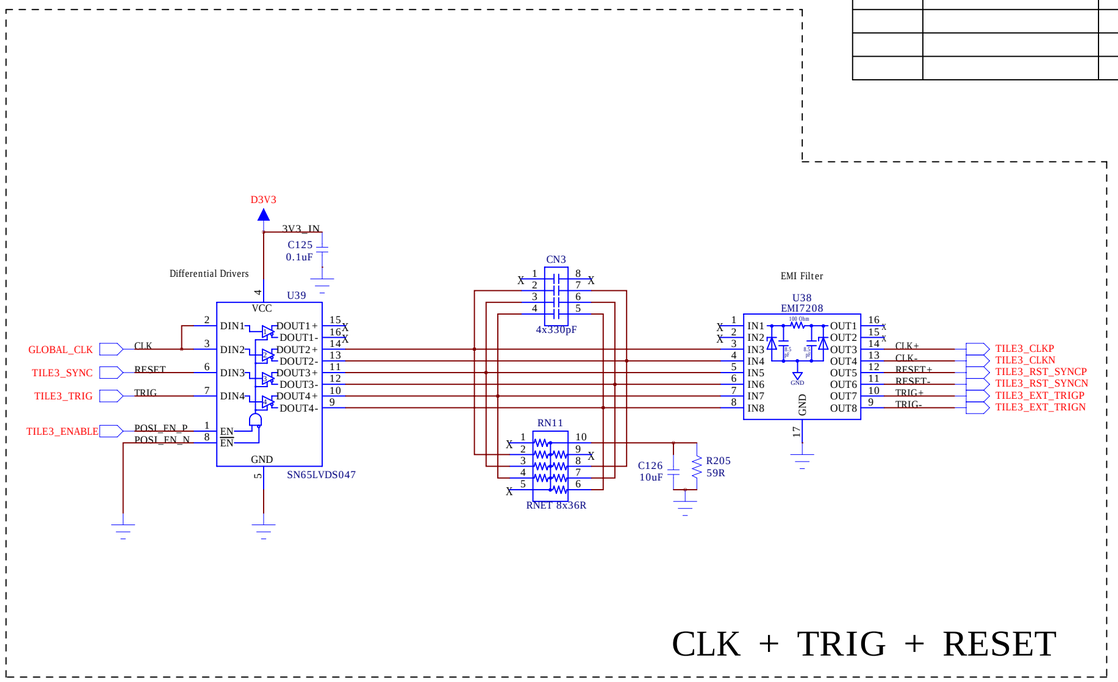
TILE2

DRAWN: H.G.Berns	DATED: 05/15/2024	COMPANY: University of California Davis	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: LarPix PACMAN Version 5	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code> / SIZE: C / DRAWING NO: PacMan_V5.sch	REV: 5
RELEASED: H.G.Berns	DATED: 05/15/2024	SCALE: <Scale>	SHEET: 6 OF 16

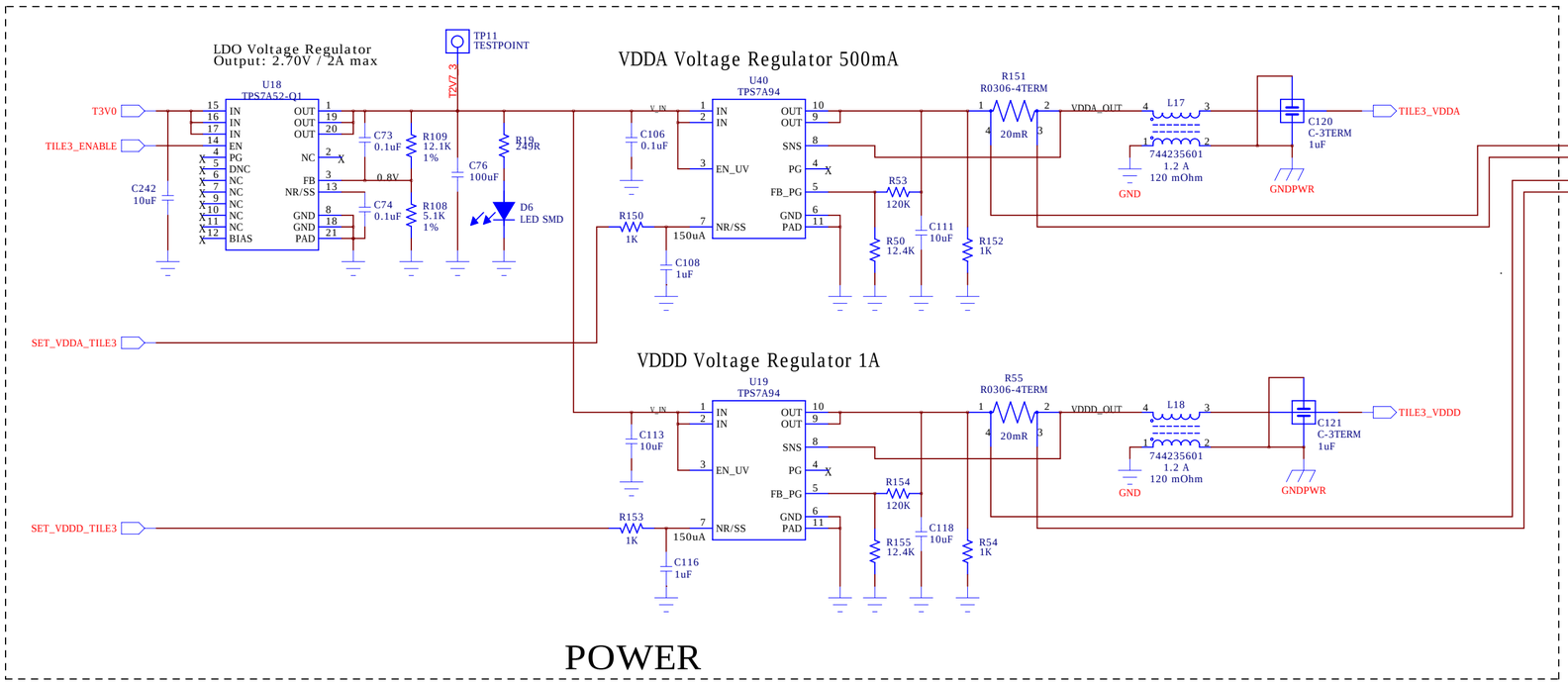
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



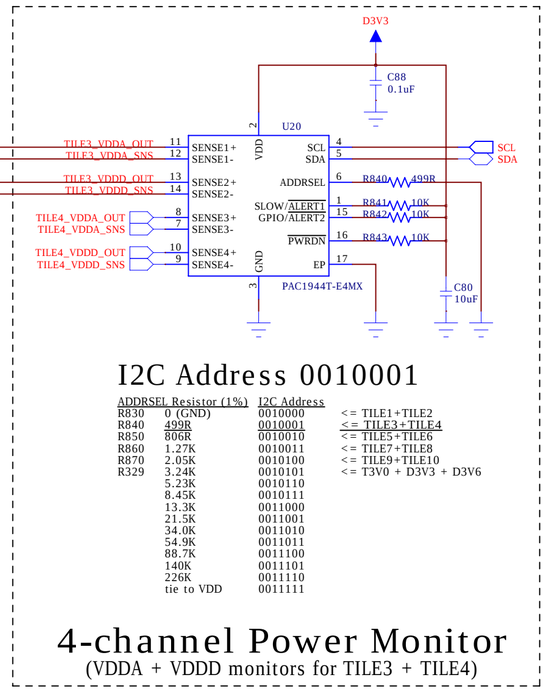
DATA LINES



CLK + TRIG + RESET



POWER



I2C Address 0010001

ADDRSEL Resistor (1%)		I2C Address	
R830	0 (GND)	0010000	<= TILE1+TILE2
R840	499R	0010001	<= TILE3+TILE4
R850	806R	0010010	<= TILE5+TILE6
R860	1.27K	0010011	<= TILE7+TILE8
R870	2.05K	0010100	<= TILE9+TILE10
R329	3.24K	0010101	<= T3V0 + D3V3 + D3V6
	5.23K	0010110	
	8.45K	0010111	
	13.3K	0011000	
	21.5K	0011001	
	34.0K	0011010	
	54.9K	0011011	
	88.7K	0011100	
	140K	0011101	
	226K	0011110	
	tie to VDD	0011111	

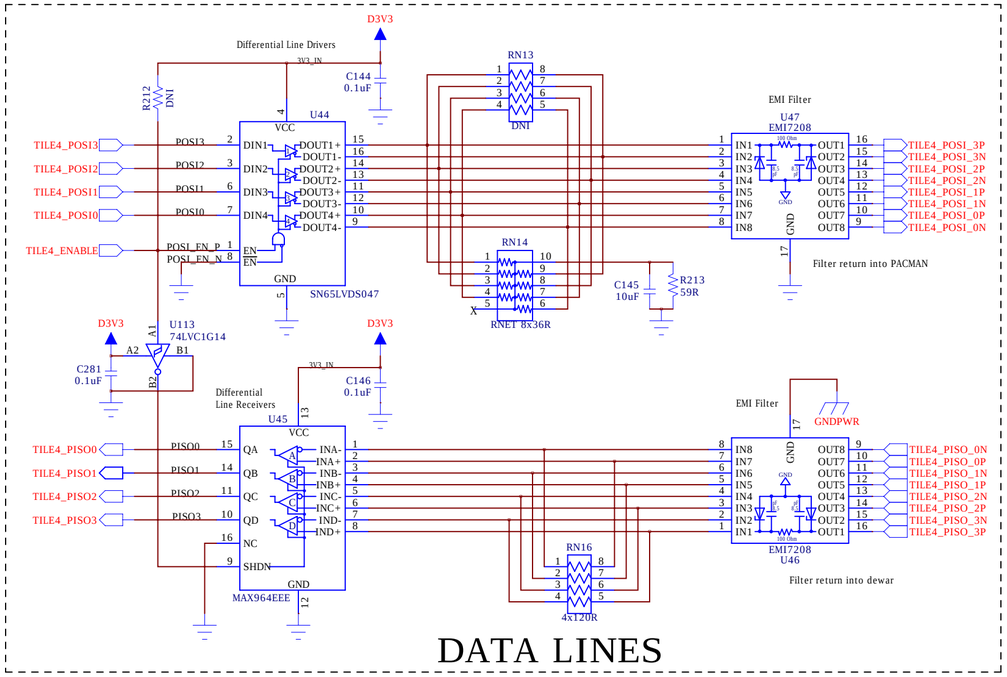
4-channel Power Monitor

(VDDA + VDDD monitors for TILE3 + TILE4)

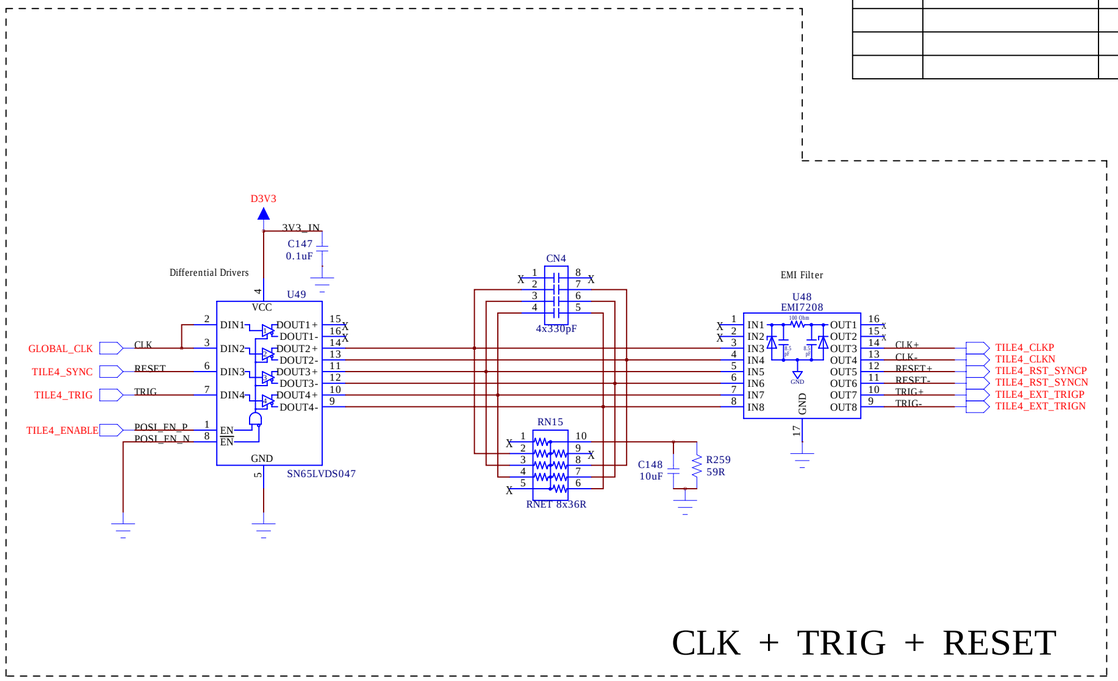
TILE3

DRAWN: H.G.Berns	DATED: 05/15/2024	COMPANY: University of California Davis	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: LarPix PACMAN Version 5	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: C
RELEASED: H.G.Berns	DATED: 05/15/2024	DRAWING NO: PacMan_V5.sch	REV: 5
		SCALE: <Scale>	SHEET: 7 OF 16

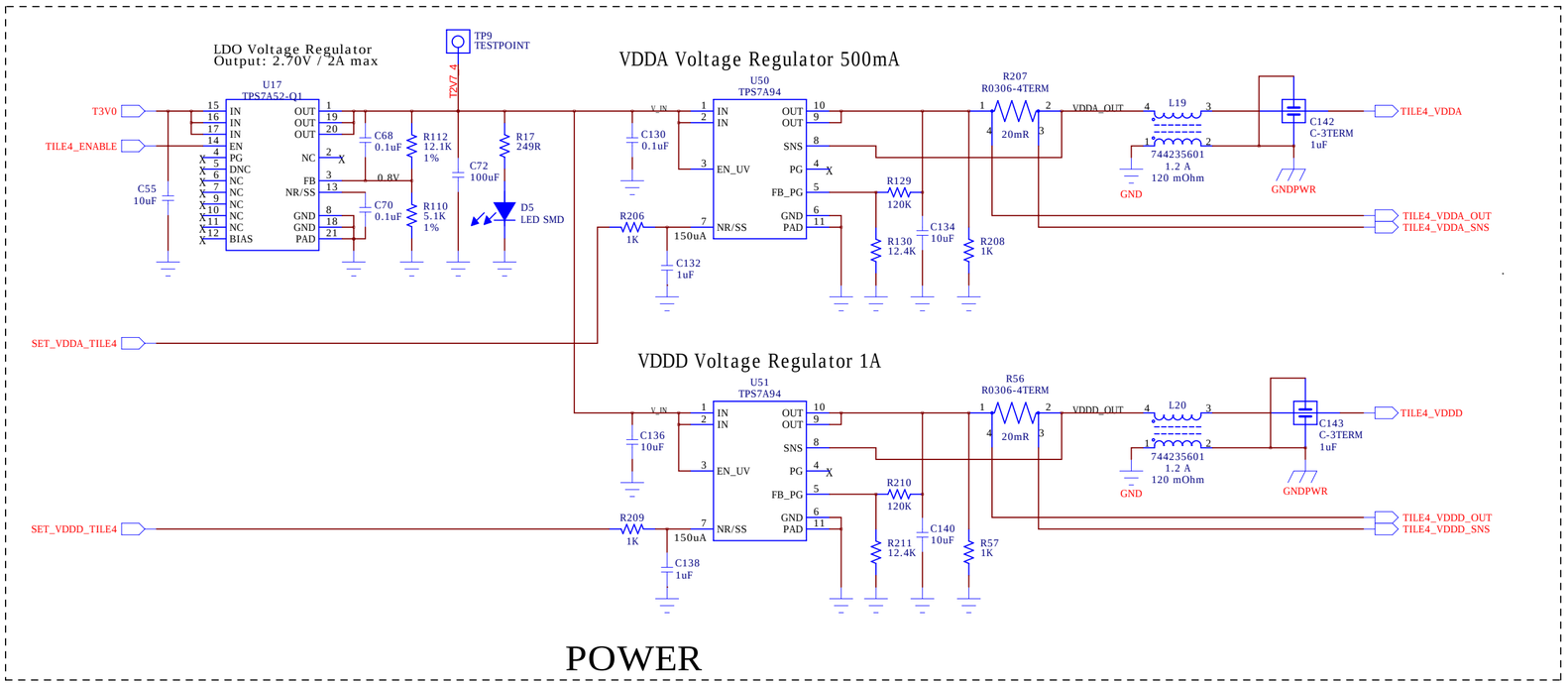
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



DATA LINES



CLK + TRIG + RESET

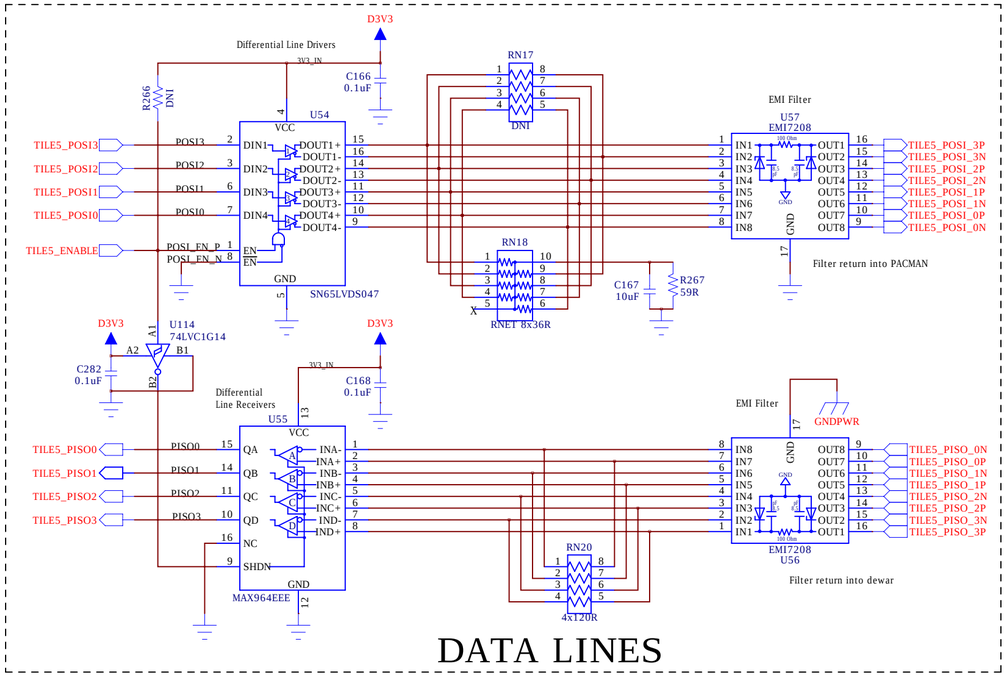


POWER

TILE4

DRAWN: H.G.Berns	DATED: 05/15/2024	COMPANY: University of California Davis	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: LarPix PACMAN Version 5	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code> / SIZE: C	DRAWING NO: PacMan_V5.sch / REV: 5
RELEASED: H.G.Berns	DATED: 05/15/2024	SCALE: <Scale>	SHEET: 8 OF 16

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



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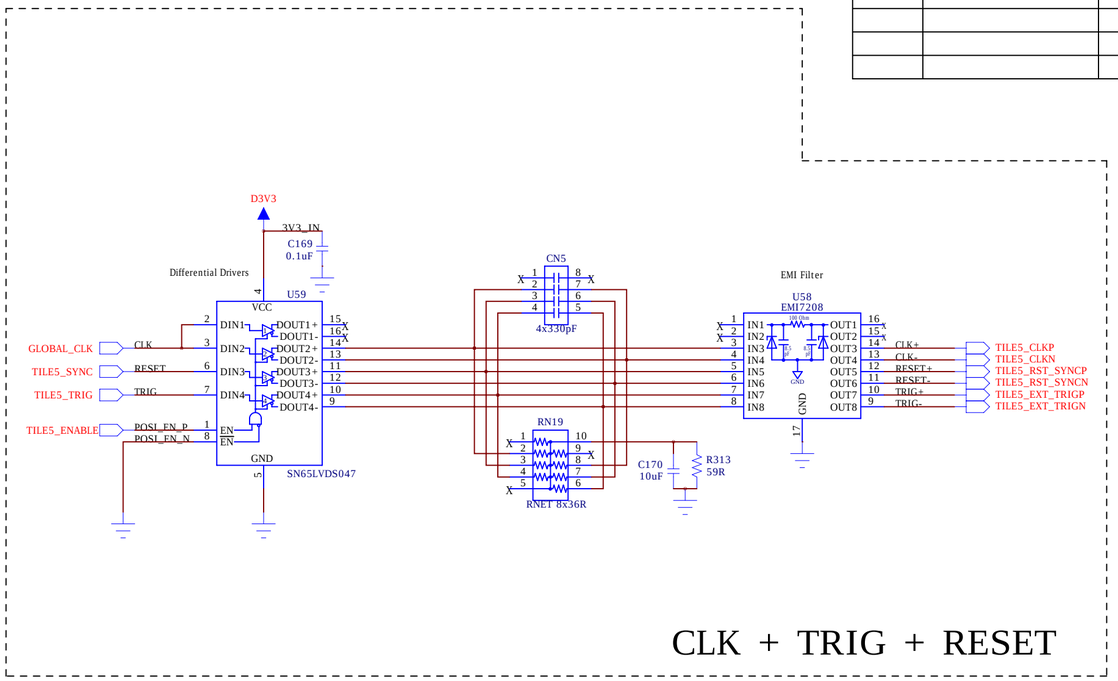
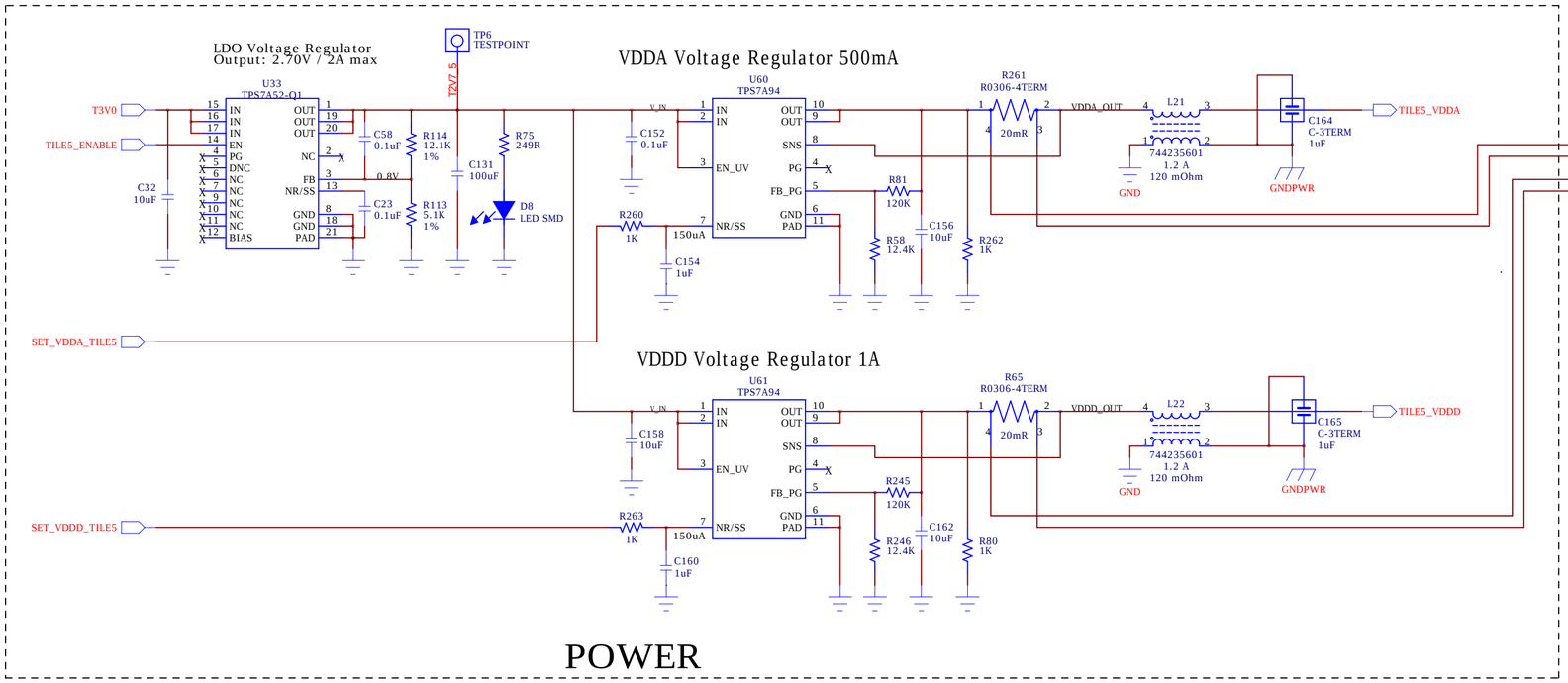


CLK + TRIG + RESET



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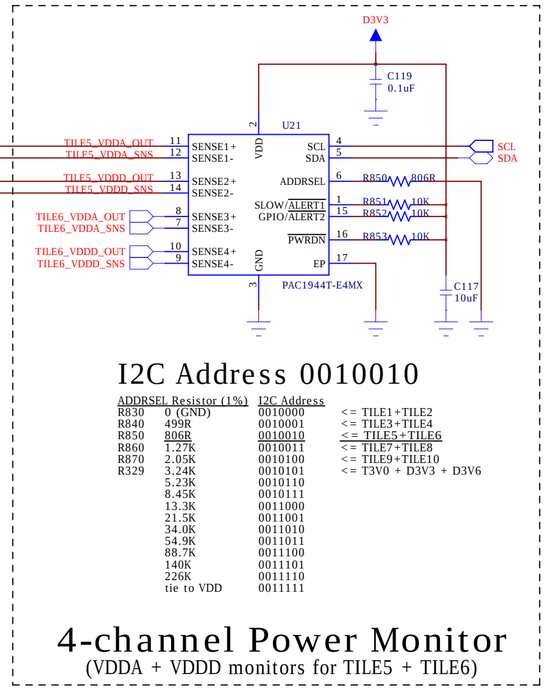


I2C Address 0010010

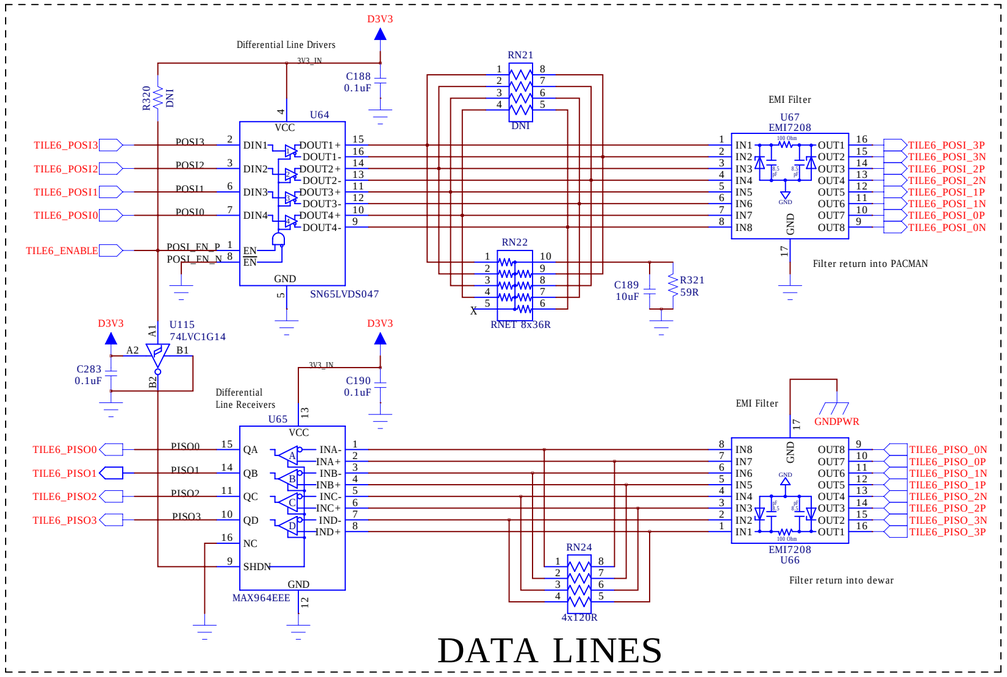
ADDRSEL Resistor (1%)		I2C Address	
R830	0 (GND)	0010000	<= TILE1+TILE2
R840	499R	0010001	<= TILE3+TILE4
R850	806R	0010010	<= TILE5+TILE6
R860	1.27K	0010011	<= TILE7+TILE8
R870	2.05K	0010100	<= TILE9+TILE10
R329	3.24K	0010101	<= T3V0 + D3V3 + D3V6
	5.23K	0010110	
	8.45K	0010111	
	13.3K	0011000	
	21.5K	0011001	
	34.0K	0011010	
	54.9K	0011011	
	88.7K	0011100	
	140K	0011101	
	226K	0011110	
	tie to VDD	0011111	

4-channel Power Monitor
(VDDA + VDDD monitors for TILE5 + TILE6)

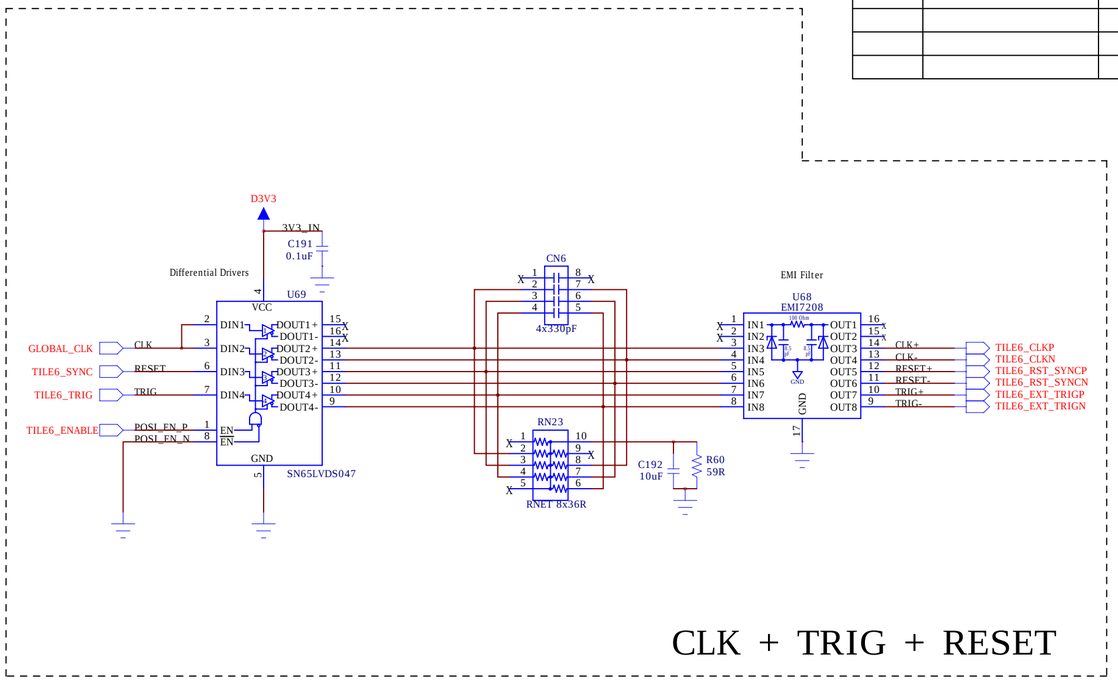
TILE5

DRAWN: H.G.Berns	DATED: 05/15/2024	COMPANY: University of California Davis	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: LarPix PACMAN Version 5	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: C
RELEASED: H.G.Berns	DATED: 05/15/2024	DRAWING NO: PacMan_V5.sch	REV: 5
		SCALE: <Scale>	SHEET: 9 OF 16

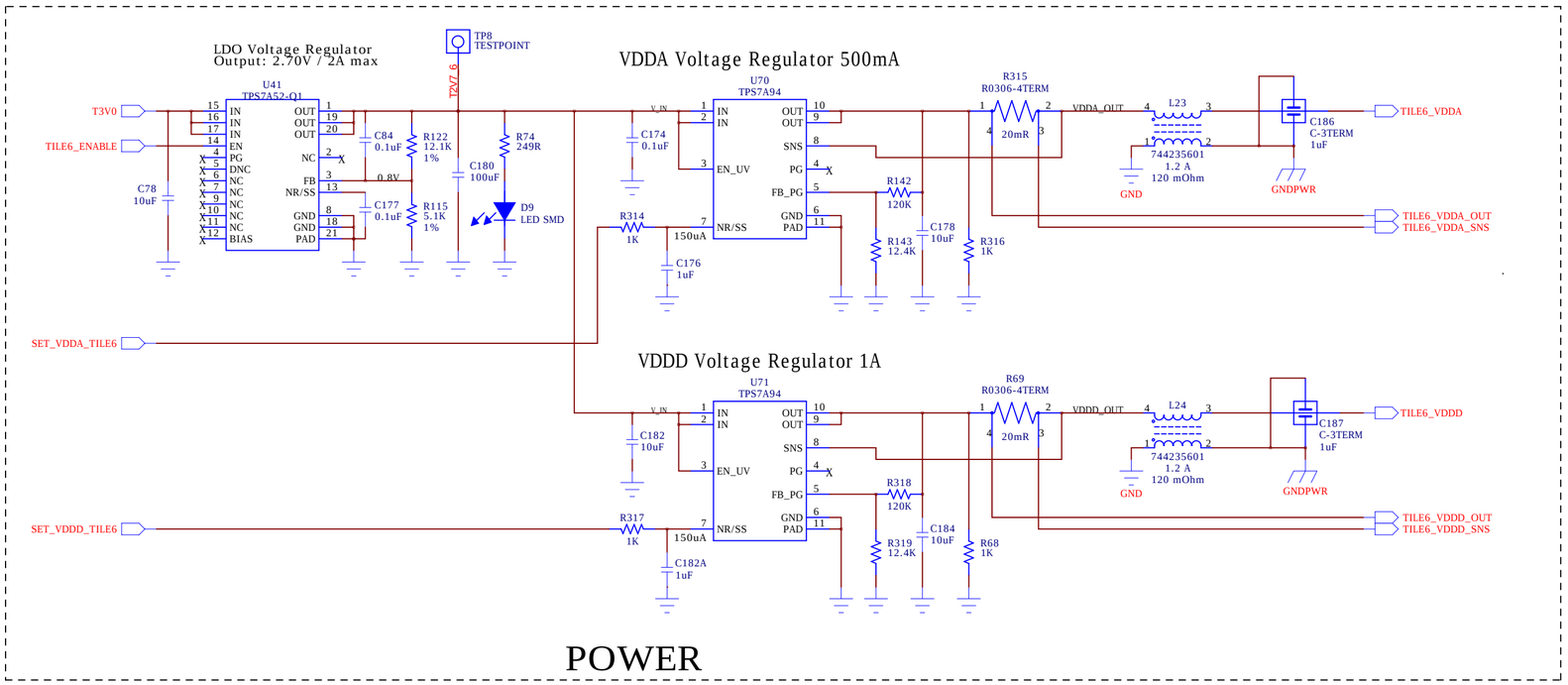
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



DATA LINES



CLK + TRIG + RESET

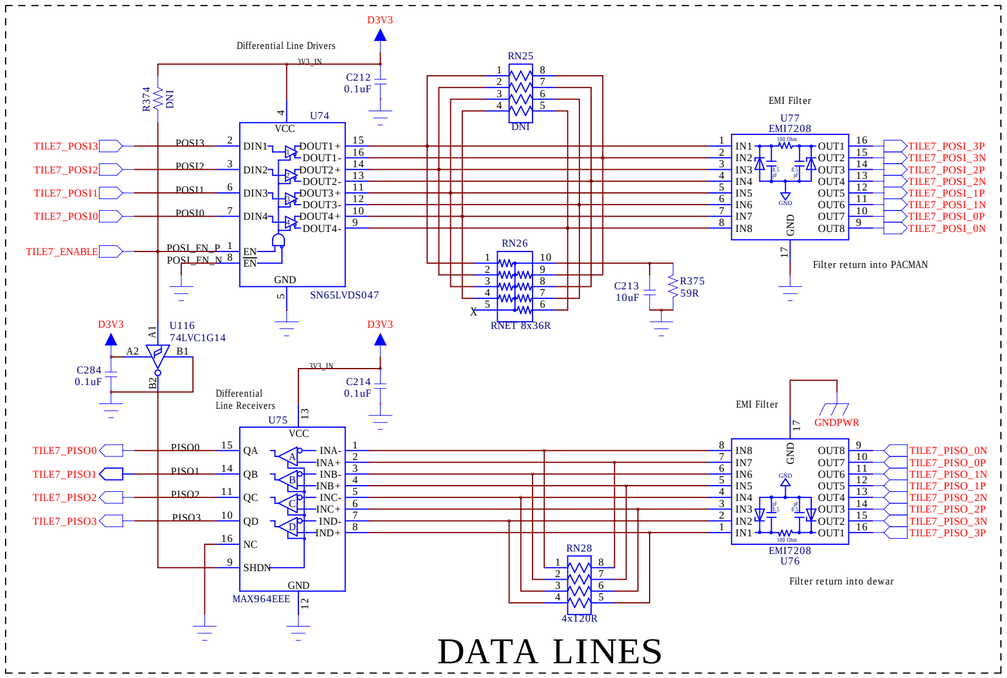


POWER

TILE6

COMPANY: University of California Davis			
TITLE: LarPix PACMAN Version 5			
DRAWN: H.G.Berns	DATED: 05/15/2024	CODE: <Code>	SIZE: C
CHECKED: <Checked By>	DATED: <Checked Date>	DRAWING NO: PacMan_V5.sch	REV: 5
QUALITY CONTROL: <QC By>	DATED: <QC Date>		
RELEASED: H.G.Berns	DATED: 05/15/2024	SCALE: <Scale>	SHEET: 10 of 16

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



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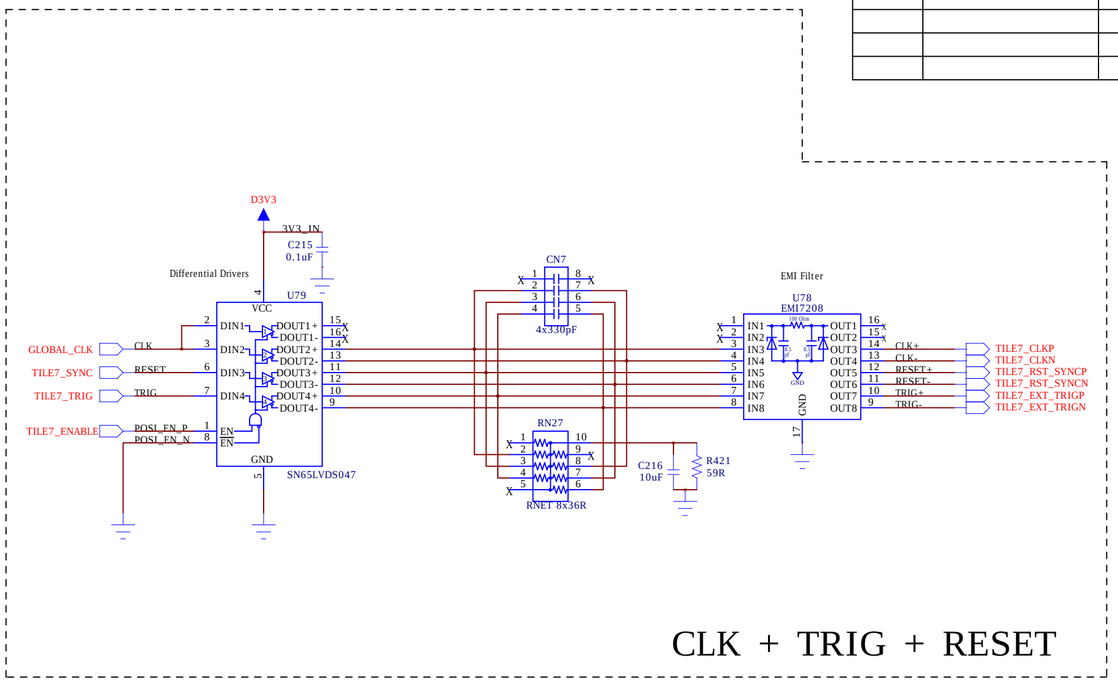
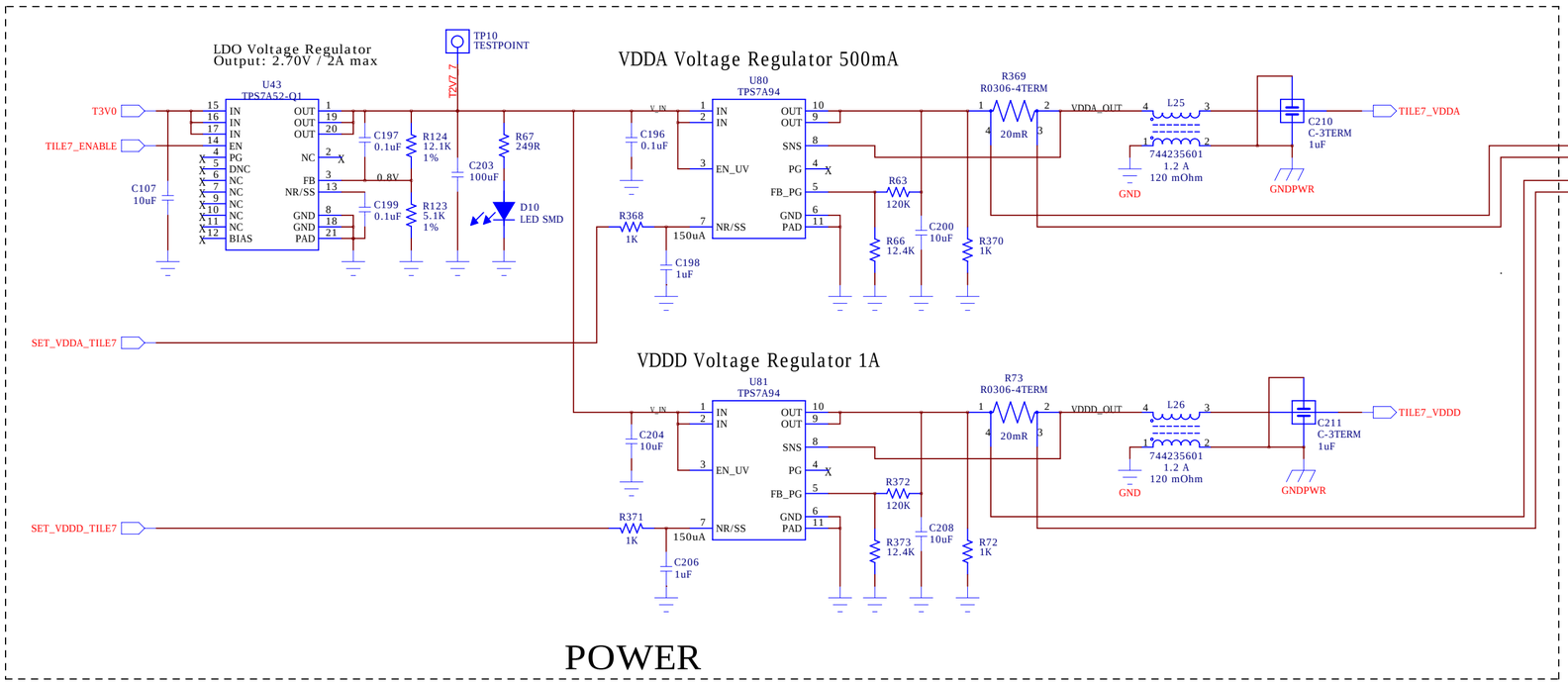
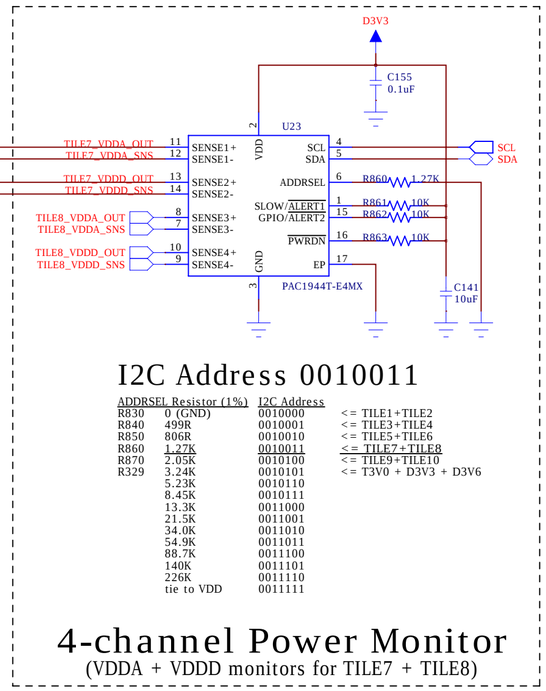


CLK + TRIG + RESET



POWER



I2C Address 0010011

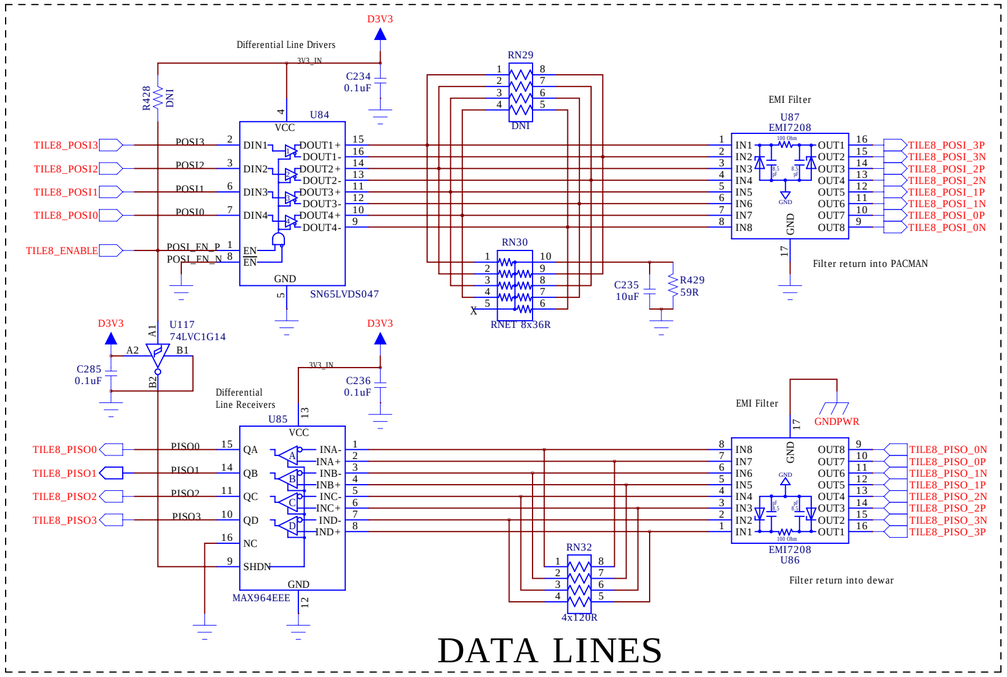
ADDRSEL Resistor (1%)		I2C Address	
R830	0 (GND)	0010000	<= TILE1+TILE2
R840	499R	0010001	<= TILE3+TILE4
R850	806R	0010010	<= TILE5+TILE6
R860	1.27K	0010011	<= TILE7+TILE8
R870	2.05K	0010100	<= TILE9+TILE10
R329	3.24K	0010101	<= T3V0 + D3V3 + D3V6
	5.23K	0010110	
	8.45K	0010111	
	13.3K	0011000	
	21.5K	0011001	
	34.0K	0011010	
	54.9K	0011011	
	88.7K	0011100	
	140K	0011101	
	226K	0011110	
	tie to VDD	0011111	

4-channel Power Monitor
(VDDA + VDDD monitors for TILE7 + TILE8)

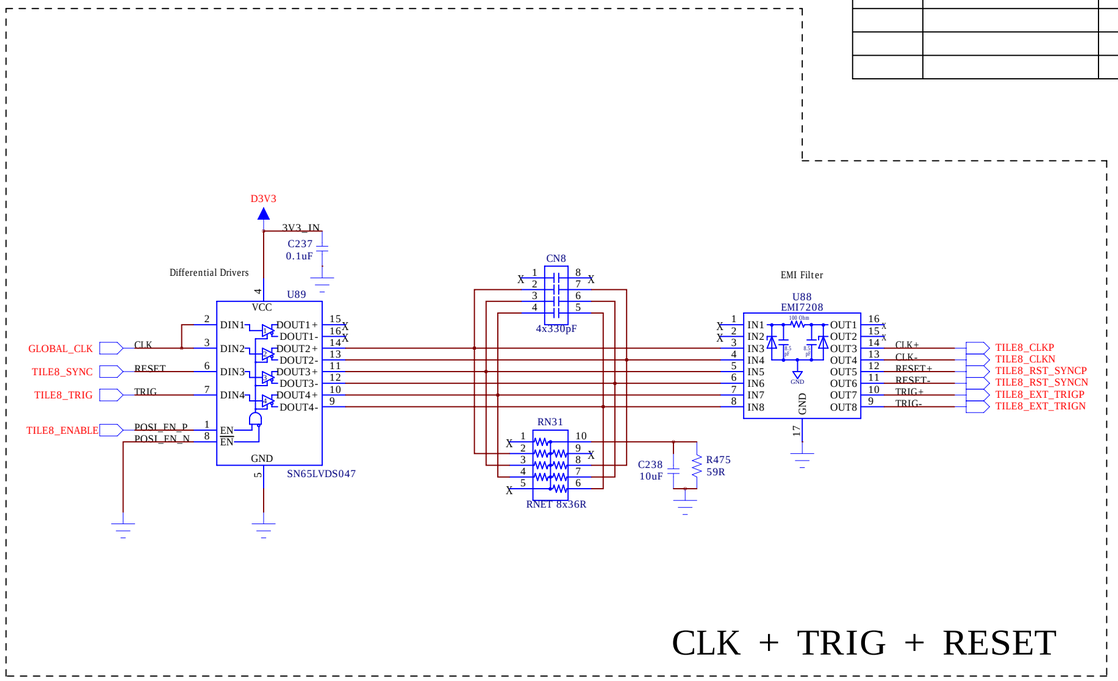
TILE7

DRAWN: H.G.Berns	DATED: 05/15/2024	COMPANY: University of California Davis	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: LarPix PACMAN Version 5	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: C
RELEASED: H.G.Berns	DATED: 05/15/2024	DRAWING NO: PacMan_V5.sch	REV: 5
		SCALE: <Scale>	SHEET: 1 of 16

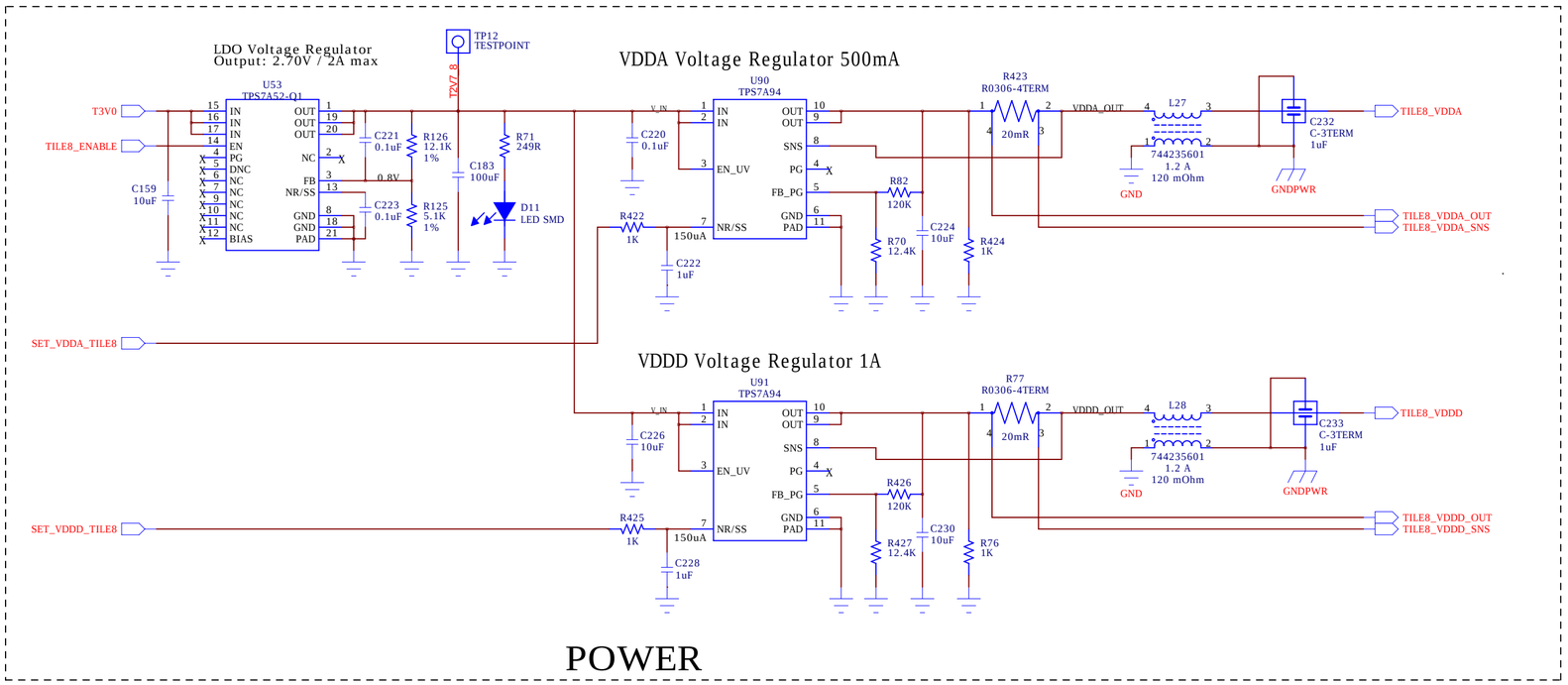
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



DATA LINES



CLK + TRIG + RESET

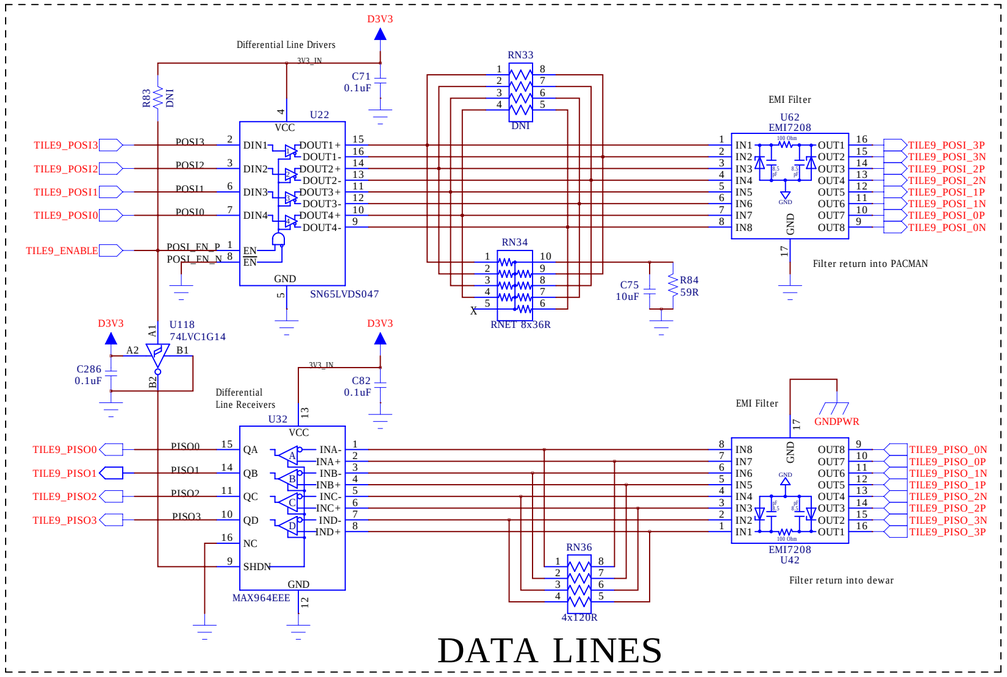


POWER

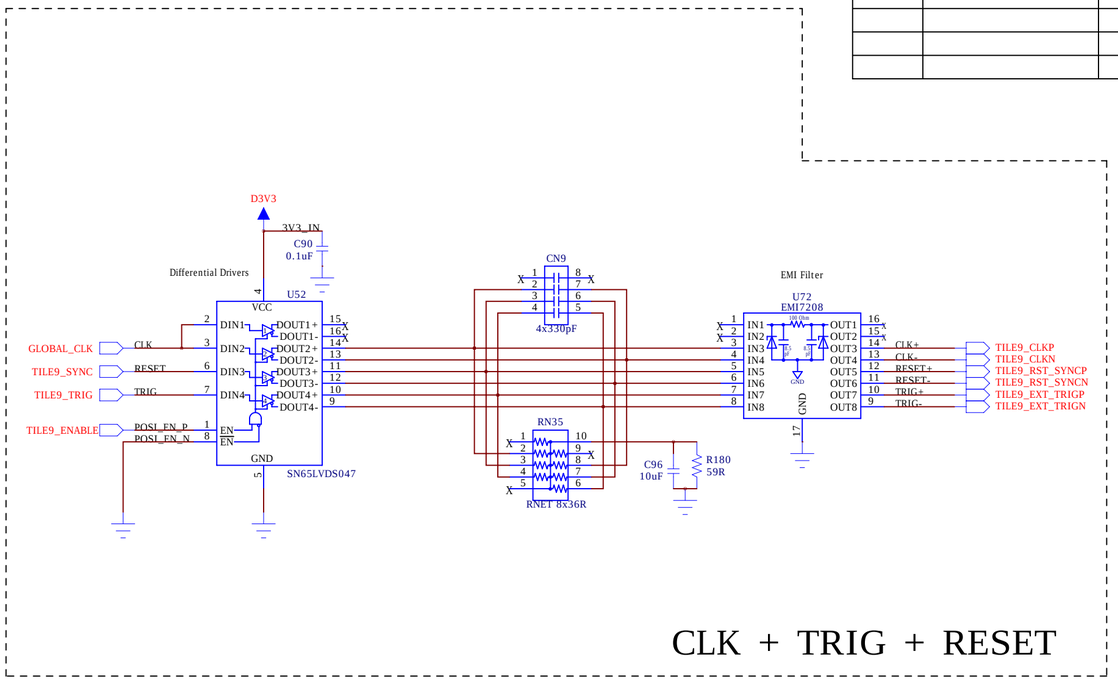
TILE8

DRAWN: H.G.Berns	DATED: 05/15/2024	COMPANY: University of California Davis	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: LarPix PACMAN Version 5	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: C
RELEASED: H.G.Berns	DATED: 05/15/2024	DRAWING NO: PacMan_V5.sch	REV: 5
		SCALE: <Scale>	SHEET: 2 of 16

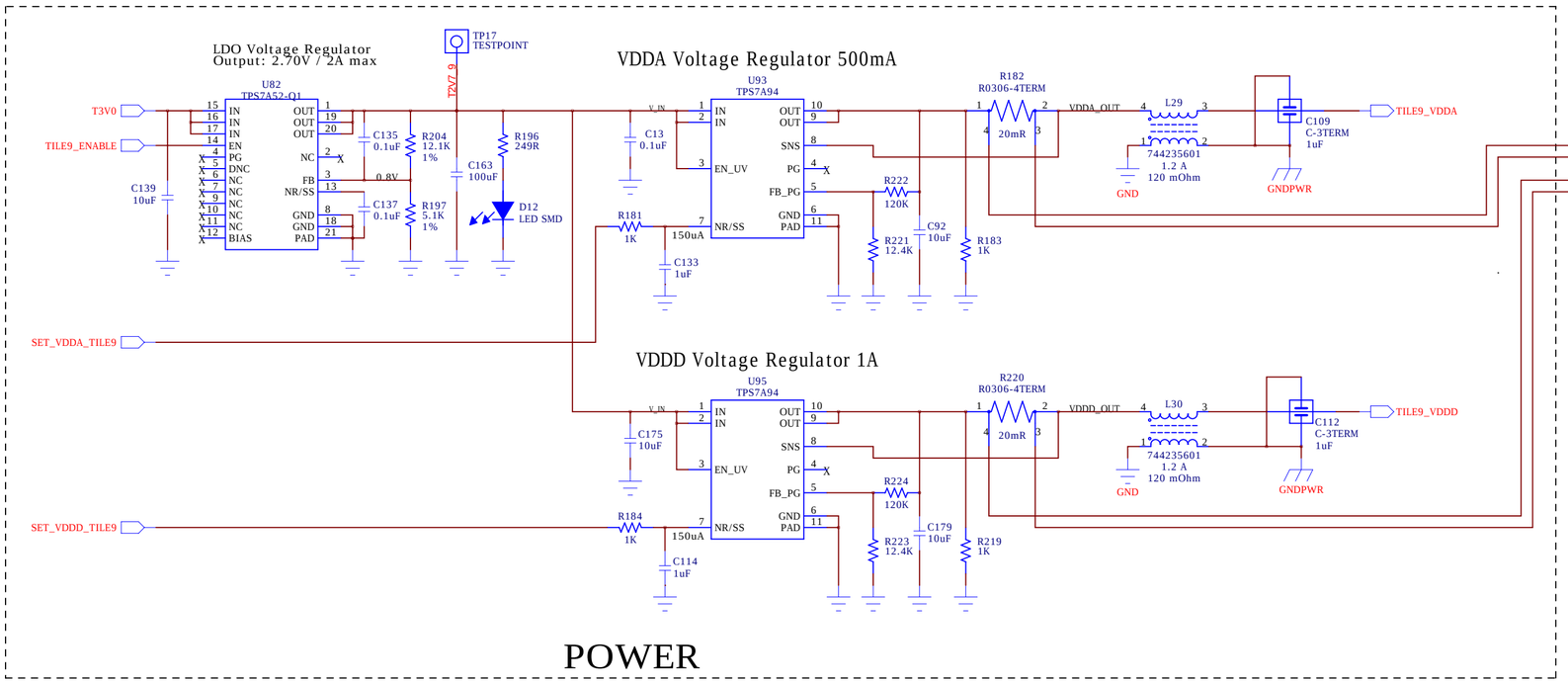
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



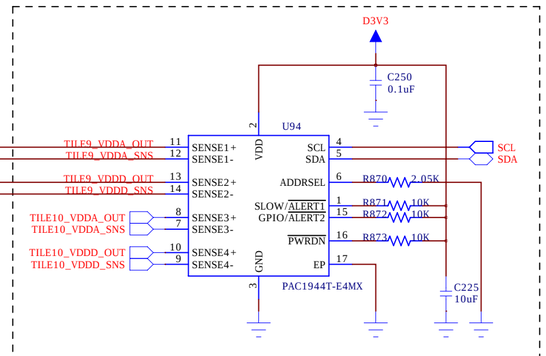
DATA LINES



CLK + TRIG + RESET



POWER



I2C Address 0010100

ADDRSEL Resistor (1%)		I2C Address	
R830	0 (GND)	0010000	<= TILE1+TILE2
R840	499R	0010001	<= TILE3+TILE4
R850	806R	0010010	<= TILE5+TILE6
R860	1.27K	0010011	<= TILE7+TILE8
R870	2.05K	0010100	<= TILE9+TILE10
R329	3.24K	0010101	<= T3V0 + D3V3 + D3V6
	5.23K	0010110	
	8.45K	0010111	
	13.3K	0011000	
	21.5K	0011001	
	34.0K	0011010	
	54.9K	0011011	
	88.7K	0011100	
	140K	0011101	
	226K	0011110	
	tie to VDD	0011111	

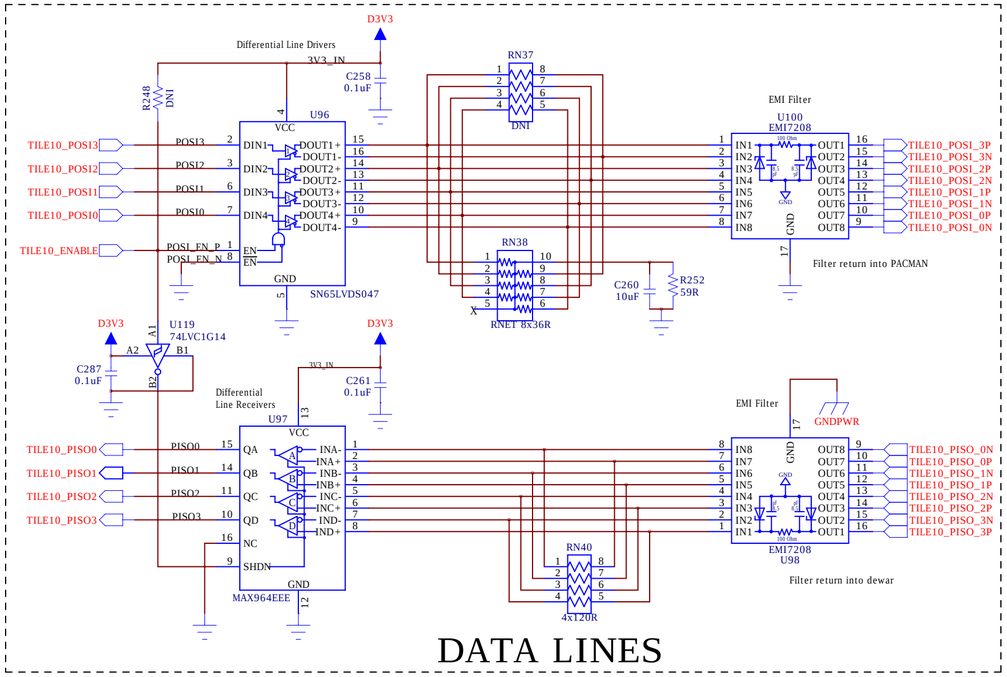
4-channel Power Monitor

(VDDA + VDDD monitors for TILE9 + TILE10)

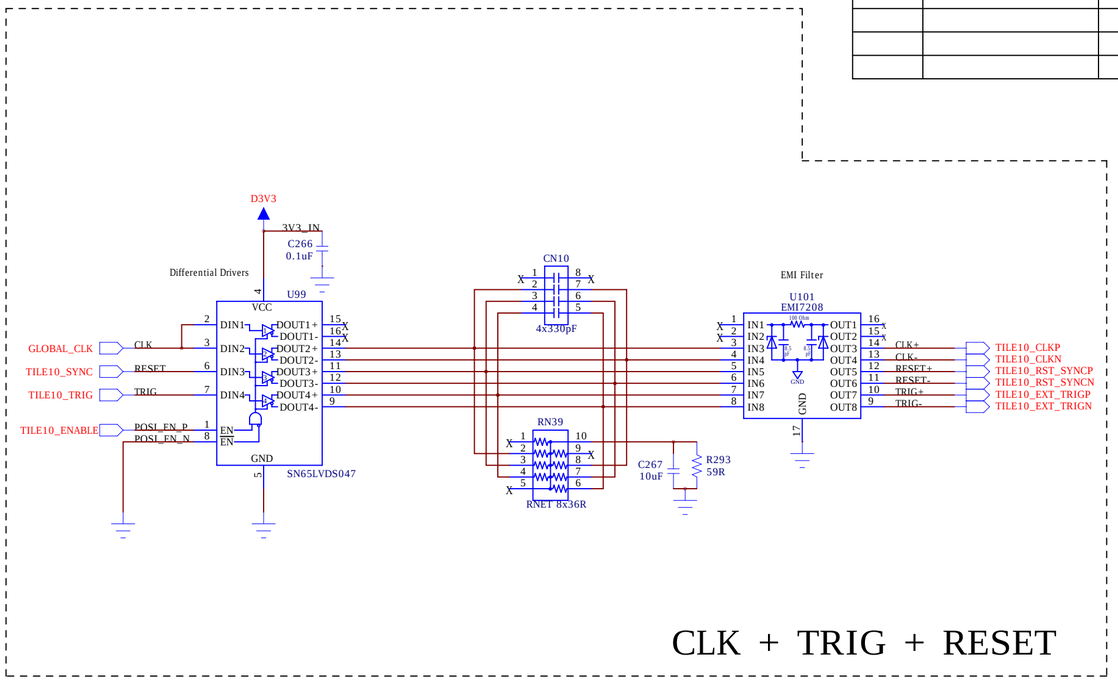
TILE9

DRAWN: H.G.Berns	DATED: 05/15/2024	COMPANY: University of California Davis	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: LarPix PACMAN Version 5	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: C
RELEASED: H.G.Berns	DATED: 05/15/2024	DRAWING NO: PacMan_V5.sch	REV: 5
		SCALE: <Scale>	SHEET: 13 of 16

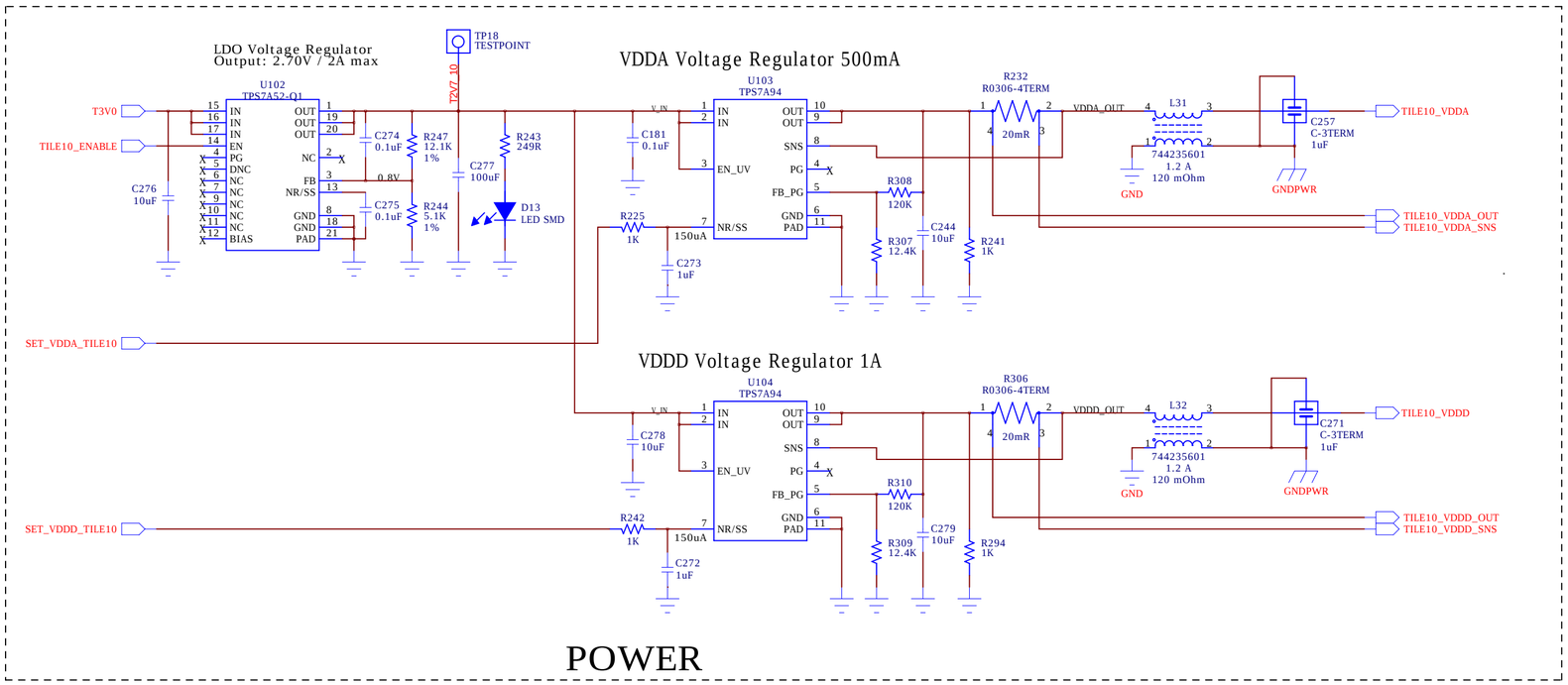
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



DATA LINES



CLK + TRIG + RESET



POWER

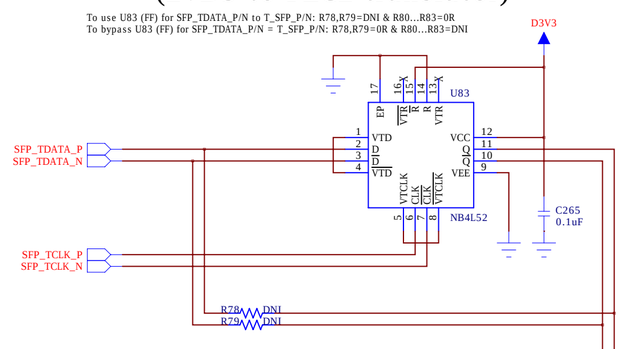
TILE10

DRAWN: H.G.Berns	DATED: 05/15/2024	COMPANY: University of California Davis	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: LarPix PACMAN Version 5	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: C
RELEASED: H.G.Berns	DATED: 05/15/2024	DRAWING NO: PacMan_V5.sch	REV: 5
		SCALE: <Scale>	SHEET: 4 OF 16

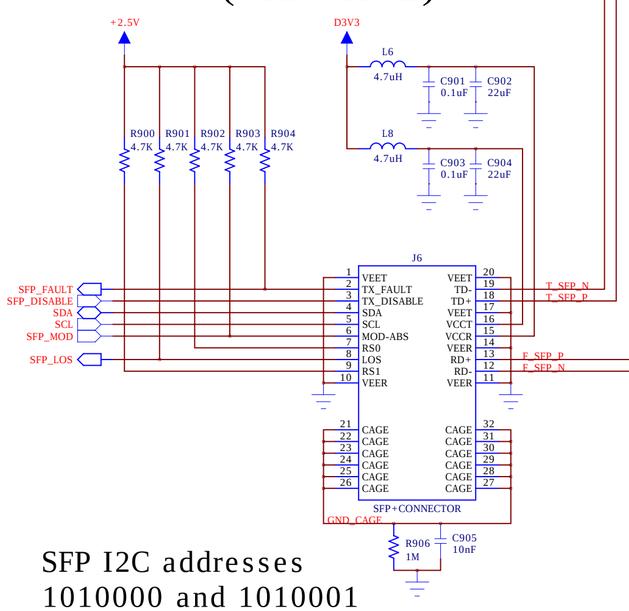
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

SFP TX Data/Clock Flip-Flop
(LVDS to PECL translator)

To use U83 (FF) for SFP_TDATA_P/N to T_SFP_P/N: R78,R79=DNI & R80...R83=0R
To bypass U83 (FF) for SFP_TDATA_P/N = T_SFP_P/N: R78,R79=0R & R80...R83=DNI

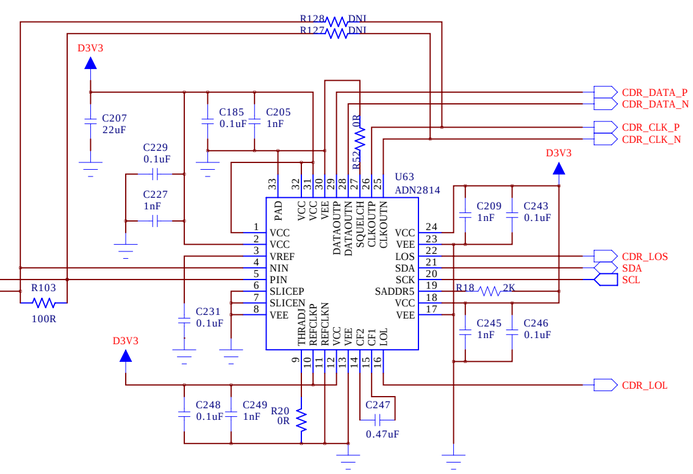


Optical Fiber Transceiver (SFP CAGE)



SFP I2C addresses
1010000 and 1010001

Clock & Data Recovery (CDR)

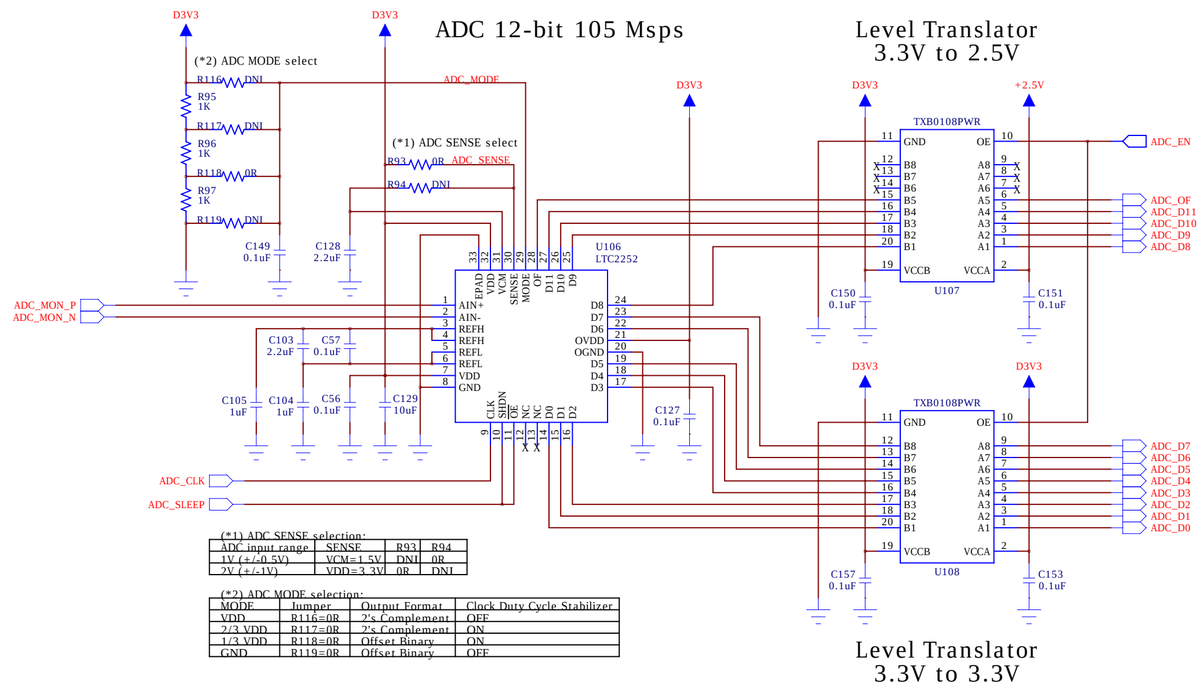


CDR I2C Address 1100000

TIMING

DRAWN: H.G.Berns	DATED: 05/15/2024	COMPANY: University of California Davis	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: LarPix PACMAN Version 5	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: C
RELEASED: H.G.Berns	DATED: 05/15/2024	DRAWING NO: PacMan_V5.sch	REV: 5
		SCALE: <Scale>	SHEET: 16 of 16

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



(*1) ADC SENSE selection:

ADC input range	SENSE	R93	R94
1V (+/-0.5V)	VCM=1.5V	DNI	0R
2V (+/-1V)	VDD=3.3V	0R	DNI

(*2) ADC MODE selection:

MODE	Jumper	Output Format	Clock Duty Cycle Stabilizer
VDD	R116=0R	2's Complement	OFF
2/3 VDD	R117=0R	2's Complement	ON
1/3 VDD	R118=0R	Offset Binary	ON
GND	R119=0R	Offset Binary	OFF

ADC

DRAWN: H.G.Berns	DATED: 05/15/2024
CHECKED: <Checked By>	DATED: <Checked Date>
QUALITY CONTROL: <QC By>	DATED: <QC Date>
RELEASED: H.G.Berns	DATED: 05/15/2024

COMPANY: University of California Davis

TITLE: LarPix PACMAN Version 5

CODE:	SIZE:	DRAWING NO:	REV:
<Code>	C	PacMan_V5.sch	5

SCALE: <Scale> SHEET: 16 of 16