COL215 Digital Logic and System Design

Sequential Circuits :

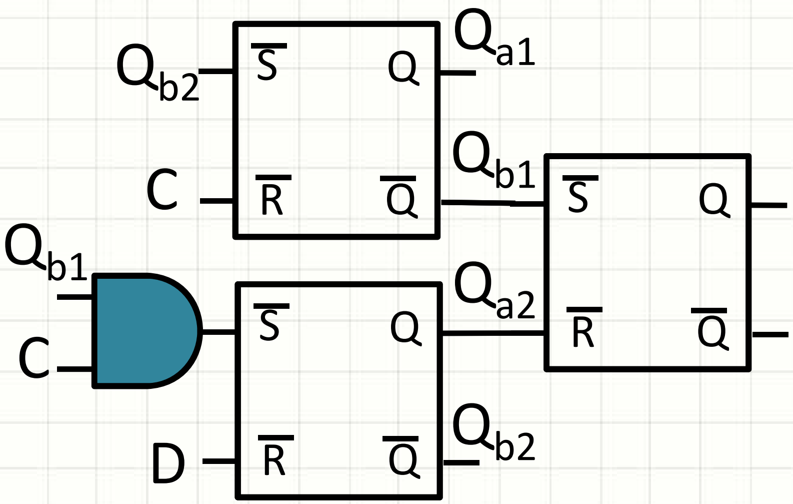
Registers and Register File

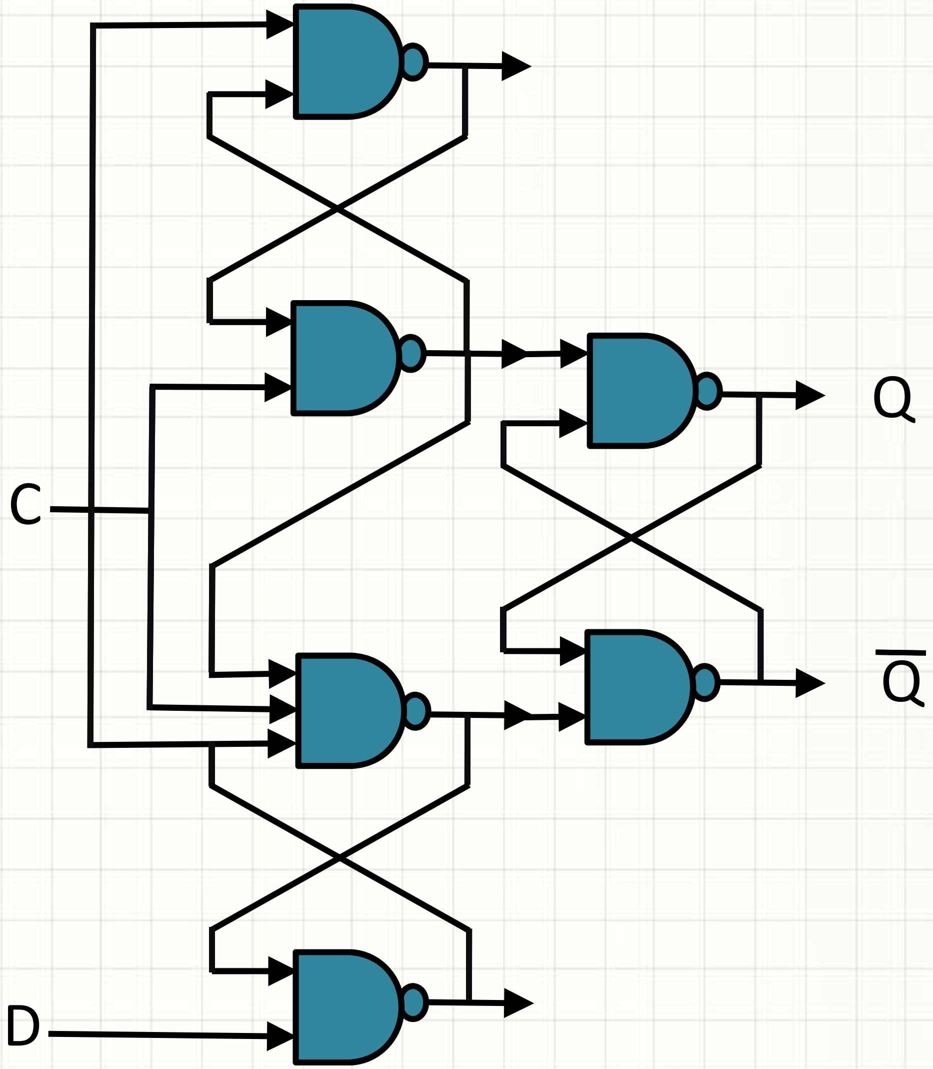
08 August 2017

Lecture Outline

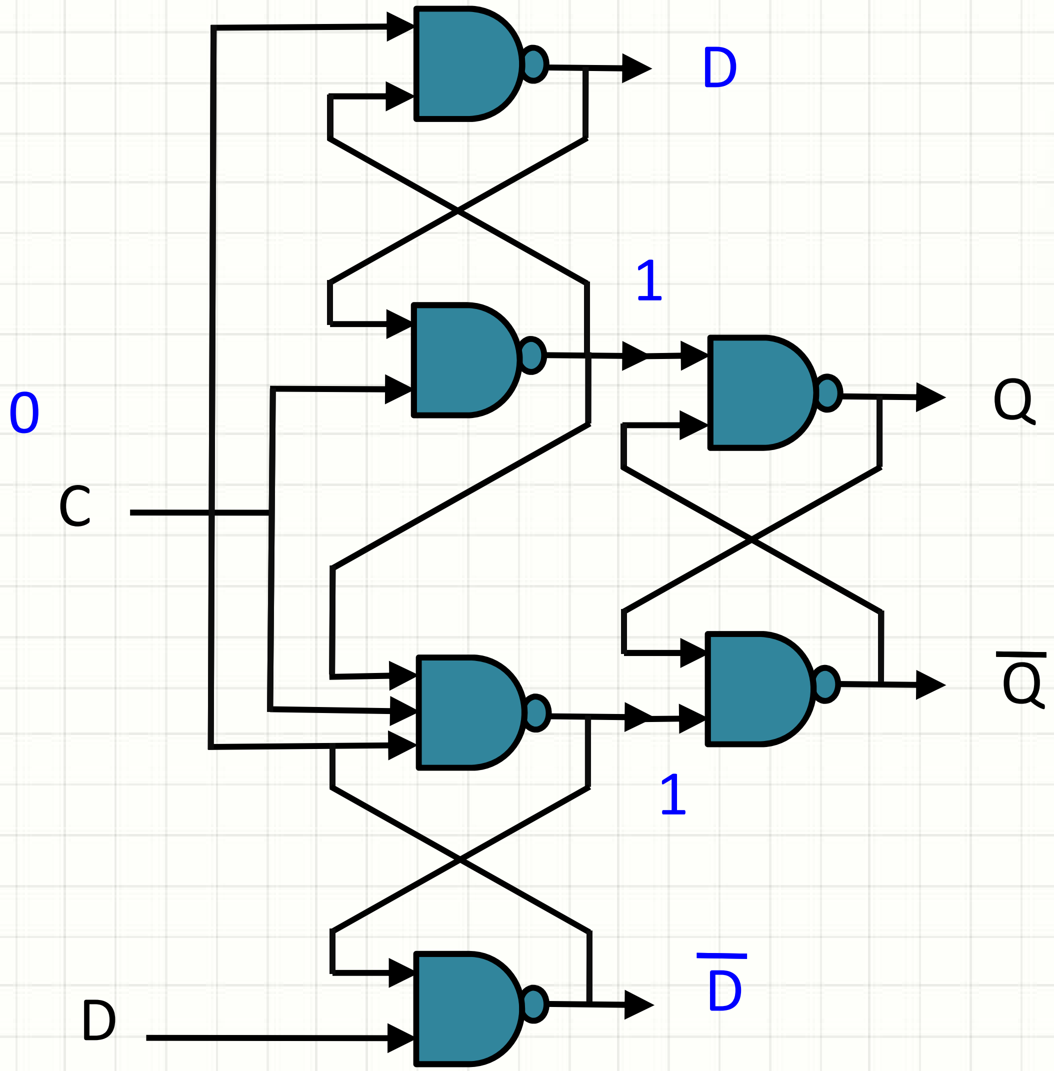
- Flip-flops
  - Initializing contents
  - Different types of flip-flops
- Registers
  - Serial
  - Parallel
- Register File
  - Addressing
- Lab Exercise 3

Edge triggered D Flip-Flop

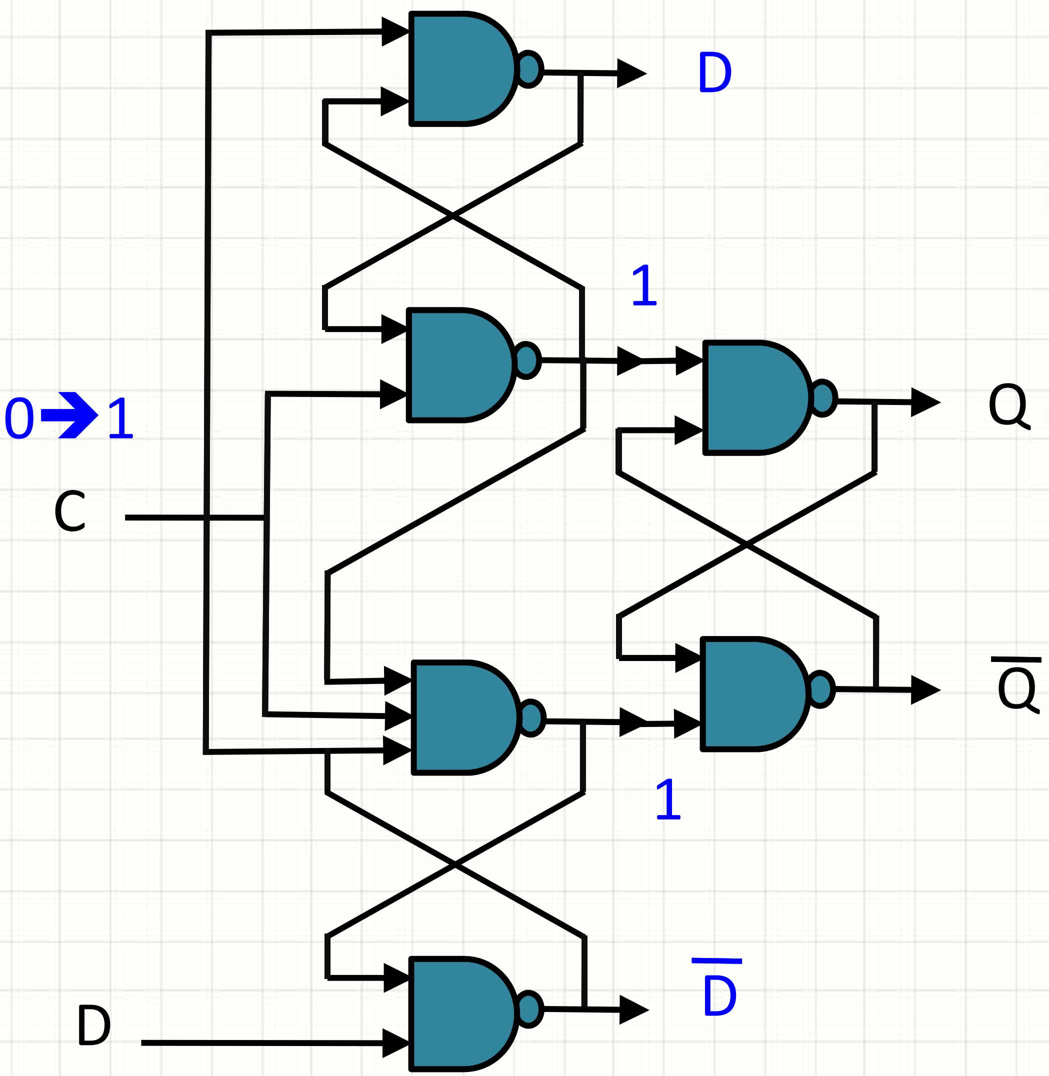




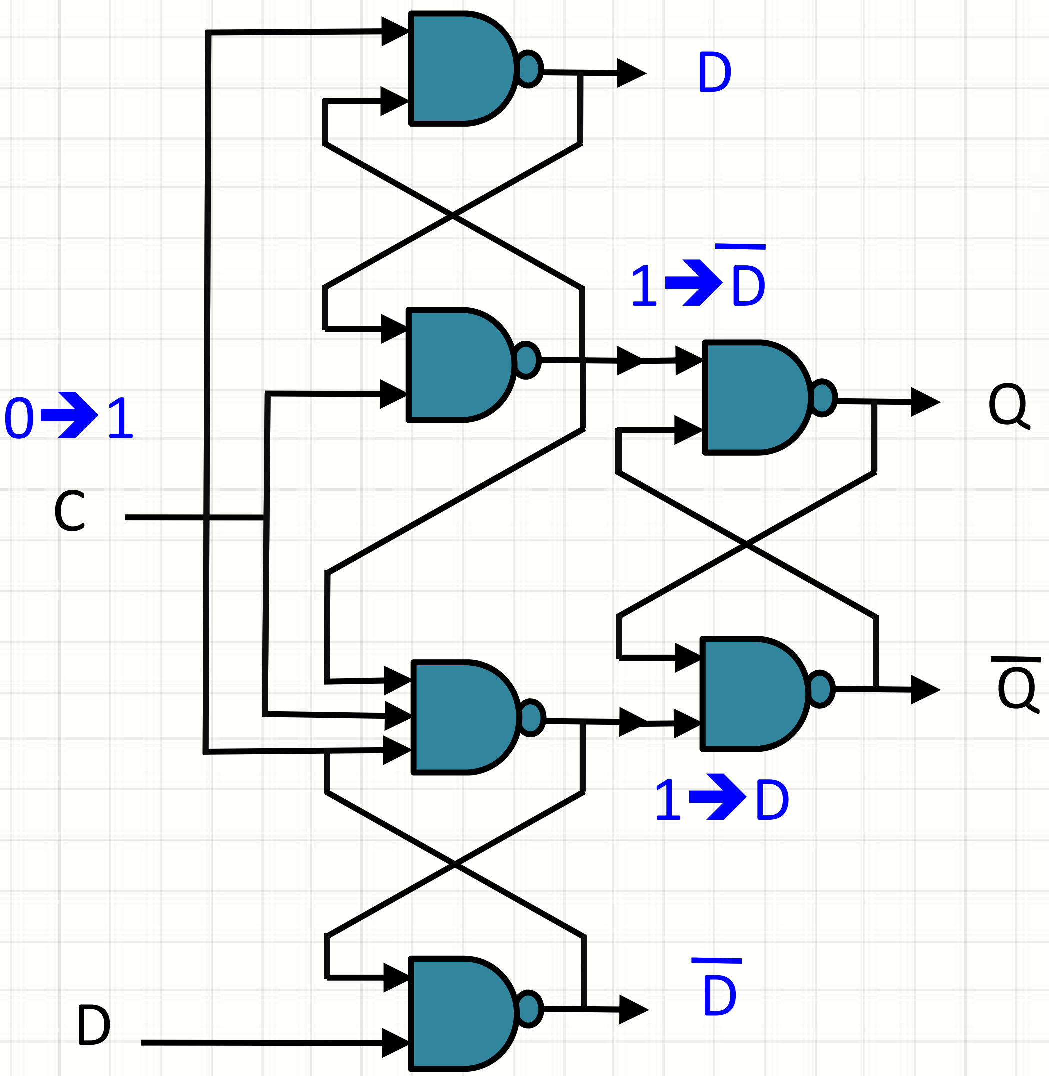
Edge triggered D Flip-Flop



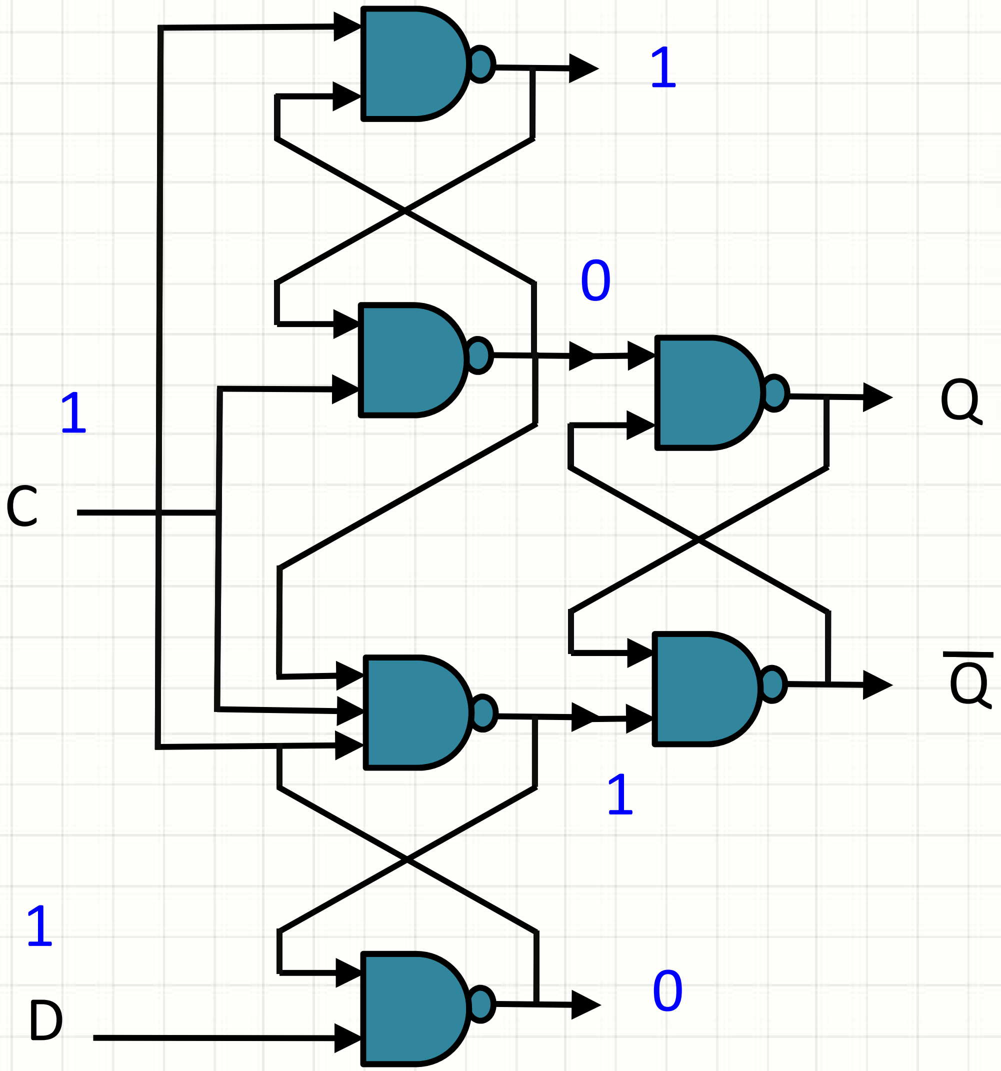
Edge triggered D Flip-Flop



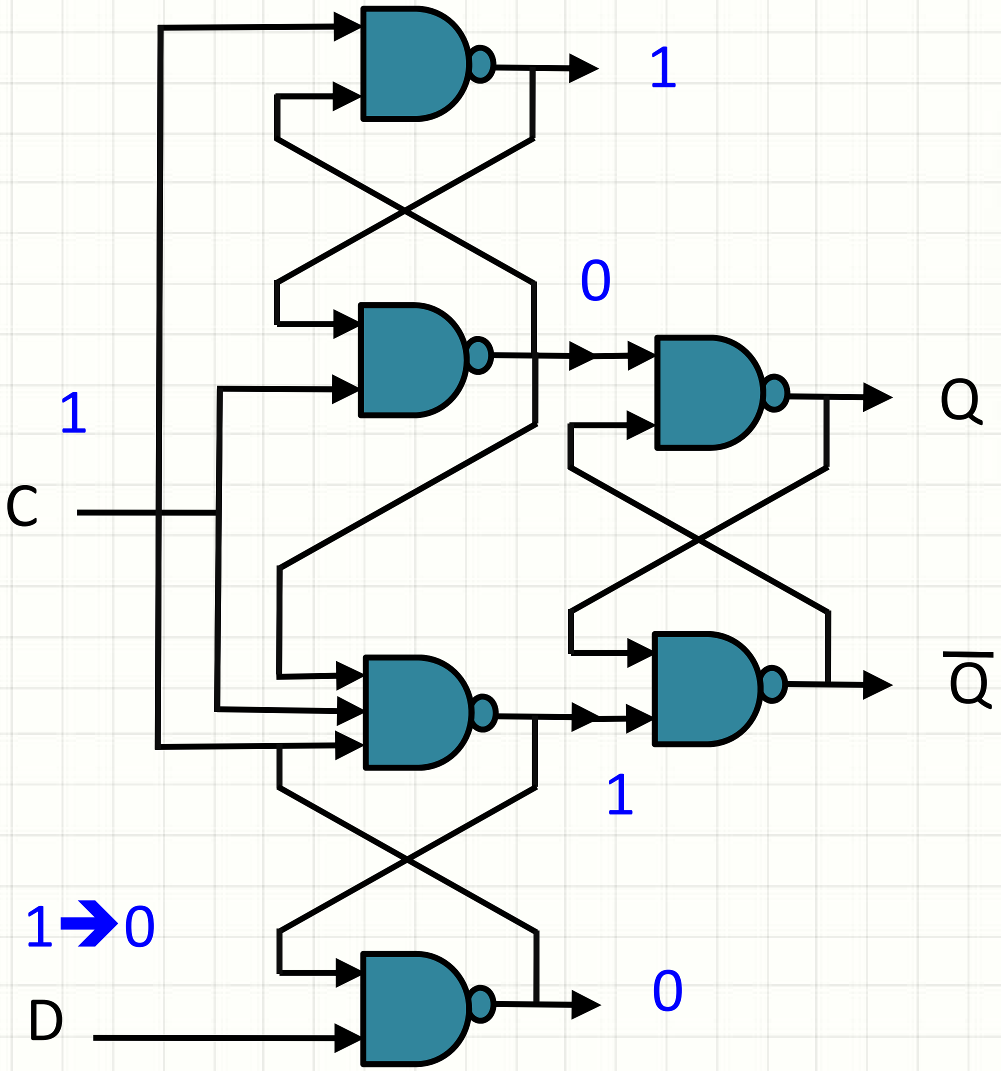
Edge triggered D Flip-Flop



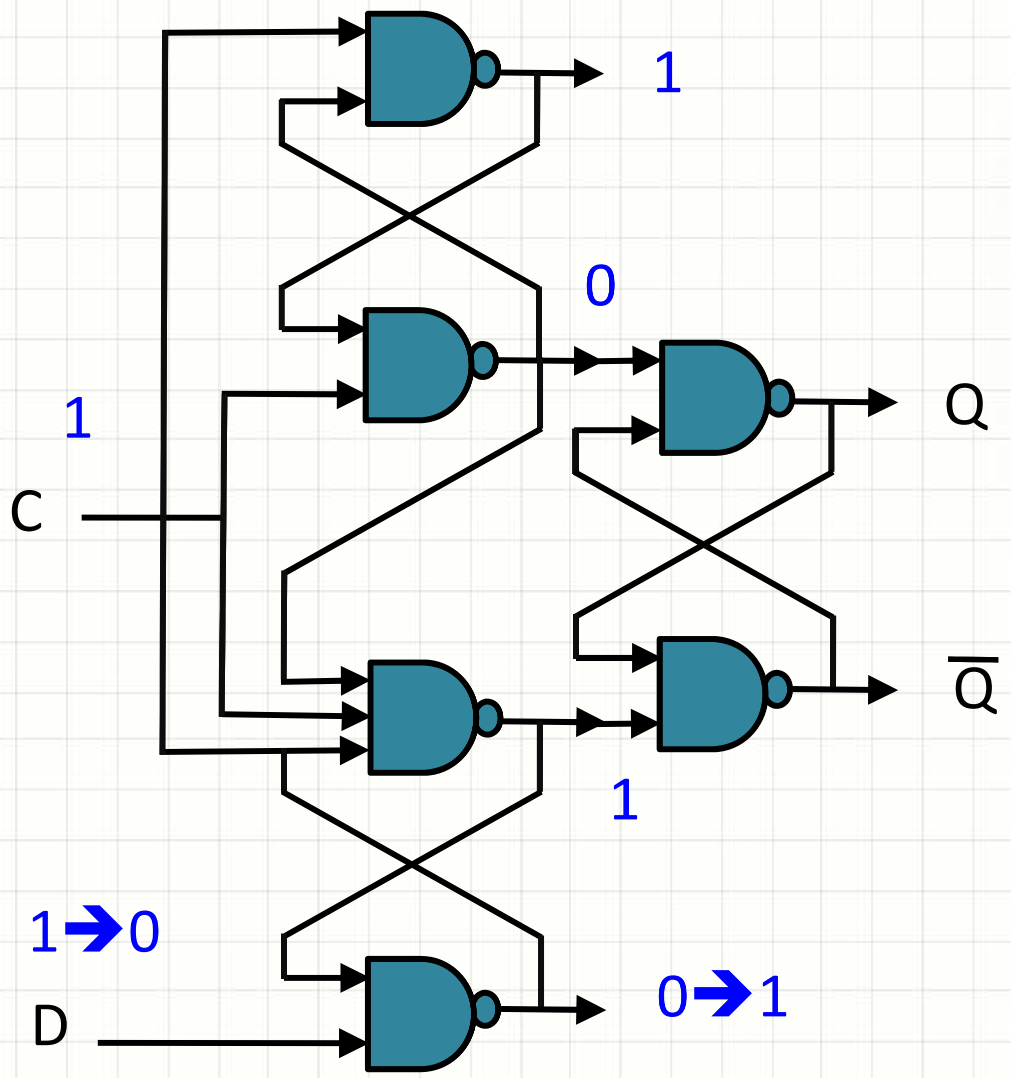
Edge triggered D Flip-Flop



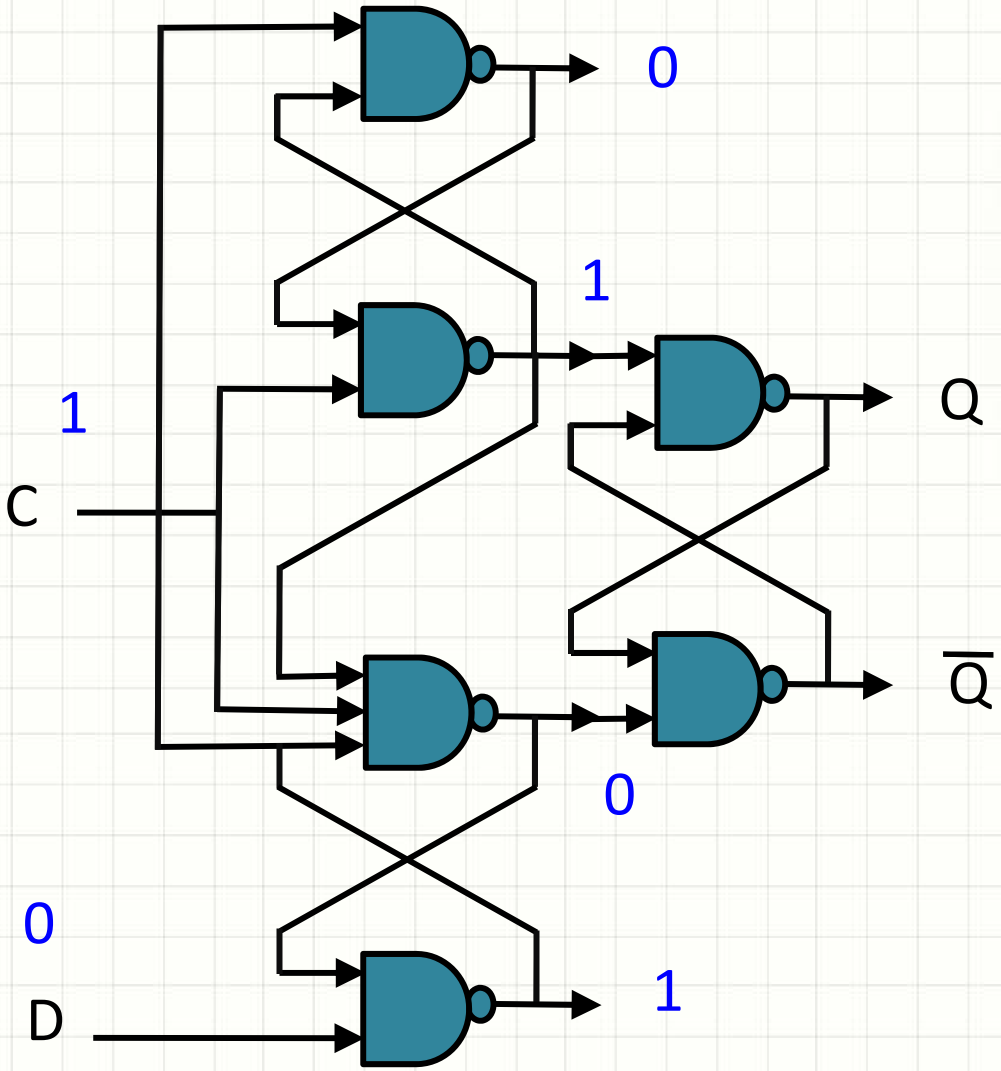
Edge triggered D Flip-Flop



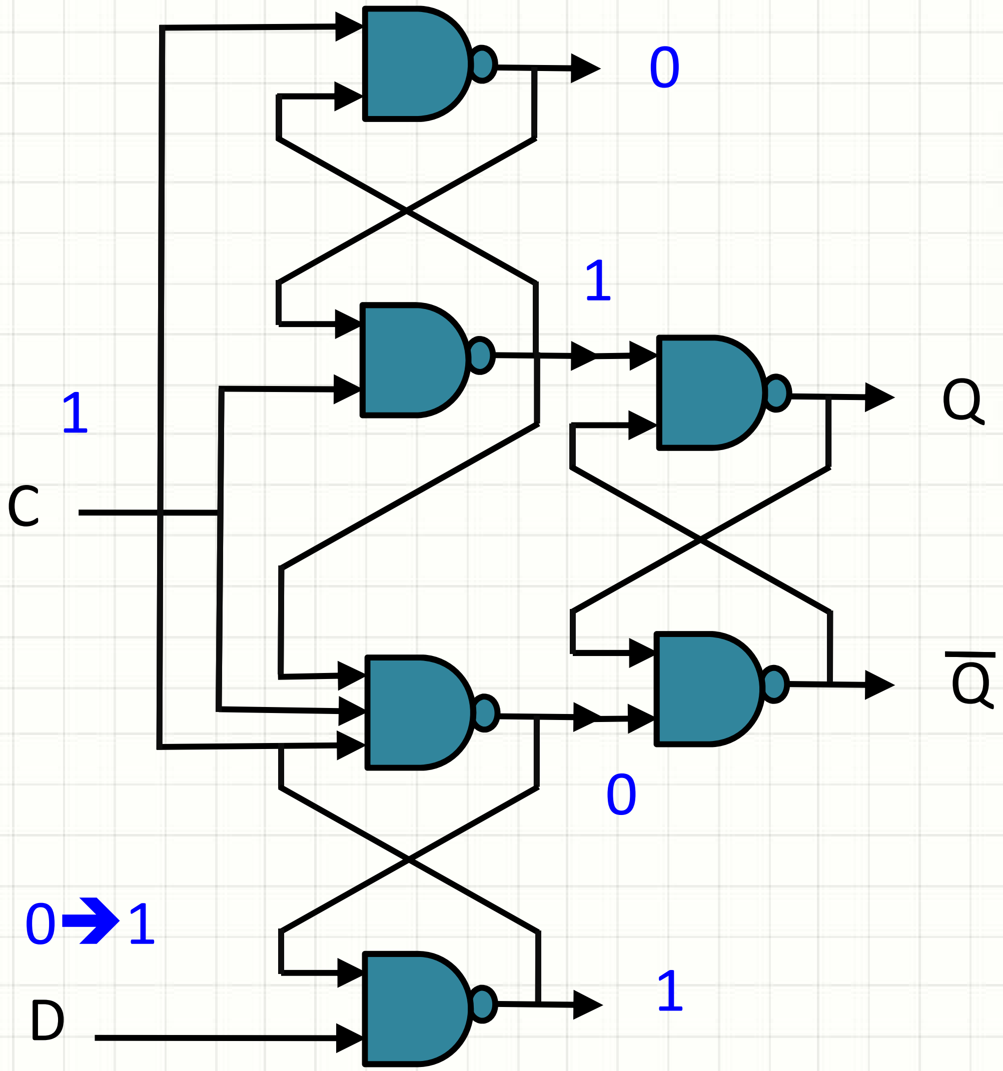
Edge triggered D Flip-Flop



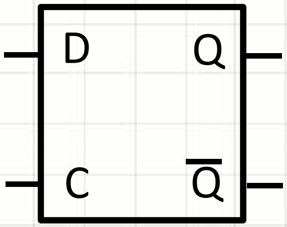
Edge triggered D Flip-Flop



Edge triggered D Flip-Flop

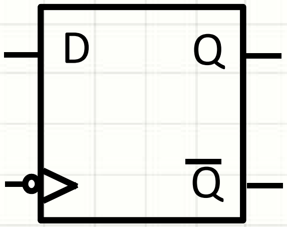


D Latch and Flip-Flops



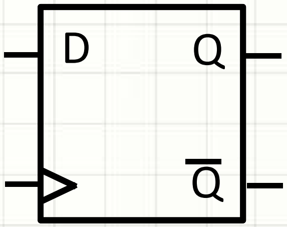
Level
triggered

Level
sensitive



Negative edge
triggered

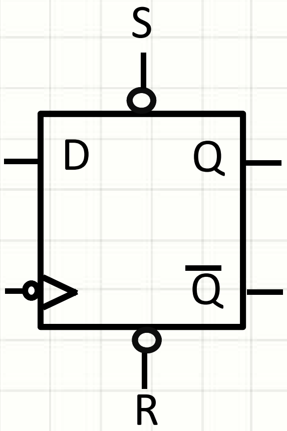
Negative edge
sensitive

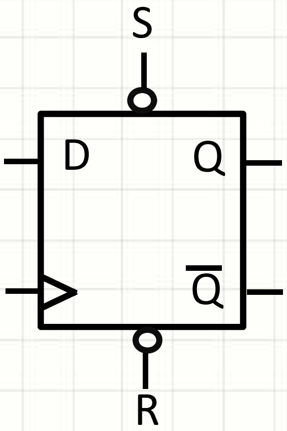


Positive edge
triggered

Positive edge
sensitive

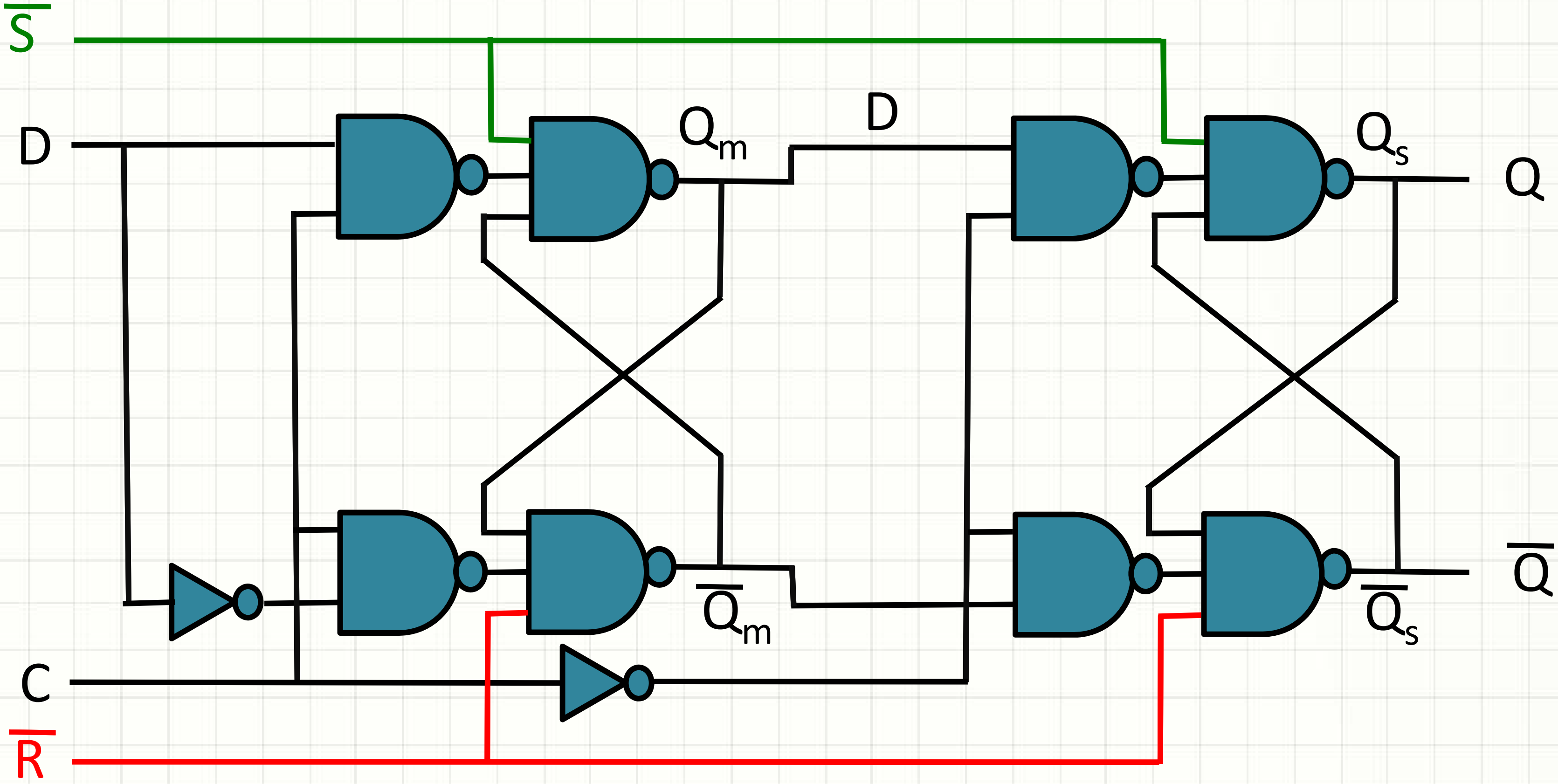
D Flip-Flops with Set and Reset



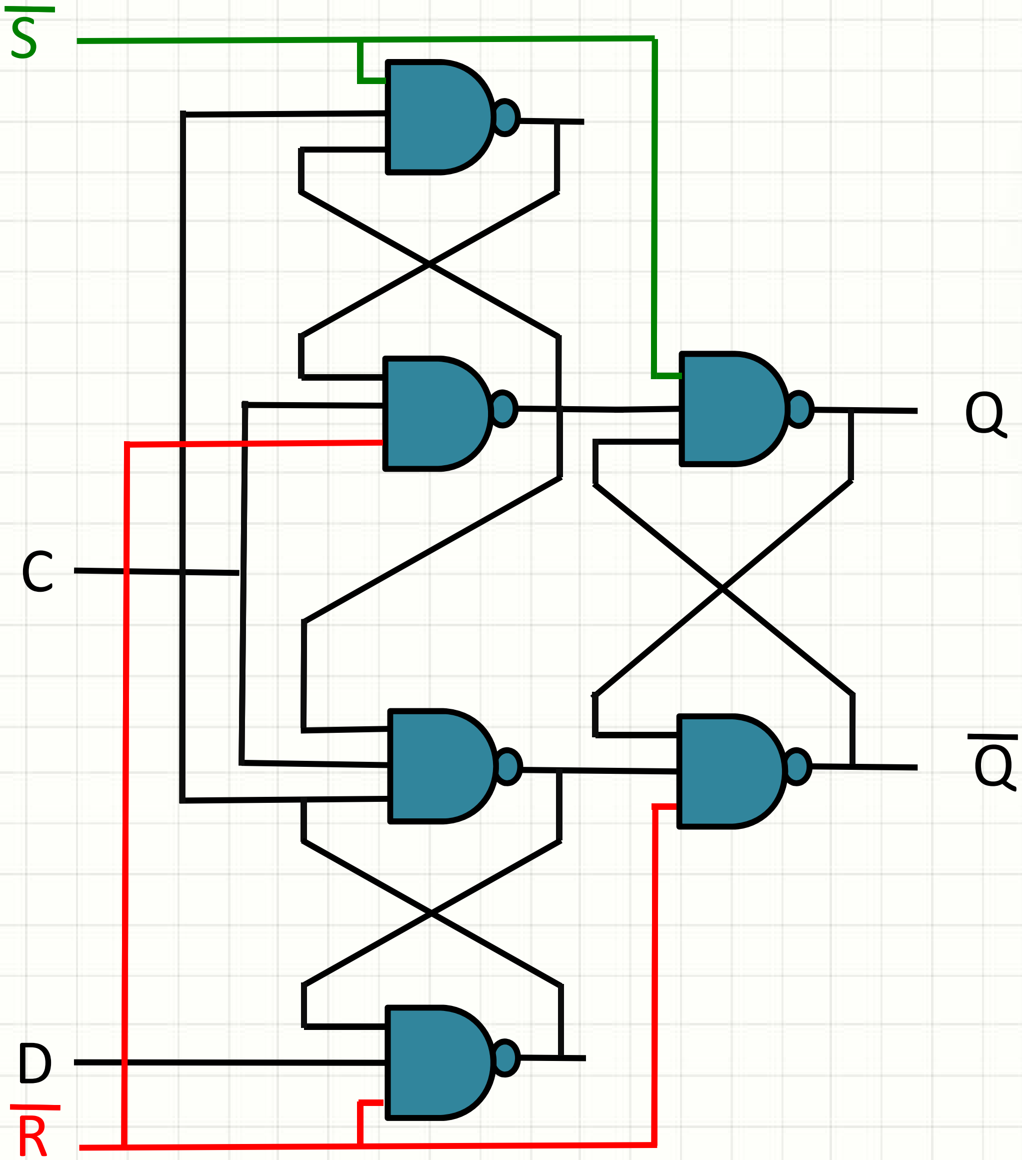


“Set” and “Reset” are also called “Preset” and “Clear”

Master-Slave D Flip-Flop with S, R



Edge triggered D Flip-Flop with S, R

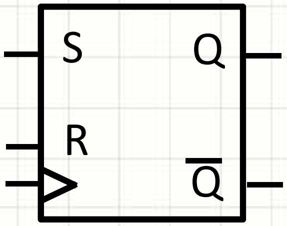


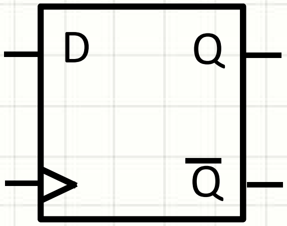
Set/Reset :
synchronous or asynchronous

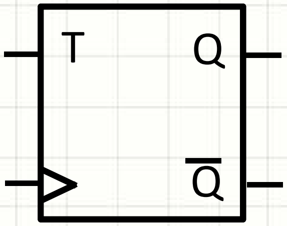
- Asynchronous : not timed with clock
- Synchronous : timed with clock

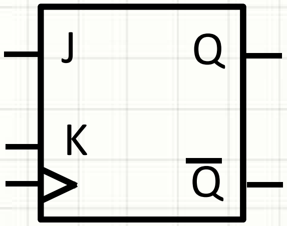
Set / Reset operation	D input of flip-flop
Set operation only	$S + D$
Reset operation only	$D \, . \, \overline{R}$
Set & Rest, Set overrides	$S + (D \, . \, \overline{R})$
Set & Reset, Reset overrides	$(S + D) \, . \, \overline{R}$

Different types of Flip-Flops









S	R	Q(t+1)
0	0	Q (t)
0	1	0
1	0	1
1	1	XXX

D	Q(t+1)
0	0
1	1

T	Q(t+1)
0	Q (t)
1	$\overline{Q}$ (t)

J	K	Q(t+1)
0	0	Q (t)
0	1	0
1	0	1
1	1	$\overline{Q}$ (t)

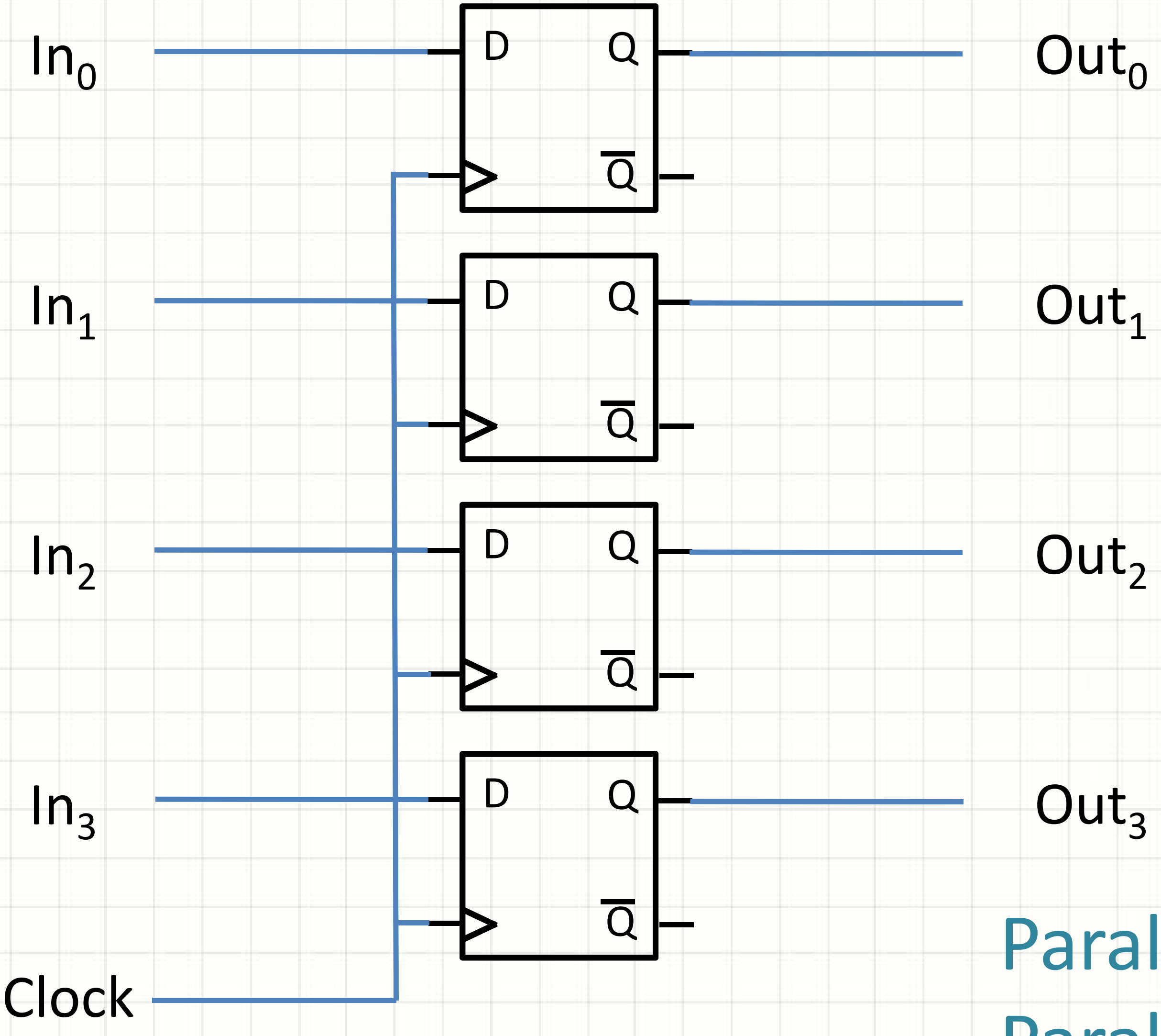
$D = T.\overline{Q} + \overline{T}.Q$

$D = J.\overline{Q} + \overline{K}.Q$

$S = T.\overline{Q},\ R = T.Q$

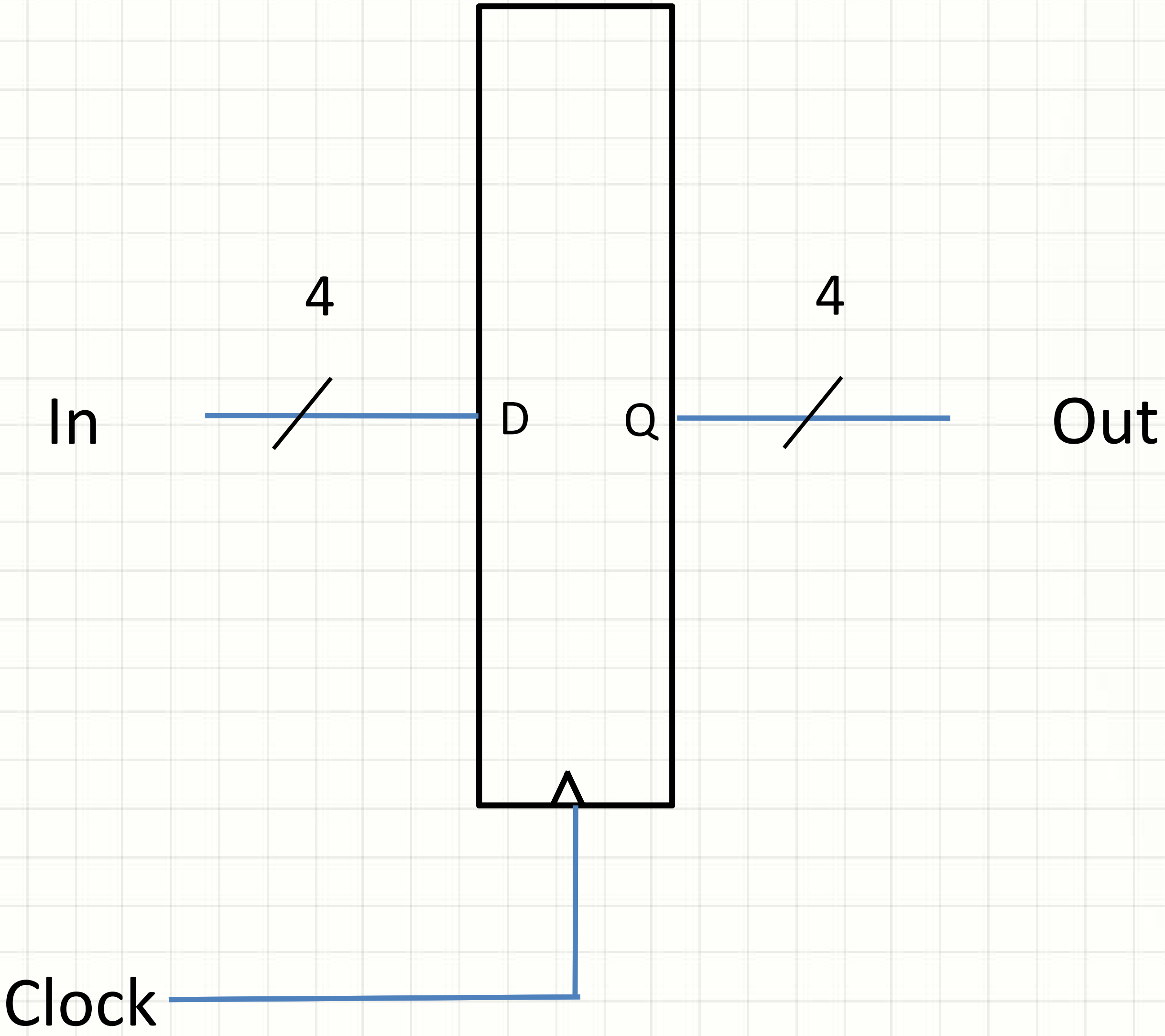
$S = J.\overline{Q},\ R = K.Q$

Register



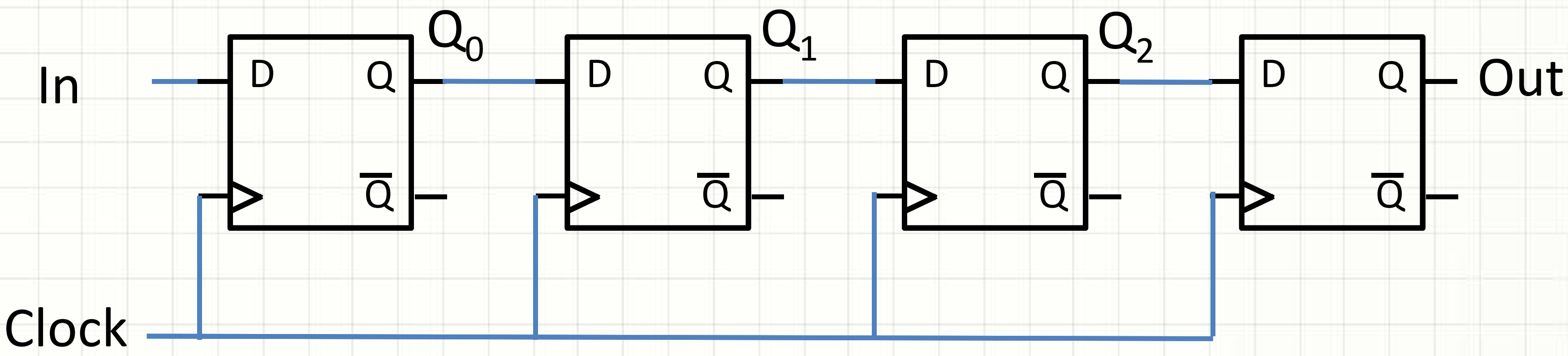
Parallel In
Parallel Out

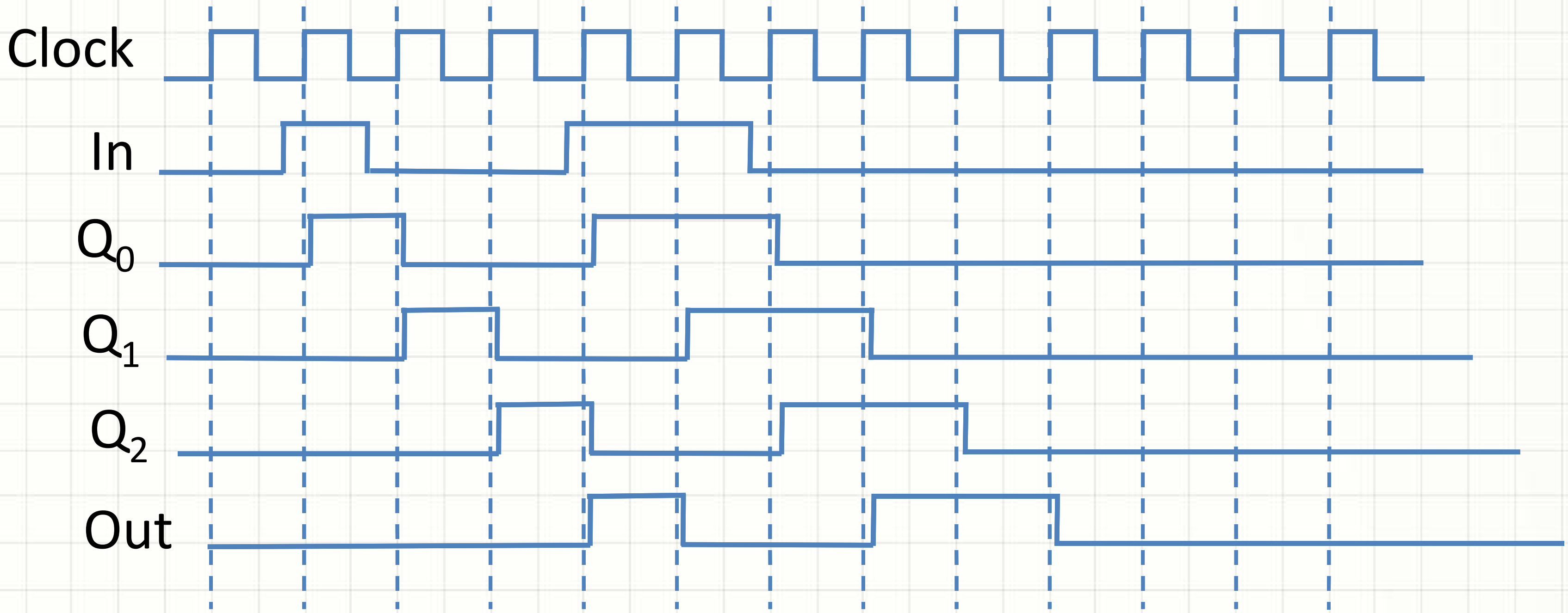
Parallel in Parallel out Register Symbol



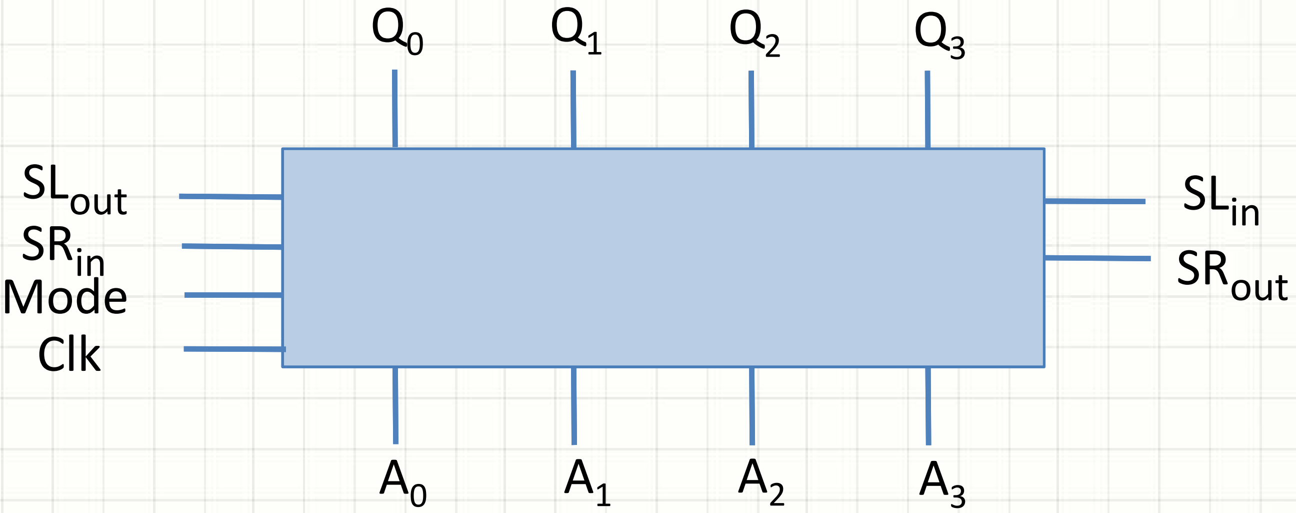
Register

Serial In
Serial Out



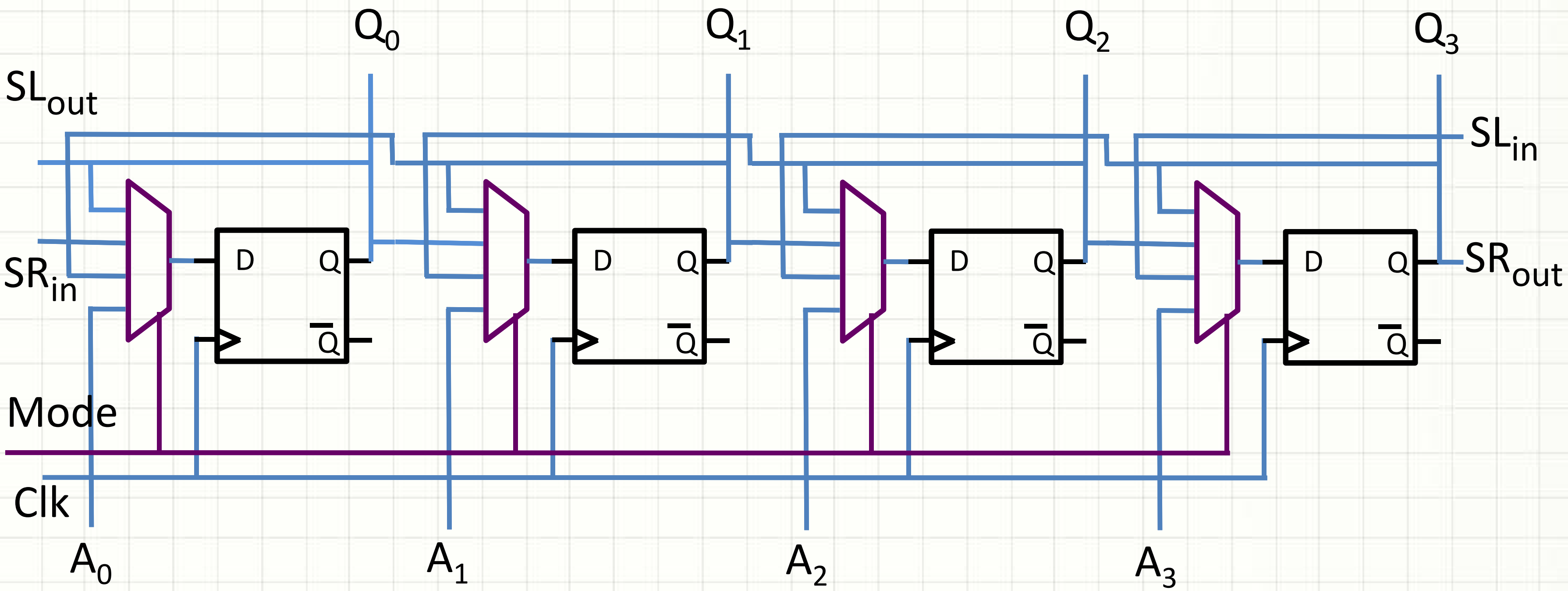


Register : Serial & Parallel



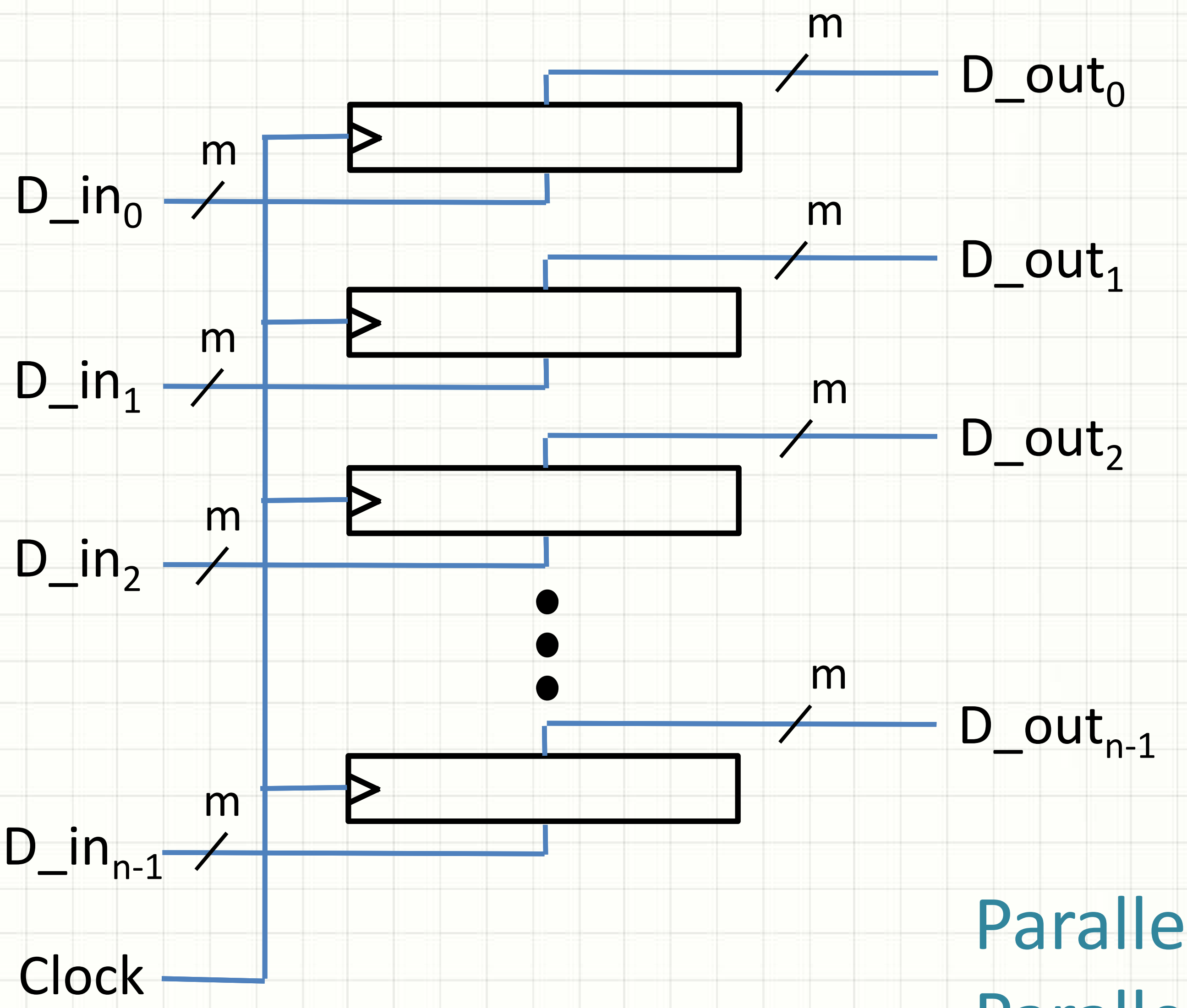
Mode	Operation
0 0	No change
0 1	Shift right
1 0	Shift left
1 1	Parallel load

Register : Serial & Parallel



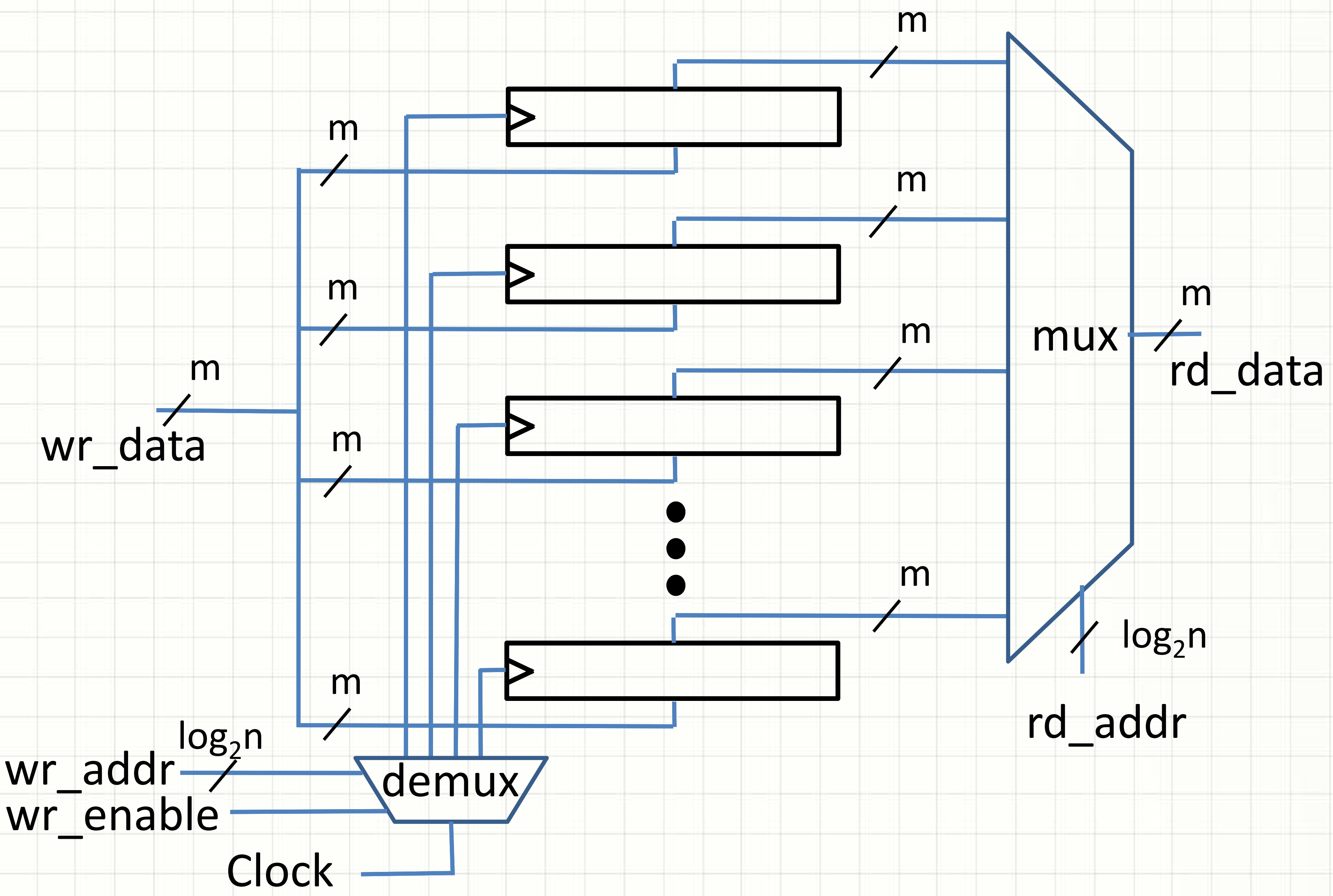
Mode	Operation
0 0	No change
0 1	Shift right
1 0	Shift left
1 1	Parallel load

Register File n x m



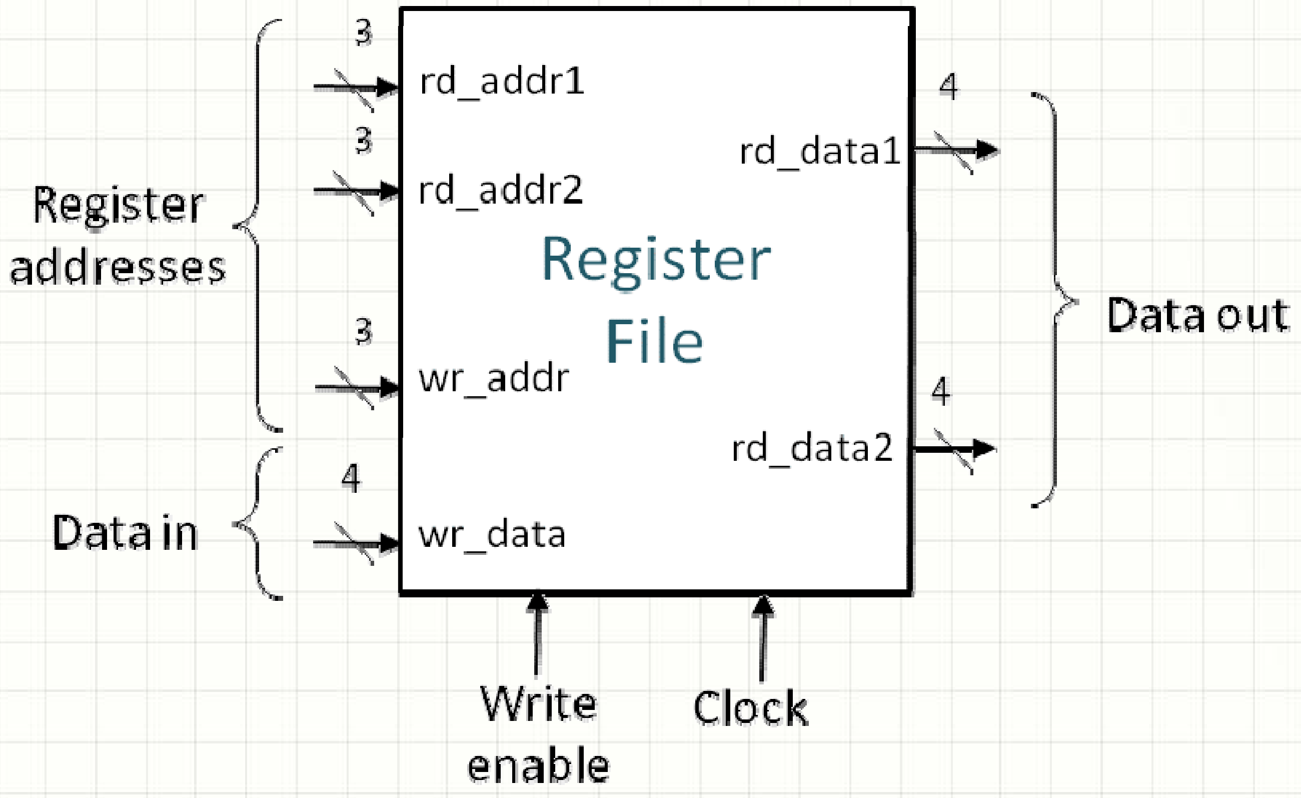
Parallel In
Parallel Out

Register File with addressing



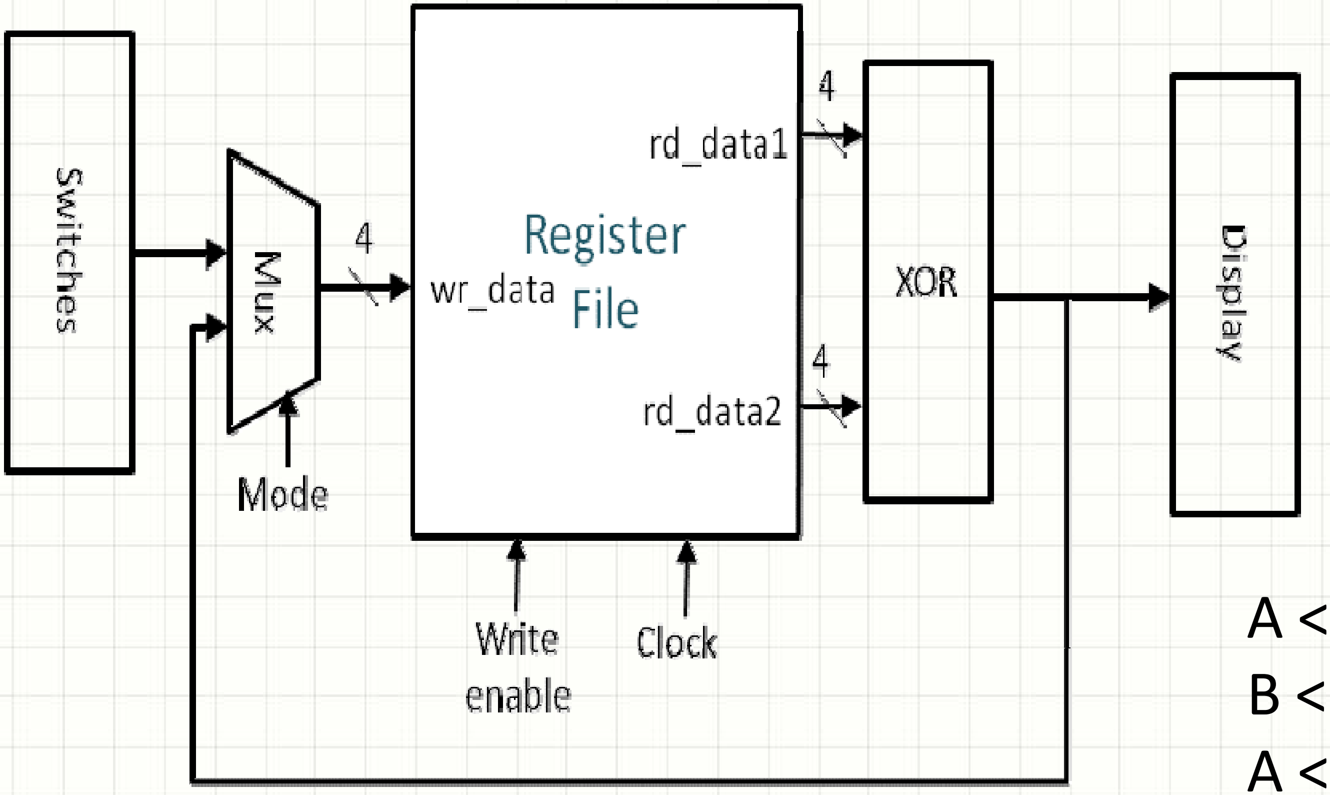
Lab Exercise 3

- Design 8x4 register file with 2 read and 1 write ports



Lab Exercise 3 continued

- In-place interchange of two registers in three XOR steps



A <= A XOR B
B <= A XOR B
A <= A XOR B

THANKS