COL215 Digital Logic and System Design

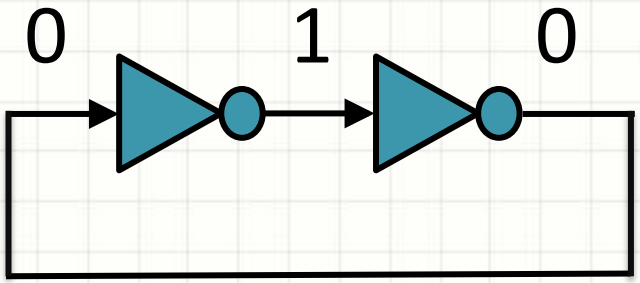
Sequential Circuits

02 August 2017

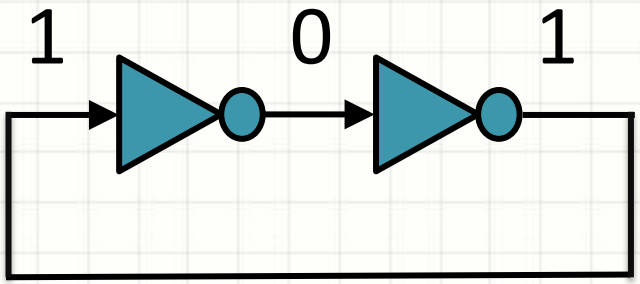
Lecture Outline

- Basic memory elements
- Gated latches
- Master-Slave flip-flops
- Edge triggered flip-flops

A simple storage element

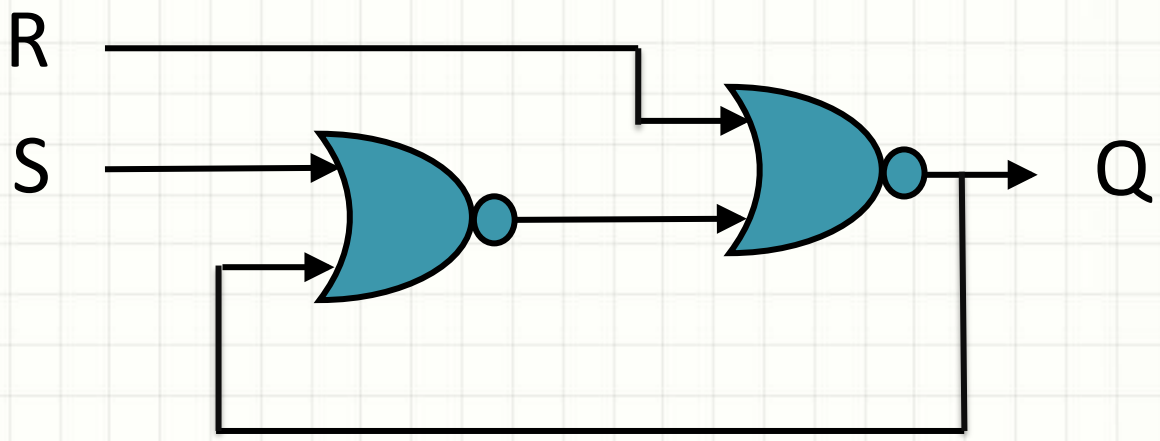


A simple storage element



How to change the stored value?

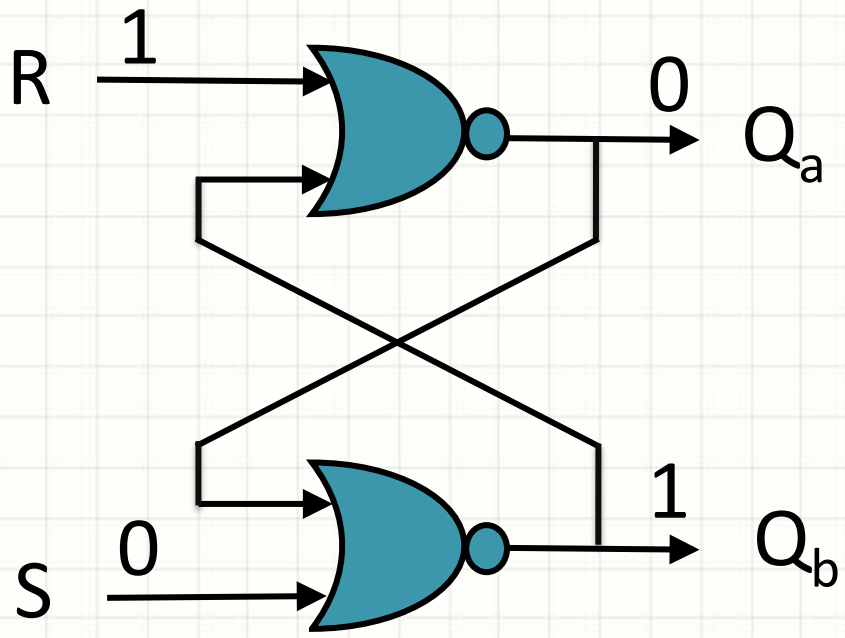
A Set-Reset Latch (SR Latch)



R : Reset

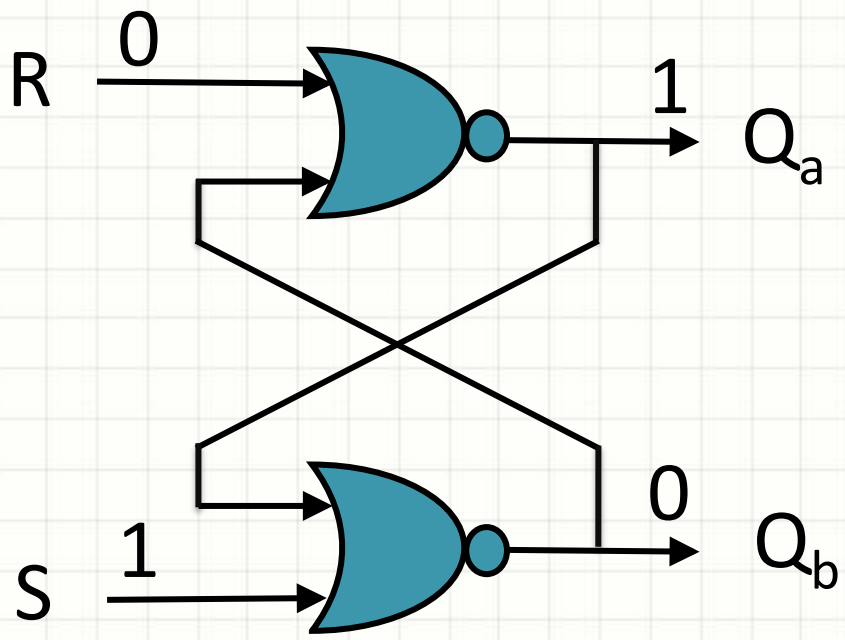
S : Set

SR Latch redrawn



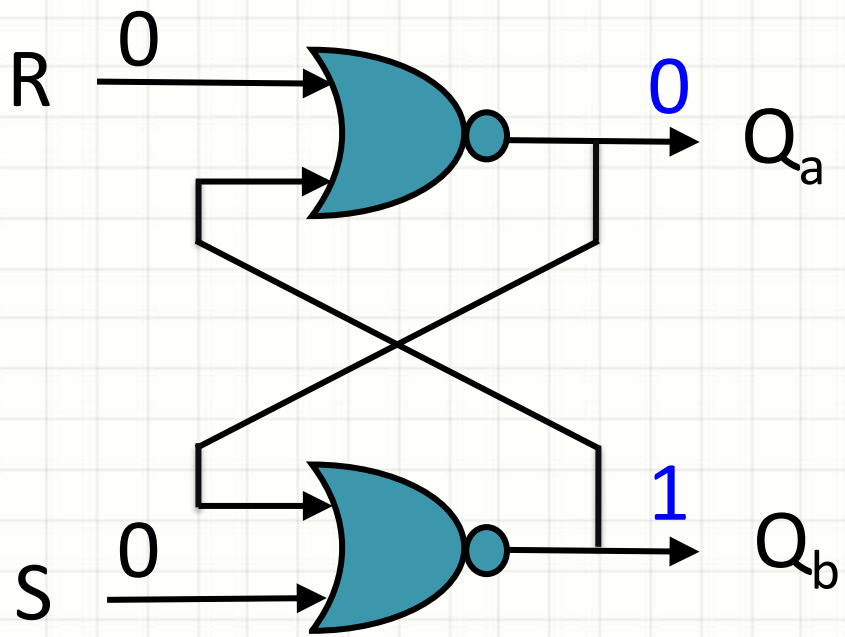
S	R	Q_a	Q_b

SR Latch redrawn



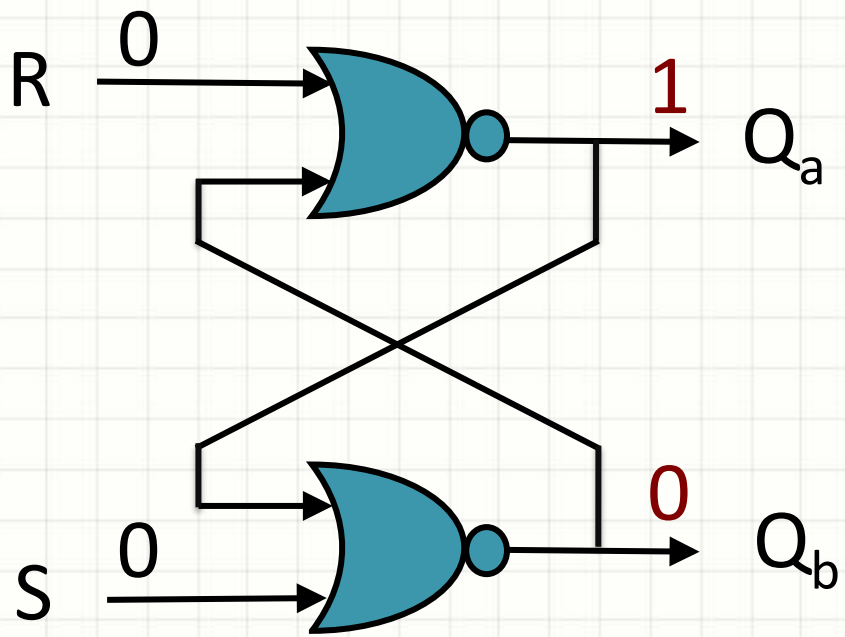
S	R	Q_a	Q_b
0	1	0	1
1	0		

SR Latch redrawn



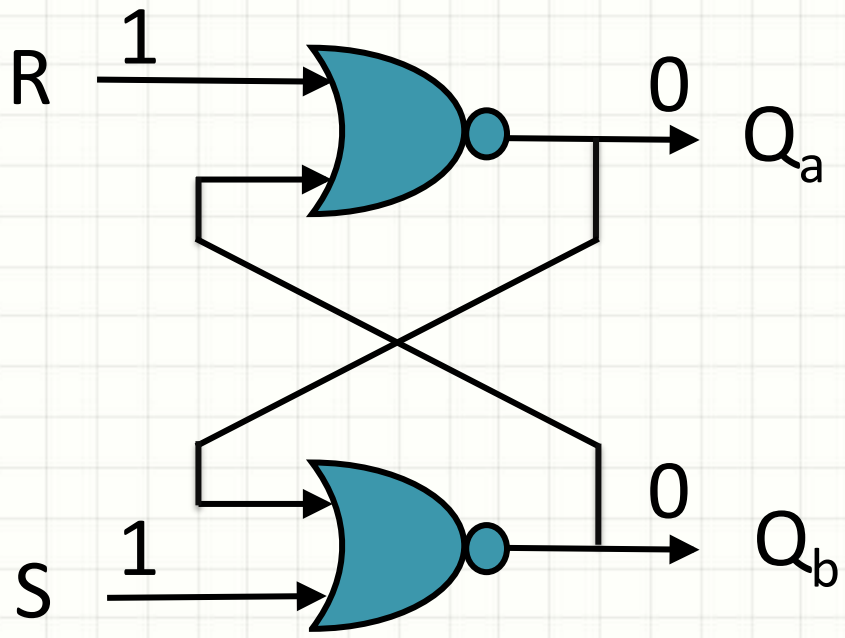
S	R	Q_a	Q_b
0	0		
0	1	0	1
1	0	1	0

SR Latch redrawn



S	R	Q_a	Q_b
0	0		
0	1	0	1
1	0	1	0

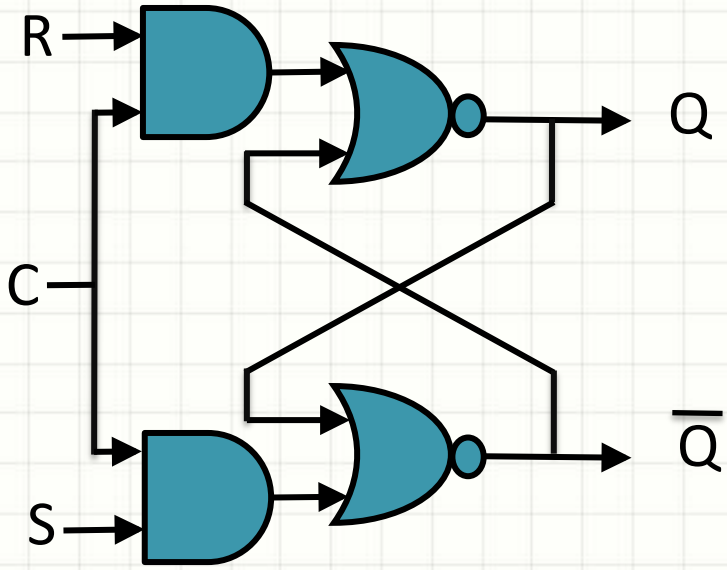
SR Latch redrawn



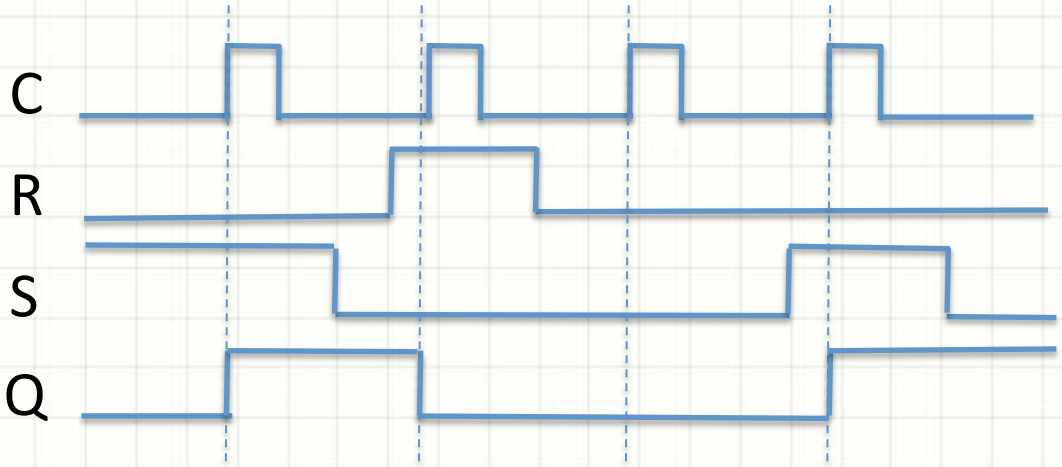
S	R	Q_a	Q_b
0	0	0/1	1/0
0	1	0	1
1	0	1	0
1	1		

Don't allow S = 1 as well as R = 1 or allow above, but allow only one input change at a time

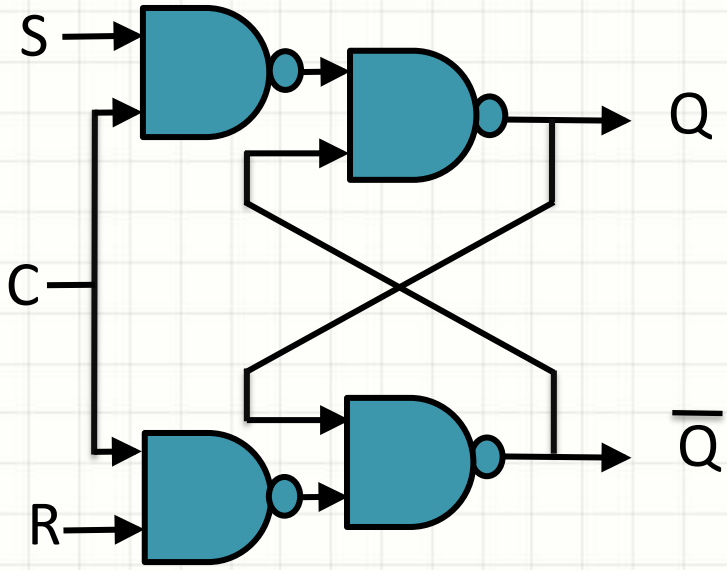
Gated SR Latch



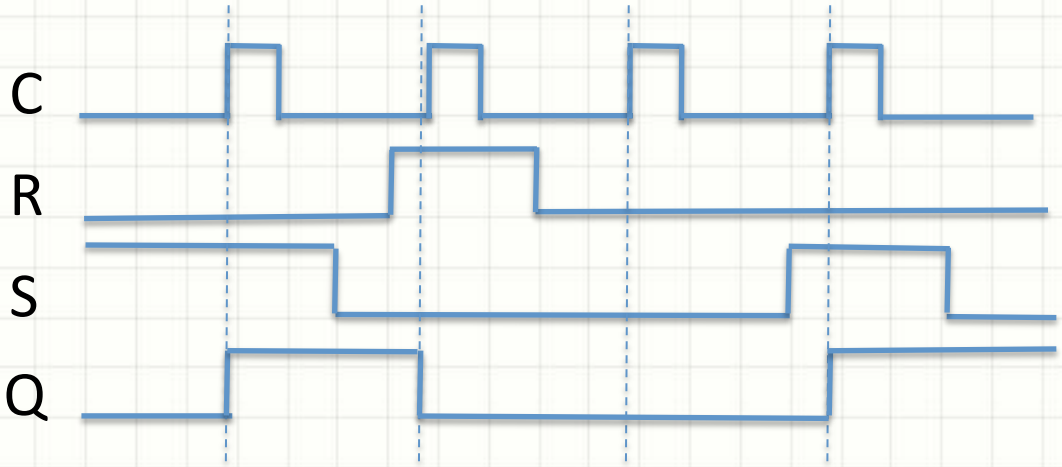
C	S	R	Q (t+1)
0	-	-	
1	0	0	
1	0	1	
1	1	0	
1	1	1	



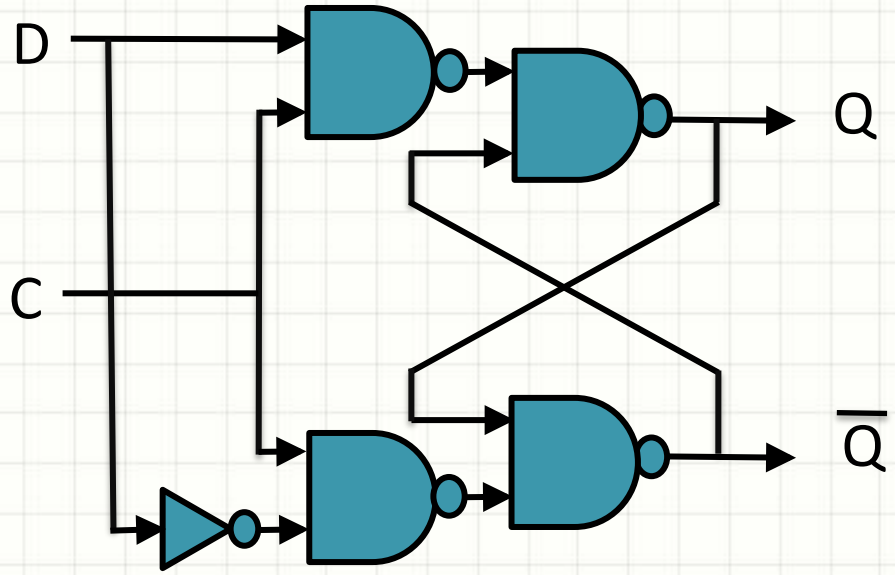
Gated SR Latch using NAND gates



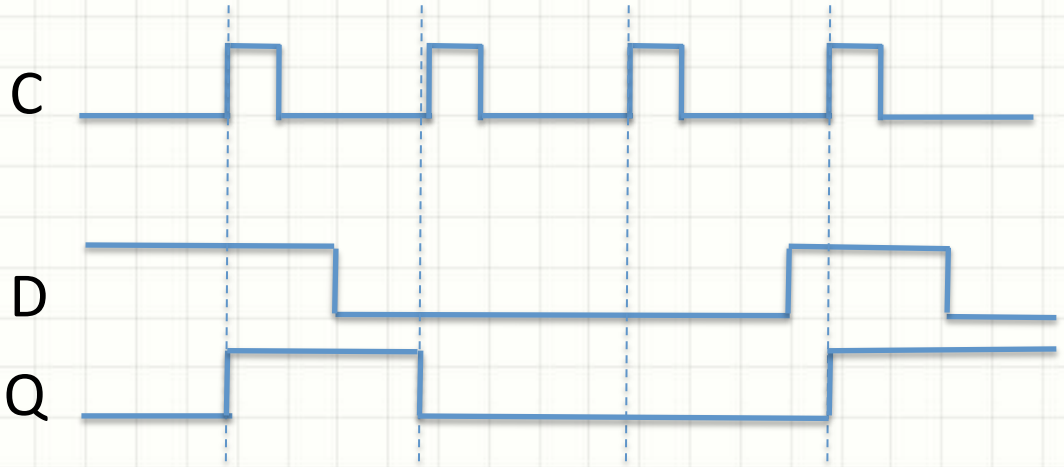
C	S	R	Q(t+1)
0	-	-	Q(t)
1	0	0	Q(t)
1	0	1	0
1	1	0	1
1	1	1	?



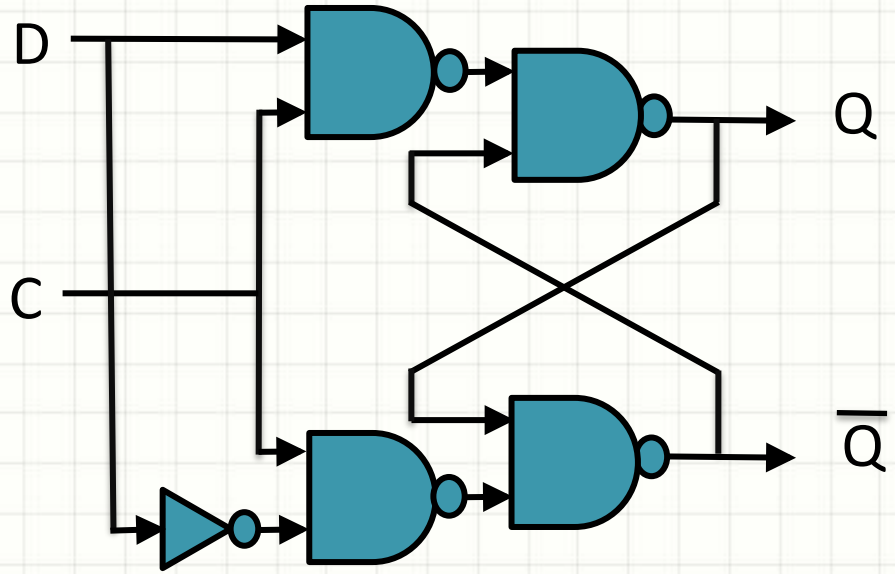
D Latch



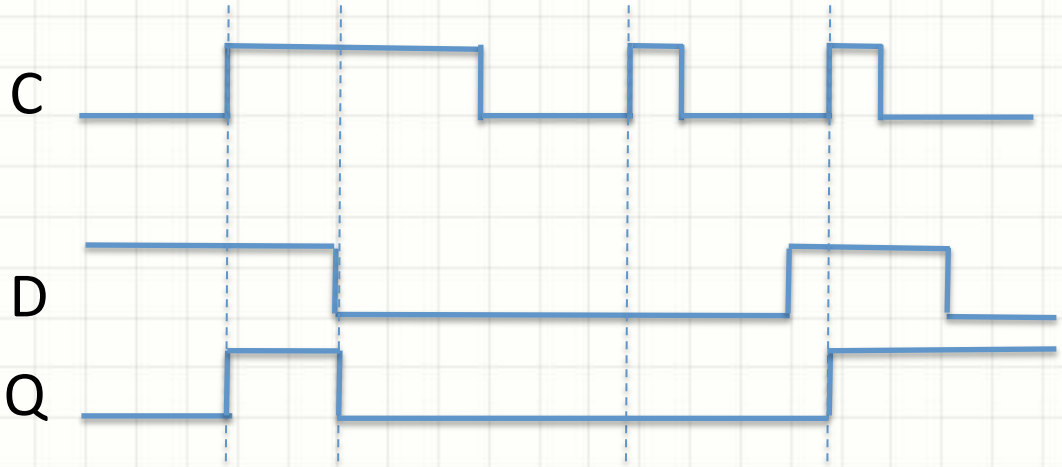
C	D	Q(t+1)
0	-	Q(t)
1	0	0
1	1	1

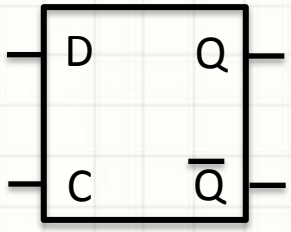


D Latch (D changes while C = 1)

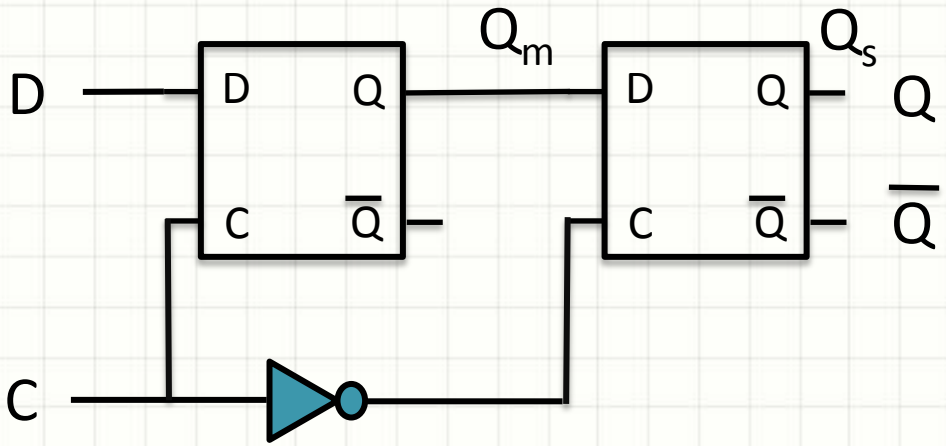


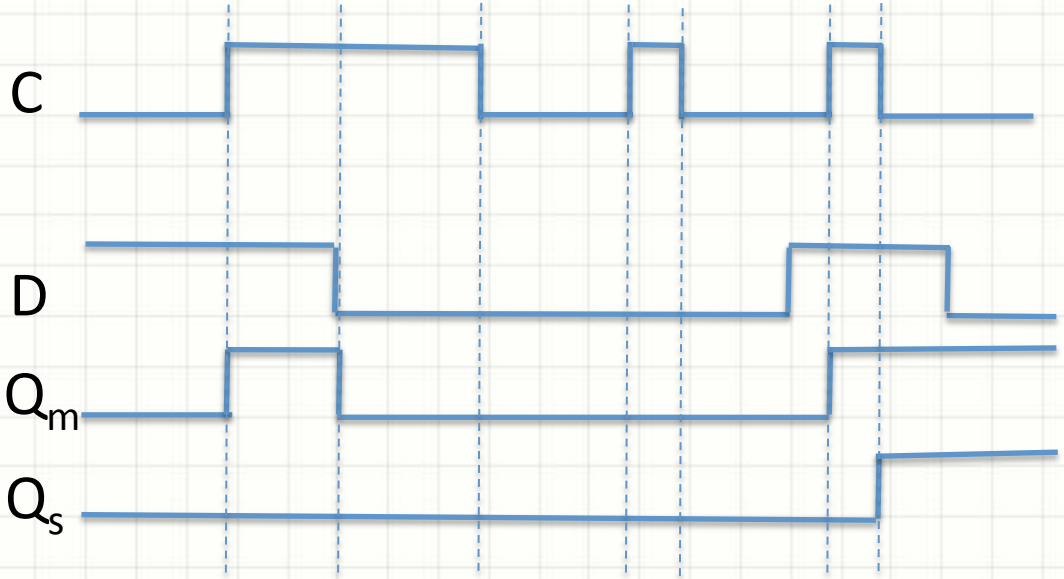
C	D	Q(t+1)
0	-	Q(t)
1	0	0
1	1	1





Master-Slave D Flip-FLop





QUESTIONS?