COL215 Digital Logic and System Design

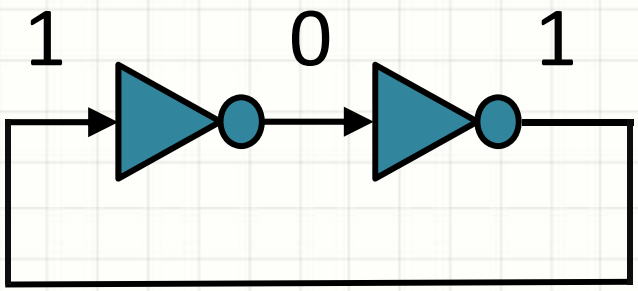
Sequential Circuits

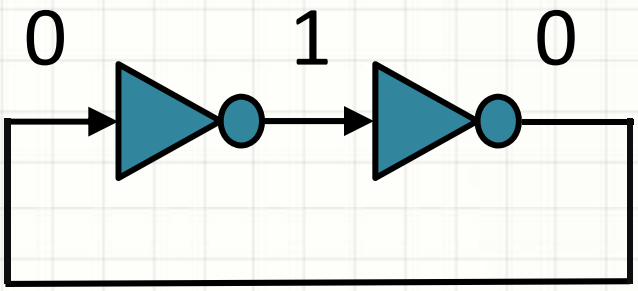
04 August 2017

Lecture Outline

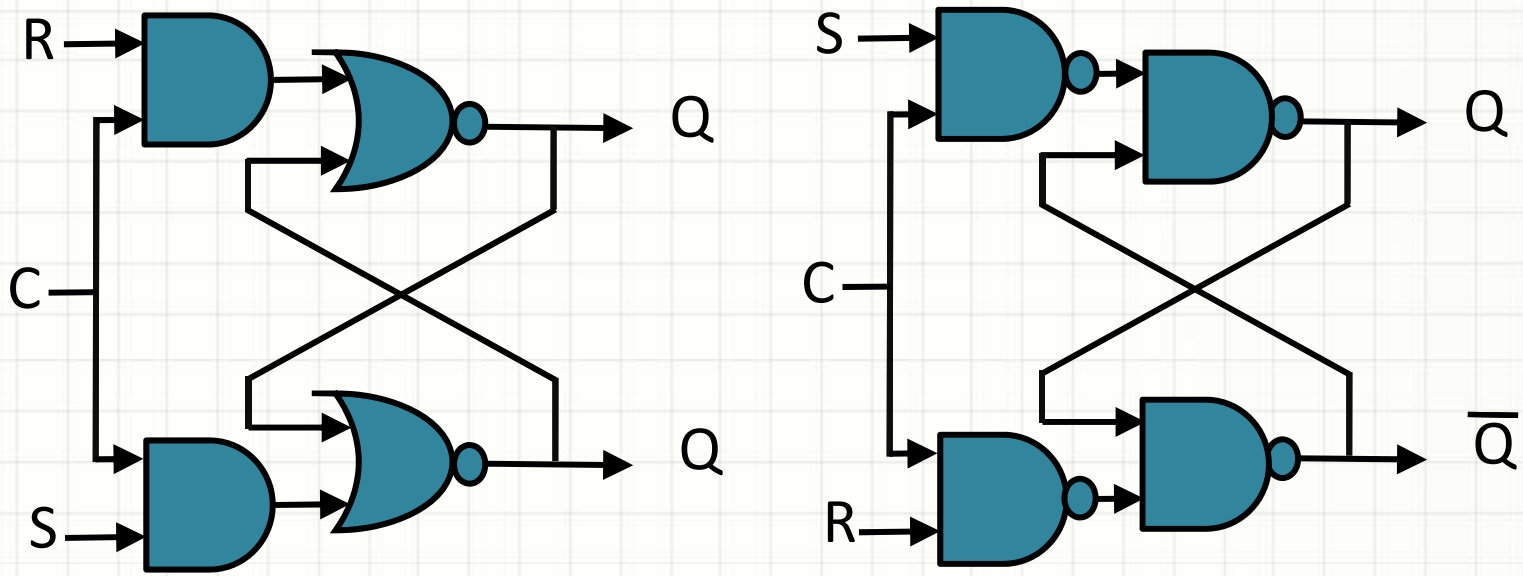
- Basic memory elements
- Gated latches
- Master-Slave flip-flops
- Edge triggered flip-flops

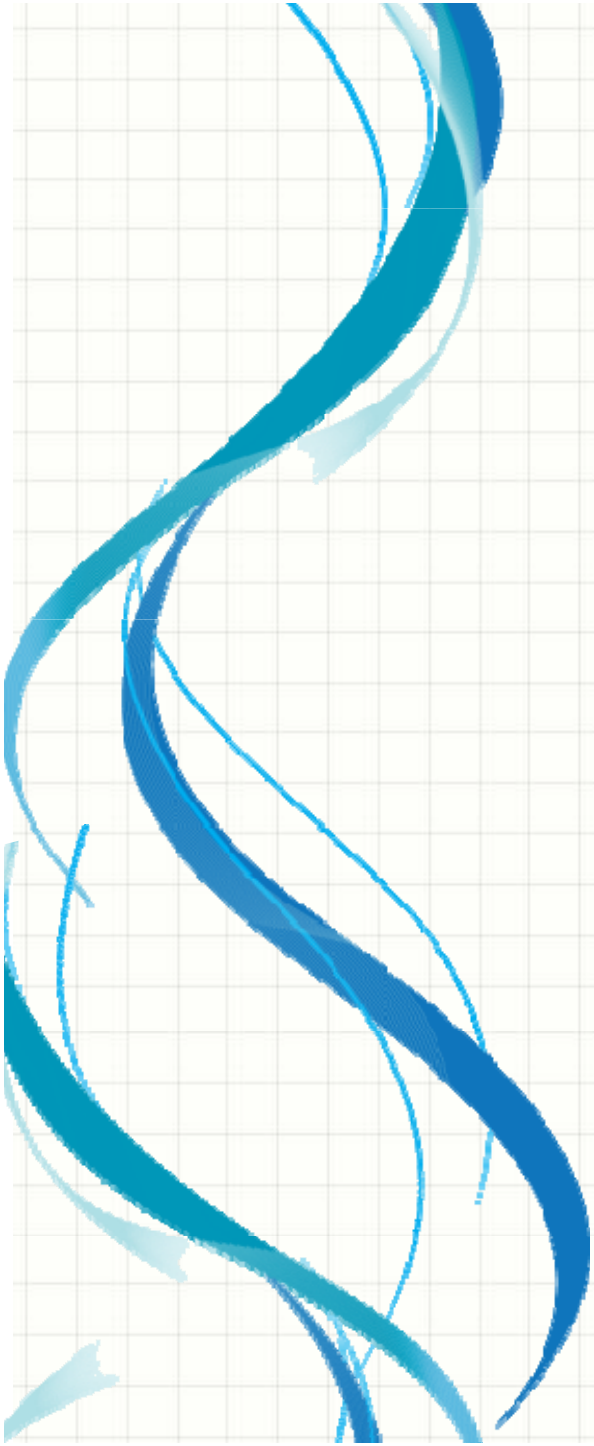
Storage element design





Gated SR Latch





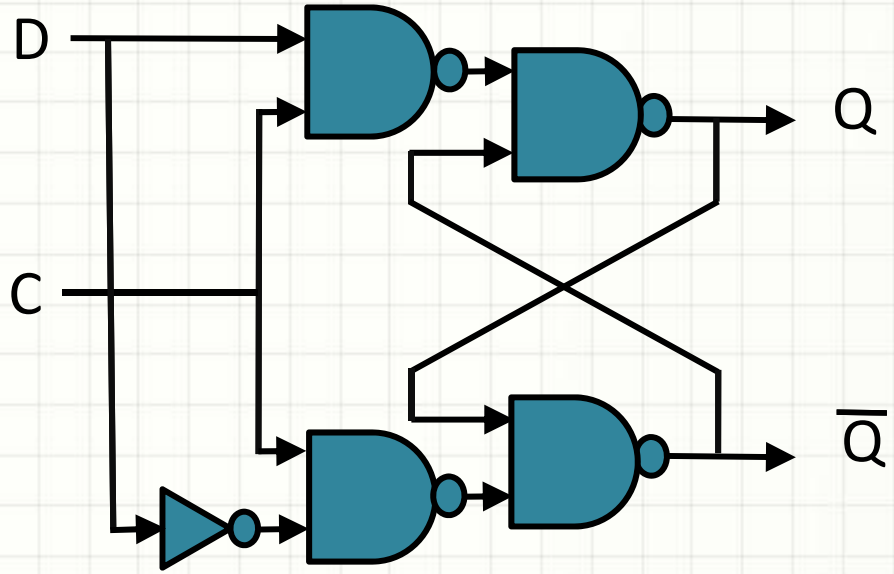
Problems with SR latch design

- Problem of transition from (S = R = 1) to (S = R = 0)
  uncertain output | oscillations | meta-stability
- Problem of change in S, R while C = 1
  output change not timed with clock

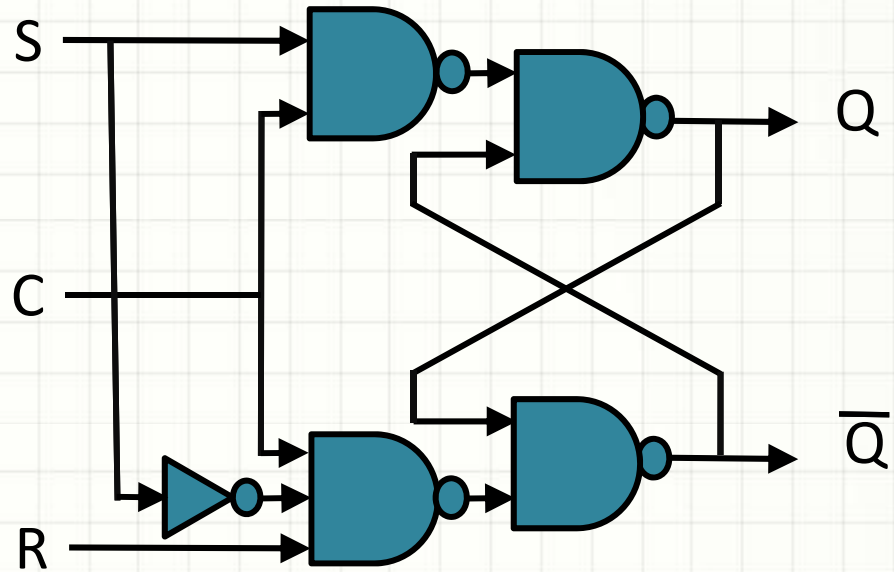
Solutions

- Don’t connect S, R directly
  - S = D, R = $\overline{D}$
  - Gate R input with $\overline{S}$ or vice versa
- Edge triggering, not level triggering
  - Master-slave flip-flop (8 gates)
  - Edge triggered flip-flop (6 gates)

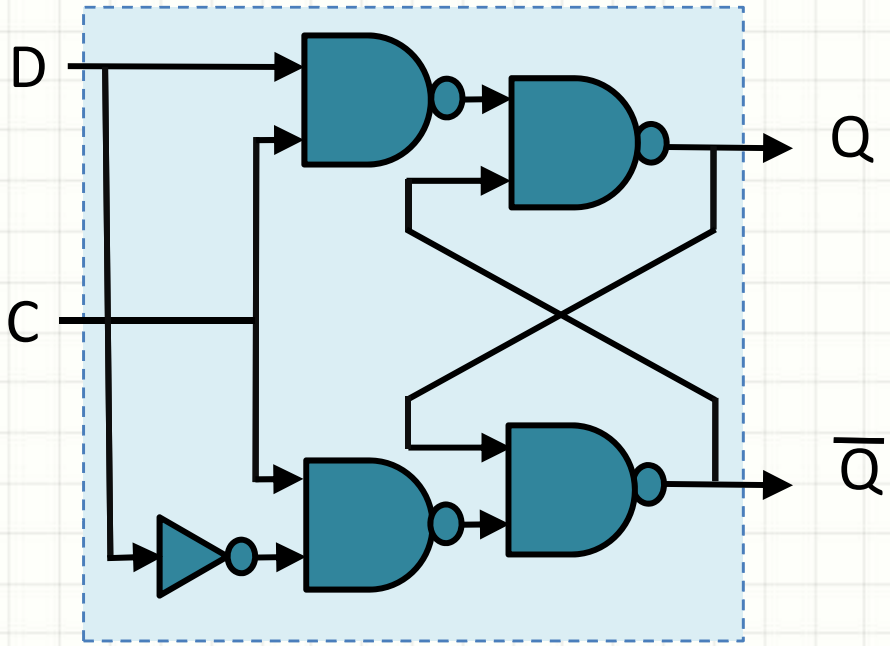
D Latch

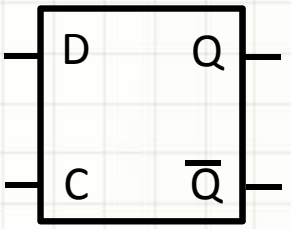


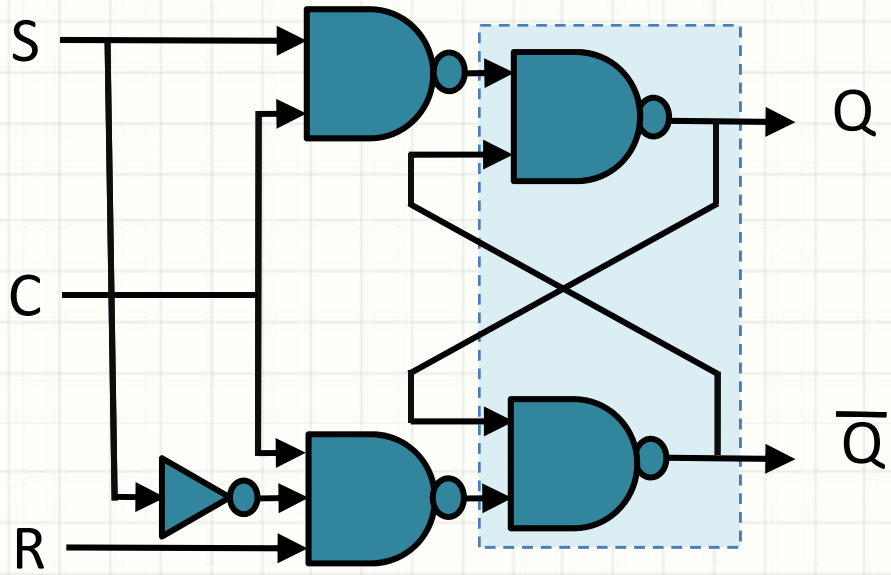
S overrides R

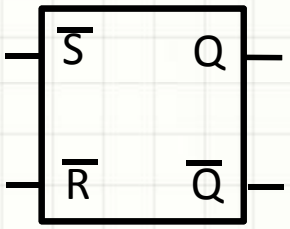


Abstraction

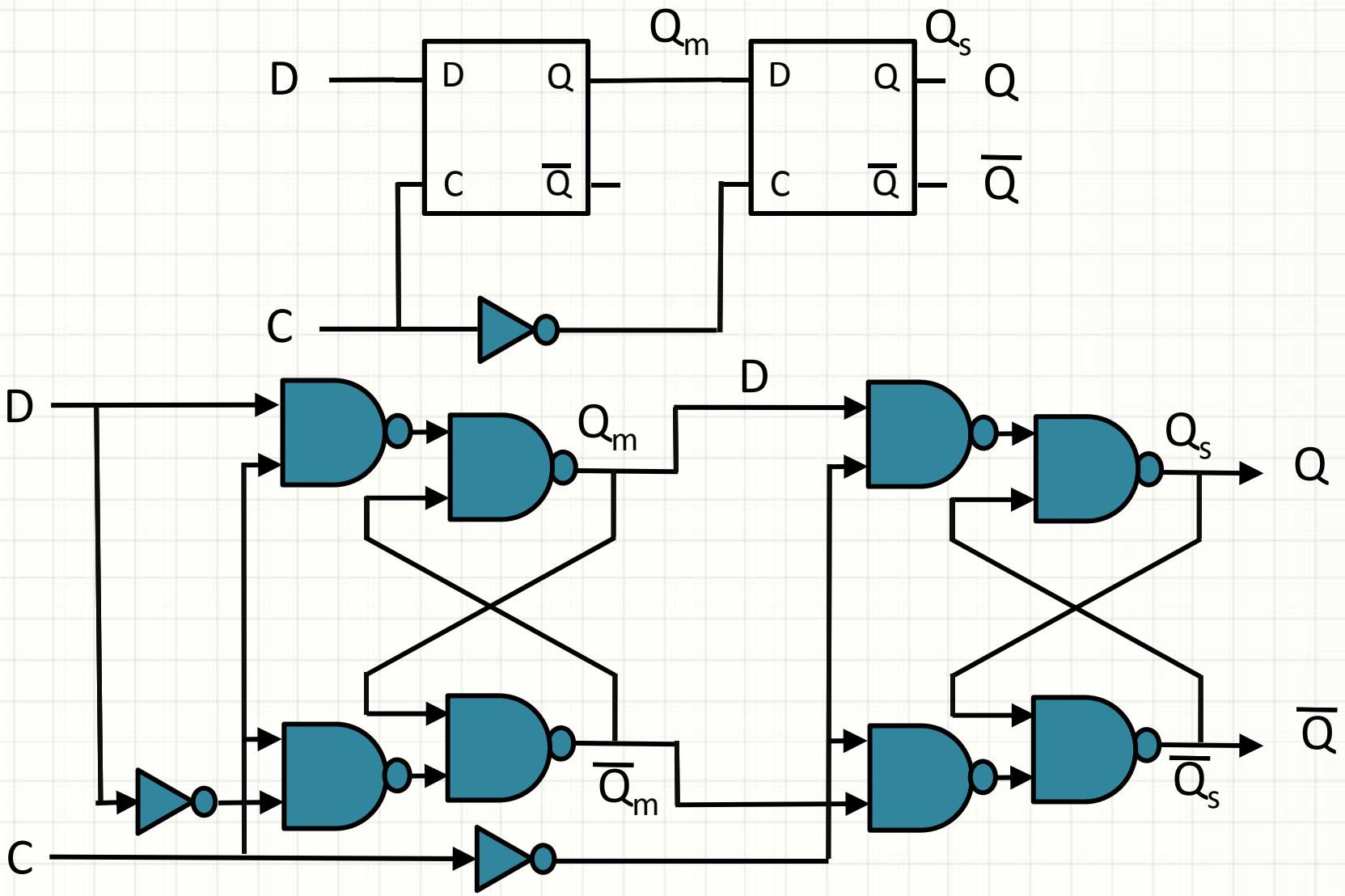




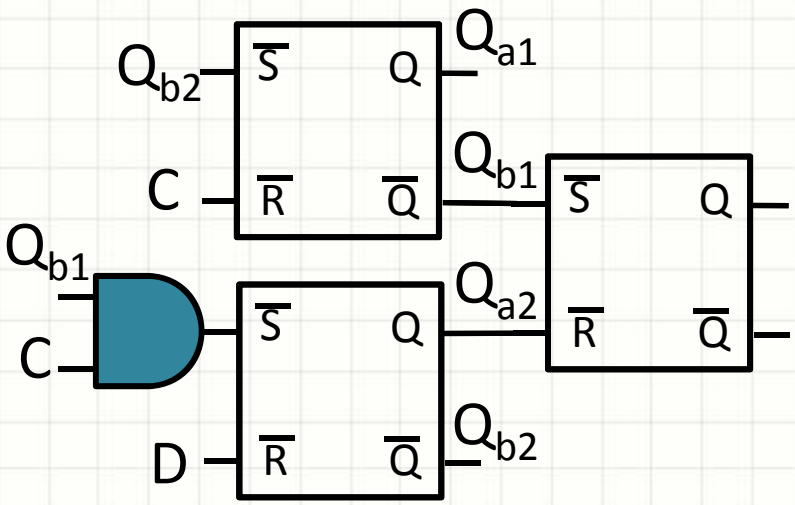


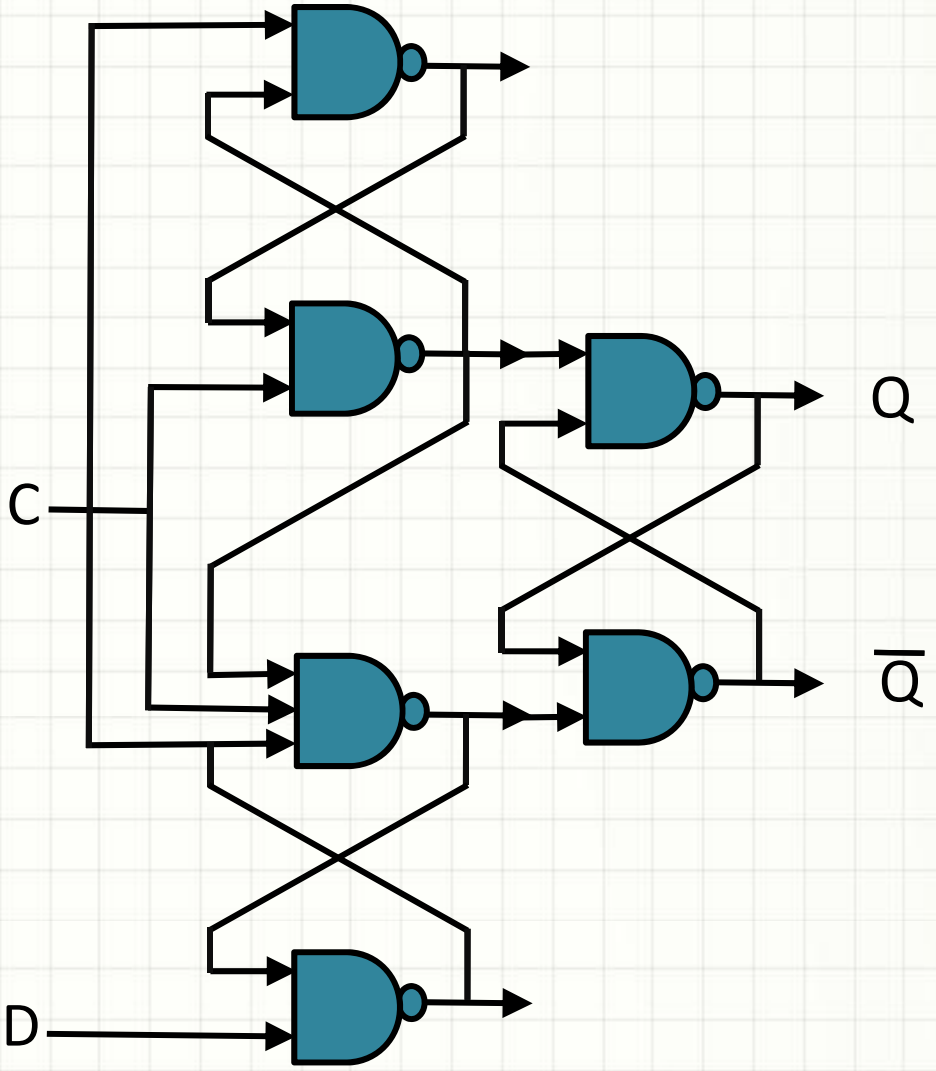


Master-Slave D Flip-Flop

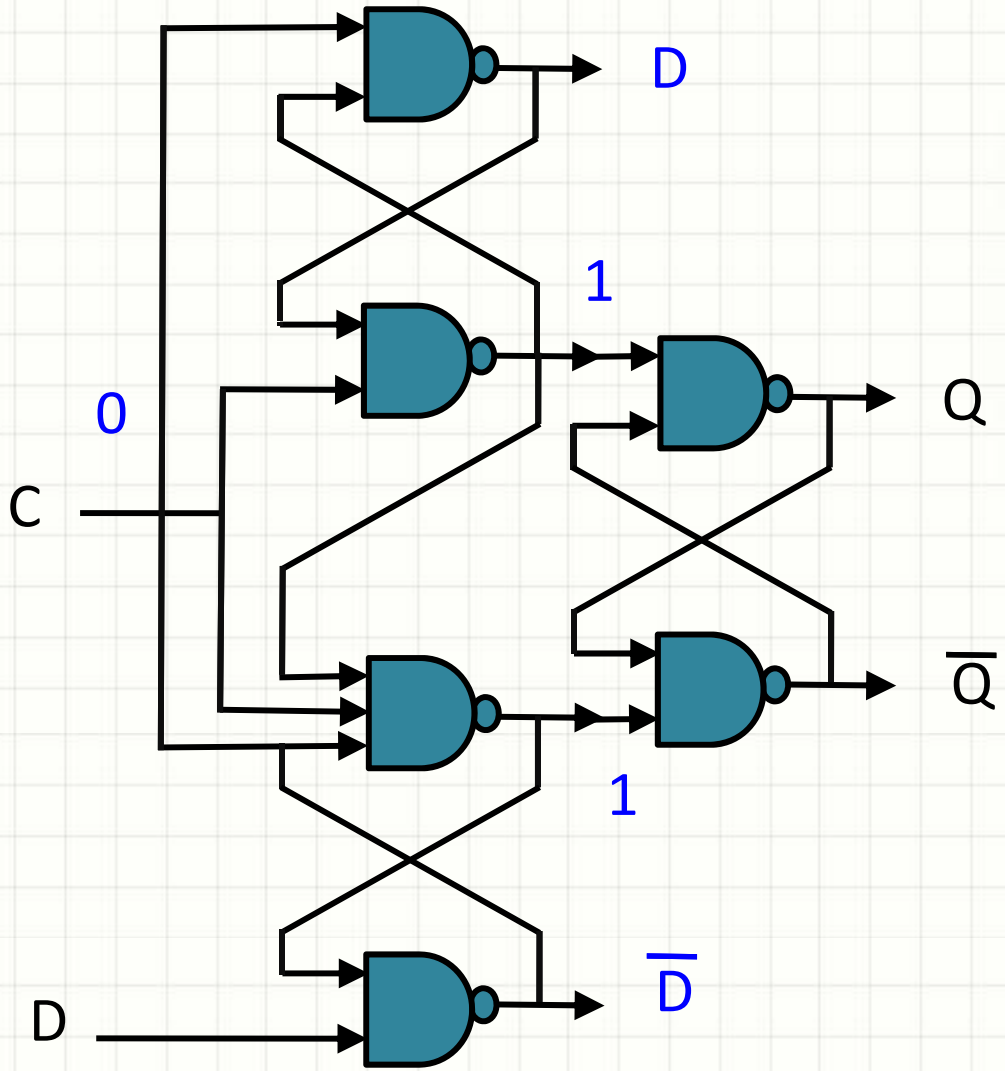


Edge triggered D Flip-Flop

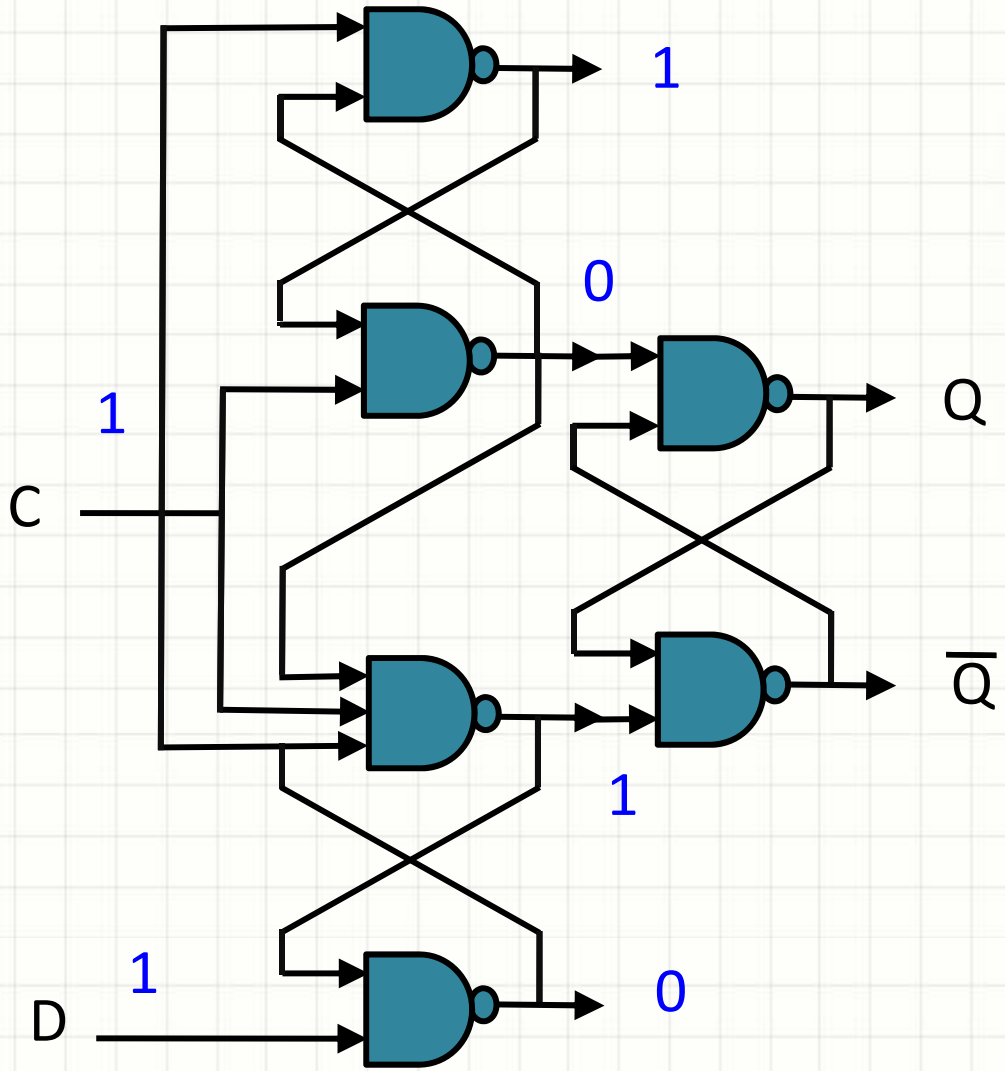




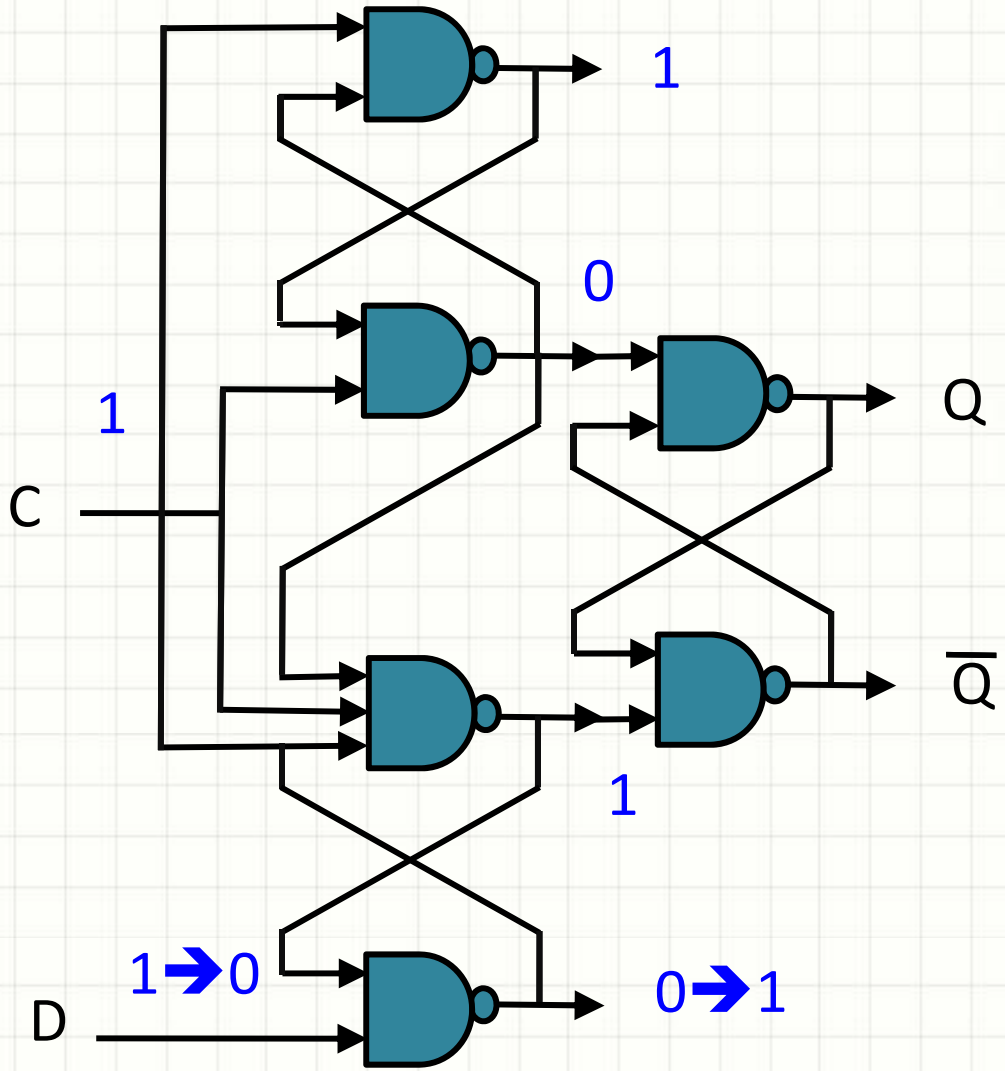
Edge triggered D Flip-Flop



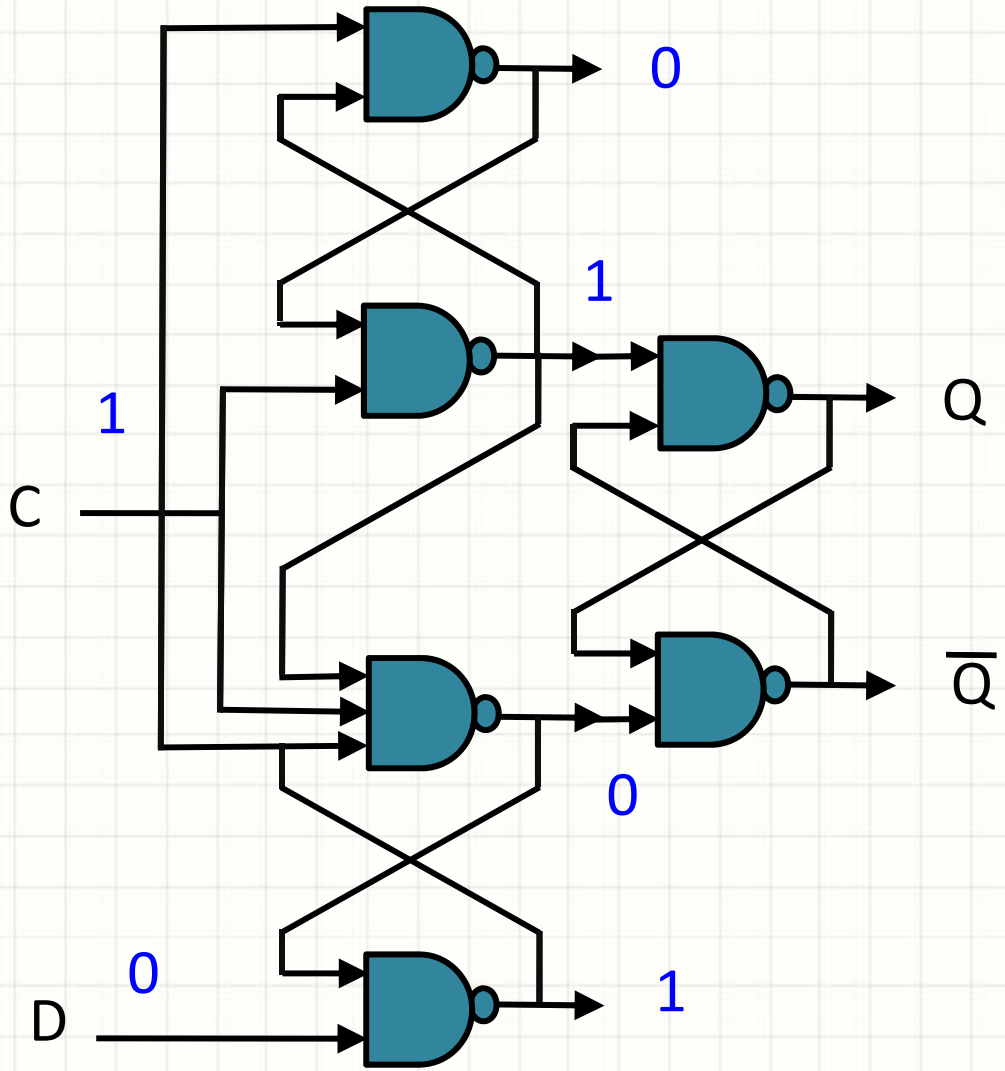
Edge triggered D Flip-Flop



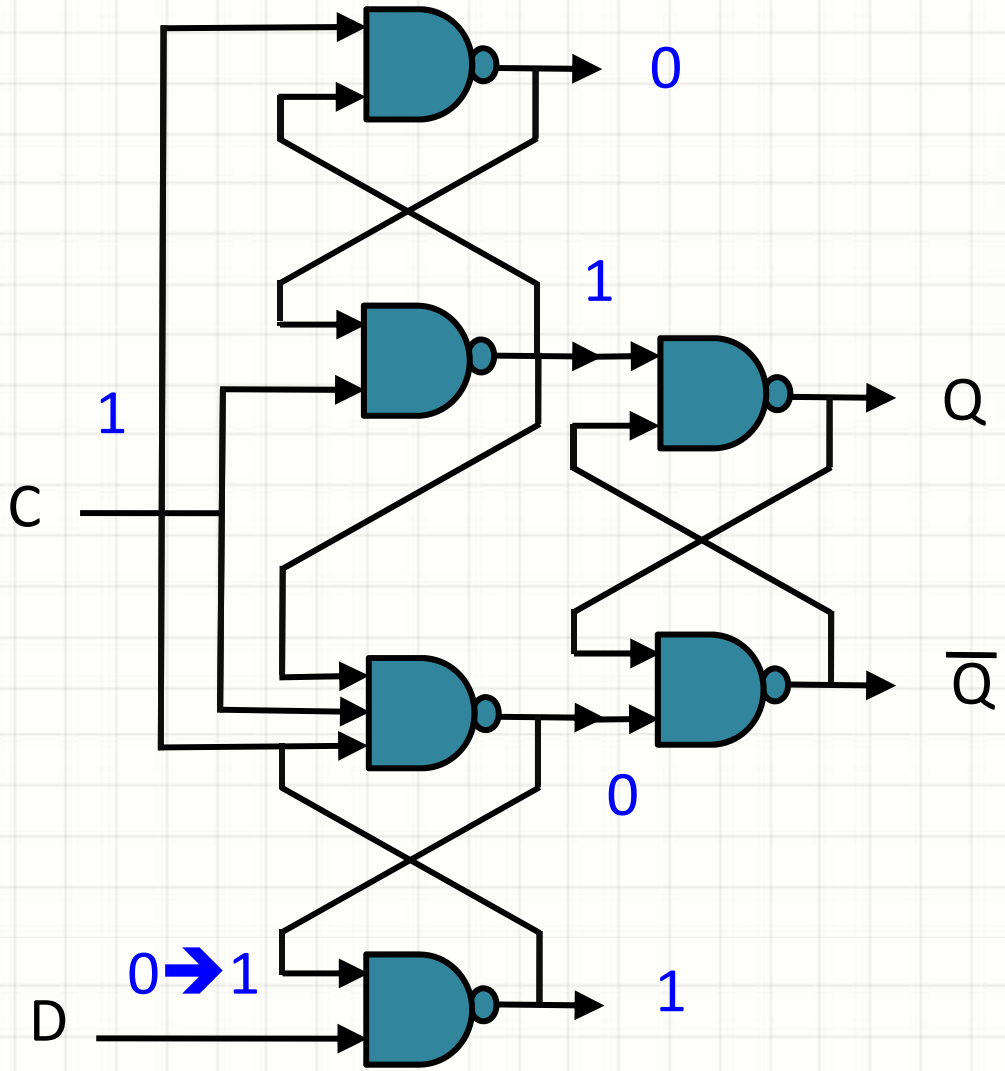
Edge triggered D Flip-Flop



Edge triggered D Flip-Flop



Edge triggered D Flip-Flop



THANKS