COL215 Digital Logic and System Design

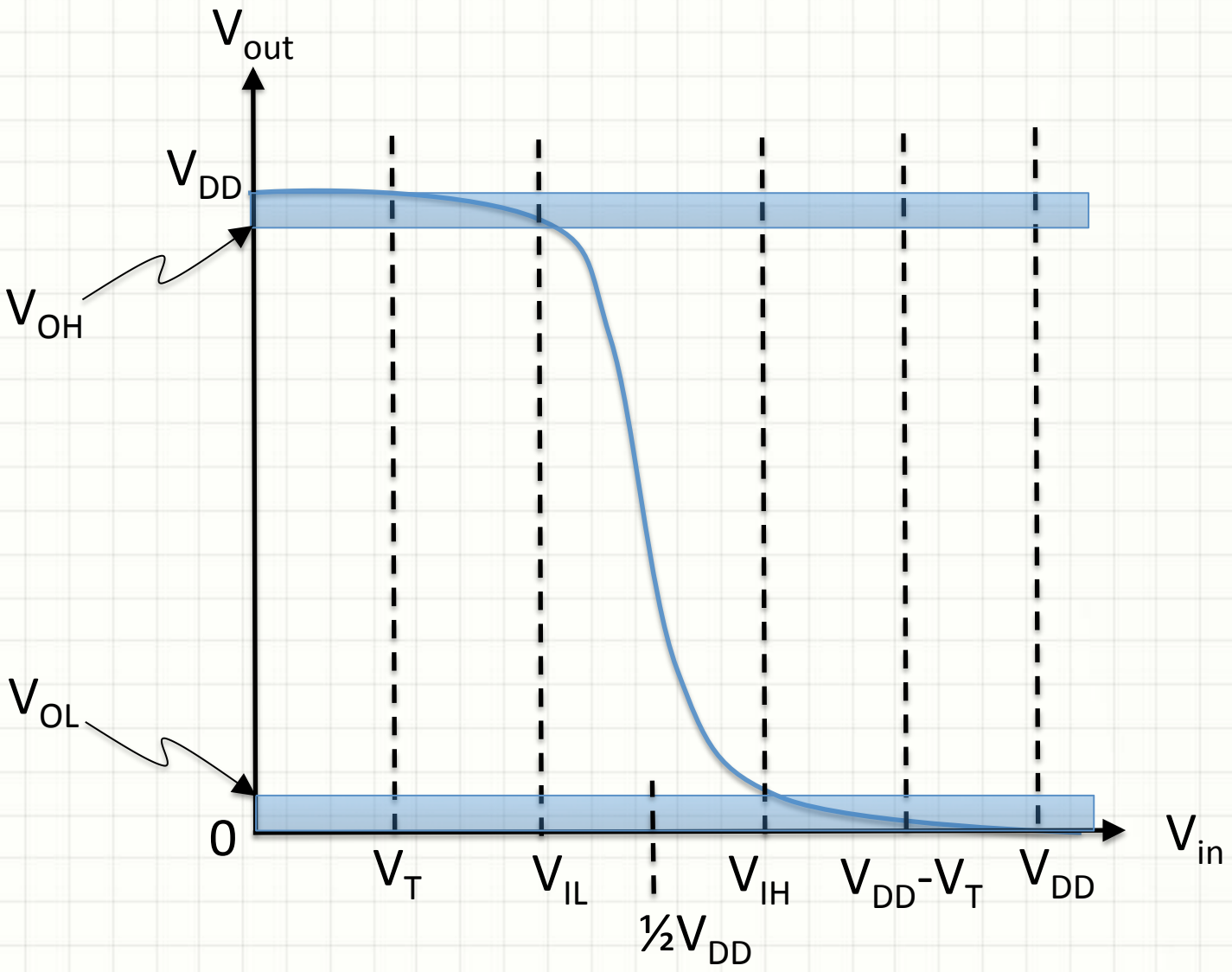
Real Circuits :

Transistors and Gates

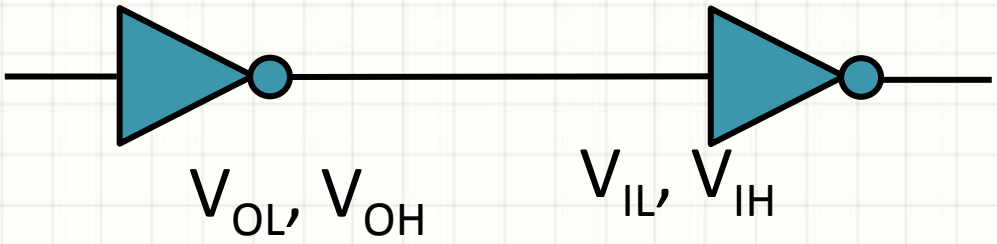
continued

20 September 2017

I/O characteristics of CMOS inverter



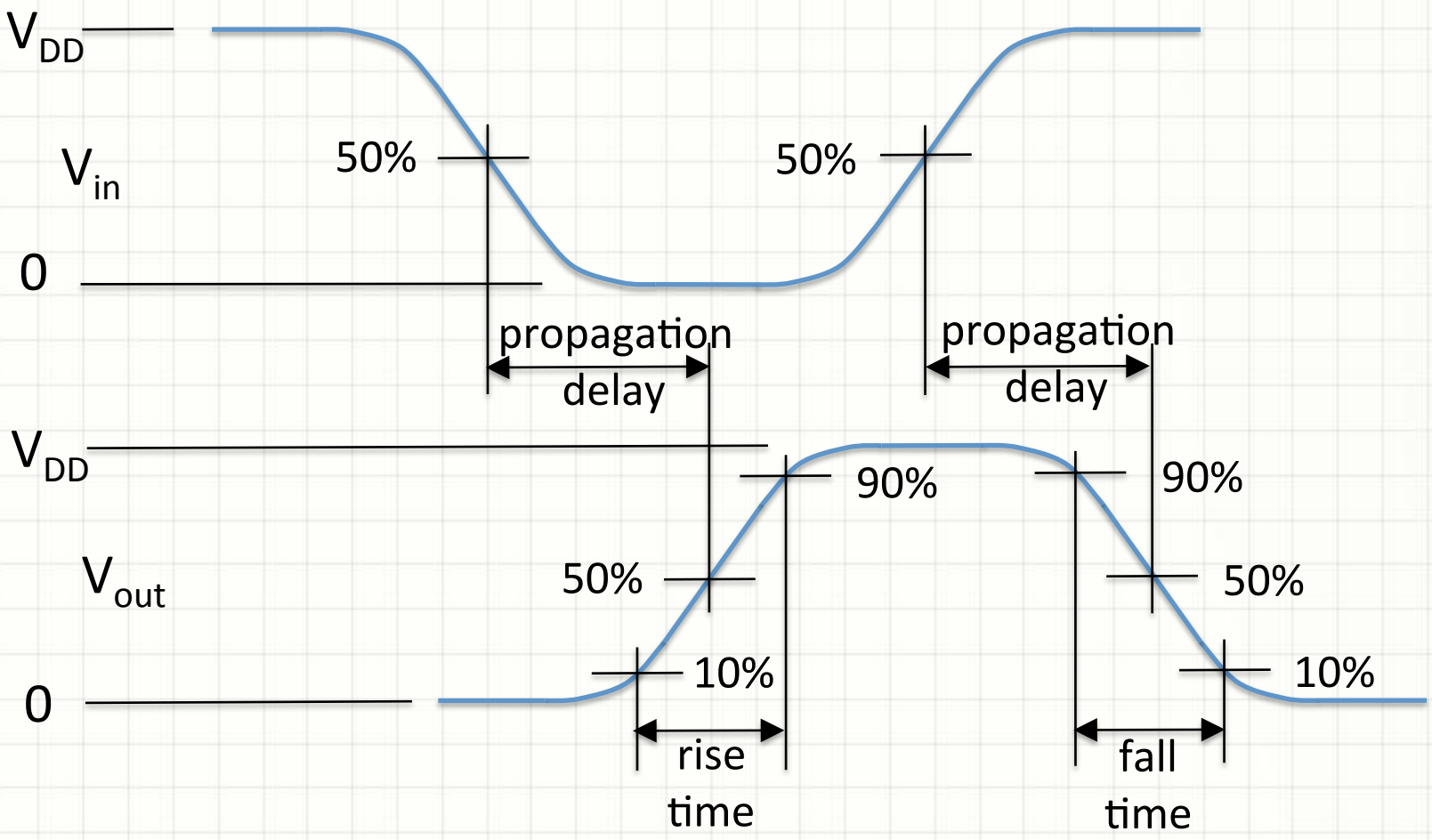
Noise Margin



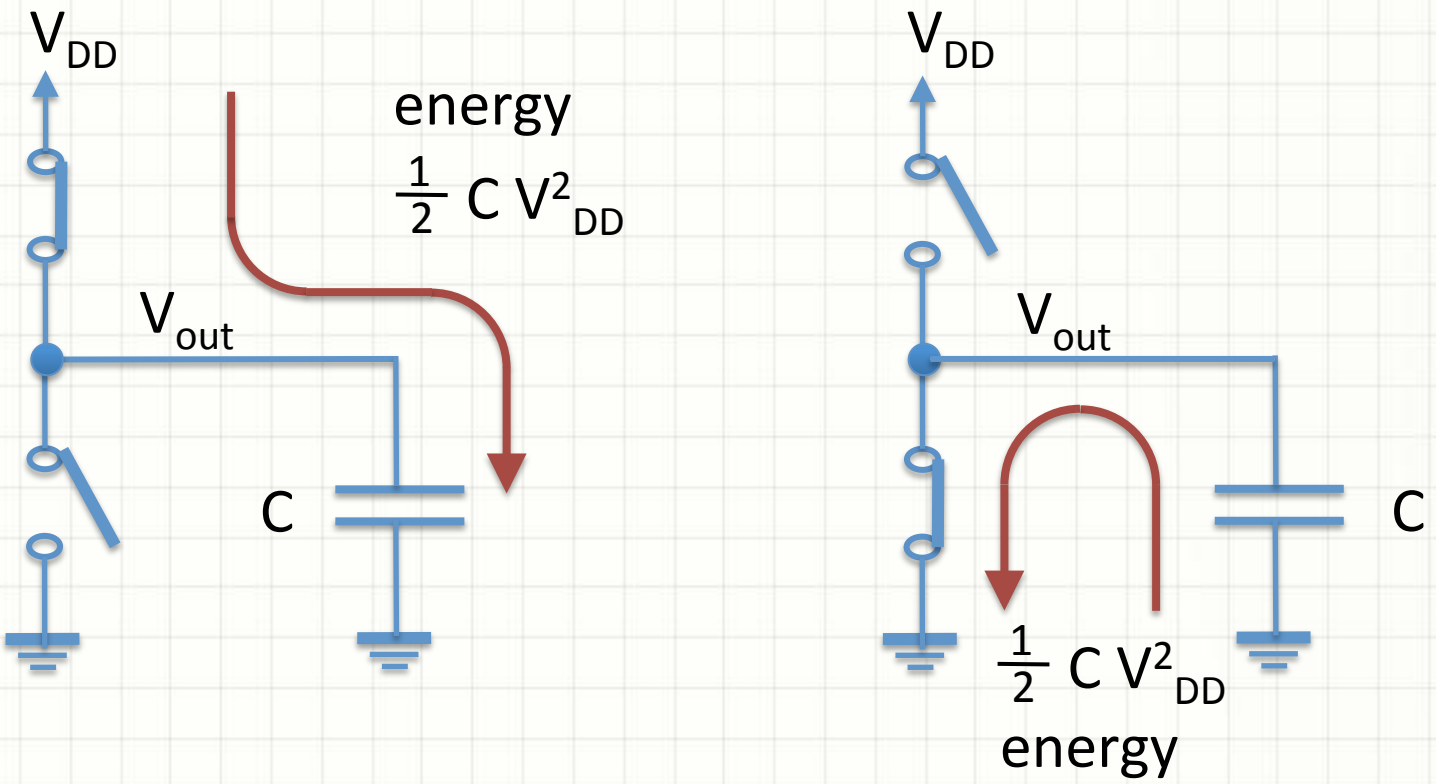
$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$

Dynamic operation and delays

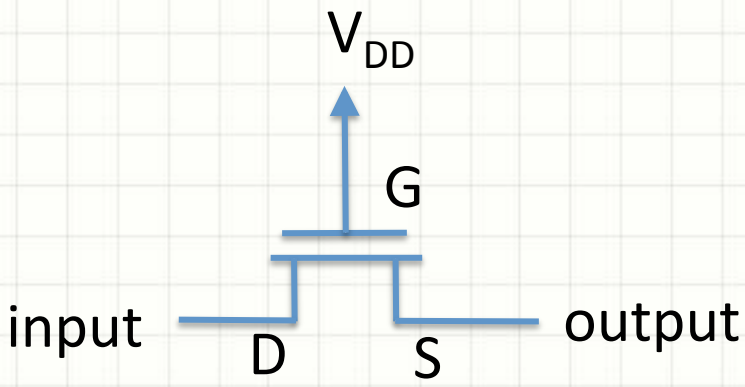


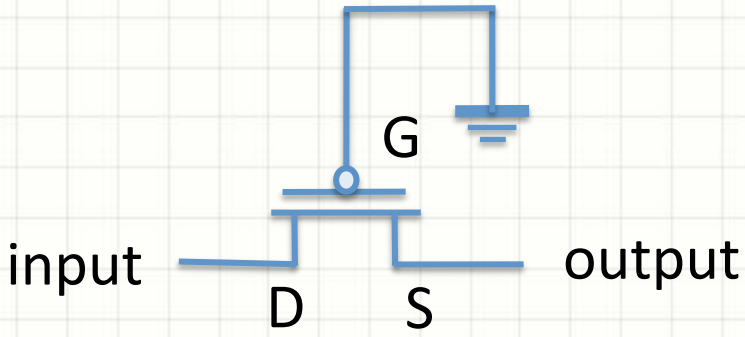
Power dissipation in CMOS inverter



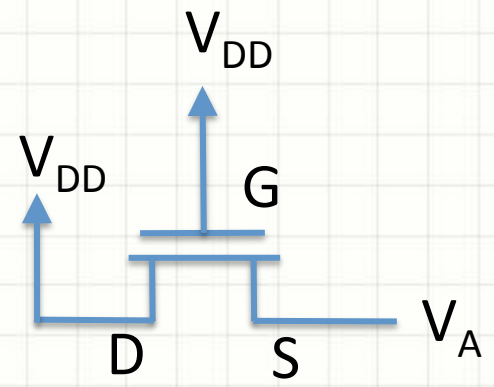
power = f C V^2_{DD}

Using NMOS / PMOS transistors as switches

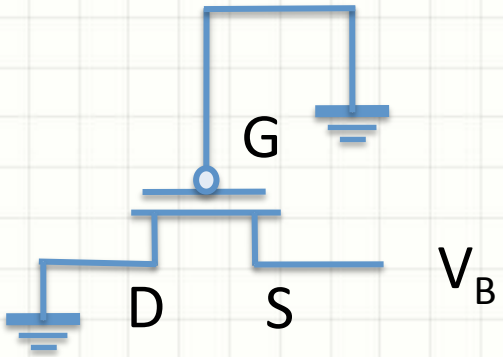




Passing 1's through NMOS switch
Passing 0's through PMOS switch

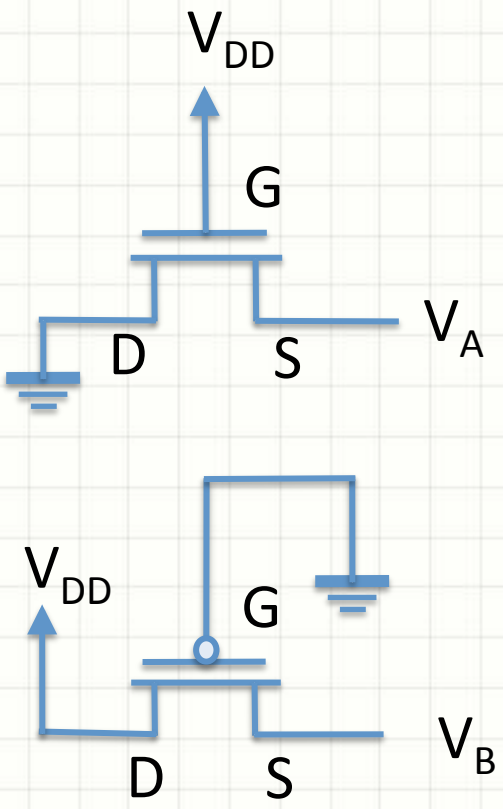


$V_{GS} = V_{DD} - V_A$
Transistor cuts off if
V_A rises above $V_{DD} - V_T$



$V_{GS} = 0 - V_B$
Transistor cuts off if
V_B falls below V_T

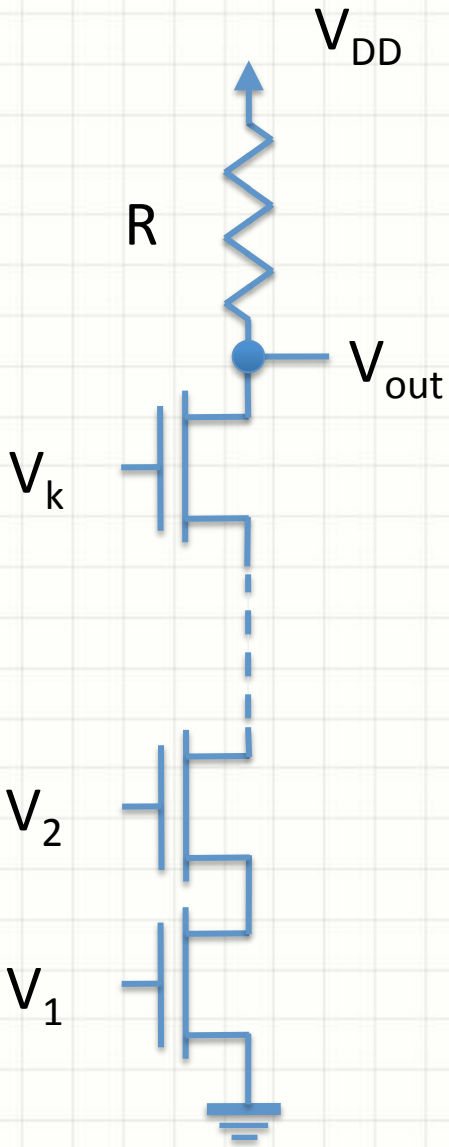
Passing 0's through NMOS switch
Passing 1's through PMOS switch



Transistor remains ON
V_A is 0

Transistor remains ON
V_B equals V_{DD}

Fan-in limitation



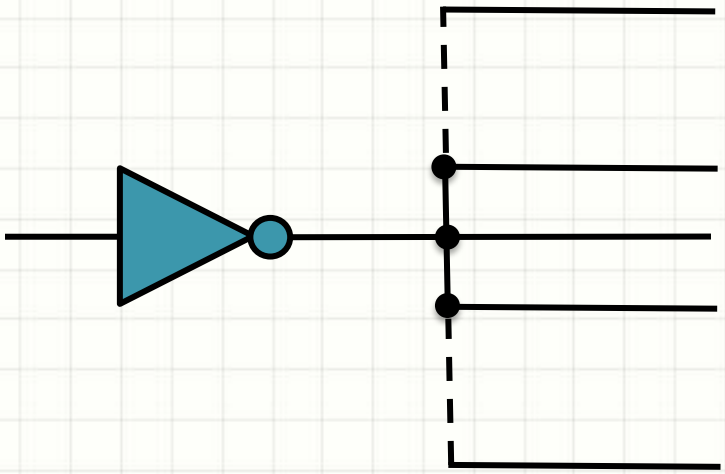
Effective channel length = k . L

$\Rightarrow$ increased delay
increased V_{OL}

This llimits the fan-in

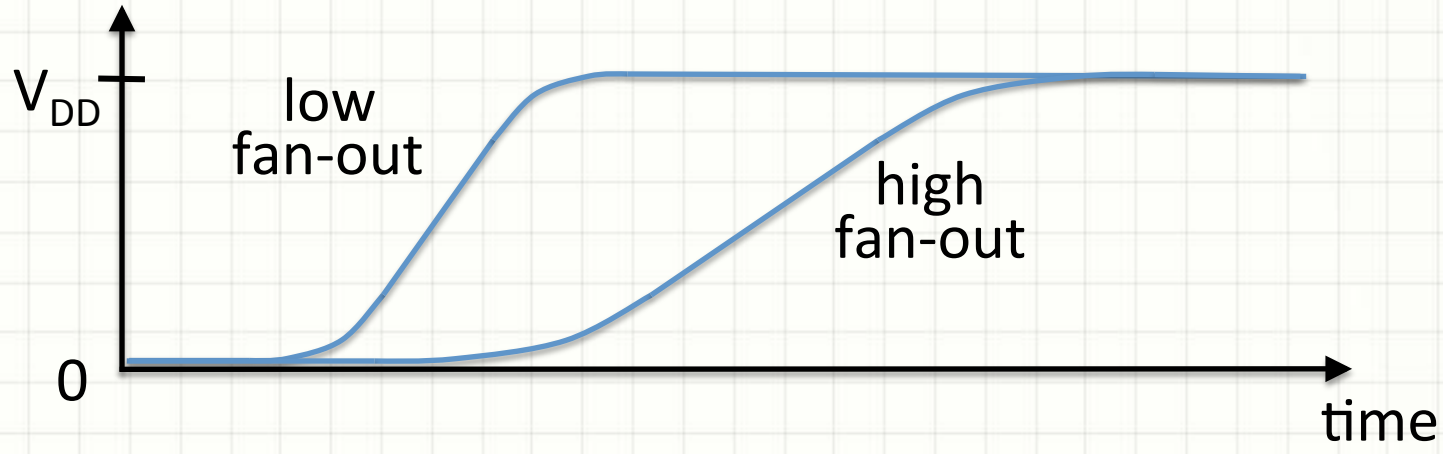
Higher fan-in in CMOS

Fan-out limitation



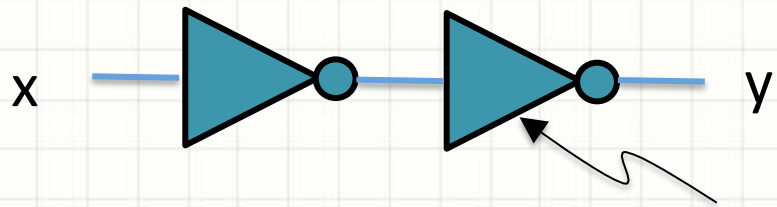
Increased load capacitance

⇒ increased delay
slower rise / fall

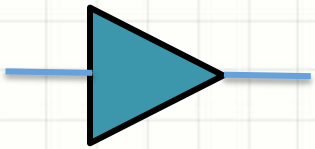


Simple buffer

y = x



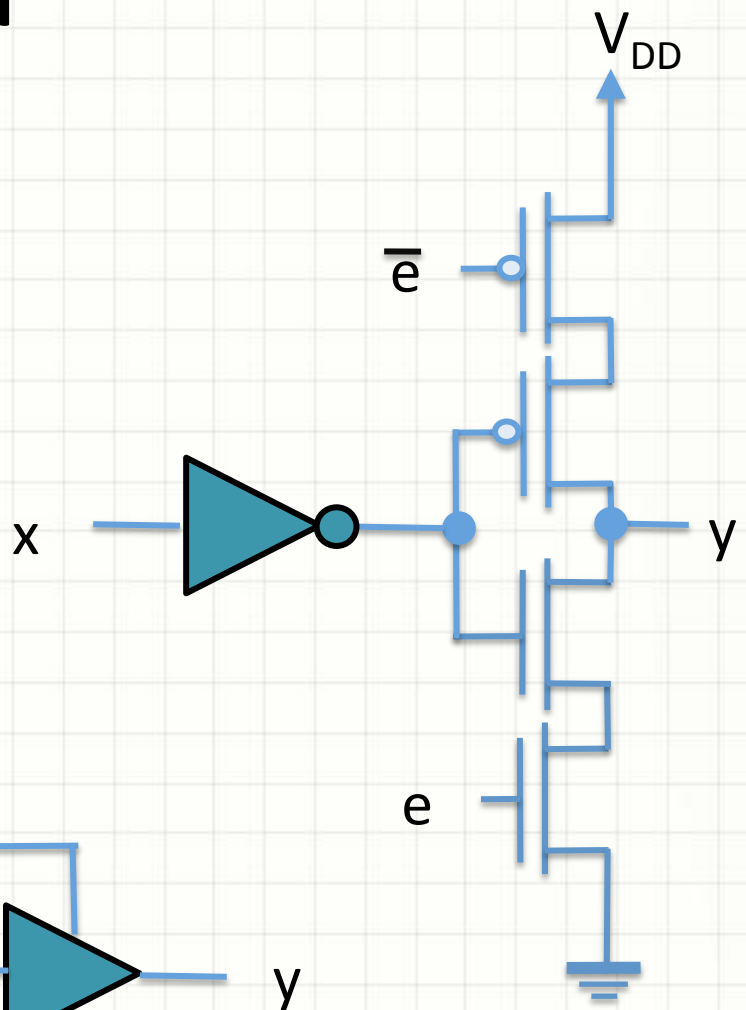
designed to drive large loads



symbol

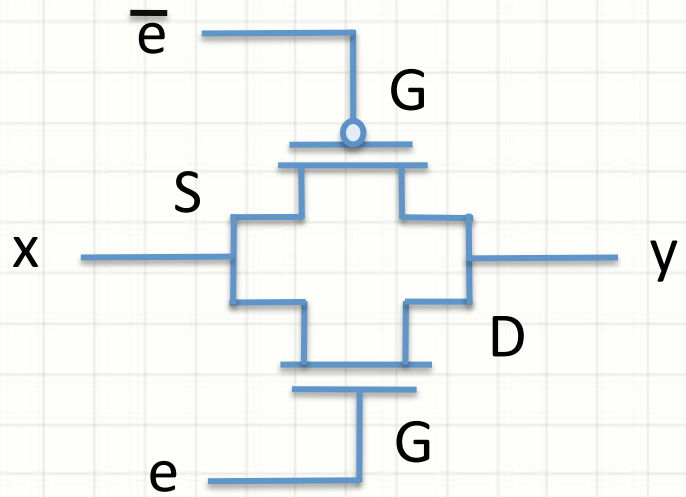
Tri-state buffer

e	x	y
0	0	Z
0	1	Z
1	0	0
1	1	1

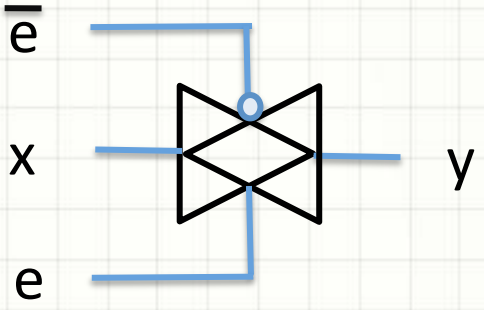


symbol

Transmission Gate

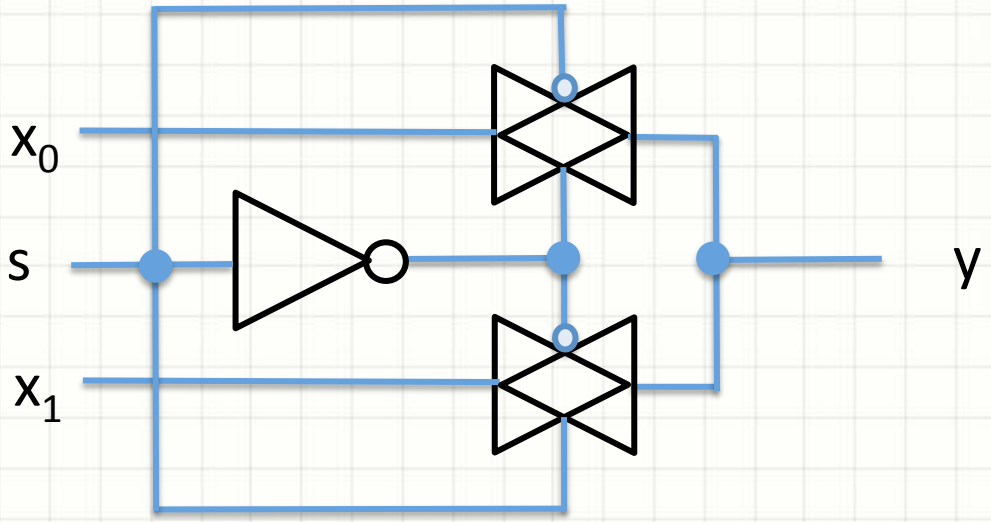


Same truth table as tri-state buffer

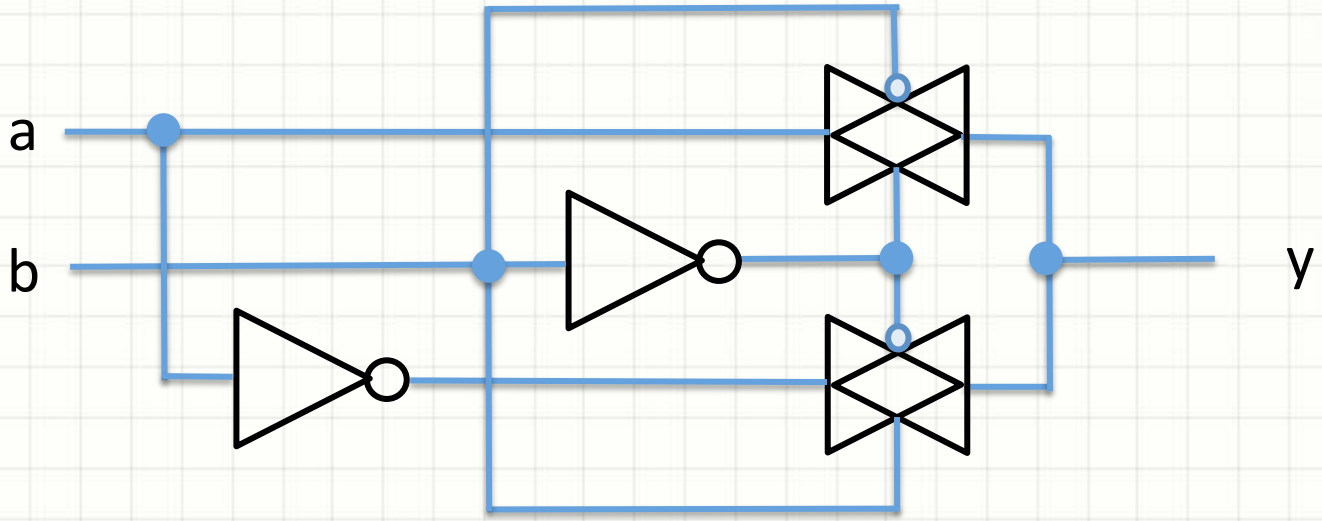


symbol

Multiplexer



Ex-OR Gate



THANKS