COL215 Digital Logic and System Design

Sequential Circuits :

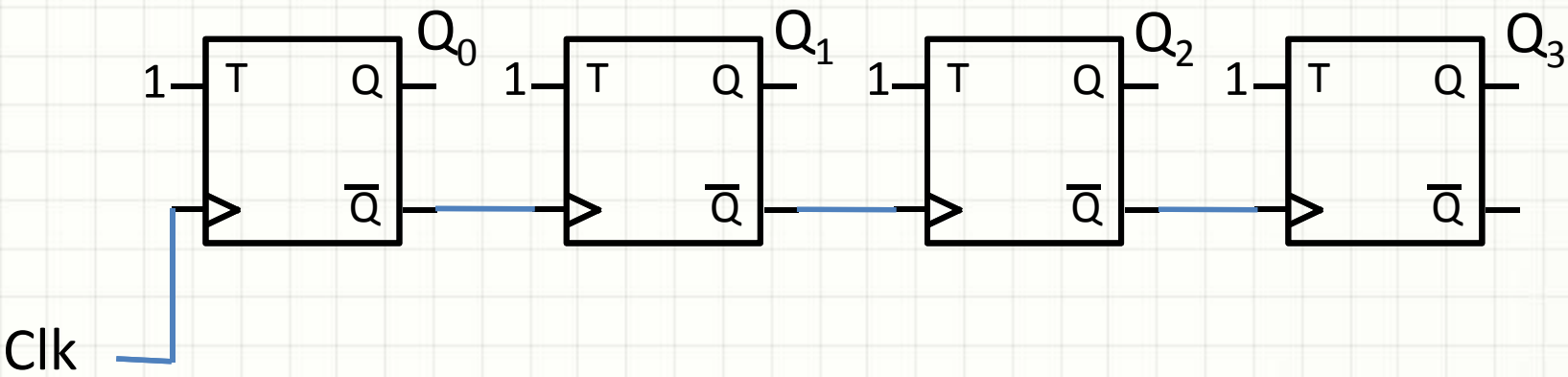
Counters and Timing

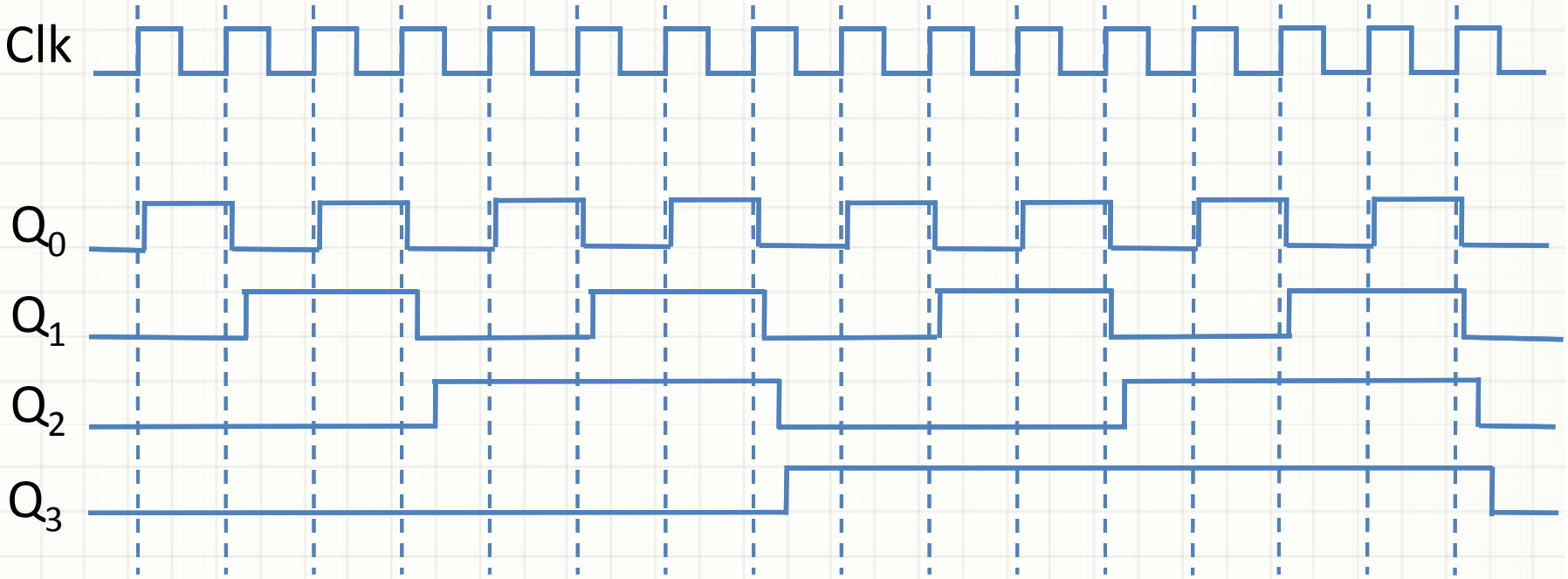
9 August 2017

Binary Counters

0	0 0 0 0
1	0 0 0 1
2	0 0 1 0
3	0 0 1 1
4	0 1 0 0
5	0 1 0 1
6	0 1 1 0
7	0 1 1 1
8	1 0 0 0
9	1 0 0 1
10	1 0 1 0
11	1 0 1 1
12	1 1 0 0
13	1 1 0 1
14	1 1 1 0
15	1 1 1 1

Asynchronous Counter





Asynchronous Counter

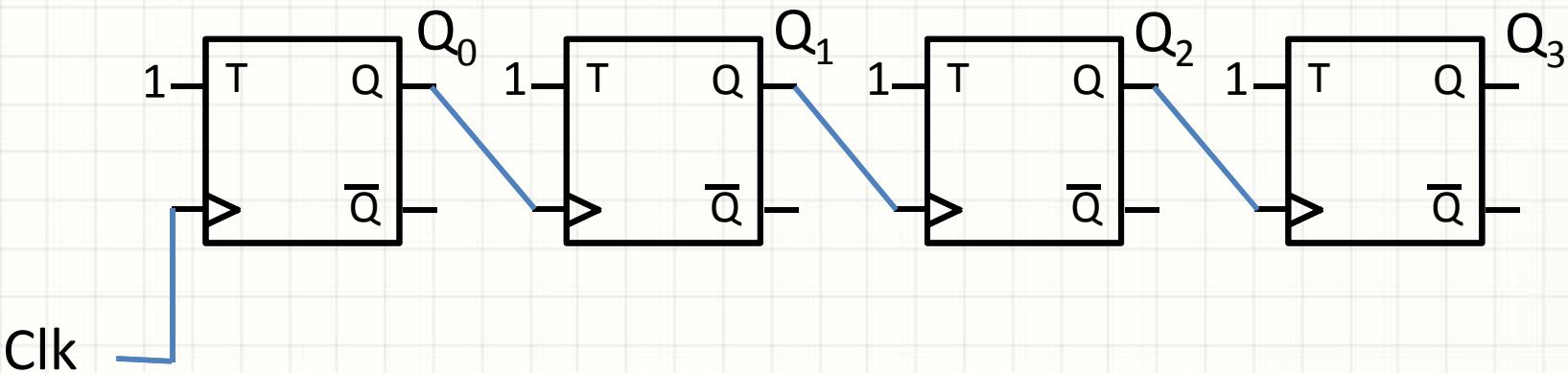
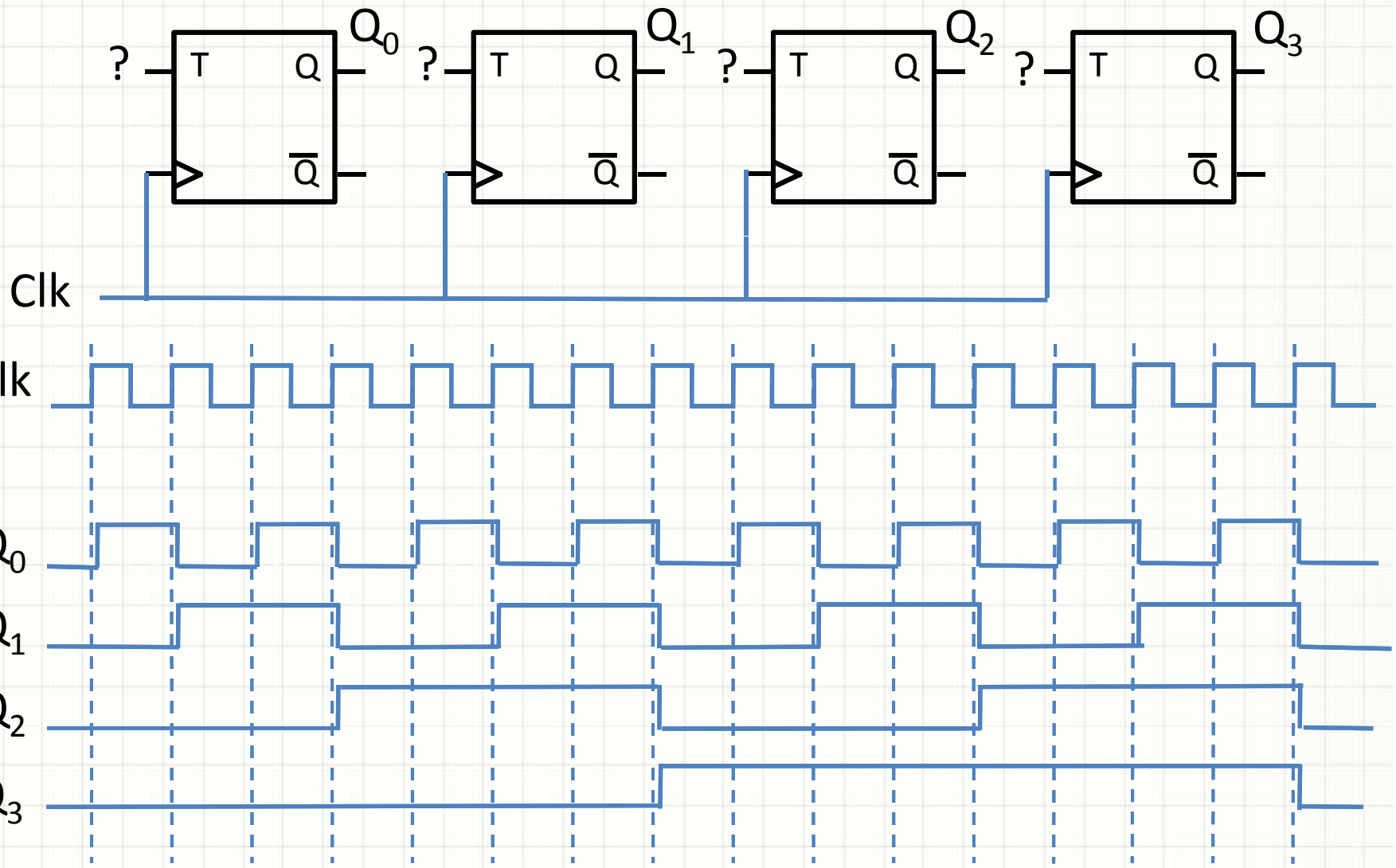


Figure out what this circuit does

Synchronous Counter



Synchronous Counter

- $T_0 = 1$
- $T_1 = Q_0$
- $T_2 = Q_0 \cdot Q_1$
- $T_3 = Q_0 \cdot Q_1 \cdot Q_2$
- . . .
- $T_{i+1} = T_i \cdot Q_i$

Modulo-n Synchronous Counter

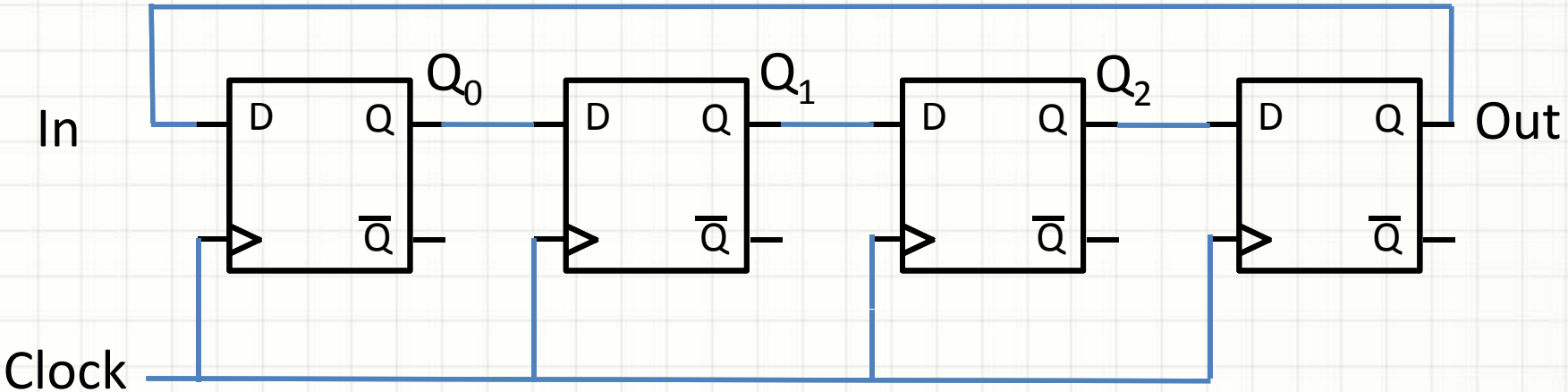
As an example, let n = 13

After 12 (1100), the count should go to 0 (0000)

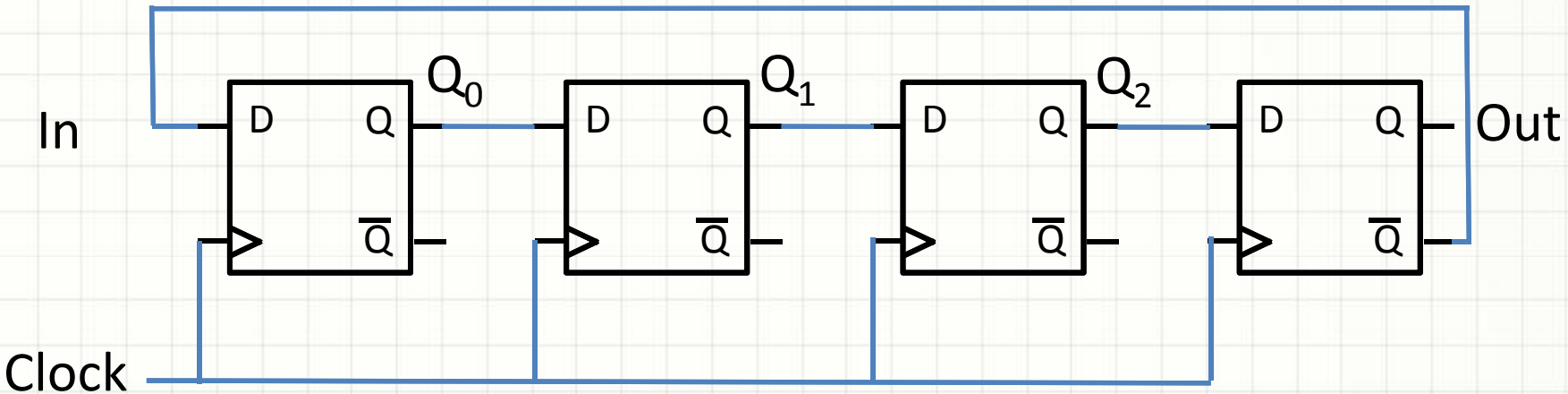
Signal $EoC = Q_3 . Q_2 . Q'_1 . Q'_0$

- $T_0 = 1 . EoC'$
- $T_1 = Q_0 . EoC'$
- $T_2 = Q_0 . Q_1 + EoC$
- $T_3 = Q_0 . Q_1 . Q_2 + EoC$

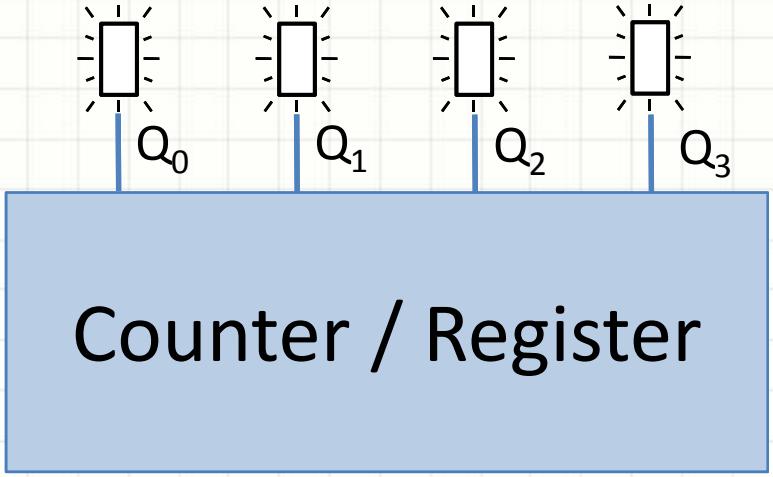
Ring Counter



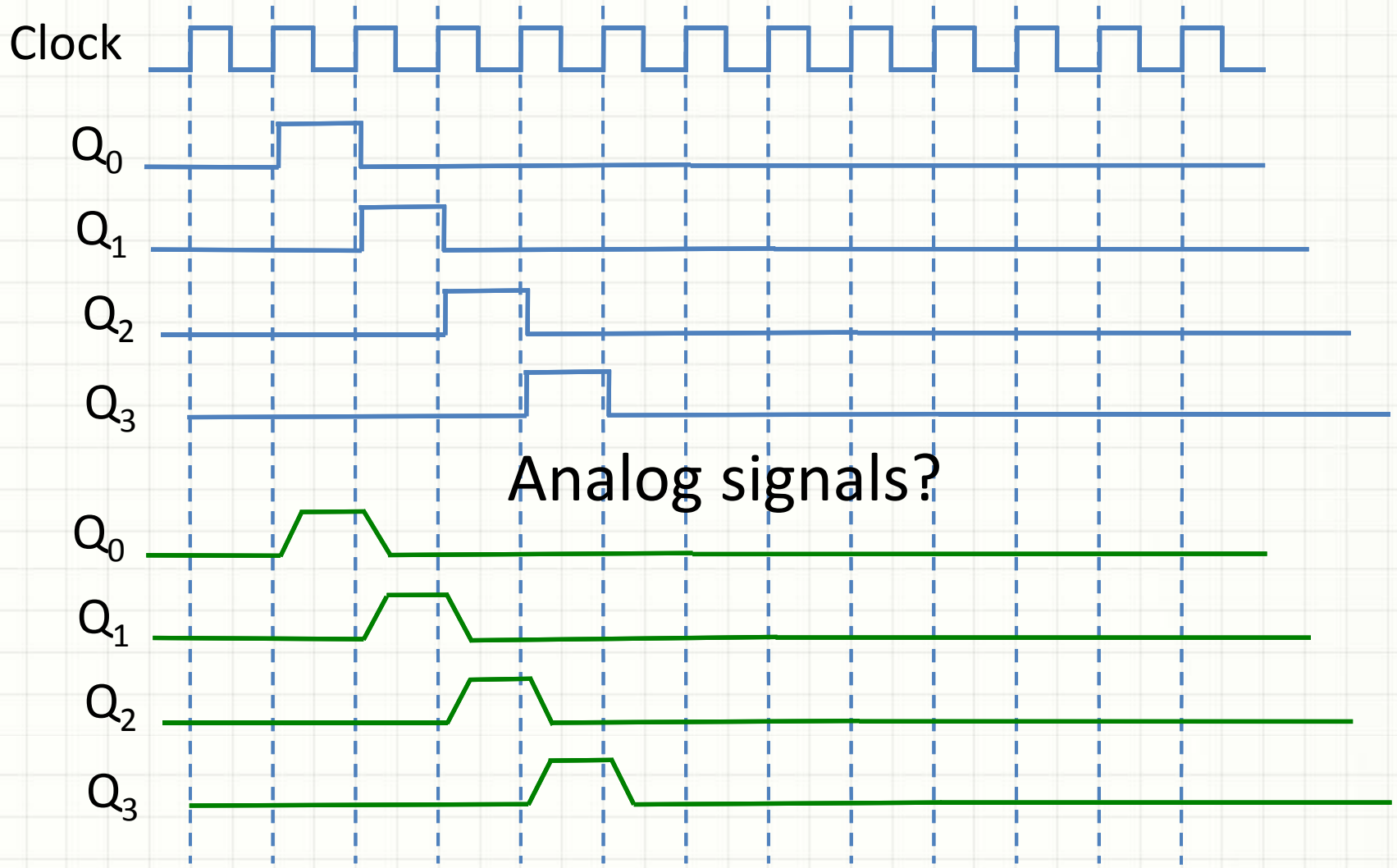
Johnson Counter



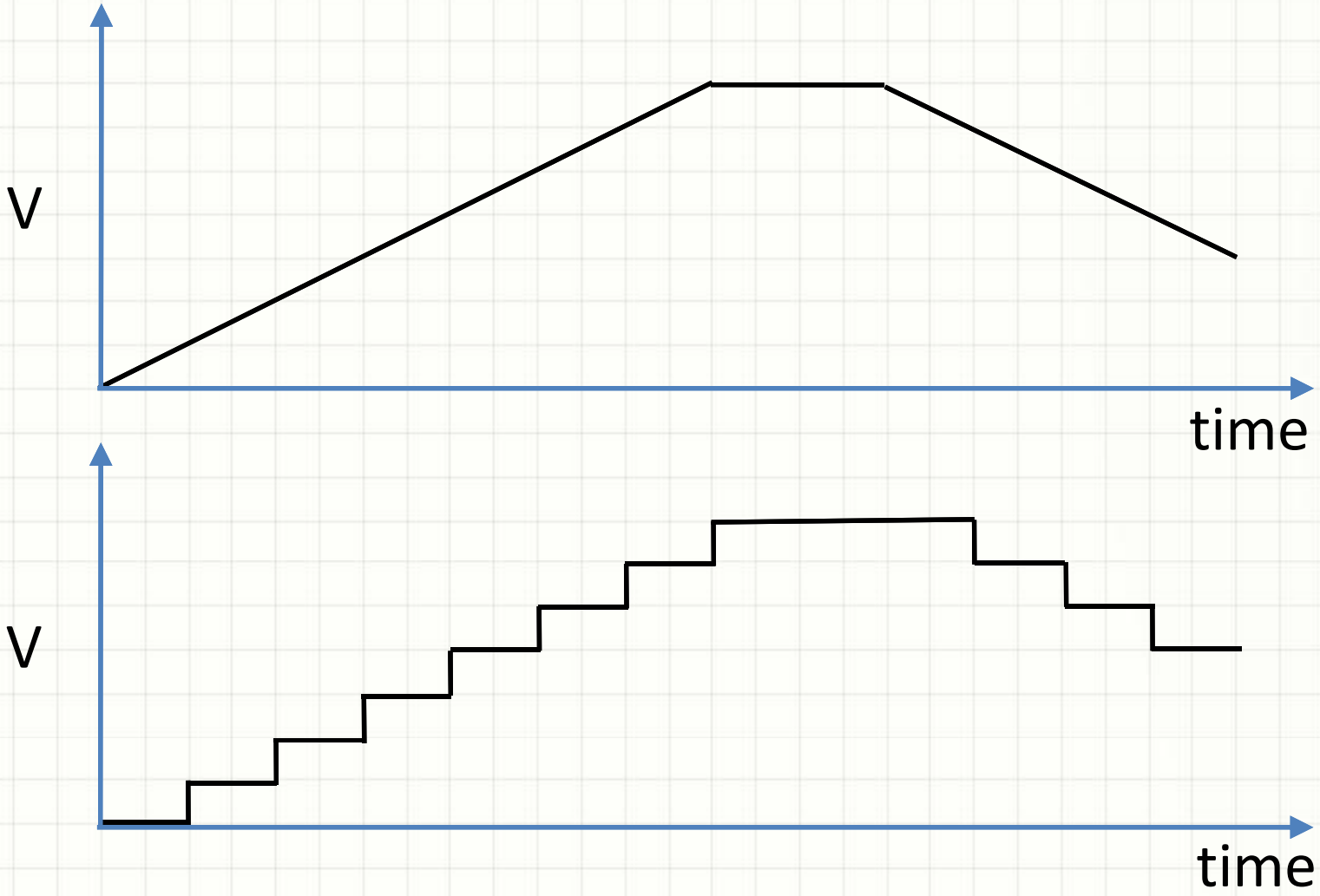
Displaying counter / register contents



Sharp and smooth transitions

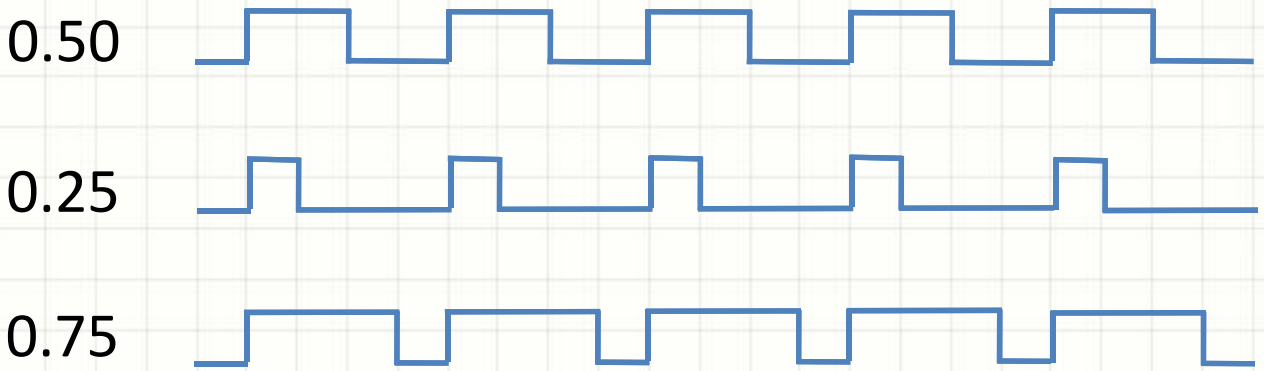


Continuous and discrete levels



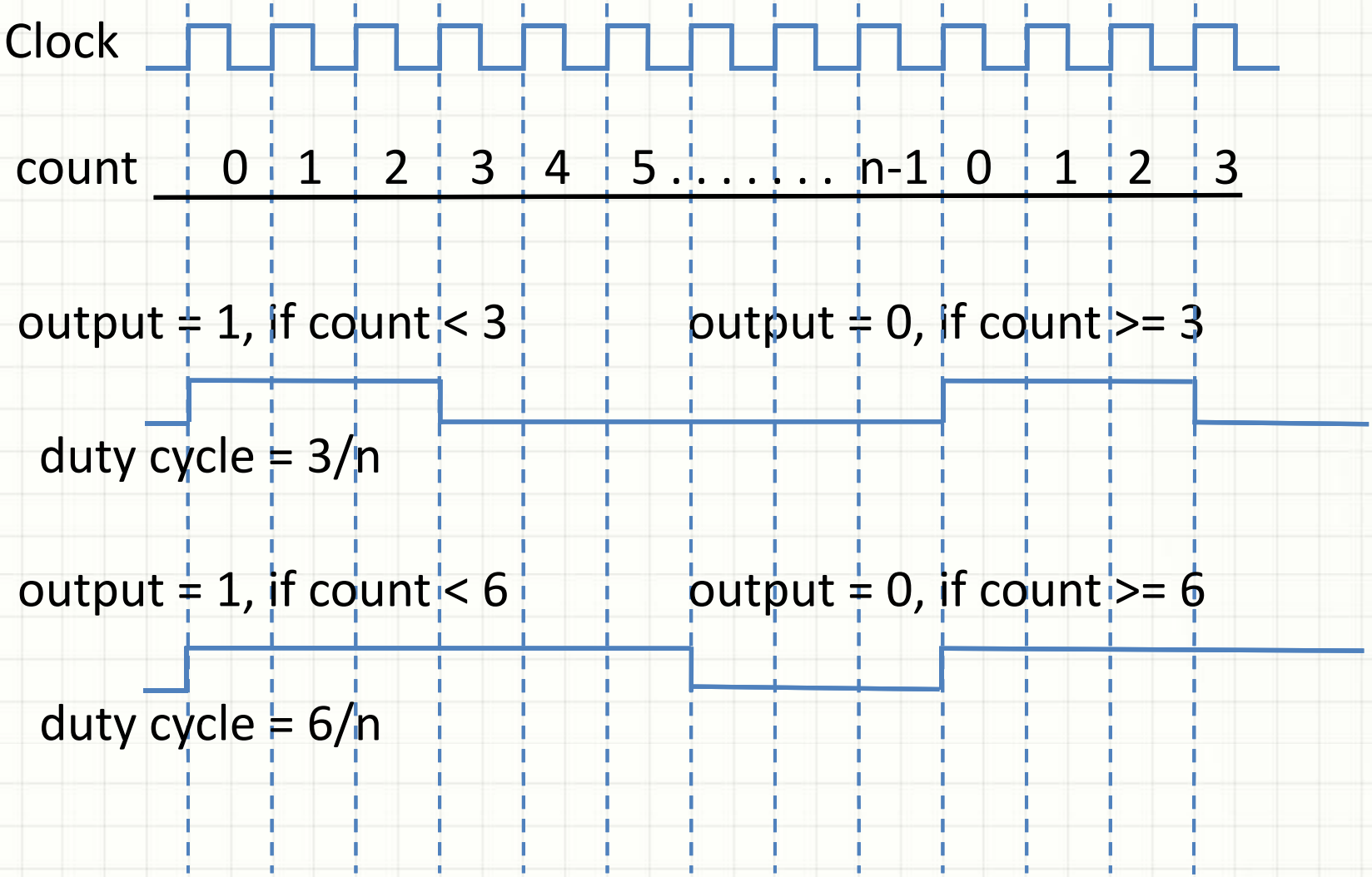
Brightness level and Duty cycle

duty cycle =
fraction of the time for which signal is 1
=> brightness level

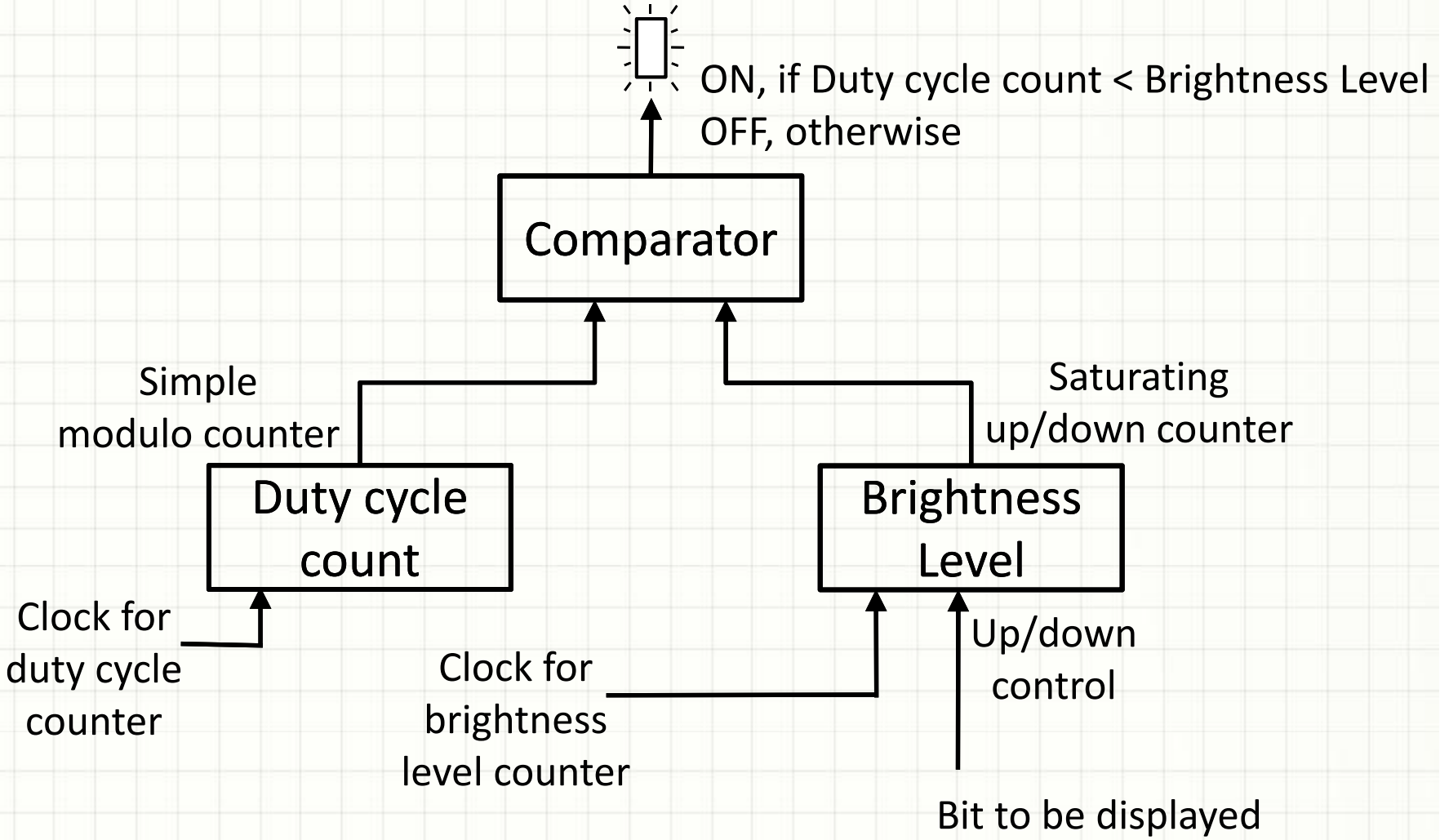


for persistence of vision
frequency >= 25 Hz

Generating signal with given duty cycle



Signal to drive LED



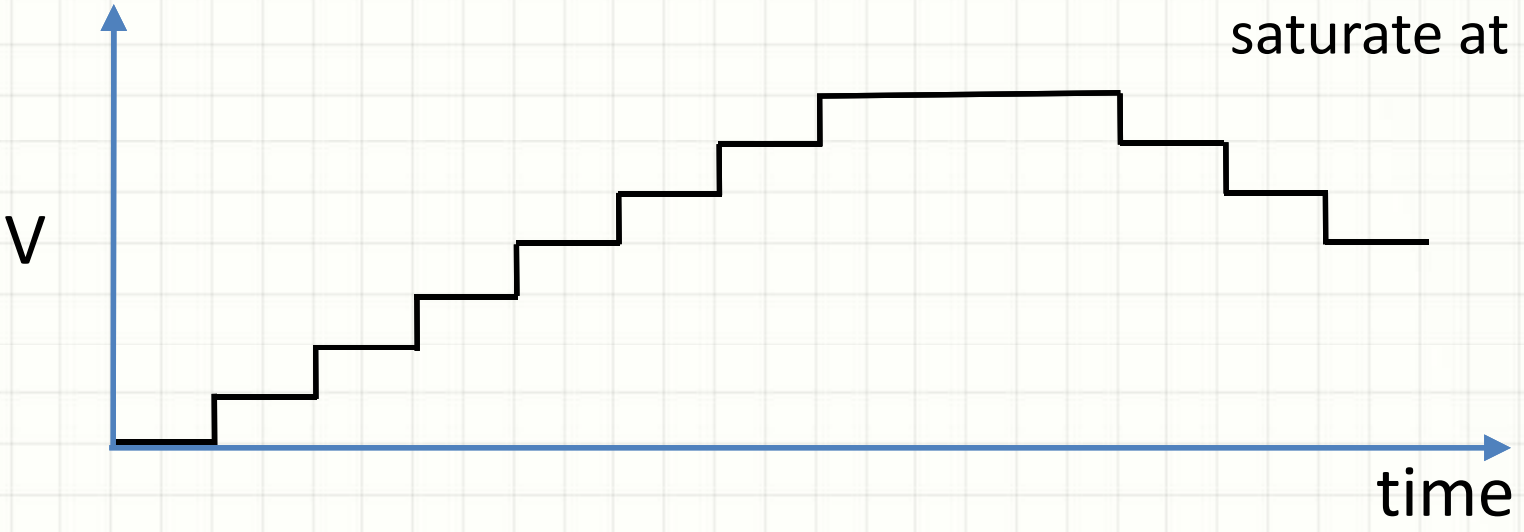
Brightness Level

Brightness Level

Saturating up/down counter

count up 0 to n-1, saturate at n-1

count down n-1 to 0, saturate at 0



Saturating up/down counter

0 0 0 0
0 0 0 1
0 0 1 0
0 0 1 1
0 1 0 0
0 1 0 1
0 1 1 0
0 1 1 1
1 0 0 0
1 0 0 1
1 0 1 0
1 0 1 1
1 1 0 0
1 1 0 1
1 1 1 0
1 1 1 1

$max = Q_0.Q_1. .Q_{k-1}$

$min = \overline{Q}_0.\overline{Q}_1. .\overline{Q}_{k-1}$

Count up (x=1):

- $T_0 = 1$
- $T_{i+1} = T_i . Q_i$

Saturation:

- $T_0 = \overline{max}$
- $T_{i+1} = T_i . Q_i$

Count down (x=0):

- $T_0 = 1$
- $T_{i+1} = T_i . \overline{Q}_i$

Saturation:

- $T_0 = \overline{min}$
- $T_{i+1} = T_i . \overline{Q}_i$

- $T_0 = x . \overline{max} + \overline{x} . \overline{min}$
- $T_{i+1} = T_i . (x . Q_i + \overline{x} . \overline{Q}_i)$

What we have discussed so far

Text book: "Fundamentals of Digital Logic with VHDL Design" by S Brown and Z Vranesic.

Chapter 1: Design Concepts

Chapter 2: Introduction to Logic (2.1 to 2.9)

Chapter 4: Optimized Implementation . . . (4.1 to 4.3)

Chapter 6: Combinational Circuit Building . . . (6.1 to 6.3)

Chapter 7: Flip-flops, Registers . . . (7.1 to 7.11)

THANKS