Course coverage chapter-wise

Chapter	Topics	Sections to read	Relevant Exercises
1	Introduction	all	
2	Combinational circuits • Basic gates, Boolean Algebra • Proving Boolean identities, functionally complete sets of gates, PoS, SoP, canonical forms • VHDL - introduction	all	2.1 - 2.3, 2.7 - 2.15, 2.20 - 2.47, 2.50 - 2.52
3	Transistor circuits • NMOS/PMOS/CMOS gates, transistor characteristics, voltage levels, noise margins, delays, power, fan-in, fan-out, tri-state buffer, transmission gate Programmable modules • Programmable logic and universal logic modules (ULMs), multiplexers as ULMs, Shannon's expansion, look-up tables as ULMs, PLAs, PALs, CPLDs, FPGAs, Various programmable structures, mask programmable gate arrays, field programming techniques, floating gate transistor, SRAM and DRAM cells	3.1 - 3.10	3.1 - 3.13, 3.25 - 3.28, 3.36 - 3.55
4	Logic minimization • Karnaugh maps and their use for logic minimization • Tabular method for logic minimization	4.1 - 4.5, 4.8 - 4.9	all
5	Number representation and arithmetic circuits • Representing unsigned and signed numbers, radix conversion, BCD • Operations and circuit design for binary addition, subtraction, comparison, shift • Overflow detection, addition speed up using carry look ahead • Array multipliers with carry propagate andcarry save adders	5.1 - 5.6, 5.7.3, 5.9	all
6	Combinational modules • Common modules - multiplexers, de-multiplexers, decoder, encoder, priority encoder • VHDL - concurrent and sequential assignments	all	6.1 - 6.15, 6.18 - 6.37
7	Sequential Circuits • Simple storage element, SR and D latches, Edge triggered flip-flops, Registers and counters • VHDL - sequential circuits	7.1 - 7.14.1, 7.15 - 7.16	7.1 - 7.11, 7.13 - 7.31, 7.33 - 7.40
8	Synchronous sequential circuits • State transition diagrams, state transition tables, circuit structure, state representation, implementation with different types of flip-flops, VHDL representation • FSM model, state equivalence, equivalence partitioning, state compatibility in incompletely specified FSMs • Algorithmic state machine (ASM) charts	all	all
9	Asynchronous sequential circuits • Analyzing asynchronous sequential circuits by building excitation tables and flow tables • Synthesizing asynchronous circuits from flow tables and excitation tables • Static and dynamic hazards, state assignment and races	all	9.1 - 9.14, 9.16 - 9.22
10	System design • Datapath - controller partition, building blocks • Design examples • Clock skew, flip-flop/register set up and hold times, datapath delays and clock period, meta-stability, switch de-bouncing	all	10.1 - 10.9, 10.12 - 10.23

11	Testing • Testing problem, fault models, fault coverage • Boolean differences, path sensitization, D-algorithm • ATPG, DFT, BIST	11.1 - 11.7	11.1 - 11.14
FPGA literature	Spartan-6 FPGA configurable logic block user guide: Configurable logic block in Spartan 6 FPGA, types of slices, resources in a slice (look-up tables, flip-flops, multiplexers, fast carry chain)	Pages 7-16, 31-35, 40,42	
	Block memory generator product guide: Overview, memory type, selectable memory algorithm, operating modes	Pages 5,7,9, 39-47	
	Spartan-6 FPGA DSP48A1 slice user guide: DSP48A1 in Spartan 6 FPGA, using DSP48A1 for weighted sum, pipelining options	Pages 5-8, 14-19, 23-27	
	Basys 3 FPGA board reference manual: Overview, VGA port, Basic I/O	Pa,ges 1,2, 10-17	