Semiconductor Manufacturing International Corporation

Doc. No.: TD-MM18-SP-2004	Doc. Title: 0.18um Mixed Signal Enhanced 1.8V/3.3V SPICE Model	Doc.Rev: 2	Tech Dev Rev: 1.11	Page No.: 0/90

Document Level: (For Engineering & Quality Document/工程暨品质文件专用)

☐ Level 1 - Manual ☑ Level 2 – Procedure/SPEC/Report ☐ Level 3 - Operation Instruction

Security Level:

☐ Security 1 - SMIC Confidential ☑ Security 2 - SMIC Restricted ☐ Security 3 - SMIC Internal

Document Change History

Doc. Rev.	Tech Dev. Rev.	Effective Date	Author	Change Description
0R	1.0	2015-04-17	Claude Zhang	Initiate
1	1.10	2015-11-09	Sifeng Wu	1. Change the version number of Title from Version 1.0 to Version 1.10. Change the model file names in this document from v1p0 to v1p10 in section 7.5 & 8.1. 2. Update the N18/P18/NNT33 fix corner parameters in section 7.2.4 of 'Table 7.2.3' and 'Table 7.2.4'. 3. Update the N18/P18/NNT33/NMVT33 PCM compare result in section 7.2.5 of 'Table 7.2.7', 'Table 7.2.8' and 'Table 7.2.9'. 4. Update the corner case R.O. simulation result in section 7.2.6 of 'Table 7.2.10~7.2.18'. 5. Update the LOD parameters of N18/P18 in section 7.2.8 of 'Table 7.2.22'. 6. Update resistor parameters in section 7.6.3 and section 7.6.4 of 'Table 7.6.3' and 'Table 7.6.5'. 7. Modify item 8.1: 1) Retarget n18 and p18 MOS and re-extract LOD effect model. Retarget nmvt33 MOS model. Retarget nnt33 MOS corner model. Re-extract p33 and pmvt18 MOS cjgate parameters. Set all MOS devices WPEMOD=0 to turn off WPE effect. Update model parameters in 'ms018_enhanced_v1p10.mdl' and 'ms018_enhanced_v1p10_mis.mdl'. 2) Retarget n+ poly silicide, p+ poly silicide, p+ poly sab, nwell AA resistor model. Update parameters in 'ms018_enhanced_v1p10_res.mdl' and 'ms018_enhanced_v1p10_res.ckt'. 3) Modify mim default wr lr value and mismatch random variable in 'ms018_enhanced_v1p10_mim.ckt' and 'ms018_enhanced_v1p10_mim_spe.ckt'. 4) Update npn18a100_mis_ckt model, and update the related file in hspice/bjt/npn18a100.mdl. 8. Update 1.8V/3.3V native NMOS Wmin from 0.22um to 0.42um to follow DR, and update in section 7.2.2.

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2	1.11	2016-10-14	Sifeng Wu	1. Update the version from v1.10 to v1.11 in title and section 7.5.2/7.6.4/8 in main document. 2. Deleted 3K HRP resistor related models for PIE request in attachment "ms018_enhanced_v1p11_res.ckt", "ms018_enhanced_v1p11_res.mdl", "ms018_enhanced_v1p11_res_spe.ckt", "ms018_enhanced_v1p11_res_spe.mdl","ms018_fit_G.pdf" and "ms018_fit_D.pdf", and updated in section 7.6.1/7.6.2/7.6.3/7.6.4/7.9 in main document. 3. Modified 'l=lr w=wr' to 'l=10e-6 w=1e-6' for resistor in "ms018_enhanced_v1p11_res.ckt" and "ms018_enhanced_v1p11_res_spe.ckt". 4. Deleted doubld defined parameter "+sigma_mis_res=agauss(0,1,1)" for resistor in "ms018_enhanced_v1p11_res.ckt" and "ms018_enhanced_v1p11_res_spe.ckt".. 5. Updated SPECTRE diode parameter tcv to match HSPICE simualton result in "ms018_enhanced_v1p11_dio_spe.mdl". 6. Updated gate current to match HSPICE in "gc.va" file. 7. Updated 'rbm' in all npn BJT devices to avoid warning in bjt folder. 8. Updated nmvt18 model to avoid acde parameter warning in "ms018_enhanced_v1p11.mdl", "ms018_enhanced_v1p11_mis.mdl", "ms018_enhanced_v1p11_spe.mdl" and "ms018_enhanced_v1p11_mis_spe.mdl". 9. Updated mismatch for mim_ckt in SPECTRE to match HSPICE in "ms018_enhanced_v1p11_mim_spe.ckt". 10. Updated “ASCII.7z” zip file name to “SMIC_SP_model_018MSE_1833.tar.gz” for new naming rule, and update in section 8.1 11. Align attached document format to pdf with ECN, and updated in section 8.3. 12. Update document title to "0.18um Mixed Signal Enhanced 1.8V/3.3V SPICE Model" for new naming rule. 13. Updated attachment “GDS.7z” zip file name to “SMIC_SP_GDS_018MSE_1833.tar.gz” for new naming rule. 14. Updated attachment name for new naming rule , from “ms018_fit_A.pdf/ms018_fit_B1.pdf/ms018_fit_B2.pdf/ms018_fit_C.pdf/ms018_fit_D.pdf/ms018_fit_F.pdf/ms018_fit_G.pdf” to “SMIC_SP_fit_A_018MSE_1833.pdf/SMIC_SP_fit_B1_018MSE_1833.pdf/SMIC_SP_fit_B2_018MSE_1833.pdf/SMIC_SP_fit_C_018MSE_1833.pdf/SMIC_SP_fit_D_018MSE_1833.pdf/SMIC_SP_fit_F_018MSE_1833.pdf/SMIC_SP_fit_G_018MSE_1833.pdf”

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1. Title:

   0.18um Mixed Signal Enhanced 1.8V/3.3V SPICE Model

2. Purpose:

   To provide SPICE model for circuit designers who use SMIC 0.18um Mixed Signal 1.8V/3.3V process.

3. Scope:

   This document describes detailed information about devices modeling, covering MOSFETs Model (wafer information, model capability, fixed corner model table, 1/f noise model, LOD Stress Effect Model,), as well as wafer information, model capability and fixed corner model table of Bipolar Gummel-Poon Model, Diode Model, Interconnection Model, Resistor Model, MOS Varactor Model, and MIM Capacitor Model.

4. Nomenclature:

   1P6M: Single Poly Sextuple Metal

5. Reference:

   TD-LO18-DR-2001 0.18um Logic & Mix-signal 1.8V/3.3V Design Rule
   TD-MM18-PC-2004 0.18um Logic/Mixed Signal & RF 1P6M Salicide 1.8V/3.3V Enhanced WAT PCM SPEC

6. Responsibility:

   It is the responsibility of Technology R&D/Tech-Bas Des-Enb division to generate and release SPICE models for internal and external customers

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7. Subject Content:

7.1 Model Overview

7.1.1 SPICE Model Introduction

SPICE (simulation program with integrated circuit emphasis) is a transistor-level simulator developed by experts from UC Berkeley, which is a public domain software specially designed for integrated circuit (IC) applications. The circuit simulators for SPICE include public domain ones (e.g. SPICE1, SPICE2 and SPICE3, etc, all from UC Berkeley) and commercial ones, such as HSPICE from Synopsys used by 90% fables design houses, SPECTRE from Cadence for RF and IDM design, ELDO from Mentor Graphics widely used in Europe, Smart-SPICE from Silvaco mainly applied by small design houses and board level PSPICE. Additionally, there're also some proprietary SPICE simulators developed by MCSPICE, TISPICE, IBM, Intel, and more.

The SPICE model is defined as a set of parameters describing devices' electrical characteristics for SPICE simulation, almost covering all device models, such as models of MOSFETs, diodes, BJTs, JFETs, MESFETs, and as well the passive device (resistors, capacitors and inductors)models. It's actually a set of sophisticated equations that correctly reproduce the exact transistor characteristics for SPICE simulation, which is not only a mathematical model of a prototype transistor, but also provides series of accurate models to simulate many real device effects of the modern transistor.

For SPICE modeling, a complete set of electrical parameters of arbitrary device dimensions is extracted from a set of relevant data, such as physical parameters, electrical parameters, technology specific data and process data. By this, each value of the required model parameters can be regarded as a function of the aforementioned data, describing its dependence on the operating conditions, temperature environments, electrical data (e.g. capacitance, sheet resistance) and also technology data (layout design rules).

It's too difficult to directly analyze numerous in-line test data, and then the SPICE model allows us to leverage the large volumes of measured data and provides a statistical modeling for circuit designers to simulate realistic integrated circuits.

7.1.2 SMIC's SPICE Model Introduction

The simplified steps of SPICE modeling would be wafer preparation (including data measurement) and model parameter extraction. Wafer preparation is to select a golden wafer and its golden die by comparing the WAT data with the PCM specification to make sure the wafer is suitable for model extraction. The extracted parameters for different devices are all listed in their relative sections. We modeled MOSFET, BJT, diode, resistor, MOS varactor and MIM, and their modeling methods and results would be discussed in this document.

SMIC applies the commercial BSIMProPlus model extraction tool to derive parameters of MOSFET, BJT, diode, MOS varactor and MIM, as well adopts MBP(Model Building Program) for model extraction of resistor. The extracted models are compatible with HSPICE (Synopsys) and SPECTRE (Cadence) formats. If the circuit designers need to use simulators other than the two above mentioned types, please contact SMIC to convert the format to meet your specified input requirement. All the model files are given in the attachment.

The naming of SMIC model version follows the following rule: Version 0.X (Under Development); Version 1.X (Process frozen); Furthermore, the tech. version would be changed if the model card has been modified and the modification affects device characteristics and performances, however if just some errors about document or model parameters are corrected, which would not influence any device characteristics, we would just update the document version only.

7.2 MOSFET Model

7.2.1 Wafer Information

The transistors for MOSFET SPICE modeling include 1.8V thin oxide Standard Vt NMOS/PMOS, 1.8V thin oxide Medium Vt NMOS/PMO，1.8V thin oxide Native NMOS, 3.3V thick oxide NMOS/PMOS, 3.3V thick oxide medium Vt NMOS, 3.3V thick oxide native NMOS.

The silicon data of the above mentioned components are extracted from different wafers, and each wafer is 8 inches with 26 dies. The data is provided by the Wafer Acceptance Test (WAT) team: determining the golden die whose median value (Idsat, Idlin, Vtlin and Vtsat) almost approximates that of mapping data and then sweeping IV and CV curve to obtain the measured data. The detailed lot and wafer information is shown in Table 7.2.1.

Lot number	Wafer number
DL2291	1.8V MOS: #13
DL1737	1.8V MVT MOS: #5 3.3V MOS: #5 3.3V MVT MOS: #5

Table 7.2.1 Wafer Information for MOSFET Device Simulation

A typical single MOSFET contains active area (AA), poly and contact (CT), as illustrated in Fig7.2.1, green as active area and blue as poly, and it typically has four terminals: Gate, Source, Drain and Bulk.

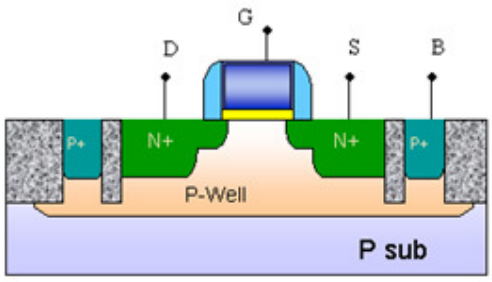

Fig 7.2.1 The cross section of MOSFETs (NMOS)

Idsat and Vth of all types of MOSFETs devices on the modeling wafer are on target or close to the target. The poly CD values on the wafers are smaller than the mask drawing sizes. The on-target Idsat device

sizes are W/L=10/0.18 for 1.8V N&PMOS and N&PMOS in DNW, W/L=10/0.35 for 3.3V NMOS, W/L=10/0.3 for 3.3V PMOS, W/L=10/0.3 for 1.8V MVT NMOS, W/L=10/0.25 for 1.8V MVT PMOS, W/L=10/0.35 for 1.8V native NMOS, W/L=10/0.6 for 3.3V MVT NMOS,W/L=10/1.8 for 3.3V native NMOS. Since not all device parameters on the wafers are exactly on targets, after model parameter extraction, some model parameters are adjusted to make all simulation values on target. The parameters adjusted will be mentioned in subsequent sections.

The geometries for of different types of MOSFETs for measurement and modeling are listed in Fig 7.2.2 to Fig 7.2.9.

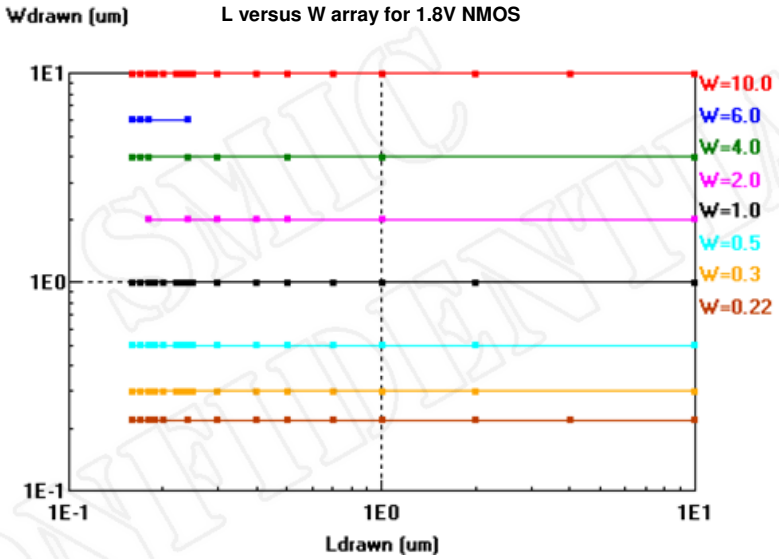

Fig 7.2.2 Device sizes for 1.8V NMOS

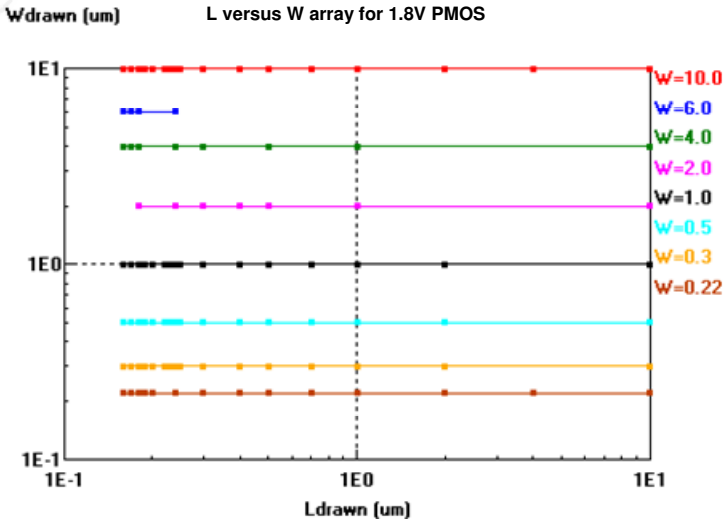

Fig 7.2.3 Device sizes for 1.8V PMOS

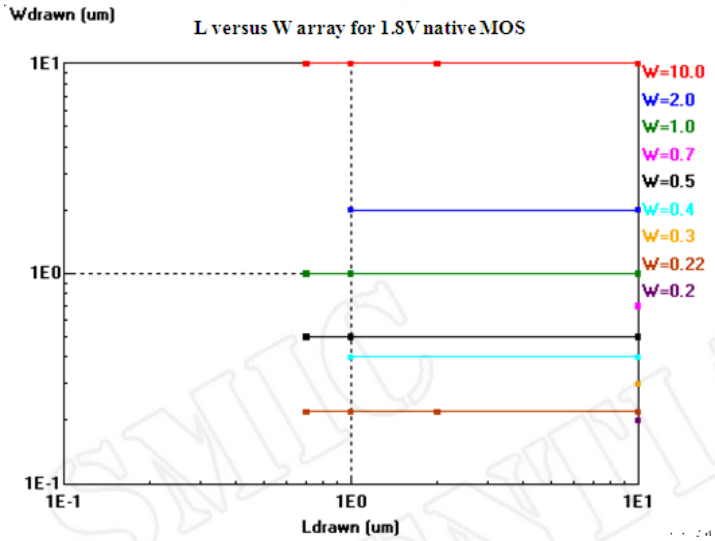

Fig 7.2.4 Device sizes for 1.8V Native NMOS

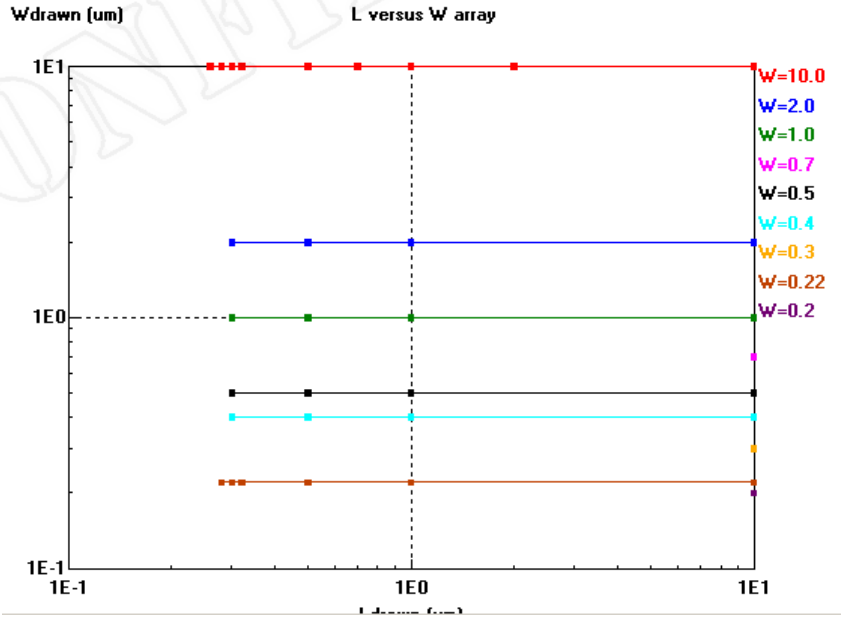

Fig 7.2.5 Device sizes for 1.8V MVT NMOS

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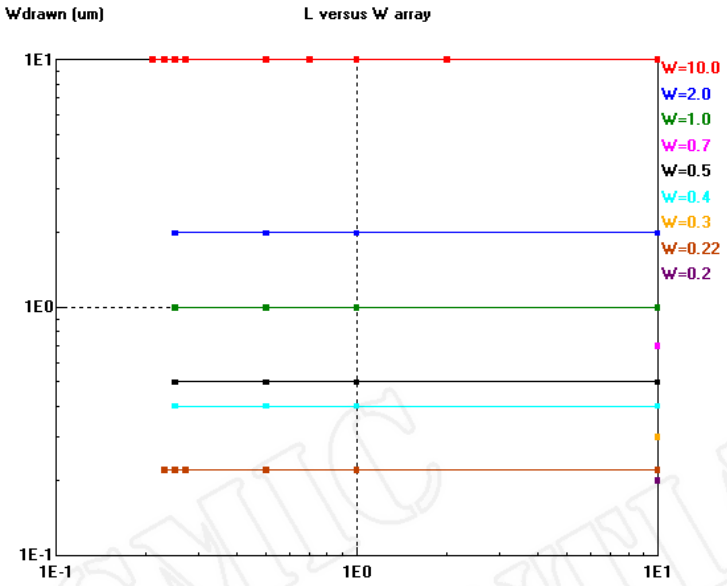

Fig 7.2.6 Device sizes for 1.8V MVT PMOS

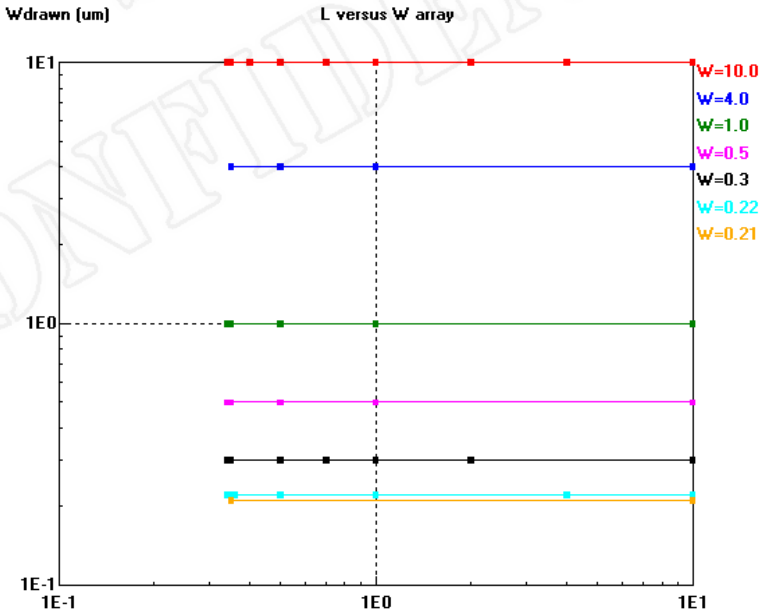

Fig 7.2.7 Device sizes for 3.3V NMOS

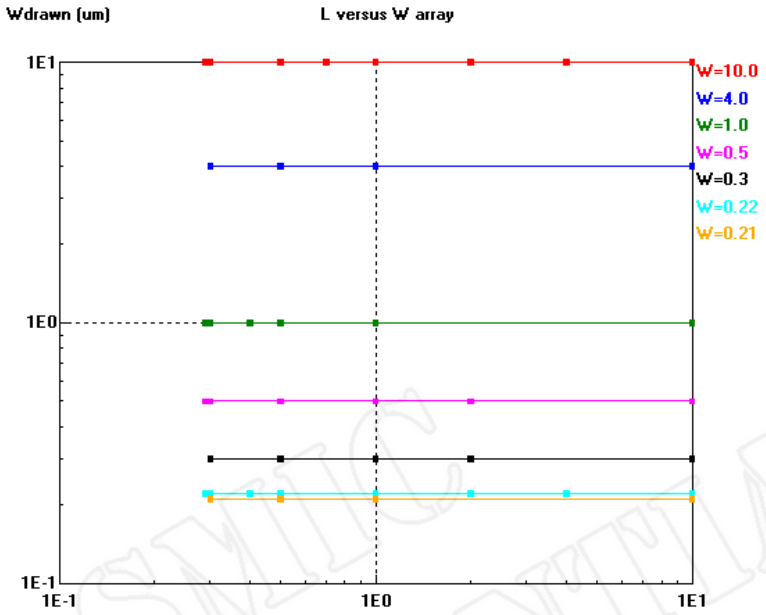

Fig 7.2.8 Device sizes for 3.3V PMOS

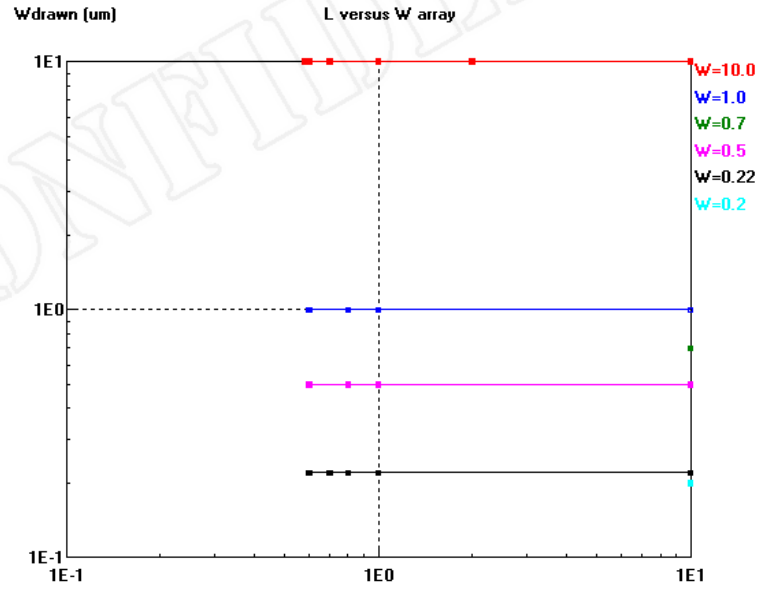

Fig 7.2.9 Device sizes for 3.3V MVT NMOS

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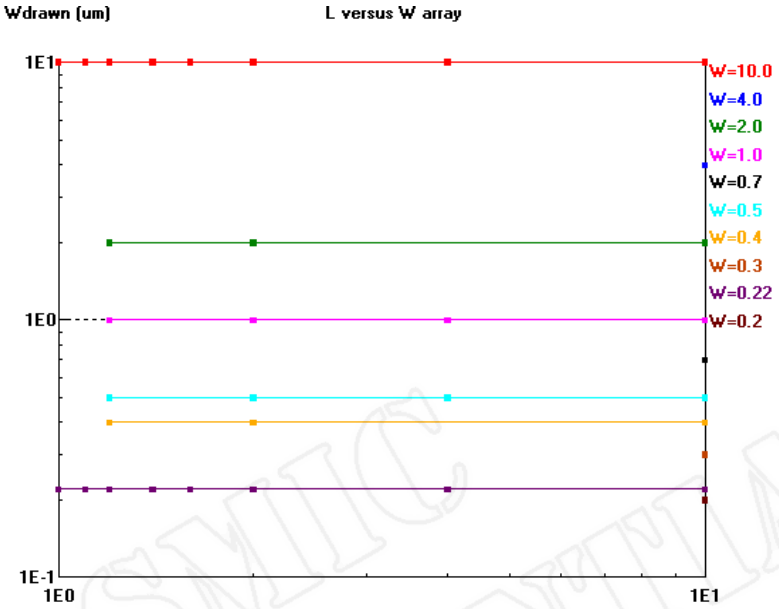


Fig 7.2.10 Device sizes for 3.3V Native NMOS

7.2.2 Capability of Model

The MOSFET modeling in this technology node covers five fixed corner models: TT, FF, SS, FNSP and SNFP ; monte carlo corners: MOS_MC, which would be discussed in detail in the flowing section. Furthermore, the effect models of MOSFET, including 1/f noise model, LOD effect model are all simulated.

According to the industry standard of general devices, for measurement and modeling of MOSFETs, the ambient temperature ranges from -40°C to 125°C. In this version of the technology node, we model the MOSFET devices with BSIM4v4.5 model which is accounting for physical effects in sub-100nm devices. The BSIM model consists of two main components- core model and real device models. The core is a ideal long channel model, which is threshold voltage based [1] [2], while the real device models are being used to simulate the effects in real devices e.g. short channel effect, velocity saturation effect, quantum mechanical effect and more.

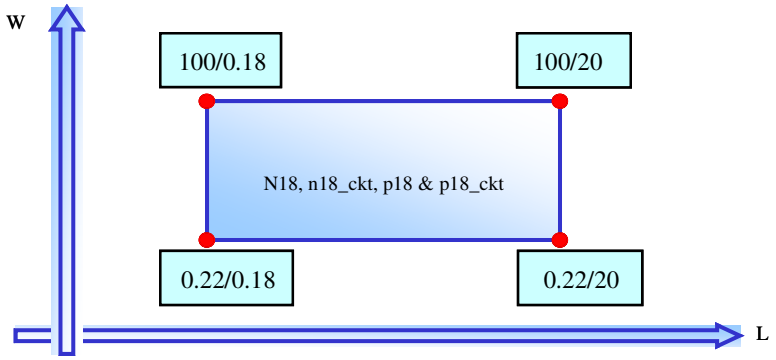
Here in this technology node, our model covers the following effects that would influence MOSFETs' electrical performances: short channel effects, mobility/transport dependent on field/doping/L, output conductance, current saturation, gate current, GIDL current, impact ionization current, 1/f noise model, S/D resistance, fringe capacitance, random variation, WPE, LOD, LDE, temperature effect, self heating, parasitic diode, inversion layer thickness.

The SPICE model can be classified into global model and bin model. The global model means modeling all the geometries of one type of devices via one model, whereas the bin model is to model the same kind of device with several model equations that follow some certain rule. The former one is more physical while the latter one is more accurate but is more challenging to keep the continuity between models. The model used by SMIC is the global model extraction strategy with different geometries measured and modeled. The MOSFETs sizes used for modeling are shown below: The transistor sizes used in the extraction are 0.18um≦length≦20um, 0.22um≦width≦100um for 1.8V thin-oxide and in dnw devices, 0.35um≦length≦20um, 0.22um≦width≦100um for 3.3V NMOS and NMOS in DNW, 0.3um≦length≦20um, 0.22um≦width≦100um for 3.3V PMOS and PMOS in DNW, 1um≦length≦20um, 0.42um≦width≦100um for 1.8V thin-oxide native NMOS, 1.8um≦length≦20um, 0.42um≦width≦100um for 3.3V native NMOS, 0.3um≦length≦20um, 0.22um≦width≦100um for 1.8V thin-oxide MVT NMOS, 0.25um≦length≦20um, 0.22um≦width≦100um for 1.8V thin-oxide MVT PMOS, 0.6um≦length≦20um, 0.22um≦width≦100um for 1.8V thick-oxide MVT NMOS

The circuit engineers should keep the geometries of designed devices in the limited ranges, and devices out of the ranges, especially beyond the minimum geometry, are not recommended. Otherwise, the accuracy of the SPICE model cannot be guaranteed.

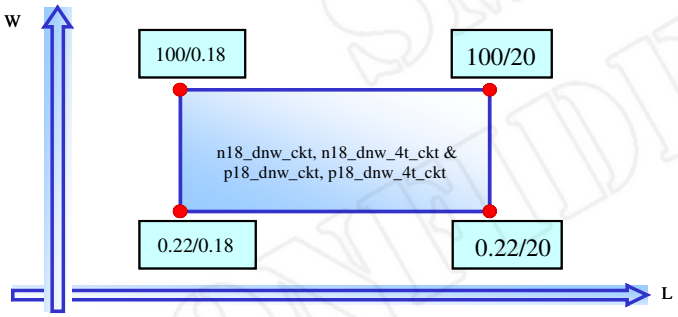
The valid range of device sizes is graphically shown below in Fig 7.2.11-Fig 7.2.19

A. 1.8V thin-oxide MOS model



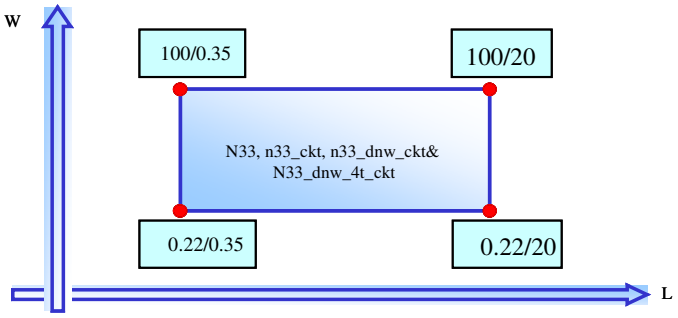
Where n18, p18 are the model names for 1.8V NMOS, PMOS transistors, respectively.
And n18_ckt, p18_ckt are the subckt model names for 1.8V NMOS, PMOS transistors, respectively.

B. 1.8V thin-oxide MOS in DNW model



Where n18_dnw_ckt, n18_dnw_4t_ckt, p18_dnw_ckt and p18_dnw_4t_ckt are the subckt model names for 1.8V NMOS, PMOS in DNW transistors, respectively.

C. 3.3V thin-oxide NMOS and NMOS in DNW model



Where n33, n33_ckt are the model names for 3.3V NMOS transistors, and n33_dnw_ckt, n33_dnw_4t_ckt are the model names for 3.3V NMOS in DNW transistors, respectively.

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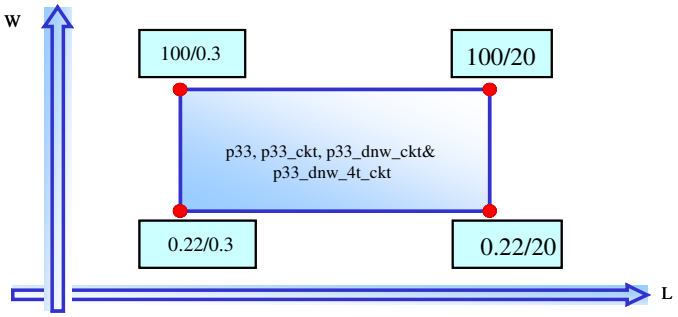
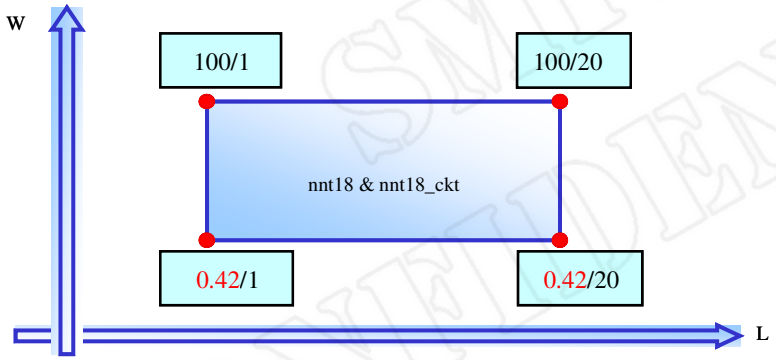
D. 3.3V thin-oxide PMOS and PMOS in DNW model



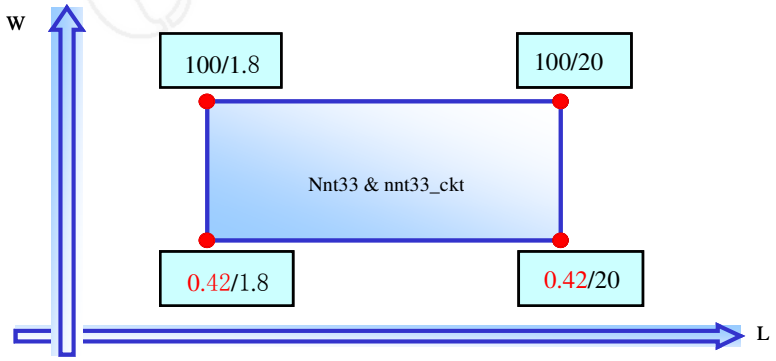
Where p33, p33_ckt are the model names for 3.3V PMOS transistors, and p33_dnw_ckt, p33_dnw_4t_ckt are the model names for 3.3V PMOS in DNW transistors, respectively.

E. 1.8V thin-oxide native NMOS model



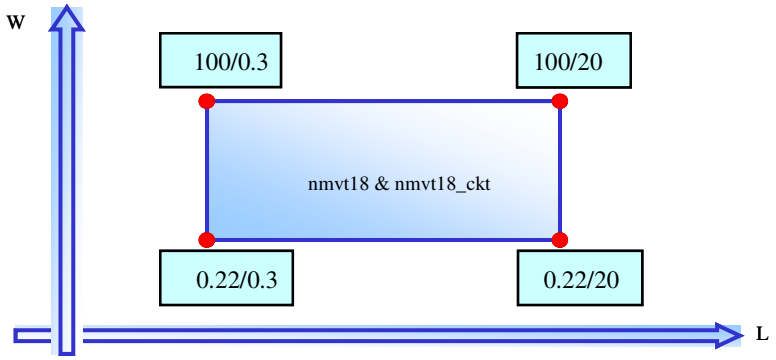
Where nnt18, nnt18_ckt are the model names for 1.8V native NMOS transistors.

F. 3.3V thin-oxide native NMOS model



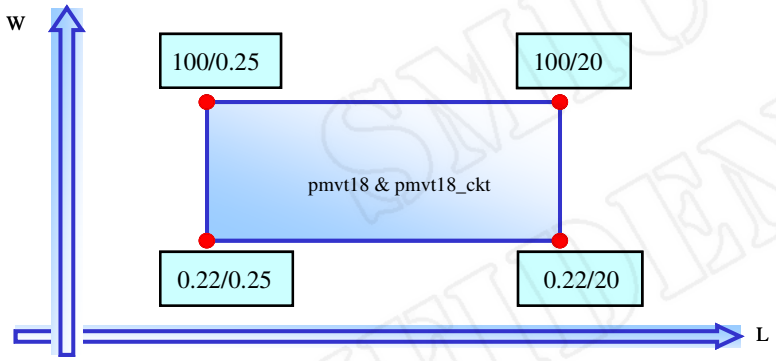
Where nnt33, nnt33_ckt are the model names for 3.3V native NMOS transistors.

G. 1.8V thin-oxide MVT NMOS model



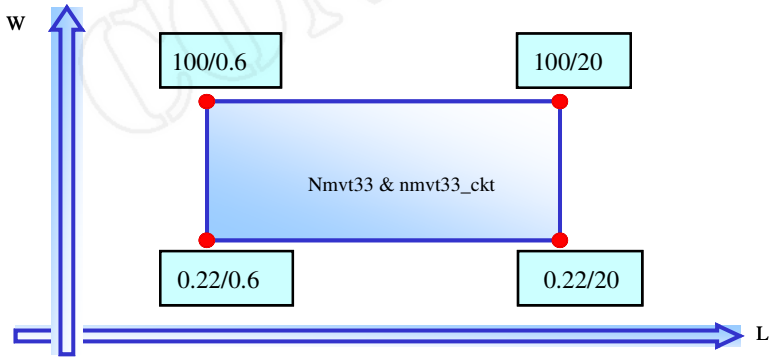
Where nmvt18, nmv18_ckt are the model names for 1.8V MVT NMOS transistors.

H. 1.8V thin-oxide MVT PMOS model



Where nmvt18, nmv18_ckt are the model names for 1.8V MVT PMOS transistors.

I. 3.3V thin-oxide MVT NMOS model



Where nmvt33, nmv33_ckt are the model names for 3.3V MVT NMOS transistors.

7.2.3 Sub-circuit Model

The MOSFETs models provided by the SMIC Model team are sub-circuit models. For normal MOSFETs, the sub-circuit model is established by adding the mismatch model part to the original compact model.

The sub-circuit model can compatible with any simulator which allows great flexibility for circuit designers.

To set up a unique sub-circuit model, the netlist should be established whose Hspice format is as shown below:

For normal MOSFET:
xm1 d g s b n18_ckt l=0.18u w=20u sa=0.48u sb=0.48u sd=0.54u as=1e-18 ad=1e-18 ps=1e-15 pd=1e-15 sca=0 scb=0 scc=0 nf=4 mr=1 mismod=1

Where:
- w: Total device width
- l: Device length
- sa: Distance between OD edge to Poly from one side
- sb: Distance between OD edge to Poly from other side
- sd: Distance between neighbouring fingers
- as: Total source area
- ad: Drain area defined by Nwell or Pwell
- ps: Total source perimeter
- pd: Drain perimeter defined by Nwell or Pwell
- nrd: Number of squares of drain diffusion for resistance calculations
- nrs: Number of squares of source diffusion for resistance calculations
- nf: Number of device fingers
- mr: Multiplier

7.2.4 Fixed Corner Model of MOSFETs

The process variation occurs due to the variation of process parameters, for example changes of etching rate, photolithography misalignment, dopant fluctuation, day-to-day operating status of foundry equipments and more all can result in process variation, which would lead to device parameters variations. Therefore device fixed corner models are used to simulate the best/worst-case circuit performance in light of process variations.

The SMIC model team models five fixed corner cases to simulate the sensitivities of corners to the process parameters. The provided fixed corner models by SMIC are primarily for predicting most important corner cases: TT, FF, SS, FNSP and SNFP. Their definitions are listed in Table 7.2.2.

Fixed Corner Model	Definition
TT	Typical model, for Nominal process modeling
FF	Fast N, Fast P corner. Performance corner for best cases of the static MOSFET circuit, including both global (e.g. chip to chip) and local (e.g. mismatch) variations.
SS	Slow N, Slow P corner. Performance corner for worst cases of the static MOSFET circuit, including both global (e.g. chip to chip) and local (e.g. mismatch) variations.
FNSP	Fast N, Slow P corner. Corner for bounding the range that single NMOS/PMOS devices can move in opposite performance directions, including both global (e.g. chip to chip) and local (e.g. mismatch) variations.
SNFP	Slow N, Fast P corner. Corner for bounding the range that single NMOS/PMOS devices can move in opposite performance directions, including both global (e.g. chip to chip) and local (e.g. mismatch) variations.

Table 7.2.2 Fixed corner model definitions for MOSFET

The following tables from Table 7.2.3 to Table 7.2.6 show the values of the data for compensating the corner cases of every device, and please refer to Section 7.10 for detailed info about the meaning of relevant parameters.

A. 1.8V thin-oxide MOS

Parameters	Unit	TT	FF	SS	FNSP	SNFP
dtox_n18	m	0	-4.60E-11	4.60E-11	0	0
dxl_n18	m	0	-5.00E-09	5.00E-09	0	0
dxw_n18	m	0	9.10E-09	-9.10E-09	0	0
dcj_n18	F/m^2	0	-4.94E-05	4.94E-05	-3.95E-05	3.95E-05
dcjsw_n18	F/m	0	-2.91E-12	2.91E-12	-2.33E-12	2.33E-12
dcjswg_n18	F/m	0	-1.85E-11	1.85E-11	-1.48E-11	1.48E-11
dcgdo_n18	F/m	0	9.00E-12	-9.00E-12	0	0
dcgdl_n18	F/m	0	4.50E-12	-4.50E-12	0	0

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dcf_n18	F/m	0	4.27E-12	-4.27E-12	0	0
dvth0_n18	V	0	-0.0325	0.0376	-0.028	0.032
dlvth0_n18	V	0	-2.40E-09	2.82E-09	-2.00E-09	2.40E-09
dpvth0_n18	V	0	-1.24E-15	1.16E-15	-1.05E-15	9.86E-16
du0_n18	$m^2/(Vs)$	0	1.00E-03	-9.40E-04	8.50E-04	-8.00E-04
dlu0_n18	$m^2/(Vs)$	0	1.20E-10	-1.20E-10	1.02E-10	-1.02E-10
dpu0_n18	$m^2/(Vs)$	0	0	-4.20E-17	0	-3.57E-17
dvsat_n18	m/s	0	0.00E+00	0.00E+00	0.00E+00	0.00E+00
dlvsat_n18	m/s	0	9.00E-04	-1.08E-03	7.70E-04	-9.18E-04
dpvsat_n18	m/s	0	4.00E-11	-1.40E-10	4.00E-11	-1.19E-10
dvoff_n18	V	0	-0.01	0	-0.0085	0
dwvth_n18	V	0	-6.50E-09	5.70E-09	-5.50E-09	4.85E-09
dwu0_n18	$m^2/(Vs)$	0	0	-1.80E-10	0	-1.53E-10
dtox_p18	m	0	-4.60E-11	4.60E-11	0	0
dxl_p18	m	0	-5.00E-09	5.00E-09	0	0
dxw_p18	m	0	9.10E-09	-9.10E-09	0	0
dcj_p18	F/m^2	0	-5.53E-05	5.53E-05	4.42E-05	-4.42E-05
dcjsw_p18	F/m	0	-4.37E-12	4.37E-12	3.50E-12	-3.50E-12
dcjswg_p18	F/m	0	-2.11E-11	2.11E-11	1.69E-11	-1.69E-11
dcgdo_p18	F/m	0	1.05E-11	-1.05E-11	0	0
dcgdl_p18	F/m	0	8.80E-12	-8.80E-12	0	0
dcf_p18	F/m	0	4.25E-12	-4.25E-12	0	0
dvth0_p18	V	0	5.40E-02	-4.80E-02	-3.84E-02	4.32E-02
dlvth0_p18	V	0	2.00E-09	-3.60E-09	-2.88E-09	1.60E-09
dpvth0_p18	V	0	6.80E-16	-5.00E-16	-4.00E-16	5.44E-16
du0_p18	$m^2/(Vs)$	0	0.00E+00	-1.00E-04	-8.00E-05	0.00E+00
dlu0_p18	$m^2/(Vs)$	0	0.00E+00	-4.00E-11	0.00E+00	0.00E+00
dpu0_p18	$m^2/(Vs)$	0	1.60E-17	-3.00E-17	-2.40E-17	1.28E-17
dvoff_p18	$m^2/(Vs)$	0	-7.00E-03	7.00E-03	5.60E-03	-5.60E-03
dvsat_p18	m/s	0	0.00E+00	0.00E+00	0.00E+00	0.00E+00
dlvsat_p18	m/s	0	0.00E+00	0.00E+00	0.00E+00	0.00E+00
dpvsat_p18	m/s	0	0.00E+00	0.00E+00	0.00E+00	0.00E+00
dwvth_p18	V	0	3.00E-09	-3.00E-09	-2.40E-09	2.40E-09
dwu0_p18	$m^2/(Vs)$	0	5.00E-11	-9.00E-11	-7.20E-11	4.00E-11

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dlpe0_p18	m	0	0.00E+00	0.00E+00	0.00E+00	0.00E+00
dminv_p18	--	0	0.00E+00	0.00E+00	0.00E+00	0.00E+00
dlminv_p18	---	0	-5.00E-08	5.00E-08	4.00E-08	-4.00E-08
dtoxe_nt18	m	0	-4.60E-11	4.60E-11	0.00E+00	0.00E+00
dxl_nt18	m	0	-5.00E-09	5.00E-09	0.00E+00	0.00E+00
dxw_nt18	m	0	9.10E-09	-9.10E-09	0.00E+00	0.00E+00
dcj_nt18	F/m^2	0	-6.60E-06	6.60E-06	-5.28E-06	5.28E-06
dcjsw_nt18	F/m	0	-7.21E-12	7.21E-12	-5.77E-12	5.77E-12
dcjswg_nt18	F/m	0	-1.83E-12	1.83E-12	-1.46E-12	1.46E-12
dcgdo_nt18	F/m	0	5.05E-12	-5.05E-12	0.00E+00	0.00E+00
dcgdl_nt18	F/m	0	1.88E-11	-1.88E-11	0.00E+00	0.00E+00
dcf_nt18	F/m	0	4.27E-12	-4.27E-12	0.00E+00	0.00E+00
dvth0_nt18	V	0	-6.90E-02	7.00E-02	-5.52E-02	5.60E-02
dlvth0_nt18	V	0	-2.82E-08	2.63E-08	-2.26E-08	2.10E-08
dpvth0_nt18	V	0	0.00E+00	0.00E+00	0.00E+00	0.00E+00
du0_nt18	$m^2/(Vs)$	0	2.50E-03	-3.40E-03	2.00E-03	-2.72E-03
dlu0_nt18	$m^2/(Vs)$	0	1.00E-09	-1.85E-09	8.00E-10	-1.48E-09
dpu0_nt18	$m^2/(Vs)$	0	2.00E-16	-3.00E-16	1.60E-16	-2.40E-16
dvsat_nt18	m/s	0	9.30E+03	-1.46E+04	7.44E+03	-1.17E+04
dlvsat_nt18	m/s	0	1.00E-02	-1.29E-02	8.00E-03	-1.03E-02
dpvsat_nt18	m/s	0	0.00E+00	0.00E+00	0.00E+00	0.00E+00
dvoff_nt18	V	0	0.00E+00	0.00E+00	0.00E+00	0.00E+00
dwvth0_nt18	V	0	-2.50E-09	3.00E-09	-2.00E-09	2.40E-09
dwu0_nt18	$m^2/(Vs)$	0	0.00E+00	-4.00E-10	0.00E+00	-3.20E-10
dtoxe_n18_dnw	m	0	-4.60E-11	4.60E-11	0.00E+00	0.00E+00
dxl_n18_dnw	m	0	-5.00E-09	5.00E-09	0.00E+00	0.00E+00
dxw_n18_dnw	m	0	9.10E-09	-9.10E-09	0.00E+00	0.00E+00
dcj_n18_dnw	F/m^2	0	-4.94E-05	4.94E-05	-3.95E-05	3.95E-05
dcjsw_n18_dnw	F/m	0	-2.91E-12	2.91E-12	-2.33E-12	2.33E-12
dcjswg_n18_dnw	F/m	0	-1.85E-11	1.85E-11	-1.48E-11	1.48E-11
dcgdo_n18_dnw	F/m	0	9.00E-12	-9.00E-12	0.00E+00	0.00E+00
dcgdl_n18_dnw	F/m	0	4.50E-12	-4.50E-12	0.00E+00	0.00E+00
dcf_n18_dnw	F/m	0	4.27E-12	-4.27E-12	0.00E+00	0.00E+00
dvth0_n18_dnw	V	0	-3.25E-02	3.76E-02	-2.80E-02	3.20E-02

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dlvth0_n18_dnw	V	0	-2.40E-09	2.82E-09	-2.00E-09	2.40E-09
dpvth0_n18_dnw	V	0	-1.24E-15	1.16E-15	-1.05E-15	9.86E-16
du0_n18_dnw	$m^2/(Vs)$	0	1.00E-03	-9.40E-04	8.50E-04	-8.00E-04
dlu0_n18_dnw	$m^2/(Vs)$	0	1.20E-10	-1.20E-10	1.02E-10	-1.02E-10
dpu0_n18_dnw	$m^2/(Vs)$	0	0.00E+00	-4.20E-17	0.00E+00	-3.57E-17
dvsat_n18_dnw	m/s	0	0.00E+00	0.00E+00	0.00E+00	0.00E+00
dlvsat_n18_dnw	m/s	0	9.00E-04	-1.08E-03	7.70E-04	-9.18E-04
dpvsat_n18_dnw	m/s	0	4.00E-11	-1.40E-10	4.00E-11	-1.19E-10
dvoff_n18_dnw	V	0	-1.00E-02	0.00E+00	-8.50E-03	0.00E+00
dwvth0_n18_dnw	V	0	-6.50E-09	5.70E-09	-5.50E-09	4.85E-09
dwu0_n18_dnw	$m^2/(Vs)$	0	0.00E+00	-1.80E-10	0.00E+00	-1.53E-10
dtoxe_p18_dnw	m	0	-4.60E-11	4.60E-11	0.00E+00	0.00E+00
dxl_p18_dnw	m	0	-5.00E-09	5.00E-09	0.00E+00	0.00E+00
dxw_p18_dnw	m	0	9.10E-09	-9.10E-09	0.00E+00	0.00E+00
dcj_p18_dnw	F/m^2	0	-5.53E-05	5.53E-05	4.42E-05	-4.42E-05
dcjsw_p18_dnw	F/m	0	-4.37E-12	4.37E-12	3.50E-12	-3.50E-12
dcjswg_p18_dnw	F/m	0	-2.11E-11	2.11E-11	1.69E-11	-1.69E-11
dcgdo_p18_dnw	F/m	0	1.05E-11	-1.05E-11	0.00E+00	0.00E+00
dcgdl_p18_dnw	F/m	0	8.80E-12	-8.80E-12	0.00E+00	0.00E+00
dcf_p18_dnw	F/m	0	4.25E-12	-4.25E-12	0.00E+00	0.00E+00
dvth0_p18_dnw	V	0	5.40E-02	-4.80E-02	-3.84E-02	4.32E-02
dlvth0_p18_dnw	V	0	2.00E-09	-3.60E-09	-2.88E-09	1.60E-09
dpvth0_p18_dnw	V	0	6.80E-16	-5.00E-16	-4.00E-16	5.44E-16
du0_p18_dnw	$m^2/(Vs)$	0	0.00E+00	-1.00E-04	-8.00E-05	0.00E+00
dlu0_p18_dnw	$m^2/(Vs)$	0	0.00E+00	-4.00E-11	0.00E+00	0.00E+00
dpu0_p18_dnw	$m^2/(Vs)$	0	1.60E-17	-3.00E-17	-2.40E-17	1.28E-17
dvsat_p18_dnw	m/s	0	0.00E+00	0.00E+00	0.00E+00	0.00E+00
dlvsat_p18_dnw	m/s	0	0.00E+00	0.00E+00	0.00E+00	0.00E+00
dpvsat_p18_dnw	m/s	0	0.00E+00	0.00E+00	0.00E+00	0.00E+00
dvoff_p18_dnw	V	0	-7.00E-03	7.00E-03	5.60E-03	-5.60E-03
dwvth0_p18_dnw	V	0	3.00E-09	-3.00E-09	-2.40E-09	2.40E-09
dwu0_p18_dnw	$m^2/(Vs)$	0	5.00E-11	-9.00E-11	-7.20E-11	4.00E-11
dlpe0_p18_dnw	m	0	0.00E+00	0.00E+00	0.00E+00	0.00E+00
dminv_p18_dnw	--	0	0.00E+00	0.00E+00	0.00E+00	0.00E+00

dlminv_p18_dnw	--	0	-5.00E-08	5.00E-08	4.00E-08	-4.00E-08

Table 7.2.3 Fixed corner parameters for 1.8V MOSFET

where: TT: Typical model
SS: Slow model
FF: Fast model
SNFP: Slow N fast P model
FNSP: Fast N slow P model

B. 3.3V MOS

Parameters	Unit	TT	FF	SS	FNSP	SNFP
dtoxe_n33	m	0	-7.55E-11	7.55E-11	0	0
dxl_n33	m	0	-5.00E-09	5.00E-09	0	0
dxw_n33	m	0	9.10E-09	-9.10E-09	0	0
dcjs_n33	F/m^2	0	-4.30E-05	4.30E-05	-4.30E-05	4.30E-05
dcjsws_n33	F/m	0	-4.84E-12	4.84E-12	-4.84E-12	4.84E-12
dcjswgs_n33	F/m	0	-1.41E-11	1.41E-11	-1.41E-11	1.41E-11
dcgdo_n33	F/m	0	5.00E-12	-5.00E-12	0	0
dcgdl_n33	F/m	0	1.30E-11	-1.30E-11	0	0
dcgso_n33	F/m	0	5.00E-12	-5.00E-12	0	0
dcgsl_n33	F/m	0	1.30E-11	-1.30E-11	0	0
dcf_n33	F/m	0	3.78E-12	-3.78E-12	0	0
dvth0_n33	V	0	-5.54E-02	5.42E-02	-3.88E-02	3.79E-02
dlvth0_n33	V	0	-7.65E-09	8.25E-09	-5.36E-09	5.77E-09
dwvth0_n33	V	0	-8.56E-09	7.53E-09	-5.99E-09	5.27E-09
dpvth0_n33	V	0	1.02E-15	-9.89E-16	7.14E-16	-6.92E-16
du0_n33	$m^2/(Vs)$	0	1.82E-03	-2.28E-03	1.27E-03	-1.60E-03
dlu0_n33	$m^2/(Vs)$	0	1.07E-10	-1.01E-11	7.49E-11	-7.08E-11
dwu0_n33	$m^2/(Vs)$	0	-9.43E-11	-6.13E-11	-6.60E-11	-4.29E-11
dpu0_n33	$m^2/(Vs)$	0	2.59E-16	-2.09E-16	1.81E-16	-1.46E-16
dvsat_n33	m/sec	0	0	0.00E+00	0	0.00E+00
dlvsat_n33	m/sec	0	1.07E-03	-1.41E-03	0.00074655	-0.000985005
dwvsat_n33	m/sec	0	0.00E+00	0.00E+00	0	0
dpvsat_n33	m/sec	0	3.00E-10	-4.00E-10	2.1E-10	-2.8E-10

djtsswgs_n33	A/m	0	8.22E-09	-1.50E-09	5.76E-09	-1.05E-09
djtsswgd_n33	A/m	0	8.22E-09	-1.50E-09	5.76E-09	-1.05E-09
dlagidl_n33	-	0	1.68E-14	0.00E+00	1.18E-14	0.00E+00
dpagidl_n33	-	0	5.57E-21	0.00E+00	3.90096E-21	0
dtoxe_p33	m	0	-7.55E-11	7.55E-11	0	0
dxl_p33	m	0	-5.00E-09	5.00E-09	0	0
dxw_p33	m	0	9.10E-09	-9.10E-09	0	0
dcjs_p33	F/m^2	0	-5.22E-05	5.22E-05	5.2200E-05	-5.2200E-05
dcjsws_p33	F/m	0	-4.285E-12	4.285E-12	4.29E-12	-4.29E-12
dcjswgs_p33	F/m	0	-2.02E-11	2.02E-11	2.02E-11	-2.02E-11
dcgdo_p33	F/m	0	5.00E-12	-5.00E-12	0.00E+00	0.00E+00
dcgso_p33	F/m	0	5.00E-12	-5.00E-12	0.00E+00	0.00E+00
dcgdl_p33	F/m	0	1.26E-11	-1.26E-11	0.00E+00	0.00E+00
dcgsl_p33	F/m	0	1.26E-11	-1.26E-11	0	0
dcf_p33	F/m	0	1.525E-12	-1.525E-12	0	0
dvth0_p33	V	0	5.4786E-02	-5.3996E-02	-3.7797E-02	3.8350E-02
dlvth0_p33	V	0	1.1949E-09	-1.2638E-09	-8.8466E-10	8.3643E-10
dwvsat_p33	V	0	0	0	0	0
dpvth0_p33	V	0	1.0598E-15	-1.0536E-15	-7.3752E-16	7.4186E-16
du0_p33	$m^2/(Vs)$	0	5.5526E-04	-7.8951E-04	-5.5265E-04	3.8868E-04
dlu0_p33	$m^2/(Vs)$	0	5.446E-11	-6.4478E-11	-4.51346E-11	3.8122E-11
dwu0_p33	$m^2/(Vs)$	0	1.05E-10	-1.08E-10	-7.54838E-11	7.3416E-11
dpu0_p33	$m^2/(Vs)$	0	-1.40E-17	2.13E-17	1.491E-17	-9.8E-18
dvsat_p33	m/sec	0	0.00E+00	0.00E+00	0	0
dlvsat_p33	m/sec	0	9.38E-04	-1.33E-03	-0.00093345	0.00065641
dpvsat_p33	m/sec	0	3.90E-11	-1.96E-10	-1.3727E-10	2.73E-11
dwvth0_p33	m/sec	0	3.7507E-09	-2.98195E-09	-2.08737E-09	2.62549E-09
dagidl_p33	-	0	0.00E+00	-2.79E-13	-1.95E-13	0.00E+00
dlagidl_p33	-	0	4.71E-18	-3.00E-19	-2.10E-19	3.30E-18
dwagidl_p33	-	0	2.00E-18	-5.85E-19	-4.10E-19	1.40E-18
dpagidl_p33	-	0	1.00E-24	9.00E-26	6.30E-26	7.00E-25
dtoxe_nnt33	m	0	-7.55E-11	7.55E-11	0.00E+00	0.00E+00
dxl_nnt33	m	0	-5.00E-09	5.00E-09	0.00E+00	0.00E+00
dxw_nnt33	m	0	9.10E-09	-9.10E-09	0.00E+00	0.00E+00

dcjs_nnt33	F/m^2	0	-0.000006583	6.58E-06	-0.000006583	6.58E-06
dcjsws_nnt33	F/m	0	-1.07E-11	1.07E-11	-1.0666E-11	1.07E-11
dcjswgs_nnt33	F/m	0	-3.86E-12	3.86E-12	-3.86025E-12	3.86E-12
dcgdo_nnt33	F/m	0	1.50E-11	-1.50E-11	0	0
dcgdl_nnt33	F/m	0	3.00E-11	-3.00E-11	0	0
dcgso_nnt33	F/m	0	1.50E-11	-1.50E-11	0	0
dcgsl_nnt33	F/m	0	3.00E-11	-3.00E-11	0	0
dcf_nnt33	F/m	0	3.78E-12	-3.78E-12	0	0
dvth0_nnt33	V	0	-3.48E-02	3.59E-02	-2.75E-02	2.79E-02
dlvth0_nnt33	V	0	-2.63E-08	2.50E-08	-1.4742E-08	1.4105E-08
dwvth0_nnt33	V	0	-4.64E-09	4.04E-09	-3.248E-09	2.8273E-09
dpvth0_nnt33	V	0	3.50E-16	-3.75E-16	2.45E-16	-2.625E-16
du0_nnt33	$m^2/(Vs)$	0	8.10E-04	-8.55E-04	5.67E-04	-5.99E-04
dlu0_nnt33	$m^2/(Vs)$	0	1.34E-09	-1.52E-09	9.35E-10	-1.07E-09
dwu0_nnt33	$m^2/(Vs)$	0	-2.61E-11	2.15E-10	-3.05E-11	-5.15E-11
dvsat_nnt33	m/sec	0	0	0	0	0
dlvsat_nnt33	m/sec	0	3.92E-03	-4.16E-03	2.75E-03	-2.91E-03
dpvsat_nnt33	m/sec	0	3.00E-11	-3.00E-11	2.10E-11	-2.10E-11
dpu0_nnt33	$m^2/(Vs)$	0	2.70E-17	-1.75E-16	1.89E-17	-1.22E-16
dwvsat_nnt33	m/sec	0	0	0	0	0
dvoff_nnt33	V	0	0	0	0	0
dpagidl_p33	-	0	1.00E-24	9.00E-26	6.30E-26	7.00E-25
dtoxe_nnt33	m	0	-7.55E-11	7.55E-11	0.00E+00	0.00E+00
dxl_nnt33	m	0	-5.00E-09	5.00E-09	0.00E+00	0.00E+00
dxw_nnt33	m	0	9.10E-09	-9.10E-09	0.00E+00	0.00E+00
dcjs_nnt33	F/m2	0	-0.000006583	6.58E-06	-0.000006583	6.58E-06
dcjsws_nnt33	F/m	0	-1.07E-11	1.07E-11	-1.0666E-11	1.07E-11
dcjswgs_nnt33	F/m	0	-3.86E-12	3.86E-12	-3.86025E-12	3.86E-12
dcgdo_nnt33	F/m	0	1.50E-11	-1.50E-11	0	0
dcgdl_nnt33	F/m	0	3.00E-11	-3.00E-11	0	0
dcgso_nnt33	F/m	0	1.50E-11	-1.50E-11	0	0
dcgsl_nnt33	F/m	0	3.00E-11	-3.00E-11	0	0
dcf_nnt33	F/m	0	3.78E-12	-3.78E-12	0	0
dvth0_nnt33	V	0	-3.48E-02	3.59E-02	-2.75E-02	2.79E-02

dlvth0_nnt33	V	0	-2.63E-08	2.50E-08	-1.4742E-08	1.4105E-08
dwvth0_nnt33	V	0	-4.64E-09	4.04E-09	-3.248E-09	2.8273E-09
dpvth0_nnt33	V	0	3.50E-16	-3.75E-16	2.45E-16	-2.625E-16
du0_nnt33	m2/(Vs)	0	8.10E-04	-8.55E-04	5.67E-04	-5.99E-04
dlu0_nnt33	m2/(Vs)	0	1.34E-09	-1.52E-09	9.35E-10	-1.07E-09
dwu0_nnt33	m2/(Vs)	0	-2.61E-11	2.15E-10	-3.05E-11	-5.15E-11
dvsat_nnt33	m/sec	0	0	0	0	0
dlvsat_nnt33	m/sec	0	3.92E-03	-4.16E-03	2.75E-03	-2.91E-03
dpvsat_nnt33	m/sec	0	3.00E-11	-3.00E-11	2.10E-11	-2.10E-11
dpu0_nnt33	m2/(Vs)	0	2.70E-17	-1.75E-16	1.89E-17	-1.22E-16
dwvsat_nnt33	m/sec	0	0	0	0	0
dvoff_nnt33	V	0	0	0	0	0

Table 7.2.4 Fixed corner parameters for 3.3V MOSFET

where: TT: Typical model
SS: Slow model
FF: Fast model
SNFP: Slow N fast P model
FNSP: Fast N slow P model

C. 1.8V MVT MOS

Parameters	Unit	TT	FF	SS	FNSP	SNFP
dtoxe_nmvt18	m	0	-4.60E-11	4.6E-11	0	0
dxl_nmvt18	m	0	-5.00E-09	5.00E-09	0	0
dxw_nmvt18	m	0	9.10E-09	-9.10E-09	0	0
dvth0_nmvt18	V	0	-3.92E-02	3.91E-02	-2.74E-02	2.74E-02
dlvth0_nmvt18	V	0	-2.06E-09	1.90E-09	-1.44E-09	1.33E-09
dwvth0_nmvt18	V	0	-2.85E-09	2.60E-09	-2.00E-09	1.82E-09
dpvth0_nmvt18	V	0	0	0	0	0
du0_nmvt18	m^2/(Vs)	0	0	-1.00E-04	0	-0.00007
dlu0_nmvt18	m^2/(Vs)	0	9.80E-10	-9.80E-10	6.86E-10	-6.86E-10
dwu0_nmvt18	m^2/(Vs)	0	0	-4.00E-11	0	-2.80E-11
dpu0_nmvt18	m^2/(Vs)	0	0	0	0	0
dvsat_nmvt18	m/sec	0	1.30E+03	-2.30E+03	9.10E+02	-1.61E+03
dpvsat_nmvt18	m/sec	0	0	0	0	0
dwvsat_nmvt18	m/sec	0	0	0	0	0
dlvsat_nmvt18	m/sec	0	0	0	0	0
dcjs_nmvt18	F/m^2	0	-4.68E-05	4.68E-05	-4.68E-05	4.68E-05
dcjsws_nmvt18	F/m	0	-3.02E-12	3.02E-12	-3.02E-12	3.02E-12
dcjswgs_nmvt18	F/m	0	-1.69E-11	1.69E-11	-1.69E-11	1.69E-11
dcgdo_nmvt18	F/m	0	1.00E-11	-1.00E-11	0	0
dcgsl_nmvt18	F/m	0	4.70E-12	-4.70E-12	0	0

dcgso_nmvt18	F/m	0	1.00E-11	-1.00E-11	0	0
dcgdl_nmvt18	F/m	0	4.70E-12	-4.70E-12	0	0
dcf_nmvt18	F/m	0	4.31E-12	-4.31E-12	0	0
dtoxe_pmvt18	m	0	-4.60E-11	4.60E-11	0	0
dxl_pmvt18	m	0	-5.00E-09	5.00E-09	0	0
dxw_pmvt18	m	0	9.10E-09	-9.10E-09	0	0
dvth0_pmvt18	V	0	5.80E-02	-5.79E-02	-4.05E-02	4.06E-02
dlvth0_pmvt18	V	0	5.90E-09	-6.23E-09	-4.36E-09	4.13E-09
dwvth0_pmvt18	V	0	4.40E-09	-4.22E-09	-2.95E-09	3.08E-09
dpvth0_pmvt18	V	0	0	0	0	0
du0_pmvt18	$m^2/(Vs)$	0	0	-9.00E-05	-6.30E-05	0
dlu0_pmvt18	$m^2/(Vs)$	0	0	-9.00E-11	-6.30E-11	0
dwu0_pmvt18	$m^2/(Vs)$	0	0	0	0	0
dpu0_pmvt18	$m^2/(Vs)$	0	0	0	0	0
dvsat_pmvt18	m/sec	0	1.20E+04	-1.00E+04	-7.00E+03	8.40E+03
dpvsat_pmvt18	m/sec	0	0	0	0	0
dwvsat_pmvt18	m/sec	0	-3.00E-03	4.70E-03	3.29E-03	-2.10E-03
dlvsat_pmvt18	m/sec	0	0	0	0	0
dcjs_pmvt18	F/m^2	0	-3.93E-05	3.93E-05	3.93E-05	-3.93E-05
dcjsws_pmvt18	F/m	0	-2.49E-12	2.49E-12	2.49E-12	-2.49E-12
dcjswgs_pmvt18	F/m	0	-3.06E-11	3.06E-11	3.06E-11	-3.06E-11
dcgdo_pmvt18	F/m	0	4.50E-12	-4.50E-12	0	0
dcgso_pmvt18	F/m	0	4.50E-12	-4.50E-12	0	0
dcgdl_pmvt18	F/m	0	2.14E-11	-2.14E-11	0	0
dcgsl_pmvt18	F/m	0	2.14E-11	-2.14E-11	0	0
dcf_pmvt18	F/m	0	4.25E-12	-4.25E-12	0	0

Table 7.2.5 Fixed corner parameters for 1.8V MVT MOSFET

where: TT: Typical model
SS: Slow model
FF: Fast model
SNFP: Slow N fast P model
FNSP: Fast N slow P model

D. 3.3V MVT MOS

Parameters	Unit	TT	FF	SS	FNSP	SNFP
dtoxe_nmvt33	m	0	-7.55E-11	7.55E-11	0	0
dxl_nmvt33	m	0	-5.00E-09	5.00E-09	0	0
dxw_nmvt33	m	0	9.10E-09	-9.10E-09	0	0
dcjs_nmvt33	V	0	-4.32E-05	4.32E-05	-4.32E-05	4.32E-05
dcjsws_nmvt33	V	0	-5.35E-12	5.35E-12	-5.35E-12	5.35E-12
dcjswgs_nmvt33	V	0	-1.33E-11	1.33E-11	-1.33E-11	1.33E-11

dcgdo_nmvt33	V	0	5.00E-12	-5.00E-12	0	0
dcgdl_nmvt33	m^2/(Vs)	0	1.85E-11	-1.85E-11	0	0
dcgso_nmvt33	m^2/(Vs)	0	5.00E-12	-5.00E-12	0	0
dcgsl_nmvt33	m^2/(Vs)	0	1.85E-11	-1.85E-11	0	0
dcf_nmvt33	m^2/(Vs)	0	3.78E-12	-3.78E-12	0	0
dvth0_nmvt33	m/sec	0	-3.72E-02	3.75E-02	-2.60E-02	2.63E-02
dlvth0_nmvt33	m/sec	0	-1.10E-08	1.05E-08	-7.70E-09	7.35E-09
dwvth0_nmvt33	m/sec	0	-5.21E-09	4.80E-09	-3.65E-09	3.36E-09
dpvth0_nmvt33	m/sec	0	1.90E-16	1.00E-17	1.33E-16	7.00E-18
du0_nmvt33	F/m^2	0	3.13E-04	-3.64E-04	2.19E-04	-2.55E-04
dlu0_nmvt33	F/m	0	1.40E-09	-1.50E-09	9.80E-10	-1.05E-09
dwu0_nmvt33	F/m	0	-1.79E-10	9.00E-11	-1.25E-10	6.30E-11
dvsat_nmvt33	F/m	0	0.00E+00	-9.54E+02	0.00E+00	-6.68E+02
dlvsat_nmvt33	F/m	0	2.00E-03	-2.00E-03	1.40E-03	-1.40E-03
dpvsat_nmvt33	F/m	0	4.05E-11	-6.00E-10	2.84E-11	-4.20E-10
dpu0_nmvt33	F/m	0	1.70E-16	-2.00E-16	1.19E-16	-1.40E-16
dwvsat_nmvt33	F/m	0	0	0	0	0
dvoff_nmvt33	V	0	0	0	0	0

Table 7.2.6 Fixed corner parameters for 3.3V MVT MOSFET

where: TT: Typical model
SS: Slow model
FF: Fast model
SNFP: Slow N fast P model
FNSP: Fast N slow P model

7.2.5 MOSFET Model Simulation compare with PCM Spec Table

Simulation Condition:

Vtlin: Vds=0.1V, ID=0.1uA*W/L
Vtsat: Vds=VDD, ID=0.1uA*W/L
Idsat: VDS=VGS=VDD
Ioff: VDS=1.1*VDD, VG=VB=VS=0
gmindc=1e-14

Idsat and Ioff normalize to width.

A. Comparison on NMOS & PMOS PCM spec with typical case simulation results

1.8V thin oxide MOS (and in DNW)

Items / Types		Unit	TT		FF		SS		FNSP		SNFP	
			PCM spec.	Simulated Result	PCM spec.	Simulated Result	PCM spec.	Simulated Result	PCM spec.	Simulated Result	PCM spec.	Simulated Result
1.8V MOS	VTH_N(10/0.18)	V	0.42	0.42	0.36	0.36	0.48	0.48	------	0.37	------	0.47
	IDSAT_N(10/0.18)	mA/um	0.600	0.600	0.690	0.692	0.510	0.509	------	0.663	------	0.532
	VTH_P(10/0.18)	V	-0.485	-0.485	-0.395	-0.4	-0.575	-0.570	------	-0.551	------	-0.419
	IDSAT_P(10/0.18)	mA/um	-0.260	-0.260	-0.300	-0.305	-0.220	-0.215		-0.236		-0.283
1.8V in DNW MOS	VTH_N(10/0.18)	V	0.42	0.42	0.36	0.36	0.48	0.48	------	0.37	------	0.47
	IDSAT_N(10/0.18)	mA/um	0.600	0.600	0.690	0.690	0.510	0.510	------	0.663	------	0.532
	VTH_P(10/0.18)	V	-0.485	-0.484	-0.395	-0.4	-0.575	-0.570	------	-0.552	------	-0.419
	IDSAT_P(10/0.18)	mA/um	-0.260	-0.260	-0.300	-0.305	-0.220	-0.215		-0.231		-0.291

Table 7.2.7 Comparison of PCM spec for 1.8V MOSFET

3.3V thick oxide MOS (and in DNW)

Items / Types		Unit	TT		FF		SS		FNSP		SNFP	
			PCM spec.	Simulated Result	PCM spec.	Simulated Result	PCM spec.	Simulated Result	PCM spec.	Simulated Result	PCM spec.	Simulated Result
3.3V MOS	VTH_N(10/0.35)	V	0.720	0.720	0.620	0.621	0.820	0.820	-	0.654	-	0.788
	IDSAT_N(10/0.35)	uA/um	600.0	600.5	680.0	680.4	520.0	520.0	-	647.4	-	548.4
	IOFF_N(10/0.35)	pA/um	0.30	0.30	3.00	3.14	-	0.02	-	2.07	-	0.10
	VTH_P(10/0.3)	V	-0.650	-0.650	-0.580	-0.580	-0.720	-0.721	-	-0.696	-	-0.605
	IDSAT_P(10/0.3)	uA/um	-300.0	-300.9	-345.0	-345.2	-255.0	-255.2	-	-273.6	-	-324.8
	IOFF_P(10/0.3)	pA/um	-0.90	0.90	-9.00	-9.62	-	-0.22	-	-0.42	-	-6.26
3.3V Native MOS	VTH_N(10/1.2)	V	-0.149	-0.149	-0.201	-0.202	-0.097	-0.095	-	-0.187	-	-0.110
	IDSAT_N(10/1.2)	mA/um	447.5	447.5	489	489.3	405	405.3	-	474	-	419.7

Table 7.2.8 Comparison of PCM spec for 3.3V MOSFET

1.8V&3.3V MVT NMOS

Items / Types		Unit	TT		FF		SS		FNSP		SNFP	
			PCM spec.	Simulated Result	PCM spec.	Simulated Result	PCM spec.	Simulated Result	PCM spec.	Simulated Result	PCM spec.	Simulated Result
1.8V MVT MOS	VTH_N(10/0.3)	V	0.275	0.275	0.225	0.225	0.325	0.326	-	0.241	-	0.311
	IDSAT_N(10/0.3)	uA/um	520.0	520.4	580.0	580.1	460.0	460.2	-	554.2	-	484.2
	VTH_P(10/0.25)	V	-0.240	-0.240	-0.150	-0.151	-0.330	-0.331	-	-0.304	-	-0.178
	IDSAT_P(10/0.25)	uA/um	-270.0	-270.2	-310.0	-309.6	-230.0	-230.8	-	-245.7	-	-292.5
3.3V MVT MOS	VTH_N(10/0.6)	V	0.450	0.451	0.390	0.391	0.510	0.510	-	0.409	-	0.492
	IDSAT_N(10/0.6)	uA/um	525.0	524.7	570.0	570.7	480.0	477.9	-	552.4	-	495.2

Table 7.2.9 Comparison of PCM spec for MVT MOSFET

7.2.6 Corner-Case Simulation Results of Inverter, NAND and NOR Ring-Oscillator

In this section, model simulation results with different fixed corners for Inverter, NAND and NOR ring oscillator are shown. For 1.8V device, the W/L of NMOS and PMOS are 4/0.18 and 6/0.18 respectively. For 3.3V devices, the W/L of NMOS and PMOS are 4/0.35 and 6/0.3. For 1.8V MVT devices, the W/L of NMOS and PMOS are 4/0.3 and 6/0.25.

A. 1.8V R.O.

Temp	F.O.	TT	FF	SS	FNSP	SNFP
25C	1	24.20	20.63	29.13	24.40	24.58
125C	1	27.39	23.45	32.93	27.32	28.07
-40C	1	21.80	18.61	26.17	22.08	22.01
25C	3	46.34	39.94	55.23	46.58	47.20
125C	3	52.25	45.05	62.31	51.99	53.68
-40C	3	41.86	36.07	50.10	42.44	42.40

Table 7.2.10 1.8V Inverter Ring-Oscillator: (Vdd=1.8V, unit=ps/gate)

Temp	F.O.	TT	FF	SS	FNSP	SNFP
25C	1	40.92	34.85	49.15	40.38	42.39
125C	1	48.14	41.22	57.98	47.42	49.97
-40C	1	35.90	30.71	43.01	35.52	37.17
25C	3	87.05	74.95	103.62	85.48	90.78
125C	3	102.03	87.84	121.58	99.77	106.70
-40C	3	76.71	66.12	91.22	75.60	79.82

Table 7.2.11 1.8V NAND Ring-Oscillator: (Vdd=1.8V, unit=ps/gate)

Temp	F.O.	TT	FF	SS	FNSP	SNFP
25C	1	50.05	42.66	60.56	51.15	50.14

125C	1	55.80	47.77	67.20	56.28	56.36
-40C	1	45.25	38.41	54.92	46.57	44.92
25C	3	113.56	97.41	136.30	117.38	111.93
125C	3	125.21	107.63	149.33	127.55	125.32
-40C	3	103.26	88.37	124.70	107.73	101.26

Table 7.2.12 1.8V NOR Ring-Oscillator: (Vdd=1.8V, unit=ps/gate)

B. 1.8V MVT R.O.

Temp	F.O.	TT	FF	SS	FNSP	SNFP
25C	1	32.43	28.81	37.27	32.99	32.36
125C	1	39.86	35.39	45.83	40.30	39.95
-40C	1	28.29	25.05	32.40	28.84	28.00
25C	3	66.78	59.65	76.26	67.79	66.66
125C	3	81.39	72.78	92.97	82.17	81.69
-40C	3	58.46	52.15	66.71	59.66	57.98

Table 7.2.13 1.8V MVT Inverter Ring-Oscillator: (Vdd=1.8V, unit=ps/gate)

Temp	F.O.	TT	FF	SS	FNSP	SNFP
25C	1	56.19	49.26	65.06	56.55	56.43
125C	1	70.43	61.74	81.63	70.81	70.79
-40C	1	47.48	41.90	54.84	48.21	47.59
25C	3	126.62	112.24	145.25	126.63	128.12
125C	3	158.17	140.16	181.66	157.88	160.40
-40C	3	107.67	95.71	123.17	107.98	108.60

Table 7.2.14 1.8V MVT NAND Ring-Oscillator: (Vdd=1.8V, unit=ps/gate)

Temp	F.O.	TT	FF	SS	FNSP	SNFP
25C	1	64.87	57.14	75.45	66.35	64.61
125C	1	80.37	70.47	92.71	81.34	79.99
-40C	1	55.93	49.18	64.85	57.36	55.25
25C	3	150.66	133.16	173.39	155.12	148.36
125C	3	184.71	163.63	212.24	189.37	182.81
-40C	3	130.06	115.14	150.16	134.83	127.57

Table 7.2.15 1.8V MVT NOR Ring-Oscillator: (Vdd=1.8V, unit=ps/gate)

C. 3.3V R.O.

Temp	F.O.	TT	FF	SS	FNSP	SNFP
25C	1	40.02	35.09	46.85	40.55	40.30

125C	1	46.67	40.65	54.88	47.00	47.27
-40C	1	35.04	30.88	40.77	35.55	35.25
25C	3	83.73	73.82	97.13	84.86	84.28
125C	3	96.85	85.00	113.19	97.65	98.16
-40C	3	73.64	65.42	84.77	74.79	74.09

Table 7.2.16 3.3V Inverter Ring-Oscillator: (Vdd=3.3V, unit=ps/gate)

Temp	F.O.	TT	SS	FNSP	SNFP	FF
25C	1	70.21	61.49	81.87	69.89	71.69
125C	1	84.03	73.11	98.74	83.38	86.21
-40C	1	60.72	53.47	70.17	60.66	61.74
25C	3	157.57	139.00	182.27	156.00	162.09
125C	3	187.92	164.57	219.07	185.39	194.26
-40C	3	136.40	121.26	156.64	135.44	139.98

Table 7.2.17 3.3V NAND Ring-Oscillator: (Vdd=3.3V, unit=ps/gate)

Temp	F.O.	TT	SS	FNSP	SNFP	FF
25C	1	83.09	72.18	98.35	85.28	82.58
125C	1	96.92	83.59	114.76	99.11	96.64
-40C	1	72.04	63.00	84.85	74.20	71.48
25C	3	194.27	169.44	228.26	201.02	191.28
125C	3	224.61	195.39	264.65	231.50	222.34
-40C	3	169.23	148.26	198.04	175.21	166.27

Table 7.2.18 3.3V NOR Ring-Oscillator: (Vdd=3.3V, unit=ps/gate)

7.2.7 1/f Noise Model

The noise sources in MOSFETs mainly covers 1/f noise (also known as flicker noise), channel thermal noise, gate noise, thermal noise due to physical resistances, and shot noise due to the gate dielectric tunneling current. The most occurred and influencing noise is the 1/f noise, thus we would address and model it in detail.

The flicker noise is a low-frequency (<100KHz) noise. Its physical mechanism is trapping / detrapping - related charge fluctuation in oxide traps, which results in fluctuations of both mobile carrier numbers and mobilities in the channel. The unified flicker noise model available from SMIC captures this physical process [3]. The wafer information for the flicker noise simulation is listed in Table 7.2.19.

Lot number	Wafer number
DL2291	1.8V MOS: #13
DL1737	1.8V MVT MOS: #5

	3.3V MOS: #5 3.3V MVT MOS: #5

Table 7.2.19 Wafer Information for 1/f Noise

BSIM4 offers two kinds of 1/f noise models: a simple one and a unified one. The simple flicker noise model is invoked when the model selector fnoiMod=0, which model is convenient for hand calculations. The unified physical flicker noise model, the default model, is invoked when fnoiMod = 1. SMIC adopts this model. The model incorporates both the fluctuation in the number of inversion layer carriers (number fluctuation) and the fluctuation in the Coulombic scattering mobility (mobility fluctuation). We investigate that they are correlated as both of them are caused by the fluctuation in the number of trapped charge in the SiO2 near the silicon/SiO2 interface.

To simulate the real situation, the noise density in the inversion region is expressed as:

$$S_{\mathrm{id},inv}(f)=\frac{k_B T q^2 \mu_{eff} I_{ds}}{C_{oxe}(L_{eff}-2\cdot LINTNOI)^2 A_{bulk} f^{ef}\cdot 10^{10}}\left(NOIA\log\left(\frac{N_0+N^*}{N_l+N^*}\right)+NOIB(N_0-N_l)+\frac{NOIC}{2}\left(N_0{}^2-N_l^2\right)\right)$$
$$+\frac{k_B T I_{ds}^2 \Delta L_{clm}}{W_{eff}\cdot(L_{eff}-2\cdot LINTNOI)^2 f^{ef}\cdot 10^{10}}\cdot\frac{NOIA+NOIB\cdot N_l+NOIC\cdot N_l{}^2}{(N_l+N^*)^2}$$

Where μ_{eff} is the effective mobility under the given bias condition, L_{eff} and W_{eff} are the effective channel length and width, respectively. The parameter N_0 is the charge density at the source side given by

$$N_0=C_{\mathrm{oxe}}\cdot V_{gsteff}/q$$

The parameter N_l is the charge density at the drain end given by

$$C_{\mathrm{oxe}}\cdot V_{gsteff}\cdot\left(1-\frac{A_{bulk}V_{dseff}}{V_{gsteff}+2V_t}\right)\Big/q$$

N^* is given by

$$N^*=\mathrm{k}_B T\cdot(C_{oxe}+C_d+CIT)/q^2$$

Where CIT (Interface Trap Capacitance) is a model parameter from $DCIV$ and C_{d} is the depletion capacitance.

ΔL_{clm} is the channel length reduction due to channel length modulation and given by

$$\Delta L_{\text{clm}} = Litl \cdot \log\left(\frac{\frac{V_{ds} - V_{dseff}}{Litl} + EM}{E_{sat}}\right)$$

$$E_{sat} = \frac{2VSAT}{\mu_{\text{eff}}}$$

In the sub-threshold region, the noise density is written as

$$S_{\text{id},subV_t}(f) = \frac{NOIA \cdot k_B T \cdot I_{ds}^2}{W_{eff} L_{eff} f^{ef} N^{*2} \cdot 10^{10}}$$

The total flicker noise density is

$$S_{\text{id}}(f) = \frac{S_{\text{id},inv}(f) \times S_{\text{id},subV_t}(f)}{S_{\text{id},subV_t}(f) + S_{\text{id},inv}(f)}.$$

The flicker noise measurement condition is shown as follows. We cover device operating region from weak inversion to strong inversion. Please refer to Table 7.2.20 for more information.

NMOS18 (NMOS18 in DNW)				
Vgs (V)	0.64	0.84	1.5	1.8
Vds (V)	0.6	0.9	1.8	
PMOS18(PMOS18 in DNW)				
Vgs (V)	-0.68	-0.88	-1.5	-1.8
Vds (V)	-0.6	-0.9	-1.8	
NMOS33				
Vgs (V)	0.85	1	1.5	3.3
Vds (V)	1.1	2.2	3.3	
PMOS33				
Vgs (V)	-0.85	-1	-1.5	-3.3
Vds (V)	-1.1	-2.2	-3.3	
Native NMOS18				
Vgs (V)	0.46	1.5	1.8	
Vds (V)	0.6	0.9	1.8	
Native NMOS33				
Vgs (V)	-0.1	0.5	1	3.3
Vds (V)	1.1	2.2	3.3	
NMOS MVT 18				

Vgs (V)	0.4	0.6	0.9	1.8
Vds (V)	0.6	1.2	1.8	
PMOS MVT 18				
Vgs (V)	-0.4	-0.6	-0.9	-1.8
Vds (V)	-0.6	-1.2	-1.8	
NMOS MVT 33				
Vgs (V)	0.6	1	1.5	3.3
Vds (V)	1.1	2.2	3.3	

Table 7.2.20 Measurement Conditions of 1.8V/3.3V MOS

7.2.8 LOD Stress Effect Model

Feature size aggressively scaling of MOSFETs makes LOD has been widely studied for its usage in active area isolation process in advanced technologies. In sub-100nm technology node, it's more challenging for LOD process, as with the scaling down, the MOSFET characteristics would become more sensitive to its effect. LOD stress effect influences numerous MOSFETs' characteristics, and SMIC's model for it primarily considers the stress influence on mobility, velocity saturation, threshold voltage, body effect and DIBL effect. After decades of experiments, the experts find that different mechanisms could have influences on the device characteristics: one is mobility-related that is induced by the band structure modification; the other is Vth-related that is resulted from doping profile variation. The modeling method of SMIC is derived based on these phenomenons. The lot and wafer information are shown in Table 7.2.40.

Lot number	Wafer number
DL2063	1.8V MOS: #5 3.3V MOS: #5

Table 7.2.21 Wafer Information for LOD Stress Effect Model

To simulate the LOD, 1.8V N/PMOS, 1.8V MVT N/PMOS, 1.8V Native NMOS, IO 3.3V N/PMOS, 3.3V Native NMOS, 3.3V MVT NMOS are measured and modeled, and their model parameters are shown in Table 7.2.22:

Parameters	n18_ckt	p18_ckt	nnt18_ckt	n33_ckt	p33_ckt	nmvt18_ckt	pmvt18_ckt	nmvt33_ckt	nnt33_ckt
saref	4.48E-06	4.48E-06	4.54E-06	5.33E-06	5.33E-06	4.54E-06	4.54E-06	4.54E-06	4.54E-06
sbref	4.48E-06	4.48E-06	4.54E-06	5.33E-06	5.33E-06	4.54E-06	4.54E-06	4.54E-06	4.54E-06
wlod	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
ku0	-4.50E-08	8.00E-08	-2.70E-08	-2.00E-08	8.10E-08	-4.80E-08	1.08E-07	-2.40E-08	-6.00E-08
kvsat	1.00E+00	0.00E+00	1.00E+00	1.00E+00	1.00E+00	1.00E+00	1.00E+00	1.00E+00	1.00E+00
tku0	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
lku0	7.00E-07	1.50E-07	1.00E-09	5.00E-07	2.80E-07	5.00E-07	7.50E-07	5.00E-07	5.00E-07
wku0	5.00E-07	0.00E+00	1.00E-09	1.00E-06	-7.00E-08	1.00E-06	0.00E+00	1.00E-06	1.00E-06
pku0	7.00E-13	2.00E-14	0.00E+00	0.00E+00	-1.20E-14	0.00E+00	-1.93E-13	0.00E+00	0.00E+00

llodku0	1.00E+00	1.00E+00	1.30E+00	1.00E+00	1.00E+00	1.00E+00	1.00E+00	1.00E+00	1.00E+00
wlodku0	1.00E+00	1.00E+00	1.50E+00	1.00E+00	1.00E+00	1.00E+00	1.00E+00	1.00E+00	1.00E+00
kvth0	3.50E-09	-1.00E-10	8.00E-08	6.00E-09	1.00E-09	5.00E-09	-1.45E-08	7.00E-09	3.00E-09
lkvth0	-6.00E-08	-1.00E-07	2.80E-09	2.00E-07	2.90E-07	2.00E-07	4.00E-07	2.00E-07	2.00E-07
wkvth0	1.00E-07	-2.00E-07	1.00E-09	-5.00E-08	5.00E-06	-5.00E-08	-1.02E-07	-5.00E-08	-5.00E-08
pkvth0	2.00E-14	2.00E-14	0.00E+00	0.00E+00	0.00E+00	0.00E+00	-1.00E-14	0.00E+00	0.00E+00
llodvth	1.00E+00	1.00E+00	1.50E+00	1.00E+00	1.00E+00	1.00E+00	1.00E+00	1.10E+00	1.00E+00
wlodvth	1.00E+00	1.00E+00	1.55E+00	1.00E+00	1.00E+00	1.00E+00	1.00E+00	1.00E+00	1.00E+00
stk2	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
lodk2	1.00E+00	1.00E+00	1.00E+00	1.00E+00	1.00E+00	1.00E+00	1.00E+00	1.00E+00	1.00E+00
steta0	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
lodeta0	1.00E+00	1.00E+00	1.00E+00	1.00E+00	1.00E+00	1.00E+00	1.00E+00	1.00E+00	1.00E+00

Table 7.2.22 Model Parameters for LOD

7.3 Bipolar Gummel-Poon Model

7.3.1 Wafer Information

The transistors for Bipolar Junction Transistor (BJT) SPICE modeling include vertical 1.8V/3.3V NPN/PNP BJT with fixed emitter area of 1.6*1.6, 2*2, 5*5 and 10*10um^2. The silicon data are extracted from golden wafer, which is 12 inches with dies between 60 and 70. The data is provided by the Wafer Acceptance Test (WAT) team: determining the golden die whose median value (Beta , V_{BE}, I_C , I_B and I_S) almost approximates that of mapping data and then sweeping IV and CV curves to obtain the measured data. Their lot and wafer information are listed in the Table 7.3.1:

Lot number	Wafer number
DL2271	#1

Table 7.3.1 Wafer Information of BJT

BJT is a kind of vertical triode and also a parasitic device, consisting of Collector (C), Base (B) and Emitter (E), as shown in Fig7.3.1. BJT is not scalable in model, and hence, this section investigates BJT (1.05V and 1.8V) with different emitter areas, each area of every type of BJT being simulated by one unique model.

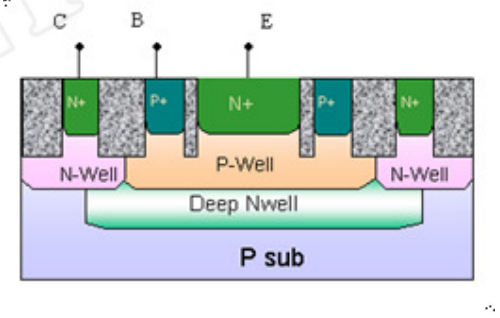


Fig 7.3.1 The cross section of BJT (NPN)

7.3.2 Capability of Model

The BJT modeling in this technology node covers three fixed corner models: BJT_TT, BJT_FF and BJT_SS, which would be discussed in detail in the flowing section.

The measurement and modeling method used for BJT is basically the same with the method applied in the MOSFETs, but as BJT is a kind of device that is not scalable (fixed geometry) in model, three single

models are used in this technology node to simulate every type of BJTs.

According to the industry standard of general devices, for measurement and modeling of BJTs, the ambient temperature ranges from -40°C to 125°C.

HSPICE bipolar Gummel-Poon Level-1 model is used to simulate BJT models. The Gummel-Poon model is the most widely used bipolar transistor model since its emergence in the early seventies. The model is based on a new, general charge-control relation connecting collector current, junction voltages and base charge.

For bipolar transistors, this model has proved very successful in dependent current generators replaced by time-dependent analysis of non-critical circuits; i.e., circuits in which the performance is dominated by passive feedback. Accurate modeling by this technique requires large numbers of parameters and is a more accurate curve-fitting approach than a physics-based representation of the transistor [12].

PNP BJT parameters are extracted from a vertical P+/Nwell/Psub test structure, and NPN BJT parameters are extracted from a vertical N+/PWELL/DNWELL test structure, as shown below in Fig. 7.3.2 and Fig. 7.3.3.

As we all know that BJT model is usually not scalable, we provide 1.8V models: pnp18a100, pnp18a25, pnp18a4, npn18a100, npn18a25, npn18a4, and 3.3V models: pnp33a100, pnp33a25, pnp33a4, npn33a100, npn33a25ll, npn33a4, with each extracted from different emitter areas. The structure and dimension (physical size) are shown below.

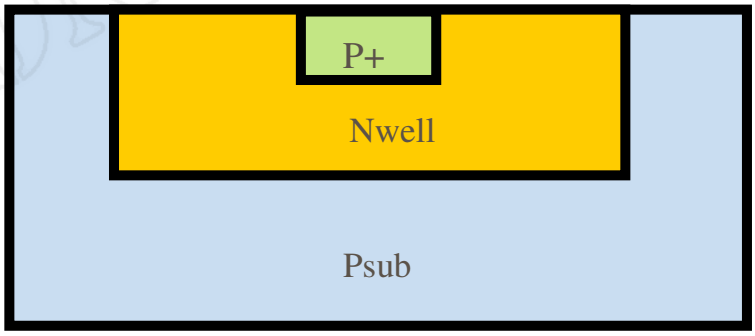


Fig 7.3.2 The cross section of PNP BJT

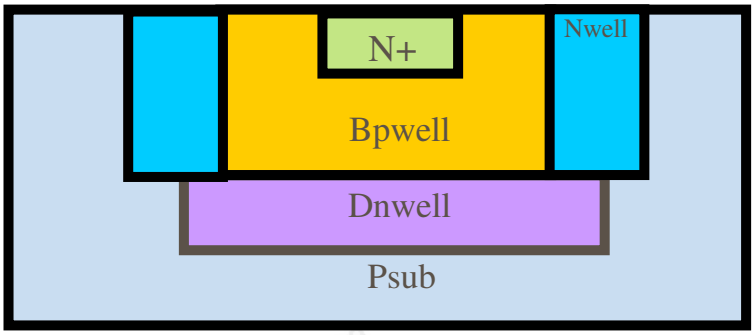


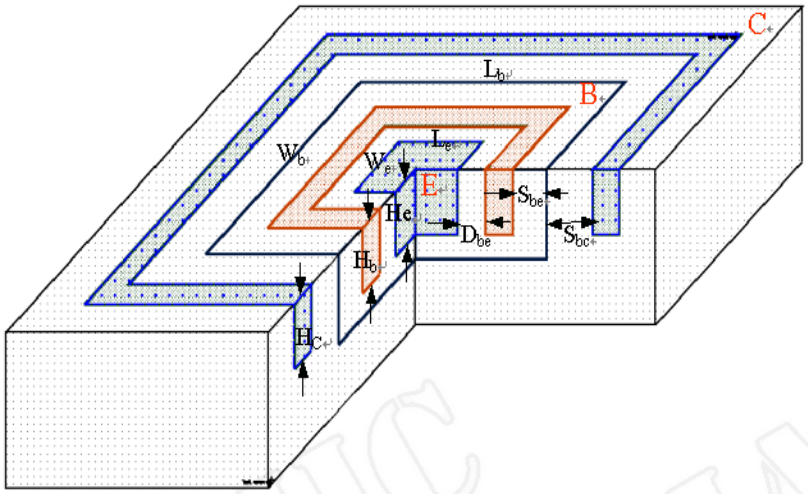
Fig 7.3.3 The cross section of NPN BJT

The dimensions used in BJT's model equations are given in Table 7.3.2.

Model Name	Vdd	Dimension [um]								
		Le	We	He/Hc	Lb	Wb	Hb	Dbe	Sbe	Sbc
pnp18a100	1.8V	10	10	0.1	12	12	0.085	0.6	0.2	0.1
pnp18a25	1.8V	5	5	0.1	7	7	0.085	0.6	0.2	0.1
pnp18a4	1.8V	2	2	0.1	4	4	0.085	0.6	0.2	0.1
pnp33a100	3.3V	10	10	0.15	12	12	0.2	0.6	0.2	0.1
pnp33a25	3.3V	5	5	0.15	7	7	0.2	0.6	0.2	0.1
pnp33a4	3.3V	2	2	0.15	4	4	0.2	0.6	0.2	0.1
npn18a100	1.8V	10	10	0.1	12	12	0.085	0.6	0.2	0.1
npn18a25	1.8V	5	5	0.1	7	7	0.085	0.6	0.2	0.1
npn18a4	1.8V	2	2	0.1	4	4	0.085	0.6	0.2	0.1
npn33a100	3.3V	10	10	0.15	12	12	0.2	0.6	0.2	0.1
npn33a25	3.3V	5	5	0.15	7	7	0.2	0.6	0.2	0.1
npn33a4	3.3V	2	2	0.15	4	4	0.2	0.6	0.2	0.1

Table 7.3.2 Dimensions of BJT Model

Semiconductor Manufacturing International Corporation



Where

Le	Length of emitter
We	Width of emitter
He/Hc	Junction depth ratio of emitter and collector
Lb	Length of base
Wb	Width of base
Hb	Junction depth of base
Dbe	Distance between base-AA to emitter-AA
Sbe	Space of base edge to base-AA
Sbc	Space of base edge to collector-AA

7.3.3 Fixed Corner Model of BJT

Variations of BJT process parameters (e.g. doping fluctuation, etching rate, photolithography misalignment) could result in process variations. The process variations then lead to device parameters variations, thus device fixed corner models are applied to simulate the best/worst-case circuit performance based on process variations. The typical key bipolar parameters are varied for bipolar fixed corner models, and some of the parameters share the same physical background such that one can't use arbitrary high/low combinations for fixed corner modeling. The provided fixed corner models by SMIC are primarily for predicting most important corner cases: BJT_TT, BJT_FF and BJT_SS, whose definitions are listed in Table 7.3.3.

Fixed corner model	Definition
BJT_TT	Typical model, for Nominal process modeling
BJT_FF	Fast corner. Performance corner for best cases of the static BJT circuit, including both global (e.g. chip to chip) and local (e.g. mismatch) variations.
BJT_SS	Slow corner. Performance corner for worst cases of the static BJT circuit, including both global (e.g. wafer to wafer) and local (e.g. mismatch) variations.

Table 7.3.3 Fixed corner model Definition of BJT

Table 7.3.4-Table 7.3.7 show the values of the data for compensating the corner cases of every device.

Parameters	UNIT	BJT_TT	BJT_FF	BJT_SS
dbf_pnp18a100	-	0	0.4118	-0.4118
dis_pnp18a100	A	0	3.74E-18	-3.74E-18
dnf_pnp18a100	-	0	-5.02E-03	5.02E-03
dbf_pnp18a25	-	0	0.4072	-0.4072
dis_pnp18a25	A	0	9.44E-19	-9.44E-19
dnf_pnp18a25	-	0	-5.00E-03	5.00E-03
dbf_pnp18a4	-	0	0.4095	-0.4095
dis_pnp18a4	A	0	1.86E-19	-1.86E-19
dnf_pnp18a4	-	0	-5.00E-03	5.00E-03
dcje_pnp18a100	F	0	-5.65E-15	5.65E-15
dcje_pnp18a25	-	0	-1.41E-15	1.41E-15
dcje_pnp18a4	-	0	-2.26E-16	2.26E-16
dcjc_pnp18a100	F	0	-1.68E-15	1.68E-15

dcjc_pnp18a25	-	0	-7.93E-16	7.93E-16
dcjc_pnp18a4	-	0	-4.19E-16	4.19E-16
drb_pnp18a100	ohm	0	-12.08	12.08
drb_pnp18a25	ohm	0	-14.08	14.08
drb_pnp18a4	ohm	0	-21.49	21.49
dre_pnp18a100	ohm	0	-0.2233	0.2233
dre_pnp18a25	ohm	0	-0.414	0.414
dre_pnp18a4	ohm	0	-0.362	0.362
drc_pnp18a100	ohm	0	-3.422	3.422
drc_pnp18a25	ohm	0	-3.422	3.422
drc_pnp18a4	ohm	0	-2.423	2.423
drbm_pnp18a100	ohm	0	-0.4	0.4
drbm_pnp18a25	ohm	0	-0.4	0.4
drbm_pnp18a4	ohm	0	-0.4	0.4
dikf_pnp18a100	A	0	4.00E-04	-4.00E-04
dikf_pnp18a25	A	0	1.80E-04	-1.80E-04
dikf_pnp18a4	A	0	5.00E-05	-5.00E-05

Table 7.3.4 Corner model parameters of 1.8V PNP-BJT

Parameters	UNIT	BJT_TT	BJT_FF	BJT_SS
dnf_pnp33a100	-	0	-5.03E-03	5.03E-03
dnf_pnp33a25	-	0	-4.98E-03	4.98E-03
dnf_pnp33a4	-	0	-5.00E-03	5.00E-03
dcje_pnp33a100	F	0	-5.20E-15	5.20E-15
dcje_pnp33a25	F	0	-1.31E-15	1.31E-15
dcje_pnp33a4	F	0	-2.09E-16	2.09E-16
dcjc_pnp33a100	F	0	-1.68E-15	1.68E-15
dcjc_pnp33a25	F	0	-7.93E-16	7.93E-16
dcjc_pnp33a4	F	0	-4.19E-16	4.19E-16
dbf_pnp33a100	-	0	0.4335	-0.4335
dbf_pnp33a25	-	0	0.4277	-0.4277
dbf_pnp33a4	-	0	0.4276	-0.4276
dis_pnp33a100	A	0	4.16E-18	-4.16E-18
dis_pnp33a25	A	0	9.84E-19	-9.84E-19
dis_pnp33a4	A	0	1.83E-19	-1.83E-19
drb_pnp33a100	ohm	0	-10.73	10.73
drb_pnp33a25	ohm	0	-14.08	14.08
drb_pnp33a4	ohm	0	-21.49	21.49
dre_pnp33a100	ohm	0	-0.4353	0.4353

dre_pnp33a25	ohm	0	-0.69	0.69
dre_pnp33a4	ohm	0	-0.362	0.362
drc_pnp33a100	ohm	0	-3.86	3.86
drc_pnp33a25	ohm	0	-3.422	3.422
drc_pnp33a4	ohm	0	-2.423	2.423
drbm_pnp33a100	ohm	0	-0.4	0.4
drbm_pnp33a25	ohm	0	-0.4	0.4
drbm_pnp33a4	ohm	0	-0.4	0.4
dikf_pnp33a100	A	0	4.00E-04	-4.00E-04
dikf_pnp33a25	A	0	2.00E-04	-2.00E-04
dikf_pnp33a4	A	0	5.00E-05	-5.00E-05

Table 7.3.5 Corner model parameters of 3.3V PNP-BJT

Parameters	UNIT	BJT_TT	BJT_FF	BJT_SS
dbf_npn18a100	-	0	2.977	-2.977
dis_npn18a100	A	0	1.00E-17	-1.00E-17
dnf_npn18a100	-	0	-5.03E-03	5.03E-03
dbf_npn18a25	-	0	3.126	-3.126
dis_npn18a25	A	0	2.95E-18	-2.95E-18
dnf_npn18a25	-	0	-5.03E-03	5.03E-03
dbf_npn18a4	-	0	3.315	-3.315
dis_npn18a4	A	0	5.08E-19	-5.08E-19
dnf_npn18a4	-	0	-5.01E-03	5.01E-03
dcje_npn18a100	F	0	-4.94E-15	4.94E-15
dcje_npn18a25	-	0	-1.24E-15	1.24E-15
dcje_npn18a4	-	0	-1.98E-16	1.98E-16
dcjc_npn18a100	F	0	-6.40E-15	6.40E-15
dcjc_npn18a25	-	0	-3.02E-15	3.02E-15
dcjc_npn18a4	-	0	-1.60E-15	1.60E-15
drb_npn18a100	ohm	0	-0.09356	0.09356
drb_npn18a25	ohm	0	-10.37	10.37
drb_npn18a4	ohm	0	-2.806	2.806
dre_npn18a100	ohm	0	-1.685	1.685
dre_npn18a25	ohm	0	-2.954	2.954
dre_npn18a4	ohm	0	-7.29	7.29
drc_npn18a100	ohm	0	-1.918	1.918
drc_npn18a25	ohm	0	-1.584	1.584
drc_npn18a4	ohm	0	-5.3	5.3
drbm_npn18a100	ohm	0	-0.02	0.02
drbm_npn18a25	ohm	0	-0.02	0.02

drbm_npn18a4	ohm	0	-0.02	0.02
dikf_npn18a100	A	0	9.00E-03	-9.00E-03
dikf_npn18a25	A	0	2.00E-03	-2.00E-03
dikf_npn18a4	A	0	2.00E-04	-2.00E-04

Table 7.3.6 Corner model parameters of 1.8V NPN-BJT

Parameters	UNIT	BJT_TT	BJT_FF	BJT_SS
dnf_npn33a100	-	0	-5.04E-03	5.04E-03
dnf_npn33a25	-	0	-5.00E-03	5.00E-03
dnf_npn33a4	-	0	-5.00E-03	5.00E-03
dcje_npn33a100	F	0	-4.31E-15	4.31E-15
dcje_npn33a25	F	0	-1.08E-15	1.08E-15
dcje_npn33a4	F	0	-1.72E-16	1.72E-16
dcjc_npn33a100	F	0	-6.38E-15	6.38E-15
dcjc_npn33a25	F	0	-3.02E-15	3.02E-15
dcjc_npn33a4	F	0	-1.60E-15	1.60E-15
dbf_npn33a100	-	0	3.831	-3.831
dbf_npn33a25	-	0	4.11	-4.11
dbf_npn33a4	-	0	4.389	-4.389
dis_npn33a100	A	0	1.36E-17	-1.36E-17
dis_npn33a25	A	0	3.03E-18	-3.03E-18
dis_npn33a4	A	0	6.19E-19	-6.19E-19
drb_npn33a100	ohm	0	-12.97	12.97
drb_npn33a25	ohm	0	-10.89	10.89
drb_npn33a4	ohm	0	-24.36	24.36
dre_npn33a100	ohm	0	-0.96	0.96
dre_npn33a25	ohm	0	-2.496	2.496
dre_npn33a4	ohm	0	-6.49	6.49
drc_npn33a100	ohm	0	-0.214	0.214
drc_npn33a25	ohm	0	-0.1616	0.1616
drc_npn33a4	ohm	0	-0.2192	0.2192
drbm_npn33a100	ohm	0	-0.02	0.02
drbm_npn33a25	ohm	0	-0.02	0.02
drbm_npn33a4	ohm	0	-0.02	0.02
dikf_npn33a100	A	0	0.03	-0.03
dikf_npn33a25	A	0	1.10E-03	-1.10E-03
dikf_npn33a4	A	0	1.40E-04	-1.40E-04

Table 7.3.7 Corner model parameters of 1.8V NPN-BJT

7.4 Diode Model

7.4.1 Wafer Information

The junction diode SPICE modeling test structures include 1.8V/3.3V N+/Pwell, P+/Nwell; 1.8V MVT N+/Pwell and P+/Nwell; 1.8V Nwell/Psub, Buried Pwell/Deep Nwell, and DNwell/Psub; and 3.3V MVT N+/Pwell, parasitic Nwell/Psub, Buried Pwell/DNwell, and DNwell/Psub, 1.8V N+/PSUB, 3.3V N+/PSUB. Every type of diodes employs area type structure and finger type structure, as shown in Fig 7.4.1 and Fig 7.4.2.

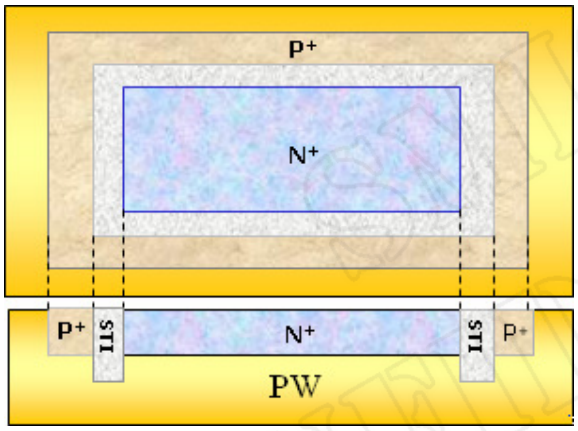


Fig 7.4.1 Area type structure of diode

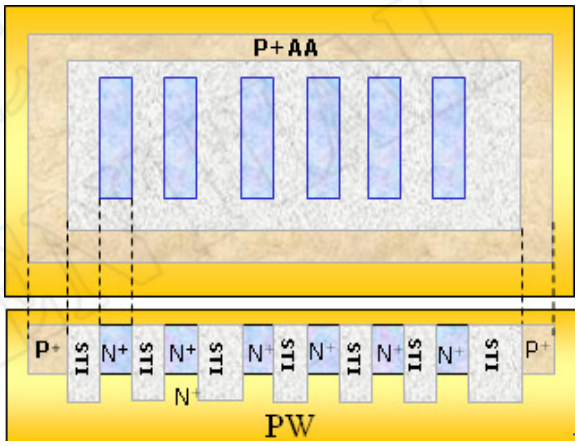


Fig 7.4.2 Finger type structure of diode

The silicon data of the junction diode are extracted from golden wafer， and the wafer is 8 inches with 26 dies. The data is provided by the Wafer Acceptance Test (WAT) team: determining the golden die whose median value (N_f ， J_s and Cj) almost approximates that of mapping data and then sweeping IV and CV curves to obtain the measured data. Their lot and wafer information are listed in Table 7.4.1:

Lot number	Wafer number
DL2271	#1
DL1737	#5

Table 7.4.1 Wafer Information for Diode

7.4.2 Capability of Model

The diode modeling in this technology node covers three fixed corner models: DIO_TT, DIO_FF and DIO_SS, which would be discussed in detail in the flowing section.

According to the industry standard of general devices, for the measurement and modeling of junction diode, the ambient temperature ranges from -40°C to 125°C. In this version of the technology node, we

model the diodes devices with HSPICE Diode Level-3 model, which is a charge-control-approach-based model.

7.4.3 Fixed Corner Model of Diode

The process variation occurs due to the variation of process parameters, for example changes of etching rate, photolithography misalignment, dopant fluctuation, and day-to-day operating status of foundry equipments and more all can result in process variation, which would lead to device parameters variations. Therefore device fixed corner models are used to simulate the best/worst-case circuit performance in light of process variations. The provided fixed corner models by SMIC are primarily for predicting most important corner cases: DIO_TT, DIO_FF and DIO_SS. Their definitions are listed in Table 7.4.2.

Fixed corner model	Definition
DIO_TT	Typical model, for Nominal process modeling
DIO_FF	Fast corner. Performance corner for best cases of the static diode circuit, including both global (e.g. chip to chip) and local (e.g. mismatch) variations.
DIO_SS	Slow corner. Performance corner for worst cases of the static diode circuit, including both global (e.g. wafer to wafer) and local (e.g. mismatch) variations.

Table 7.4.2 Fixed corner model Definition of Diode

Table 7.4.3-Table 7.4.8 shows the values of the data for compensating the corner cases of every device.

A. 1.8V and 1.8V MVT N+/Pwell, P+/Nwell,

Parameters	Unit	TT	FF	SS
djs_ndio18	A/m^2	0	3.45E-07	-3.45E-07
djsw_ndio18	A/m	0	7.10E-15	-7.10E-15
dn_ndio18	-	0	-1.13E-02	1.13E-02
dcj_ndio18	F/ m^2	0	-4.94E-05	4.94E-05
dcjsw_ndio18	F/m	0	-2.91E-12	2.91E-12
dis_pdio18	A/m^2	0	2.85E-08	-2.85E-08
djsw_pdio18	A/m^2	0	1.50E-14	-1.50E-14
dn_pdio18	-	0	-9.98E-03	9.98E-03
dcj_pdio18	F/ m^2	0	-5.64E-05	5.64E-05
dcjp_pdio18	F/m	0	-4.85E-12	4.85E-12
djs_ndiomvt18	A/m^2	0	1.77E-07	-1.77E-07
dn_ndiomvt18	-	0	-1.06E-02	1.06E-02
djsw_ndiomvt18	A/m	0	1.98E-13	-1.98E-13
dcj_ndiomvt18	F/ m^2	0	-4.68E-05	4.68E-05
dcjsw_ndiomvt18	F/m	0	-3.02E-12	3.02E-12

dis_pdiomvt18	A/m^2	0	9.15E-08	-9.15E-08
djsw_pdiomvt18	A/m	0	1.04E-13	-1.04E-13
dn_pdiomvt18	-	0	-1.05E-02	1.05E-02
dcj_pdiomvt18	F/ m^2	0	-3.93E-05	3.93E-05
dcjp_pdiomvt18	F/m	0	-2.49E-12	2.49E-12

Table 7.4.3 Fixed corner model parameters of 1.8V Diode

B. 3.3V N+/Pwell, P+/Nwell and 3.3V MVT N+/Pwell

Parameters	Unit	TT	FF	SS
djs_ndio33	A/m^2	0	1.26E-07	-1.26E-07
dn_ndio33	-	0	-1.03E-02	1.03E-02
djsw_ndio33	A/m	0	1.98E-13	-1.98E-13
dcj_ndio33	F/ m^2	0	-4.31E-05	4.31E-05
dcjsw_ndio33	F/m	0	-4.84E-12	4.84E-12
dis_pdio33	A/m^2	0	3.18E-08	-3.18E-08
djsw_pdio33	A/m	0	2.49E-14	-2.49E-14
dn_pdio33	-	0	-9.99E-03	9.99E-03
dcj_pdio33	F/ m^2	0	-5.22E-05	5.22E-05
dcjp_pdio33	F/m	0	-4.29E-12	4.29E-12
djs_ndiomvt33	A/m^2	0	2.79E-07	-2.79E-07
dn_ndiomvt33	-	0	-1.06E-02	1.06E-02
djsw_ndiomvt33	A/m	0	9.88E-14	-9.88E-14
dcj_ndiomvt33	F/ m^2	0	-4.32E-05	4.32E-05
dcjsw_ndiomvt33	F/m	0	-5.36E-12	5.36E-12

Table 7.4.3 Fixed corner model parameters of 3.3V Diode

C. Nwell/Psub, Pwell/DNW and DNW/Psub

Parameters	Unit	TT	FF	SS
dis_nwdio	A/m^2	0	7.12E-07	-7.12E-07
djsw_nwdio	A/m	0	1.46E-14	-1.46E-14
dn_nwdio	-	0	-1.09E-02	1.09E-02
dcj_nwdio	F/ m^2	0	-6.55E-06	6.55E-06
dcjp_nwdio	F/m	0	-2.50E-11	2.50E-11
djs_diobpw	A/m^2	0	3.12E-07	-3.12E-07
djsw_diobpw	-	0	7.02E-14	-7.02E-14
dn_diobpw	A/m	0	-1.12E-02	1.12E-02
dcj_diobpw	F/ m^2	0	-2.49E-05	2.49E-05
dcjsw_diobpw	F/m	0	-1.99E-11	1.99E-11
djs_dnwdio	A/m^2	0	3.05E-07	-3.05E-07

djsw_dnwdio	-	0	5.50E-16	-5.50E-16
dn_dnwdio	A/m	0	-9.79E-03	9.79E-03
dcj_dnwdio	F/ m^2	0	-6.91E-06	6.91E-06
dcjsw_dnwdio	F/m	0	-3.37E-11	3.37E-11

Table 7.4.3 Fixed corner model parameters of Well Diode

D. 1.8V and 3.3V N+/PSUB Diode

Parameters	Unit	TT	FF	SS
dis_nndio18	A/m^2	0	1.56E-06	-1.56E-06
djsw_nndio18	A/m	0	3.00E-14	-3.00E-14
dn_nndio18	-	0	-1.07E-02	1.07E-02
dcj_nndio18	F/ m^2	0	-9.92E-06	9.92E-06
dcjp_nndio18	F/m	0	-5.54E-12	5.54E-12
djs_nndio33	A/m^2	0	1.12E-06	-1.12E-06
dn_nndio33	-	0	-1.06E-02	1.06E-02
djsw_nndio33	A/m	0	1.98E-12	-1.98E-12
dcj_nndio33	F/ m^2	0	-6.58E-06	6.58E-06
dcjsw_nndio33	F/m	0	-1.07E-11	1.07E-11

7.5 Interconnection Table

For advanced technology node, a large of significant part of the chip area is occupied by interconnections between blocks and electrical components. Parameters of these interconnection lines have effects (delay, crosstalk and more) on electrical parameters of chips and are crucial to the characteristics of the circuit, and hence, precise reproduction of interconnection parasitic elements is indispensable in the circuit design. Parasitic elements cover resistances, capacitances and inductances [13]. The resistor model will be discussed in the next section and the parasitic inductor exists under high frequency which would not be further mentioned in this report, therefore we'll discuss capacitances only in this section.

7.5.1 Related Process Data and Information for Interconnection

The data of interconnection is provided by the PIE team. The related process data and the necessary information of conductor layer and dielectric layer are shown in Table 7.5.1 and Table 7.5.2.

A. Conductor layers

Conductor Name	Typical Thickness (A)	Variation (±%) (3 sigma)	Min. Width (um)	Variation (±%) (3 sigma)	Min. Space (um)
MTT2	40650	10%	2.6	2.5	2.5
MTT1	34100	10%	1.8	1.8	1.8
TM2	22000	10%	1.5	10%	1.5
M6	9825	10%	0.44	10%	0.46
MIM	2000	10%	4	10%	1.2
M5	5500	10%	0.28	10%	0.28
M4	5500	10%	0.28	10%	0.28
M3	5500	10%	0.28	10%	0.28
M2	5500	10%	0.28	10%	0.28
M1	5500	10%	0.23	10%	0.23

Table 7.5.1 Conductor layers information

Note：There is only one top metal in this technology; M6 and TM2, MTT1, MTT2 are provided for different top metal thickness options. Can't be both chosen at the same time.

B. Dielectric layers

Dielectric Name	Typical Thickness (A)	Variation(±%) (3 sigma)	Dielectric Constant
Pass2 (for thick top metal)	6000(SiN)	(+/-10%)	7.9
Pass1 (for thick top metal)	600(SRO)+ 30500(HDP Ox) +5000(SRO)	(+/-10%)	HDP Ox 4.2/SRO 4.2
Pass2 (for thin top metal)	6000(SiN)	(+/-10%)	7.9
Pass1 (for thin top metal)	10000(HDP Ox) +1500(SRO)	(+/-10%)	HDP Ox 4.2/SRO 4.2
IMD5b	3500(USG)	(USG:+/-3%)	USG 4.2
IMD5a	12000(FSG)	(FSG:+/-20%	FSG 3.7
IMD4b	2000(USG)	(USG:+/-3%)	USG 4.2
IMD4a	12000(FSG)	(FSG:+/-20%	FSG 3.7
IMD3b	2000(USG)	(USG:+/-3%)	USG 4.2
IMD3a	12000(FSG)	(FSG:+/-20%	FSG 3.7
IMD2b	2000(USG)	(USG:+/-3%)	USG 4.2
IMD2a	12000(FS G)	(FSG:+/-20%)	FSG 3.7
IMD1b	2000(USG)	(USG:+/-3%)	USG 4.2
IMD1a	12000(FSG)	(FSG:+/-20%)	FSG 3.7
ILD1b	2000(BP TEOS) + 5500(PE TEOS)	(+/-20%)	4.2
ILD1a	400(SiN)	(+/-10%)	4.3
STI	3500	(+/-17%)	4

Table 7.5.2 Dielectric layers information

Semiconductor Manufacturing International Corporation

Doc. No.: TD-MM18-SP-2004	Doc. Title: 0.18um Mixed Signal Enhanced 1.8V/3.3V SPICE Model	Doc.Rev: 2R	Tech Dev Rev: 1.11	Page No.: 48/90

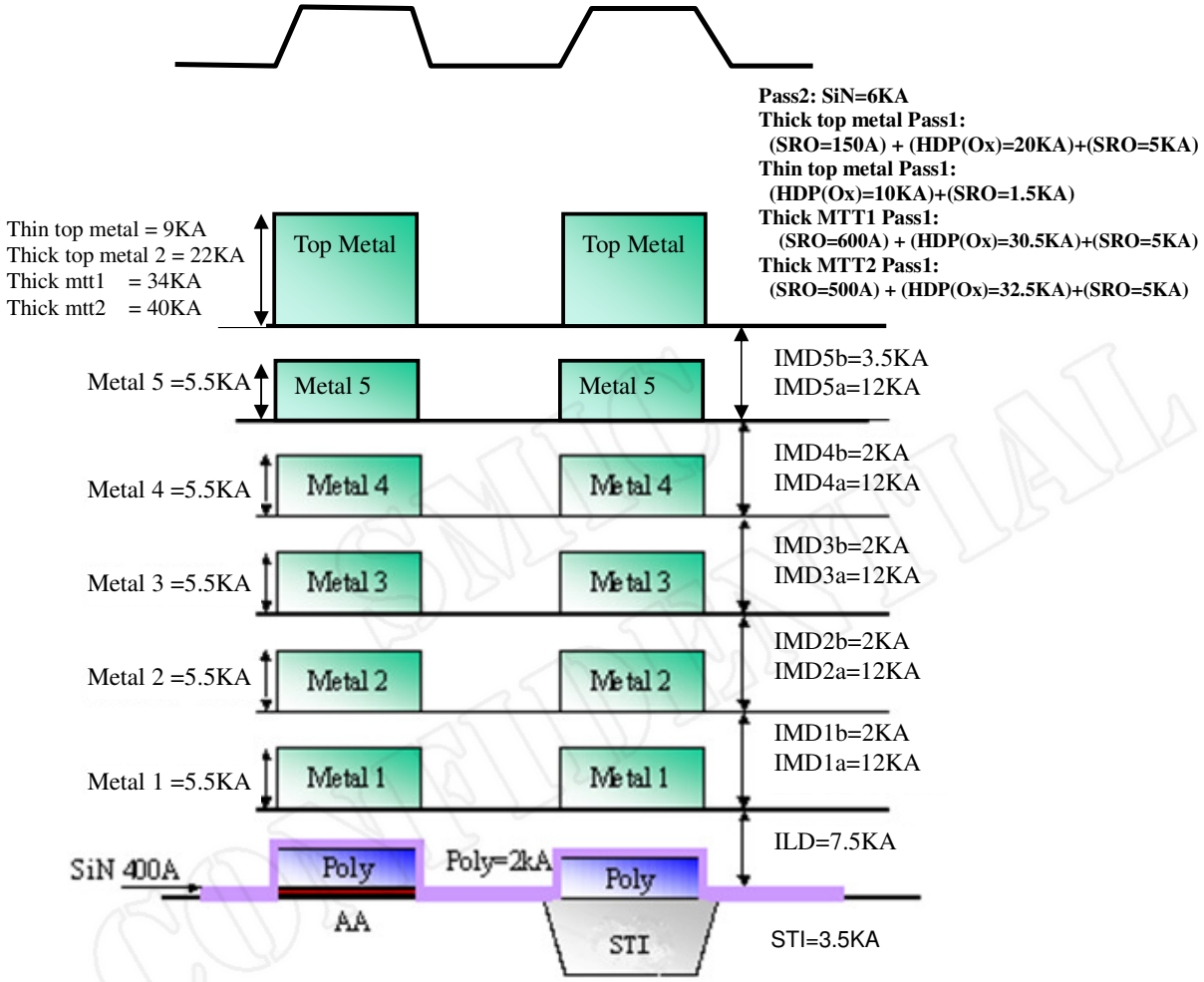


Fig 7.5.1 Cross Section of Interconnection Structures

7.5.2 Capability of Model

The SMIC model team uses Synopsys's Raphael simulation for calculating interconnection capacitance, which is a theoretical calculating method based on the back end of the line (BEOL) structure. The method is usually more convenient and affordable than direct measurements. Although a bus may include many interconnection lines, it's a simple analytical method that only the closest lines are taken into account. Two types of structures are tested: parallel lines on one plane (structure-1) and between two planes (structure-2). The simulation results of typical, fast and slow cases for both structure-1 and structure-2 are listed in a separate file. (Please refer to the attachment: ms018_enhanced_ v1p11_interconnect_structure1.txt, ms018_enhanced_ v1p11_interconnect_structure2.txt.)

The structures and definition of each capacitance component for structure 1 and structure 2 are illustrated in Fig 7.5.2 and Fig 7.5.3:

Structure 1 represents (a) conduction lines above an infinite ground plane as shown below.

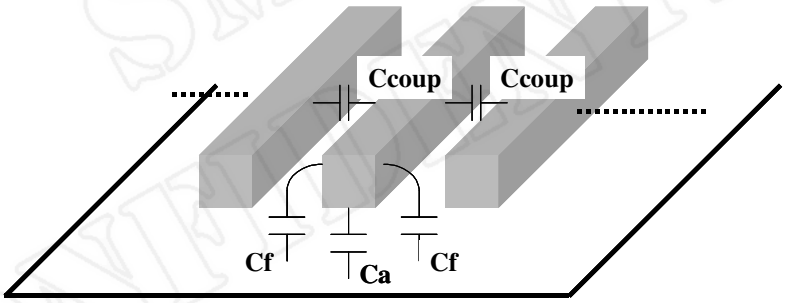


Fig.7.5.2 Lines above an infinite ground plane

*** Definitions of various capacitances:

Ctotal [fF/um]: total capacitance of a conductor to all others.

Ccoup [fF/um]: coupling capacitance between two conductors in the same layer.

Cbottom [fF/um]: capacitance between a conductor and the bottom ground plane. (=Ca+2*Cf)

Cf [fF/um]: fringing capacitance.

Structure 2 represents (b) conduction lines between two infinite ground planes as shown below.

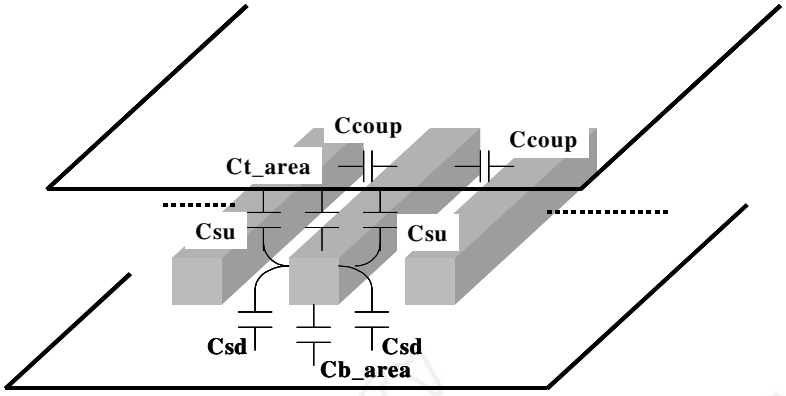


Fig. 7.5.3 Lines between two infinite ground planes

*** Definitions of various capacitances:

Ctotal [fF/um]:	total capacitance of a conductor to all others.
Ccoup [fF/um]:	coupling capacitance between two conductors in the same layer.
Cbottom [fF/um]:	capacitance between a conductor and the bottom ground plane. (=Cb_area+2*Csd)
Ctop[fF/um]:	capacitance between a conductor and the top ground plane. (=Ct_area+2*Csu)
Csd[fF/um]:	Side-wall down capacitance coefficient.
Csu[fF/um]:	Side-wall up capacitance coefficient.

7.5.3 Corner Cases of Interconnection Capacitance

Two corner cases of interconnection capacitance are simulated: one is slow resistance and fast capacitance, and the other is fast resistance and slow capacitance.

For slow resistance and fast capacitance: Thickness = (1- process variation) * typical thickness; Width = (1- process variation) * typical width;

For fast resistance and slow capacitance: Thickness = (1 + process variation) * typical thickness; Width = (1+ process variation) * typical width;

The minimum or maximum dielectric thickness is computed by subtracting or adding the statistical sum of all dielectric thickness variations between the two layers of interest.

Let $\Delta T_{total} = \sqrt{\sum_i (\Delta t_i)^2}$, where ΔT_{total} is the effective total variation between two layers, and Δt_i is the variation of interlayer dielectrics among metal, air, and substrates.

$\Delta t_i = T_i * \beta_i$, where T_i is the dielectric thickness and β_i is the thickness variation.

$TH_i = T_i \pm \Delta T_{total} * \frac{\Delta T_i}{\sum_i T_i * \beta_i}$, where TH_i is the final thickness of the dielectric[12].

7.6 Resistor Model

7.6.1 Wafer Information

The silicon data of resistors are extracted from golden wafer, and the wafer is 8 inches with 26 dies. The data is provided by the Wafer Acceptance Test (WAT) team: determining the golden die whose median value (R_{sh}) almost approximates that of mapping data and then sweeping IV curve to obtain the measured data. The lot and wafer information used for resistor simulation is listed in Table 7.6.1.

Lot number	Wafer number
DT0932	Resistor #3
DL2271	NWell resistor #1

Table 7.6.1 Wafer Information for Resistor Model

7.6.2 Capability of Model

The resistor modeling in this technology node covers three fixed corner models: RES_TT, RES_FF and RES_SS, which would be discussed in detail in the flowing section.

The resistor modeling in this technology node covers three fixed corner models: RES_TT, RES_FF and RES_SS, which would be discussed in detail in the following section.

According to the industry standard of general devices, for measurement and modeling of resistors, the ambient temperature ranges from -40℃ to 125℃. In this technology node, the SMIC model team provides sub-circuit resistor model for both 2T and its relative 3T models. For N+Poly_RS，P+Poly_RS , two capacitors for connecting substrate with high and low voltage terminals respectively (one for each), are added in the model to set up the 3T models of every type of poly resistor. For NW_RS(STI), NW_RS(AA), N+_RS , N+_RS(SAB), P+_RS and P+_RS(SAB), the resistor is split into 4 segments, and 4 pdiodes/ndiodes are added in the model to connect substrate with each segment of presistor/nresistor respectively.

For different types of resistors, their valid voltage ranges and recommended widths for measurement and extraction are shown in Table 7.6.2:

Type	Valid voltage range	Recommend Width (um)
NW_RS(STI)	0V ~ 3.3V	≥1
NW_RS(AA)	0V ~ 3.3V	≥1
N+_RS	0V ~ 3.3V	------
N+_RS(SAB)	0V ~ 3.3V	≥0.5
P+_RS	-3.3V ~ 0V	------
P+_RS(SAB)	-3.3V ~ 0V	≥0.5

N+Poly_RS	-3.3V ~ 3.3V	------
N+Poly_RS(SAB)	-3.3V ~ 3.3V	≥0.5
P+Poly_RS	-3.3V ~ 3.3V	------
P+Poly_RS(SAB)	-3.3V ~ 3.3V	≥0.5
HR Poly_1K_RS	-3.3V ~ 3.3V	≥1

Table 7.6.2 Valid Voltage Ranges and Recommended Widths of Various Resistors

Note: The square number is suggested to be larger than 5 for SAB resistor.

7.6.3 Resistor Model Parameters and Equations

Type	Sheet resistance Typical	Unit	TC1	TC2	Jc1a	Jc1b	Jc2a	Jc2b	DW(m)	DL(m)
NW_RS (STI)	887.3	ohm/sq	2.152E-03	2.055E-06	2.404E-3	2.866E-7	0	2.065E-13	1.019e-07	2.763E-11
NW_RS (AA)	450.5	ohm/sq	2.494E-03	1.909E-06	6.626e-03	1.086E-7	2.445E-10	1.614E-13	5.377E-08	-5.029E-09
Metal1_RS	0.068	ohm/sq	3.39E-03	-6.25E-07	----	----	----	----	2.3E-8	----
Metal2_RS	0.0899	ohm/sq	3.37E-03	-6.37E-07	----	----	----	----	-8E-9	----
Metal3_RS	0.0899	ohm/sq	3.37E-03	-6.37E-07	----	----	----	----	-8E-9	----
Metal4_RS	0.0899	ohm/sq	3.37E-03	-6.37E-07	----	----	----	----	-8E-9	----
Metal5_RS	0.0899	ohm/sq	3.37E-03	-6.37E-07	----	----	----	----	-8E-9	----
Metal6_RS	0.0297	ohm/sq	3.60E-03	-5.15E-07	----	----	----	----	2.7E-9	----
Top Metal2_Thick_RS(22K)	0.015	ohm/sq	3.60E-03	-5.15E-07	----	----	----	----	2.7E-9	----
MTT1_RS(34K)	0.01	ohm/sq	3.60E-03	-5.15E-07	----	----	----	----	2.7E-9	----
MTT2_RS(40K)	0.0083	ohm/sq	3.60E-03	-5.15E-07	----	----	----	----	2.7E-9	----

Type	Sheet resistance Typical	Unit	TC1	TC2	Rvc0	Rvc1	Rvc2	DW(m)	DL(m)
N+_RS	5.919	ohm/sq	3.12E-03	2.25E-07	10.59E-12	10.40E-5	0	-2.6E-8	0
P+_RS	6.933	ohm/sq	3.18E-03	3.18E-07	9.04E-12	9.98E-5	0	-3.7E-8	0
N+_RS(SAB)	56.903	ohm/sq	1.37E-03	6.22E-07	-2.90E-12	6.62E-7	4.00E-13	-4.8E-8	-5.4E-7
P+_RS(SAB)	127.895	ohm/sq	1.28E-03	8.09E-07	-13.66E-13	9.46E-7	12.83E-14	-3E-8	-3.7E-7
N+Poly_RS	6.795	ohm/sq	3.00E-03	9.75E-08	8.09E-11	2.96E-4	0	-1.3E-8	0
P+Poly_RS	7.398	ohm/sq	3.00E-03	2.76E-07	-7.96E-14	6.04E-4	0	-2E-9	0
N+Poly_RS(SAB)	275.9	ohm/sq	-1.35E-03	1.74E-06	13.69E-13	7.56E-7	2.44E-14	2.6E-8	-3.4E-7

P+Poly_RS(SAB)	316.9	ohm/sq	-2.22E-04	5.86E-07	6.44E-13	-3.70E-9	-4.52E-14	1.7E-8	-4.6E-7
HR Poly_1K_RS	1050	ohm/sq	-8.37E-04	1.72E-06	-2.95E-16	1.295E-7	2.826e-15	3.2E-9	2E-8

Table 7.6.3 Resistor Model parameters

* The resistance as a function of temperature is described by the following equation:

R(T) = R0 * [1 + TC1 * dT + TC2 * (dT)^2], where dT = T - Tnominal (25°C).
Valid temperature range: -40°C ~ 125°C.

* R0 = (RSH+DRSH) * (L – 2 * DL) / (W - 2 * (DW+DDW)) ;
Where: RSH is the sheet resistance, L is the drawn length, W is the drawn width, DRSH and DDW are the skew parameter for corner model. (L – 2 * DL) is the effective length.

* For Nwll under AA and Nwell under STI, the resistance as a function of terminal voltage is described by:
R (V) = R0 * [1 + VC1 * V + VC2 * V^2], where V is the voltage across the resistor.
VC1 = Jc1a + Jc1b / L, VC2 = (Jc2a + Jc2b / L) / L, where Jc1a, Jc1b, Jc2a, and Jc2b are the current density coefficient.

For silicide diffusion, non-silicide diffusion, poly, non-silicide npoly and BEOL resistors, the resistance as a function of terminal voltage is described by:
R (V) = R0 * [1.5 - 1 / (2 + RVC * V^2)], where V is the voltage across the resistor
RVC= (RVC0 + RVC1 * W + RVC2 * (L / W)) / (L – 2 * DL) / (L – 2 * DL), where RVC0, RVC1, RVC2 are voltage coefficient.

For non-silicide ppoly resistor, the resistance as a function of terminal voltage is described by:
R (V) = R0 * [0.5 + 1 / (2 + RVC * V^2)], where V is the voltage across the resistor
RVC= (RVC0 + RVC1 * W + RVC2 * (L / W)) / (L – 2 * DL) / (L – 2 * DL), where RVC0, RVC1, RVC2 are coefficient.

* Note: Rc does not appear in the netlist because we have subtracted it in Rsab extraction. On the other hand, Rc is a layout-dependent factor and its value varies with contact number. The designers can calculate Rc based on the resistor table and layout. Then, put it in the netlist.

7.6.4 Fixed Corner Model of Resistor

The process variation occurs due to the variation of process parameters, for example changes of etching rate, photolithography misalignment, dopant fluctuation, and day-to-day operating status of foundry equipments and more all can result in process variation, which would lead to device parameters variations. Therefore device fixed corner models are used to simulate the worst-case circuit performance in light of process variations.

The provided fixed corner models by SMIC are primarily for predicting most important corner cases: RES_TT, RES_FF and RES_SS. Their definitions are listed below.

Fixed corner model	Definition
RES_TT	Typical model, for Nominal process modeling
RES_FF	Fast corner. Performance corner for best cases of the static resistor circuit, including both global (e.g. chip to chip) and local (e.g. mismatch) variations.
RES_SS	Slow corner. Performance corner for worst cases of the static resistor circuit, including both global (e.g. wafer to wafer) and local (e.g. mismatch) variations.

Table 7.6.4 Fixed corner model Definition for Resistors

The following tables show the values of the data for compensating the corner cases of every device.

Parameters	RES_TT	RES_FF	RES_SS
drsh_rndif	0	-2.220E+00	2.220E+00
drsh_rpdif	0	-2.133E+00	2.133E+00
drsh_rnpo	0	-3.171E+00	3.171E+00
drsh_rnpo_3t	0	-3.171E+00	3.171E+00
drsh_rppo	0	-2.534E+00	2.534E+00
drsh_rppo_3t	0	-2.534E+00	2.534E+00
drsh_rnwsti	0	-1.422E+02	1.422E+02
drsh_rnwaa	0	-6.386E+01	6.386E+01
drsh_rndifsab	0	-1.035E+01	1.035E+01
drsh_rpdifsab	0	-2.558E+01	2.558E+01
drsh_rnposab	0	-3.873E+01	3.873E+01
drsh_rnposab_3t	0	-3.873E+01	3.873E+01
drsh_rpposab	0	-4.874E+01	4.874E+01
drsh_rpposab_3t	0	-4.874E+01	4.874E+01
drsh_rm1	0	-2.00E-02	2.00E-02
drsh_rm2	0	-2.464E-02	2.464E-02
drsh_rm3	0	-2.464E-02	2.464E-02
drsh_rm4	0	-2.464E-02	2.464E-02
drsh_rm6	0	-9.000E-03	9.000E-03

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drsh_rmtt1	0	-6.000E-03	6.000E-03
drsh_rmtt2	0	-4.980E-03	4.980E-03
drsh_rtm2	0	-9.000E-03	9.000E-03
drsh_rhrpo	0	-1.451E+02	1.451E+02
drsh_rhrpo_3t	0	-1.451E+02	1.451E+02
drsh_rm5	0	-2.642E-02	2.642E-02
ddw_rndif	0	0.000E+00	0.000E+00
ddw_rpdif	0	0.000E+00	0.000E+00
ddw_rnpo	0	0.000E+00	0.000E+00
ddw_rnpo_3t	0	0.000E+00	0.000E+00
ddw_rppo	0	0.000E+00	0.000E+00
ddw_rppo_3t	0	0.000E+00	0.000E+00
ddw_rnwsti	0	0.000E+00	0.000E+00
ddw_rnwaa	0	0.000E+00	0.000E+00
ddw_rndifsab	0	0.000E+00	0.000E+00
ddw_rpdifsab	0	0.000E+00	0.000E+00
ddw_rnposab	0	0.000E+00	0.000E+00
ddw_rnposab_3t	0	0.000E+00	0.000E+00
ddw_rpposab	0	0.000E+00	0.000E+00
ddw_rpposab_3t	0	0.000E+00	0.000E+00
ddw_rm1	0	0.000E+00	0.000E+00
ddw_rm2	0	0.000E+00	0.000E+00
ddw_rm3	0	0.000E+00	0.000E+00
ddw_rm4	0	0.000E+00	0.000E+00
ddw_rm6	0	0.000E+00	0.000E+00
ddw_rmtt1	0	0.000E+00	0.000E+00
ddw_rmtt2	0	0.000E+00	0.000E+00
ddw_rtm2	0	0.000E+00	0.000E+00
ddw_rhrpo	0	0.000E+00	0.000E+00
ddw_rhrpo_3t	0	0.000E+00	0.000E+00
ddw_rm5	0	0.000E+00	0.000E+00
dcox_rnpo	0	1.152E-06	-9.136E-06
dcfox_rnpo	0	3.000E-13	-2.000E-13
dcox_rppo	0	1.152E-06	-9.136E-06
dcfox_rppo	0	3.000E-13	-2.000E-13
dcox_rnposab	0	1.152E-06	-9.136E-06
dcfox_rnposab	0	3.000E-13	-2.000E-13
dcox_rpposab	0	1.152E-06	-9.136E-06
dcfox_rpposab	0	3.000E-13	-2.000E-13

dcox_rhrpo	0	1.152E-06	-9.136E-06
dcfox_rhrpo	0	3.000E-13	-2.000E-13

Table 7.6.5 Fixed corner model Table of Resistors

* In order to provide more accurate parameters for resistor, the resistor macro models which include both diodes and corner cases are listed in the attachment.
(HSPICE format: ms018_enhanced_v1p11_res.ckt, ms018_enhanced_v1p11.lib; SPECTRE format: ms018_enhanced_v1p11_res_spe.ckt, ms018_enhanced_v1p11_spe.lib ;)

7.7 MOS Varactor Model

The structure of MOS varactor is similar to the standard MOSFETs, but replacing P+ S/D with N+ S/D in PMOS. Its capacitances can be controlled by the applied gate voltage and is an electrically tunable capacitor. Characterization of technology parameters related to oxide thickness, fringing capacitance and more for MOS varactor is also quite similar with that for standard MOSFETs. Fig7.7.1- Fig7.7.2 gives the layouts and cross sections of N+/NW MOS varactor.

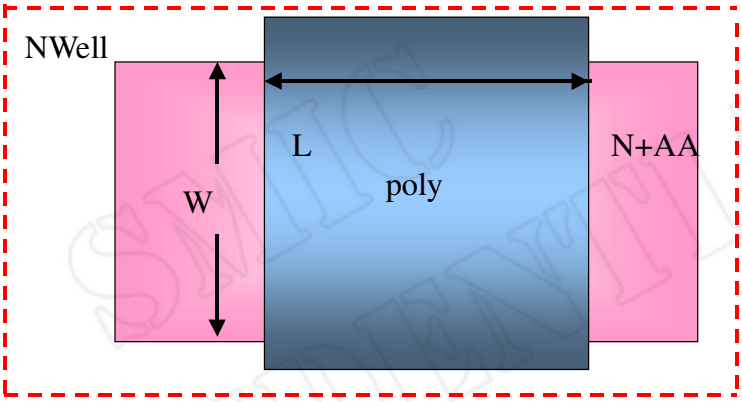

Fig. 7.7.1 The layout of N+poly/NW MOS varactor (W is AA width, L is poly length.)

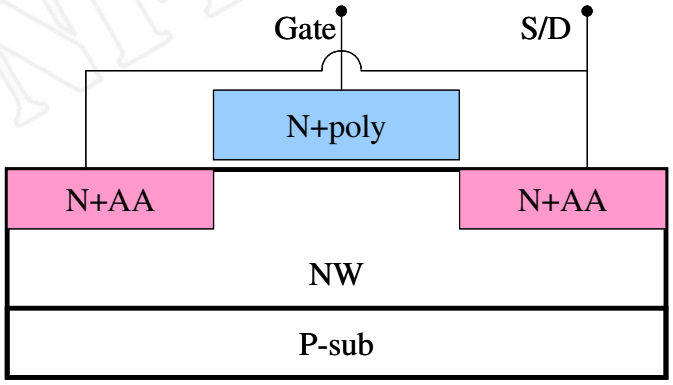

Fig. 7.7.2 The cross section of N+poly/NW MOS varactor

7.7.1 Wafer Information

The silicon data of MOS varactor are extracted from golden wafer, and the wafer is 8 inches with 26 dies. The data is provided by the Wafer Acceptance Test (WAT) team: determining the golden die whose median value (C) almost approximates that of mapping data and then sweeping CV curve to obtain the measured data. The lot and wafer information are shown in Table 7.7.1.

Lot number	**Wafer number**
DL2271	#1

Table 7.7.1 Wafer Information for MOS varactors

7.7.2 Capability of Model

According to the industry standard of general devices, for the measurement and modeling of MOS varactor, the ambient temperature ranges from -40°C to 125°C.

The capacitance and gate current models of 1.8V and 3.3V MOS varactor devices use sub-circuit model. To use the MOS varactor model for each type structure, AA width (w), gate length (l), gate finger number (nf) and array number (mr) can vary. The valid dimension ranges and valid operation conditions are listed in table 7.7.2

Type	W (Gate width)	L (Gate length)	NF (Gate finger number)	Valid voltage range	Temperature range
pvar18_ckt	10um~60um	1um~20um	1~20	-1.8V~1.8V	-40~125 C
pvar33_ckt	10um~60um	1um~20um	1~40	-3.3V~3.3V	-40~125 C

Table 7.7.2 Valid Voltages and Temperature Ranges for 1.8V/3.3V MOS Varactor Simulation

7.7.3 Fixed Corner Model of MOS Varactor

The process variation occurs due to the variation of process parameters, for example changes of etching rate, photolithography misalignment, dopant fluctuation, and day-to-day operating status of foundry equipments and more all can result in process variation, which would lead to device parameters variations. Therefore device fixed corner models are used to simulate the worst-case circuit performance in light of process variations.

The provided fixed corner models by SMIC are primarily for predicting most important corner cases: VAR_TT, VAR_FF and VAR_SS. Their definitions are listed in Table 7.7.3.

Fixed corner model	Definition
VAR_TT	Typical model, for Nominal process modeling
VAR_FF	Fast–corner. Performance corner for best cases of the static MOS varactor circuit, including both global (e.g. chip to chip) and local (e.g. mismatch) variations.
VAR_SS	Slow corner. Performance corner for worst cases of the static MOS varactor circuit, including both global (e.g. wafer to wafer) and local (e.g. mismatch) variations.

Table 7.7.3 Fixed corner model Definition of MOS Varactor Simulation

Parameters	VAR_TT	VAR_FF	VAR_SS
dtox_pvar18	0	-1E-10	1E-10
dcvar_pvar18	0	0.05	-0.05

Table 7.7.4 Fixed corner model Table of 1.05V N+ /NWell

Parameters	VAR_TT	VAR_FF	VAR_SS
dcvar_pvar33	0	0.05	-0.05

Table 7.7.5 Fixed corner model Table of 1.8V N+ /NWell

7.7.4 MOS Varactor CV fitting curve

The capacitance model is done by polynomial equation and it is valid in the following range:

W: AA width is from 5um to 60um
L: Poly length is from 1um to30um
N: Finger number is from 1 to 20
Operation voltage: -1.8~1.8V
Temperature range: -40~125C

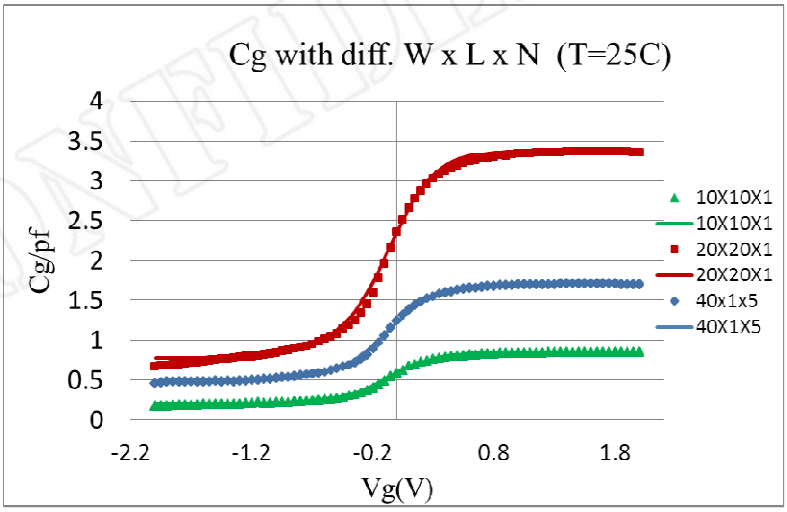

Figure 7.7.3 C versus Vg of 1.8V N+poly/NW MOS varactor (symbol: data, line: model)

The capacitance model is done by polynomial equation and it is valid in the following range:

W: AA width is from 5um to 60um
L: Poly length is1um to30um
N: Finger number is from 1 to 40
Operation voltage: -3.3~3.3V
Temperature range: -40~125C

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Doc. No.: TD-MM18-SP-2004	Doc. Title: 0.18um Mixed Signal Enhanced 1.8V/3.3V SPICE Model	Doc.Rev: 2R	Tech Dev Rev: 1.11	Page No.: 60/90

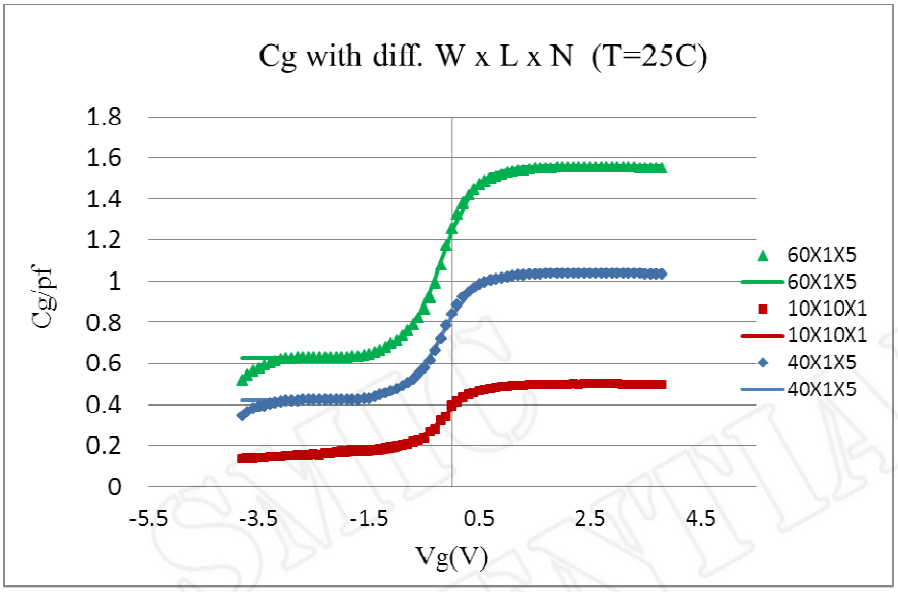

Figure 7.7.4 C versus Vg of 3.3V N+poly/NW MOS varactor (symbol: data, line: model)

7.8 MIM Capacitor Model

The MIM (metal-insulator-metal) is a common capacitor type, configured by metal layers. Fig7.8.1 shows the typical structure of MIM. Its cross section figure is shown in Fig7.8.2. The GDS files of the device layout are given in the attachment.

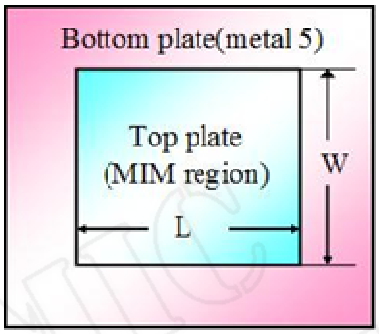

Fig. 7.8.1 Layout of MIM capacitor

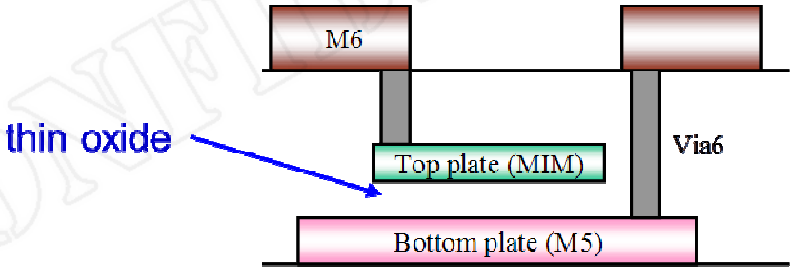

Fig. 7.8.2 Cross-section of MIM capacitor (MIM~M5)

7.8.1 Wafer information

The silicon data of MIM capacitor are extracted from golden wafer, and the wafer is 8 inches with 26 dies. The data is provided by the Wafer Acceptance Test (WAT) team: determining the golden die whose median value (C) almost approximates that of mapping data and then sweeping CV curve to obtain the measured data. The lot and wafer information for MIM capacitance simulation are listed in Table 7.8.1

Lot number	Wafer number
DT0932	#3

Table 7.8.1 Wafer Information of MIM Capacitor Model

7.8.2 Capability of Model

According to the industry standard of general devices, for measurement and modeling of MIM, the ambient temperature ranges from -40°C to 125°C. The valid dimension range and working conditions are listed in Table 7.8.2:

MIM architecture	Bottom metal layer	Top metal layer	W	L	Array number	Temperature
MIM capacitor 1fF (two terminals)	5	MIM	4~30	4~30	1~100	-40~125℃
MIM capacitor 2fF (two terminals)	5	MIM	4~30	4~30	1~100	-40~125℃

Table 7.8.2. Valid Dimension Ranges and working conditions of MIM

* To acquire better accuracy, it is recommended to use W&L≥15um for 1fF MIM and W&L≥8um for 2 fF MIM.

7.8.3 Fixed Corner Model of MIM Capacitor

The provided fixed corner models by SMIC are primarily for predicting most important corner cases: MIM_TT, MIM_FF and MIM_SS. Their definitions are listed in Table 7.8.3.

Fixed corner model	Definition
MIM_TT	Typical model, for Nominal process modeling
MIM_FF	Fast corner. Performance corner for best cases of the static MIM circuit, including both global (e.g. chip to chip) and local (e.g. mismatch) variations.
MIM_SS	Slow corner. Performance corner for worst cases of the static MIM circuit, including both global (e.g. wafer to wafer) and local (e.g. mismatch) variations.

Table 7.8.3 Fixed corner model Definition of MIM Capacitor

Table 7.8.4 shows the values of the data for compensating the corner cases of every device.

Parameters	Unit	MIM_TT	MIM_FF	MIM_SS
dmim	-	0	-1.938e-4	1.938e-4
dmim2	-	0	-1.99e-04	-1.99e-04

Table 7.8.4 Corner Model Table of MIM Capacitor

7.8.4 MIM Model

A. MIM (Cspec = 1 fF/um^2)

0.18um Mixed Signal MIM Capacitor Voltage & Temperature Coefficient				
Area (um^2)	C0 (fF/um^2)	VC 1 (ppm/V)	VC 2 (ppm/V^2)	TC 1 (ppm/C)
400	0.969	-4.76	-7.616	-22.56
900		25.67	-10.07	-22.24
1600		23.14	-10.67	-21.54
2500		24.71	-11.11	-23.48
Global Area		22.742	-10.135	-21.98

Table 7.8.5 MIM1 model parameters

* Note: The parameters listed in the row of Global Area are used for fitting all MIM capacitors.

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Doc. No.: TD-MM18-SP-2004	Doc. Title: 0.18um Mixed Signal Enhanced 1.8V/3.3V SPICE Model	Doc.Rev: 2R	Tech Dev Rev: 1.11	Page No.: 64/90

* The capacitance as a function of temperature is described by the following equation:

  $C(T) = C0 * [1 + TC1 * dT]$, where $dT = T - Tnominal$ (25°C).

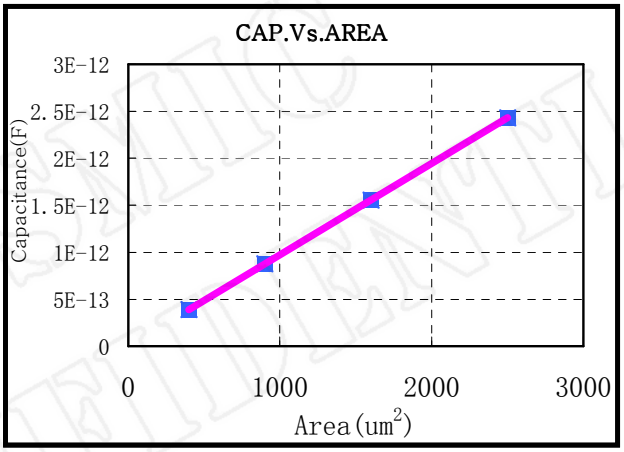
  Valid temperature range: -40°C ~ 125°C.

* The capacitance as a function of terminal voltage is described by:

  $C(V) = C0 * [1 + VC1 * V + VC2 * V^2]$, where V is the voltage across the capacitor.

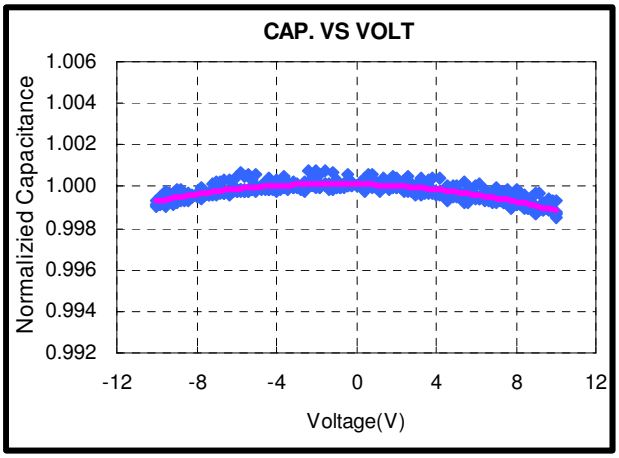
* C0 is extracted from the scalable formula by giving area.

  The slope of fitting line is C0(0.969fF/um^2) in the figure.



* VC1 and VC2 are extracted from the normalized capacitance at 25C. (C0=1 at V=0)

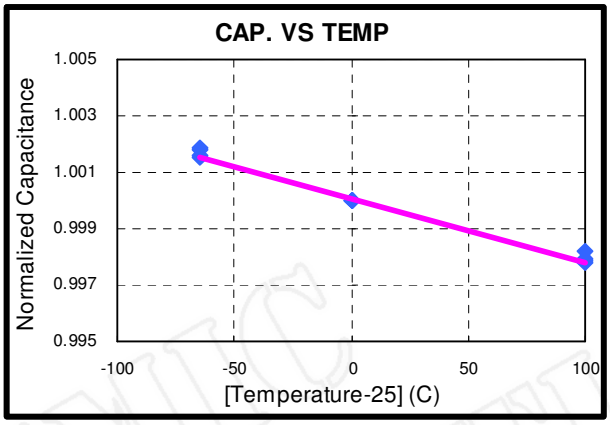
The following figure shows the normalized capacitance versus voltage for global area, both voltage coefficients VC1= 22.742ppm/V and VC2= -10.135ppm/V^2, respectively.



* TC1 is extracted from the normalized capacitance at different temperature.(C0=1 at T=25C)

The figure below shows the normalized capacitance versus temperature for global area. The

temperature coefficient TC1 is -21.98 ppm/C.



B. MIM(Cspec = 2 fF/um^2)

0.18um Mixed Signal MIM Capacitor Voltage & Temperature Coefficient				
Area (um^2)	C0 (fF/um^2)	VC 1 (ppm/V)	VC 2 (ppm/V^2)	TC 1 (ppm/C)
400	1.99	9.44	13.31	28.10
900		7.20	13.73	27.37
1600		7.71	13.72	30.00
2500		6.03	13.89	27.62
Global Area		7.68	13.59	28.74

Table 7.8.6 MIM2 model parameters

* Note: The parameters listed in the row of Global Area are used for fitting all MIM capacitors.
* The capacitance as a function of temperature is described by the following equation:
  C(T) = C0 * [1 + TC1 * dT], where dT = T - Tnominal (25°C).
  Valid temperature range: -40°C ~ 125°C.
* The capacitance as a function of terminal voltage is described by:
  C(V) = C0 * [1 + VC1 * V + VC2 * V^2], where V is the voltage across the capacitor.
* C0 is extracted from the scalable formula by giving area.
  The slope of fitting line is C0(1.99 fF/um^2) in the figure.

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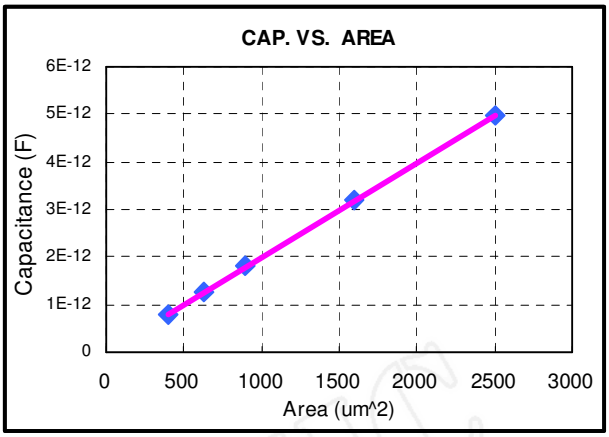
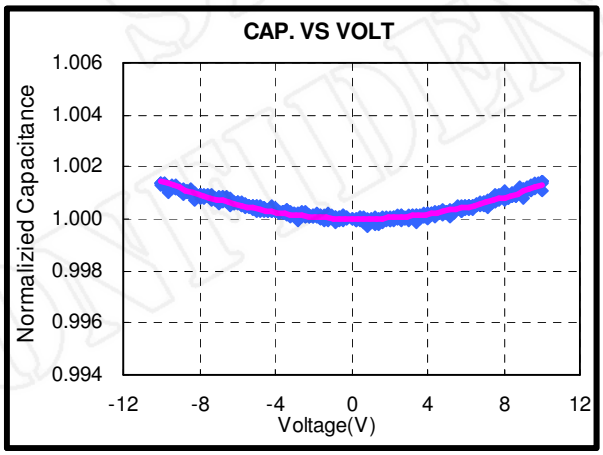


* VC1 and VC2 are extracted from the normalized capacitance at 25C. (C0=1 at V=0)

The following figure shows the normalized capacitance versus voltage for global area, both voltage coefficients VC1= 7.68ppm/V and VC2= 13.59 ppm/V^2, respectively.



* TC1 is extracted from the normalized capacitance at different temperature.(C0=1 at T=25C)

The figure below shows the normalized capacitance versus temperature for global area. The temperature coefficient TC1 is 28.74 ppm/C.

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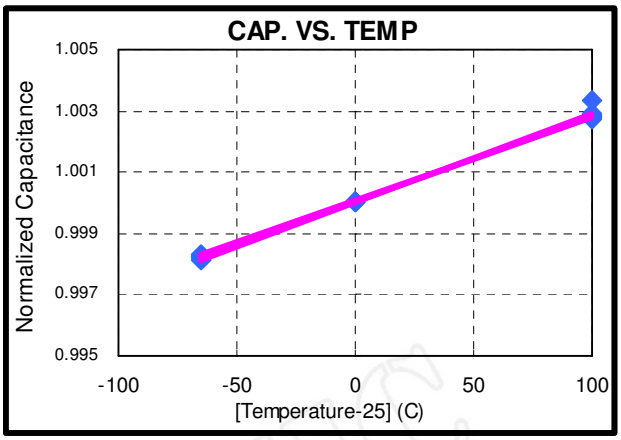

7.9 Model fitting and plotting results

Due to the size of the plots, all the fitting plots for 0.18um Mix Signal 1P6M Salicide 1.8V/3.3V Enhanced SPICE Model are given in five attachments named “ms018_fit_A.doc”, “ms018_fit_B1.doc”, “ms018_fit_B2.doc”, “ms018_fit_C.doc”, “ms018_fit_D.doc”, “ms018_fit_F.doc” and “ms018_fit_G.doc”. They are described in six sections (section A, B1, B2,C, D, F and G).

Section A. Comparison between measurement and simulation results (for MOS IV&CV)

Fig.A 1 Vth versus L at Wdrawn = 10um for 1.8V NMOS
Fig.A 2 Vtsat versus L at Wdrawn = 10um for 1.8V NMOS
Fig.A 3 Vth versus W at Ldrawn = 10um for 1.8V NMOS
Fig.A 4 Vth versus L at Wdrawn =0.22um for 1.8V NMOS
Fig.A 5 Vth versus W at Ldrawn = 0.18um for 1.8V NMOS
Fig.A 6 Idlin versus L with different width array at Vbs=0V for 1.8V NMOS
Fig.A 7 Idlin versus W with different length array at Vbs=0V for 1.8V NMOS
Fig.A 8 Idsat versus L with different width array at Vbs=0V for 1.8V NMOS
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Fig.A 14 Vth versus W at Ldrawn = 0.18um for 1.8V PMOS
Fig.A 15 Idlin versus L with different width array at Vbs=0V for 1.8V PMOS
Fig.A 16 Idlin versus W with different length array at Vbs=0V for 1.8V PMOS
Fig.A 17 Idsat versus L with different width array at Vbs=0V for 1.8V PMOS
Fig.A 18 Idsat versus W with different length array at Vbs=0V for 1.8V PMOS
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Fig.A 21 Idlin vs. T measured and simulated plot with various Vbs for 1.8V NMOS 10/0.18
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Fig.A 24 Vth vs. T measured and simulated plot with various Vbs for 1.8V PMOS 10/0.18
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Fig.A 30 Fitting ID_VD&VG, subthreshold and gds of 1.8V NMOS W/L=10/10 at temp=125C
Fig.A 31 Fitting ID_VD&VG, subthreshold and gds of 1.8V NMOS W/L=10/10 at temp=-40C
Fig.A 32 Fitting ID_VD&VG, subthreshold and gds of 1.8V NMOS W/L=10/0.18 at temp=25C
Fig.A 33 Fitting ID_VD&VG, subthreshold and gds of 1.8V NMOS W/L=10/0.18 at temp=125C
Fig.A 34 Fitting ID_VD&VG, subthreshold and gds of 1.8V NMOS W/L=10/0.18 at temp=-40C
Fig.A 35 Fitting ID_VD&VG, subthreshold and gds of 1.8V NMOS W/L=0.22/10 at temp=25C
Fig.A 36 Fitting ID_VD&VG, subthreshold and gds of 1.8V NMOS W/L=0.22/10 at temp=125C
Fig.A 37 Fitting ID_VD&VG, subthreshold and gds of 1.8V NMOS W/L=0.22/10 at temp=-40C
Fig.A 38 Fitting ID_VD&VG, subthreshold and gds of 1.8V NMOS W/L=0.22/0.18 at temp=25C

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Section B1. Comparison between measurement and simulation results (for PNP Bipolar)

Section B2. Comparison between measurement and simulation results (for NPN Bipolar)

Section C. Comparison between measurement and simulation result (for junction diode IV&CV)

Section D. Comparison between measurement and simulation results (for Resistance)

7.10 Conclusion

This document is written to provide SPICE model simulation guideline for circuit designers who use SMIC 0.18um Mix Signal Salicide 1.8V/3.3V Enhanced process. In this document, information about device modeling are given in detail, covering MOSFETs Model (wafer information, model capability, fixed corner model table, 1/f noise model, LOD Stress Effect Model,), as well as wafer information, model capability and fixed corner model table of Bipolar Gummel-Poon Model, Diode Model, Interconnection Model, Resistor Model, MOS Varactor Model, and MIM Capacitor Model.

7.11 Appendixes

7.11.1 The Flicker Noise Parameters

Parameter name	**Description**	**Default value**
NOIA	Flicker noise parameter A	6.25e41 (eV)-1s1-EFm-3 for NMOS; 6.188e40 (eV)-1s1-EFm-3 for PMOS
NOIB	Flicker noise parameter B	3.125e26 (eV)$^{-1S1-EFm-1}$ for NMOS; 1.5e25 (eV)$^{-1S1-EFm-1}$ for PMOS

NOIC	Flicker noise parameter C	8.75 (eV)-1s1-EFm
EM	Saturation field	4.1e7V/m
AF	Flicker noise exponent	1.0
EF	Flicker noise frequency exponent	1.0
KF	Flicker noise coefficient	0.0 A2-EFs1-EFF
LINTNOI	Length Reduction Parameter Offset	0.0 m
NTNOI	Noise factor for short-channel devices for TNOIMOD=0 only	1.0

7.11.2 Model Parameter Description for HSPICE Level 54

(Reference: UCB BSIM4V4.5 manual and HSPICE manual)

Parameters	**Description**	**Unit**
Model Flag Parameters		
LEVEL	MOSFET model level, set to 54 for HSPICE model	N/A
LMIN	Minimum channel length	m
LMAX	Maximum channel length	m
WMIN	Minimum channel width	m
WMAX	Maximum channel width	m
VERSION	Model version number	N/A
BINUNIT	Bin unit scale selector	N/A
PARAMCHK	Switch for parameter value check	N/A
MOBMOD	Mobility model selector	N/A
CAPMOD	Capacitance model selector	N/A
IGCMOD	Gate-to-channel tunneling current model selector	N/A
IGBMOD	Gate-to-substrate tunneling current model selector	N/A
RGATEMOD	Gate resistance model selector	N/A
GEOMOD	Geometry-dependent parasitic model selector	N/A
DIOMOD	Source/drain junction diode IV model selector	N/A
RDSMOD	Bias-dependent source/drain resistance model selector	N/A
RBODYMOD	Substrate resistance network model selector	N/A

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Parameters	Description	Unit
PERMOD	Whether PS/PD includes the gate-edge perimeter	N/A
ACNQSMOD	AC small-signal NQS model selector	N/A
TRNQSMOD	Transient NQS model selector	N/A
General Model Parameters		
TNOM	Temperature at which parameters are extracted	℃
TOXE	Electrical gate equivalent oxide thickness	m
TOXP	Physical gate equivalent oxide thickness	m
TOXM	Tox at which parameters are extracted	m
DTOX	Defined as (TOXE-TOXP)	m
EPSROX	Gate dielectric constant relative to vacuum	N/A
LINT	Length offset fitting parameter from I-V without bias	m
WINT	Width offset fitting parameter from I-V without bias	m
WL	Coefficient of length dependence for width offset	m
WLN	Power of length dependence for width offset	N/A
WW	Coefficient of width dependence for width offset	m
WWN	Power of width dependence for width offset	N/A
WWL	Coefficient of length and width cross term dependence for width offset	m
LL	Coefficient of length dependence for length offset	m
LLN	Power of length dependence for length offset	N/A
LW	Coefficient of width dependence for length offset	m
LWN	Power of width dependence for length offset	N/A
LWL	Coefficient of length and width cross term for length offset	m
WLC	Coefficient of length dependence for CV width offset	m
WWC	Coefficient of width dependence for CV width offset	m
LLC	Coefficient of length dependence for CV length offset	m
LWC	Coefficient of width dependence for CV length offset	m

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Parameters	Description	Unit
LWLC	Coefficient of length and width cross term for CV length offset	M
WWLC	Coefficient of length and width cross term dependence for CV width offset	M
XL	The masking and etching effects of channel length	M
XW	The masking and etching effects of channel width	M
DLC	Length offset fitting parameter from C-V	M
DWC	Width offset fitting parameter from C-V	M
XPART	Channel charge partitioning rate flag	N/A
TOXREF	Nominal gate oxide thickness for gate dielectric tunneling current model only	M
DLCIG	Source/drain overlap length for Igs and Igd	M
DC Parameters		
XJ	Source/Drain junction depth	M
DWG	Coefficient of Weff's gate dependence	m/V
DWB	Coefficient of Weff's substrate bias dependence	$m/V^{1/2}$
RSH	Source/drain diffusion sheet resistance	Ω/square
VTH0	Threshold voltage of long channel device at Vbs=0 and small Vds	V
K1	First-order body effect coefficient	$V^{1/2}$
K2	Second-order body effect coefficient	N/A
K3	Narrow width effect coefficient	N/A
K3B	Body effect coefficient of K3	1/V
W0	Narrow width effect coefficient	M
LDE0	Lateral non-uniform doping parameter at Vbs=0	M
LDEB	Lateral non-uniform doping effect on k1	M
DVT0	First coefficient of short channel effects on Vth	N/A
DVT1	Second coefficient of short channel effects on Vth	N/A

Parameters	Description	Unit
DVT2	Body-bias coefficient of short channel effects on Vth	1/V
DVT0W	First coefficient of narrow width effects on Vth for small channel length	1/m
DVT1W	Second coefficient of narrow width effects on Vth for small channel length	1/m
DVT2W	Body-bias coefficient of narrow width effects on Vth for small channel length	1/V
DVTP0	First coefficient of drain-induced Vth shift due to for long-channel pocket devices	M
DVTP1	Drain-induced coefficient of pocket implant correction to Vth	1/V
NGATE	Poly-Gate doping concentration	cm^{-3}
NDEP	Channel doping concentration at depletion edge for zero body bias	cm^{-3}
NSD	Source/drain doping concentration	cm^{-3}
A0	Bulk charge effect coefficient for channel length	N/A
A1	First non-saturation effect parameter	1/V
A2	Second non-saturation effect parameter	N/A
RDSW	Zero bias LDD resistance per unit width for RDSMOD=0	Ω *(um)WR
RDSWMIN	LDD resistance per unit width at high Vgs and zero Vbs for RDSMOD=0	Ω *(um)WR
RDW	Zero bias lightly-doped drain resistance Rd(V) per unit width for RDSMOD=1	Ω *(um)WR
RDWMIN	Lightly-doped drain resistance per unit width at high Vgs and zero Vbs for RDSMOD=1	Ω *(um)WR
RSW	Zero bias lightly-doped source resistance Rs(V) per unit width for RDSMOD=1	Ω *(um)WR
RSWMIN	Lightly-doped source resistance per unit width at high Vgs and	Ω *(um)WR

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Parameters	Description	Unit
	zero Vbs for RDSMOD=1	
WR	Channel-width dependence parameter of LDD resistance	N/A
PRWB	Body effect coefficient of RDSW	$V^{-0.5}$
PRWG	Gate bias effect coefficient of RDSW	1/V
U0	Mobility at TEMP=TNOM	$m^2/(V*sec)$
VSAT	Saturation velocity at TEMP=TNOM	m/sec
UA	First-order mobility degradation coefficient	m/V
UB	Second-order mobility degradation coefficient	$(m/V)^2$
UC	Body-effect of mobility degradation coefficient	m/V^2
EU	Exponent for mobility degradation of MOBMOD=2	N/A
AGS	Gate bias coefficient of Abulk	1/V
B0	Bulk charge effect coefficient for channel width	M
B1	Bulk charge effect width offset	M
PDITS	Impact of drain-induced Vth shift on Rout	1/V
PDITSL	Channel-length dependence of drain-induced Vth shift for Rout	1/m
PDITSD	Vds dependence of drain-induced Vth shift for Rout	1/V
KETA	Body-bias coefficient of bulk charge effect	1/V
CDSC	Source/drain and channel coupling capacitance	F/m^2
CDSCB	Body-bias sensitivity of CDSC	F/Vm^2
CDSCD	Drain-bias sensitivity of CDSC	F/Vm^2
NFACTOR	Subthreshold swing coefficient	N/A
CIT	Interface trap capacitance	F/m^2
VOFF	Offset voltage in the subthreshold region at large Wand L	V
VOFFL	Channel-length dependence of VOFF	V
MINV	Vgsteff fitting parameter for moderate inversion condition	N/A
PHIN	Non-uniform vertical doping effect on surface potential	V
FPROUT	Effect of pocket implant on Rout degradation	$V/m^{0.5}$

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Parameters	Description	Unit
DSUB	DIBL coefficient exponent in the subthreshold region	N/A
ETA0	DIBL coefficient in the subthreshold region	N/A
ETAB	Body-bias coefficient for the subthreshold DIBL effect	1/V
DROUT	L dependence coefficient of DIBL correction parameter in Rout	N/A
ALPHA0	The first parameter of impact ionization current	m/V
BETA0	The second parameter of impact ionization current	V
DELTA	Effective Vds parameter	V
PCLM	Channel length modulation coefficient	N/A
PDIBLC1	First output resistance DIBL effect correction parameter	N/A
PDIBLC2	Second output resistance DIBL effect correction parameter	N/A
PDIBLCB	Body-effect coefficient of DIBL correction parameter	1/V
PSCBE1	First substrate current body-effect parameter	V/m
PSCBE2	Second substrate current body-effect parameter	m/V
PVAG	Gate dependence of early voltage	N/A
AGIDL	Pre-exponential coefficient for GIDL	1/Ω
BGIDL	Exponential coefficient for GIDL	V/m
CGIDL	Paramter for body-bias effect on GIDL	V^3
EGIDL	Fitting parameter for band bending for GIDL	V
AIGBACC	First parameter for Igb in accumulation	$(Fs^2/g^{-1})^{0.5}/m$
BIGBACC	Second parameter for Igb in accumulation	$(Fs^2/g)^{0.5}/(Vm)$
CIGBACC	Third Parameter for Igb in accumulation	1/V
NIGBACC	Ideality factor for Igb in accumulation	N/A
AIGBINV	First parameter for Igb in inversion	$(Fs^2/g^{-1})^{0.5}/m$
BIGBINV	Second parameter for Igb in inversion	$(Fs^2/g)^{0.5}/(Vm)$
CIGBINV	Third Parameter for Igb in inversion	1/V
EIGBINV	Voltage offset parameter for Igb in inversion	N/A

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Parameters	Description	Unit
NIGBINV	Ideality factor for Igb in inversion	N/A
AIGC	Parameter for Igcs and Igcd	$(Fs^2/g^{-1})^{0.5}/m$
BIGC	Parameter for Igcs and Igcd	$(Fs^2/g)^{0.5}/(Vm)$
CIGC	Parameter for Igcs and Igcd	1/V
AIGSD	Parameter for Igs and Igd	$(Fs^2/g^{-1})^{0.5}/m$
BIGSD	Parameter for Igs and Igd	$(Fs^2/g)^{0.5}/(Vm)$
CIGSD	Parameter for Igs and Igd	1/V
NIGC	Parameter for Igcs, Igcd, Igs and Igd	N/A
POXEDGE	Factor for the gate oxide thickness in source/drain overlap region	N/A
PIGCD	Vds dependence of Igcs and Igcd	N/A
NTOX	Exponent for the gate oxide ratio	N/A
XRCRG1	Parameter for distributed channel-resistance effect for both intrinsic-input resistance and charge-deficit NQS models	N/A
XRCRG2	Parameter to account for the excess channel diffusion resistance for both intrinsic input resistance and charge-deficit NQS models	N/A
Temperature Effects Parameters		
KT1	Temperature coefficient for threshold voltage	V
KT1L	Channel length dependence of the temperature coefficient for threshold voltage	Vm
KT2	Body-bias coefficient of Vth temperature effect	N/A
AT	Temperature coefficient for VSAT	m/sec
UA1	Temperature coefficient for UA	m/V
UB1	Temperature coefficient for UB	$(m/V)^2$
UC1	Temperature coefficient for UC	m/V^2
UTE	Mobility temperature exponent	N/A

Parameters	Description	Unit
PRT	Temperature coefficient for RDSW	Ω *um
Capacitance Parameters		
CGSO	Non LDD region source-gate overlap capacitance per channel length	F/m
CGDO	Non LDD region drain-gate overlap capacitance per channel length	F/m
CGBO	Gate bulk overlap capacitance per unit channel length	F/m
ACDE	Exponential coefficient for charge thickness in CAPMOD=2 for accumulation and depletion regions	m/V
MOIN	Coefficient for the gate-bias dependent surface potential	N/A
NOFF	CV parameter in Vgsteff,CV for weak to strong inversion	N/A
VOFFCV	CV parameter in Vgsteff,CV for week to strong inversion	V
Noise Parameters		
NOIA	Flicker noise parameter A	$eV^{-1}s*m^{-2}$
NOIB	Flicker noise parameter B	$eV^{-1}s$
NOIC	Flicker noise parameter C	$eV^{-1}s*m^{-2}$
EM	Saturation field	V/m
AF	Flicker noise exponent	N/A
KF	Flicker noise coefficient	N/A
EF	Flicker noise frequency exponent	N/A
NTNOI	Noise factor for short-channel devices	N/A
TNOIA	Coefficient of channel-length dependence of total channel thermal noise	N/A
TNOIB	Channel-length dependence parameter for channel thermal noise partitioning	N/A
Diode Parameters		
JSS, JSD	Bottom junction reverse saturation current density	A/m^2

Parameters	Description	Unit
JSWS, JSWD	Isolation-edge sidewall reverse saturation current density	A/m
JSWGS, JSWGD	Gate-edge sidewall reverse saturation current density	A/m
IJTHSFWD, IJTHDFWD	Limiting current in forward bias region	A
BVS, BVD	Breakdown voltage	V
XJBVS, XJBVD	Fitting parameter for diode breakdown	N/A
NJS, NJD	Emission coefficients of junction for source and drain junctions, respectively	N/A
CJS, CJD	Bottom junction capacitance per unit area at zero bias	F/m^2
CJSWS, CJSWD	Isolation-edge sidewall junction capacitance per unit area	F/m
CJSWGS, CJSWGD	Gate-edge sidewall junction capacitance per unit length	F/m
MJS, MJD	Bottom junction capacitance grating coefficient	N/A
MJSWS, MJSWD	Isolation-edge sidewall junction capacitance grading coefficient	N/A
MJSWGS, MJSWGD	Gate-edge sidewall junction capacitance grading coefficient	N/A
PBS PBD	Bottom junction built-in potential	V
PBSWGS, PBSWGD	Isolation-edge sidewall junction built-in potential	V
PBSWS, PBSWD	Gate-edge sidewall junction built-in potential	V/K
TPB	Temperature coefficient of PB	V/K
TPBSW	Temperature coefficient of PBSW	V/K
TPBSWG	Temperature coefficient of PBSWG	V/K
TCJ	Temperature coefficient of CJ	1/K
TCJSW	Temperature coefficient of CJSW	1/K
TCJSWG	Temperature coefficient of CJSWG	1/K
RDC	Additional drain resistance due to contact resistance	Ω/square
RSC	Additional source resistance due to contact resistance	Ω/square
Layout Related Parameters		

Parameters	Description	Unit
DMCG	Distance from S/D contact center to the gate edge	M
DMDG	Same as DMCG but for merged for device only	M
DMCGT	DMCG of test structures	M
DWJ	Offset of the S/D junction width	M
XGW	Distance from the gate contact to the channel edge	M
XGL	Channel length offset due to mask/etch effect	M
RF Parameters		
RSHG	Gate electrode sheet resistance	Ω/ square
GBMIN	Conductance in parallel with each of the five substrate resistances	Ω
RBPB	Resistance connected between bNodePrime and bNode	Ω
RBPD	Resistance connected between bNodePrime and dbNode	Ω
RBPS	Resistance connected between bNodePrime and sbNode	Ω
RBDB	Resistance connected between dbNode and bNode	Ω
Stress Parameters		
SA	Distance between OD edge to Poly from one side	M
SB	Distance between OD edge to Poly from other side	M
SD	Distance between neighbouring fingers	M
SAREF	Reference distance between OD and edge to poly of one side	M
SAREF	Reference distance between OD and edge to poly of the other side	M
WLOD	Width parameter for stress effect	M
KU0	Mobility degradation/enhancement coefficient for stress effect	M
KVSAT	Saturation velocity degradation/enhancement parameter for stress effect	M
TKU0	Temperature coefficient of KU0	N/A
LKU0	Length dependence of ku0	N/A

Parameters	Description	Unit
WKU0	Width dependence of ku0	N/A
LLODKU0	Length parameter for u0 stress effect	N/A
WLODKU0	Width parameter for u0 stress effect	N/A
KVTH0	Threshold shift parameter for stress effect	Vm
LKVTH0	Length dependence of kvth0	N/A
WKVTH0	Width dependence of kvth0	N/A
PKVTH0	Cross-term dependence of kvth0	N/A
LLODVTH	Length parameter for Vth stress effect	N/A
WLODVTH	Width parameter for Vth stress effect	N/A
STK2	K2 shift factor related to Vth0 change	M
LODK2	K2 shift modification factor for stress effect	N/A
STETA0	Eta0 shift factor related to Vth0 change	M
LODETA0	Eta0 shift modification factor for stress effect	N/A

7.12 Reference

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8. Attachment

8.1 ASCII files: SMIC_SP_model_018MSE_1833.tar.gz

SMIC_SP_model_018MSE_1833.tar.gz

→ hspice
spectre
ms018_enhanced_v1p11_interconnect_structure1_tm_9k.txt
ms018_enhanced_v1p11_interconnect_structure1_tm_22k.txt
ms018_enhanced_v1p11_interconnect_structure1_tm_34k.txt
ms018_enhanced_v1p11_interconnect_structure1_tm_40k.txt
ms018_enhanced_v1p11_interconnect_structure2_tm_9k.txt
ms018_enhanced_v1p11_interconnect_structure2_tm_22k.txt
ms018_enhanced_v1p11_interconnect_structure2_tm_34k.txt
ms018_enhanced_v1p11_interconnect_structure2_tm_40k.txt

HSPICE and SPECTRE folder content:

hspice	spectre
*	
ms018_enhanced_v1p11_readme.txt	ms018_enhanced_v1p11_readme_spe.txt
ms018_enhanced_v1p11.lib	ms018_enhanced_v1p11_spe.lib
ms018_enhanced_v1p11.mdl	ms018_enhanced_v1p11_spe.mdl
ms018_enhanced_v1p11_mis.mdl	ms018_enhanced_v1p11_mis_spe.mdl
ms018_enhanced_v1p11_dio.mdl	ms018_enhanced_v1p11_dio_spe.mdl
ms018_enhanced_v1p11_res.ckt	ms018_enhanced_v1p11_res_spe.ckt
ms018_enhanced_v1p11_var.ckt	ms018_enhanced_v1p11_var_spe.ckt
ms018_enhanced_v1p11_mim.ckt	ms018_enhanced_v1p11_mim_spe.ckt
ms018_enhanced_v1p11_mim.mdl	ms018_enhanced_v1p11_mim_spe.mdl
ms018_enhanced_v1p11_res.mdl	ms018_enhanced_v1p11_res_spe.mdl
ms018_enhanced_v1p11_bjt.mdl	ms018_enhanced_v1p11_bjt_spe.mdl
pnp33a4.mdl	pnp33a4_spe.mdl
pnp33a25.mdl	pnp33a25_spe.mdl
pnp33a100.mdl	pnp33a100_spe.mdl
pnp18a4.mdl	pnp18a4_spe.mdl
pnp18a25.mdl	pnp18a25_spe.mdl
pnp18a100.mdl	pnp18a100_spe.mdl
npn33a4.mdl	npn33a4_spe.mdl
npn33a25.mdl	npn33a25_spe.mdl
npn33a100.mdl	npn33a100_spe.mdl
npn18a4.mdl	npn18a4_spe.mdl
npn18a25.mdl	npn18a25_spe.mdl
npn18a100.mdl	npn18a100_spe.mdl
	res.va
	gc.va

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8.2 GDS Files:

DIO_BPWDNW.gds
DIO_DNWDIO.gds
DIO_NDIOMVT18.gds
DIO_NDIOMVT33.gds
DIO_NPW18.gds
DIO_NPW33.gds
DIO_NWPSUB.gds
DIO_PDIOMVT18.gds
DIO_PNW18.gds
DIO_PNW33.gds
NPN18A100.gds
NPN18A25.gds
NPN18A4.gds
NPN33A100.gds
NPN33A25.gds
NPN33A4.gds
PNP18A100.gds
PNP18A25.gds
PNP18A4.gds
PNP33A100.gds
PNP33A25.gds
PNP33A4.gds

8.3 DOC Files

SMIC_SP_fit_A_018MSE_1833. pdf
SMIC_SP_fit_B1_018MSE_1833. pdf
SMIC_SP_fit_B2_018MSE_1833. pdf
SMIC_SP_fit_C_018MSE_1833. pdf
SMIC_SP_fit_D_018MSE_1833. pdf
SMIC_SP_fit_F_018MSE_1833. pdf
SMIC_SP_fit_G_018MSE_1833. pdf