1. Introductions

1.1. Basic Function and Design Goals

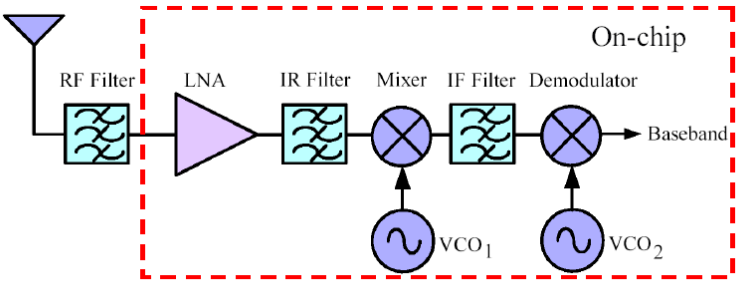


Fig. 1.1 A typical architecture of radio receiver

1.1.1. Basis Function

- Provide gain to minimize noise contributed by subsequent blocks
- Contribute as low noise as possible
- Provide high linearity
- Provide 50 ohm input impedance
- Low power dissipation

1.1.2. Design Goals

- Simultaneous Noise and Input Matching
- Any given amount of power dissipation

2. Fundamental of Low Noise Amplifier

2.1. Noise Figure and Noise Factor

The most popular basis definition of noise figure is given by Friis

$$NF = 10\log\left(\frac{SNR_{in}}{SNR_{out}}\right) = 10\log(F) \qquad (2.1)$$

where SNR_{in} and SNR_{out} are the signal-to-noise ratios measured at the input and output

NF measures how much the SNR degrades as the signal passes through a system

If a system has no noise, then $SNR_{in} = SNR_{out}$

→ NF of noiseless system is equal to 0 dB

2.2. Power Gain

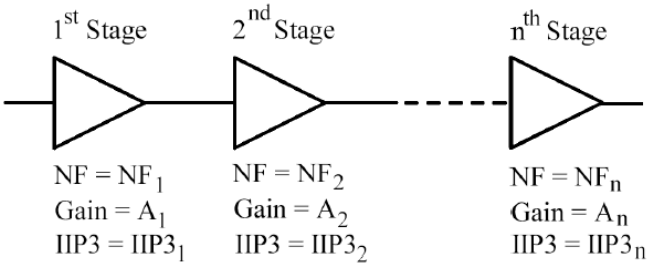


Fig. 2.1 NF of the cascade system

$$NF_{total} = NF_1 + \frac{NF_2 - 1}{A_1} + \ldots + \frac{NF_n - 1}{A_1 . A_2 \ldots A_n} \qquad (2.2)$$

- **NF of overall system is dominated by first stage**
- **→ LNA need to have high gain to suppress the noise contributed by later stages**
- **However be careful when design high gain because it easily becomes oscillator**

2.3. Linearity

- ✓ **LNA must remain linear even when strong signals are bein g received**
- ✓ **The nonlinear can be characterized by 1 dB compression point (P-1dB) or input referred third order intercept point (IIP3)**
  - **P-1dB is defined as the input power at which the output power gain drops by 1 dB**
  - **IIP3 is defined as the point at which extrapolated fundamental response and the extrapolated third order intermodulation line intersect**

$$IIP3 = \frac{P_{out} - P_{out,IM3}}{2} + P_{in} \qquad \frac{A_{P-1dB}}{A_{IIP3}} \approx -9.6\ dB$$

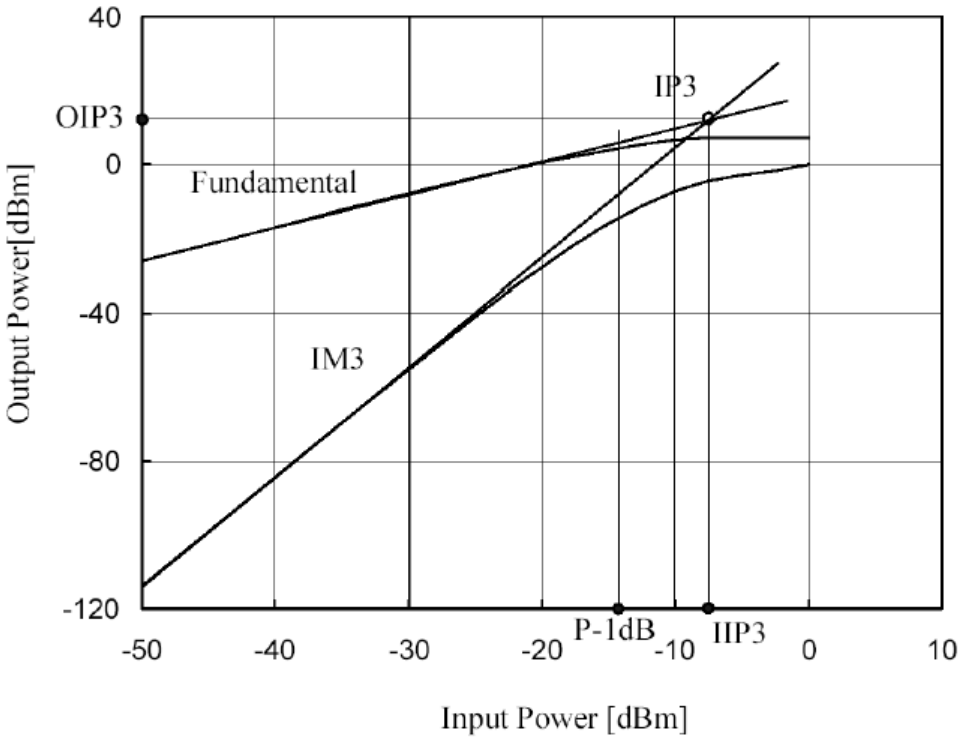


Fig. 2.2 A Plot of IIP3

3. Low Noise Amplifier Design Techniques

3.1. Classical Noise Optimization Technique

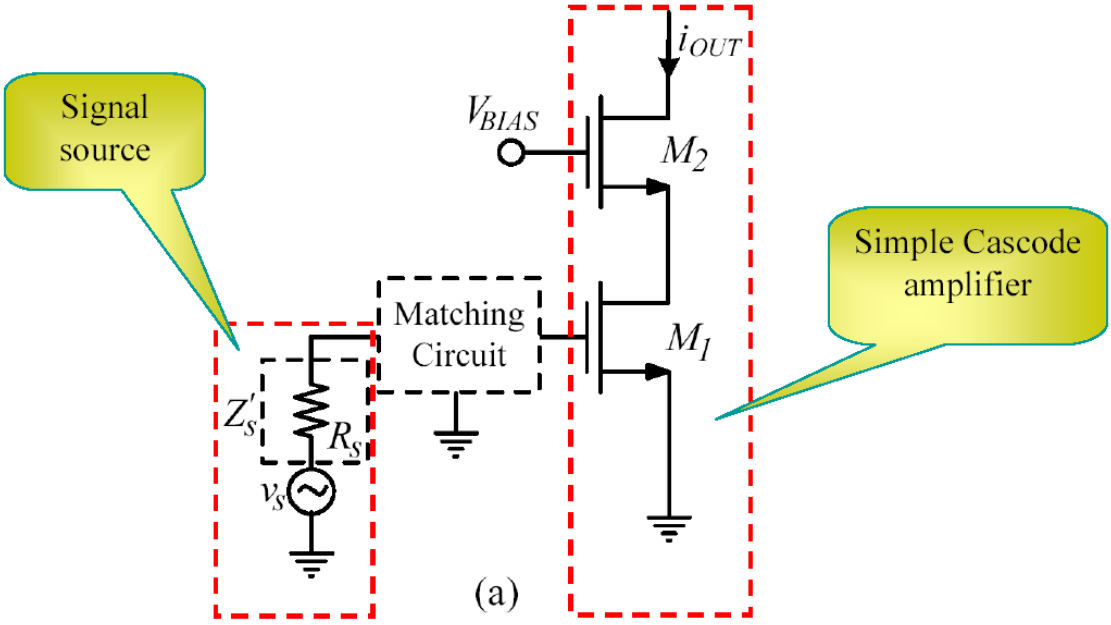
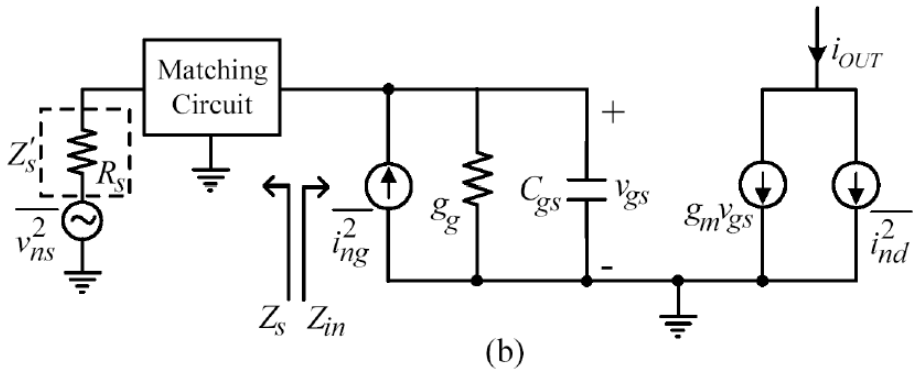


Fig. 3.1. (a) The schematic of cascode topology apply to adopt CNM technique (b) Small signal equivalent circuit



✓ **The mean-square channel thermal noise current**

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f \qquad (3.1)$$

✓ **The mean-square gate-induced noise current**

$$\overline{i_{ng}^2} = 4kT\delta g_g \Delta f \qquad (3.2)$$

$$g_g = \frac{\omega^2 C_{gs}^2}{5 g_{d0}} \qquad (3.3)$$

$$c \equiv \frac{\overline{i_{ng} \cdot i_{nd}^*}}{\sqrt{\overline{i_{ng}^2}} \cdot \sqrt{\overline{i_{nd}^2}}} \qquad (3.4)$$

- g_{do} is drain-source conductance at zero drain-source voltage
- k the Boltzmann constant
- T absolute temperature
- C_{gs} drain-source capacitor
- γ has value of 1 at V_{DS}= 0 and 2/3 at saturation mode
- γ increases to more than 2 in short channel device
- δ = 4/3 in long-channel and increases in short-channel devices
- c is correlation coefficient and equal to $j0.395$

The noise parameters are given by [3]

✓ **Noise Resistance**

$$R_n^o = \frac{\gamma}{\alpha} \cdot \frac{1}{g_m} a \qquad (3.5)$$

- For small R_n → increase transistor size and drain current

✓ **Minimum Noise Figure**

$$F_{min}^o = 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\gamma\delta(1 - |c|^2)} \qquad (3.6)$$

- Strong function of ω_T and ω
- Technology scaling → ω_T ↑ γ, σ, and c ↓ → F_{min} ↓

✓ **Optimum Noise Admittance**

$$Y_{opt}^{o} = \alpha\omega C_{gs}\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)} - sC_{gs}\left(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right) \quad (3.7)$$

$$\alpha \equiv g_m/g_{do}$$

- **Composed of real and imaginary value**
- **Increase with Tr. size and frequency**
- **Imaginary part: inductive but capacitive in frequency behavior**

  → allow only narrowband matching

✓ **From Fig. (b), the input admittance is**

$$Y_{in}^{o} = j\omega C_{gs} \quad (3.8)$$

$$\Rightarrow \quad Y_{in}^{o*} = -j\omega C_{gs}$$

$$Y_{opt}^{o} = \alpha\omega C_{gs}\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)} - sC_{gs}\left(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)$$

- Y_{in}^{o*} **Imaginary component only**
- **Inherent mismatch between** Y_{in}^{o*} **and** Y_{opt}^{o}

  → no simultaneous noise and input matching

- ✓ **Design for minimum NF by presenting Z_{opt} to the given transistor**
- ✓ **Typically require matching circuit**
- ✓ **Can achieve NF = F_{min} of input transistor**
- ✓ **Inherent mismatch between Z_{opt} and Z_{in}^{*} → input mismatch**
- ✓ **Often compromise gain and noise performance**

3.2. Simultaneous Noise and Input Matching Technique

3.2.1. Circuits Topology

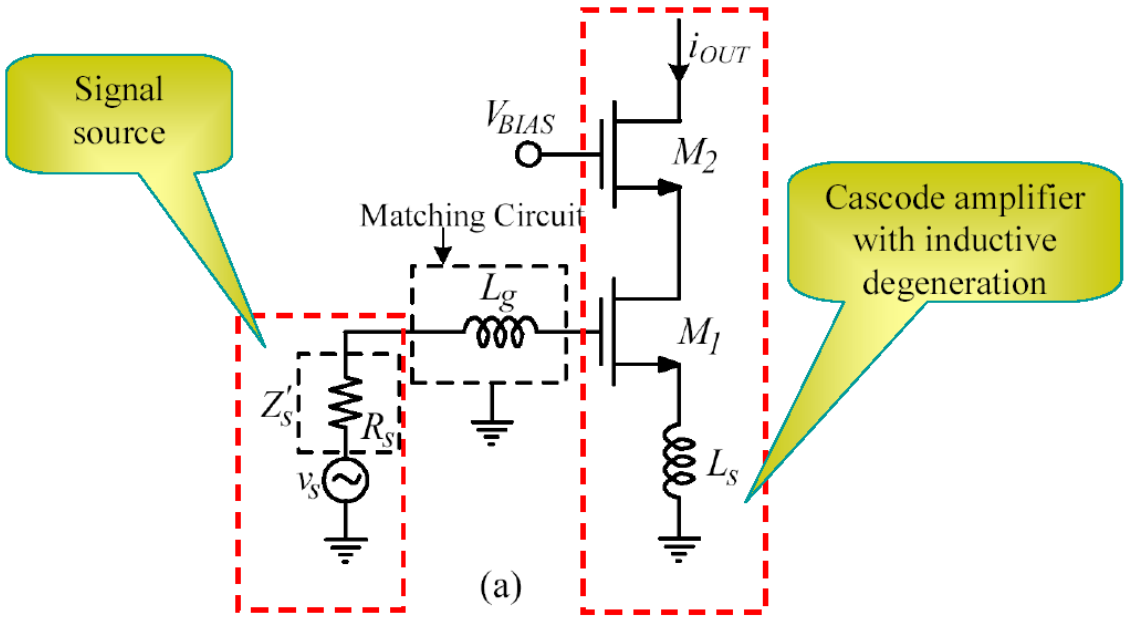
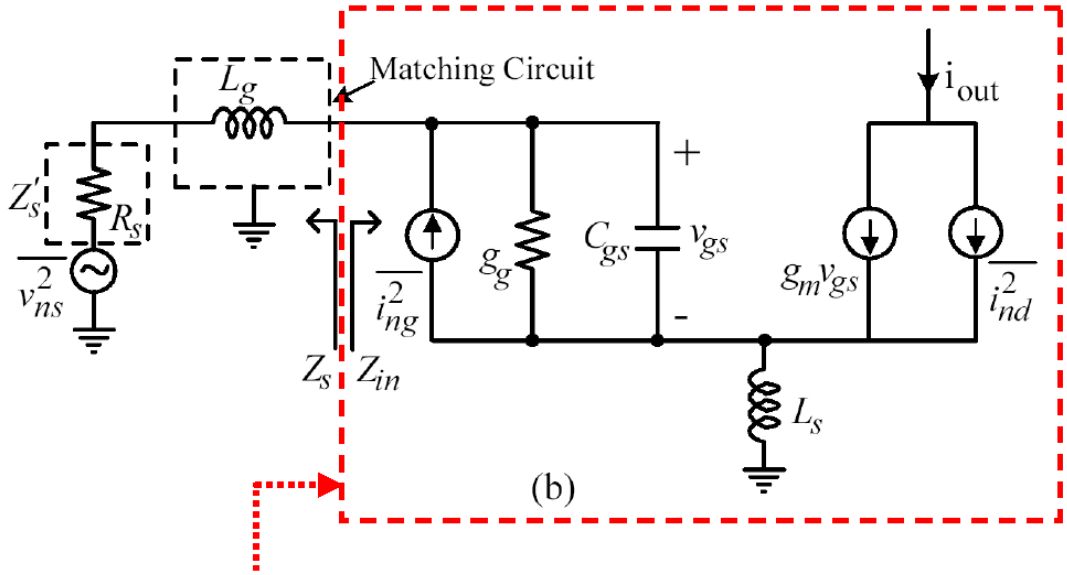


Fig. 3.2. (a) The schematic of cascode topology apply to adopt SNIM technique (b) Small signal equivalent circuit

Assume inductors are lossless, and matching circuit is implemented by a series inductor, but results are valid for arbitrary matching circuits.



Obtain noise parameters by applying KCL/KVL

3.2.2. Noise Parameters

The noise parameters are given by [Appendix]

✓ **Noise Figure Expression**

$$F = 1 + \frac{1}{g_m^2 R_s} \cdot \left\{ \begin{array}{l} \gamma g_{d0} \cdot \left\{ \begin{array}{l} \left[1 + s^2 C_{gs} \left(L_g + L_s \right) \left(1 + |c| \alpha \sqrt{\frac{\delta}{5\gamma}} \right) \right]^2 \\ -\left(sC_{gs} R_s \right)^2 \left(1 + |c| \alpha \sqrt{\frac{\delta}{5\gamma}} \right)^2 \end{array} \right\} \\ -\frac{\alpha\delta}{5} \left(1 - |c|^2 \right) g_m \left(sC_{gs} \right)^2 \left(R_s^2 - sL_g^2 \right) \end{array} \right\} \quad \textbf{(3.9)}$$

✓ **Noise Resistance**

$$R_n = R_n^o = \frac{\gamma}{\alpha} \cdot \frac{1}{g_m} \tag{3.10}$$

✓ **Minimum Noise Figure**

$$F_{min} = F_{min}^o = 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\gamma\delta(1 - |c|^2)} \tag{3.11}$$

Same as that of the CNM technique

✓ **Optimum Noise Impedance**

$$Z_{opt} = Z_{opt}^o - sL_s \tag{3.12}$$

$$Z_{opt}^o = 1/Y_{opt}^o = \frac{\alpha\sqrt{\dfrac{\delta}{5\gamma\left(1-|c|^2\right)}} + j\left(1 + \alpha|c|\sqrt{\dfrac{\delta}{5\gamma}}\right)}{\omega C_{gs}\left\{\dfrac{\alpha^2\delta}{5\gamma\left(1-|c|^2\right)} + \left(1 + \alpha|c|\sqrt{\dfrac{\delta}{5\gamma}}\right)^2\right\}} \tag{3.13}$$

- L_s → **No effect on Re[Z_{opt}], but cancel out Im[Z_{opt}]**

✓ **The input impedance Z_{in} can be expressed as**

$$Z_{in} = sL_s + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}} = sL_s + \frac{1}{sC_{gs}} + \omega_T L_s \qquad \textbf{(3.14)}$$

✓ **From Eq. (13), Eq. (12) can be re-expressed as**

$$Z_{opt} = \mathrm{Re}\left[Z_{opt}^{o} \right] - m\frac{1}{sC_{gs}} - sL_s \qquad \textbf{(3.15)}$$

- **m = 0.6 for the typical device parameters of long channel**
- **m ≈ 1 with the advantage technologies (0.25 um CMOS, c ≈ 0.5, α < 1 [39])**

→ **L_s help to bring the $Z_{opt} \approx Z_{in}^{*}$ while causing no degradation in F_{min} and R_n**

✓ **The condition that allows simultaneous noise and input matching is**

$$Z_{opt} = Z_{in}^{*} \tag{3.16}$$

✓ **Or**

$$\mathrm{Re}[Z_{opt}] = \mathrm{Re}[Z_s] \tag{3.17}$$

$$\mathrm{Im}[Z_{opt}] = \mathrm{Im}[Z_s] \tag{3.18}$$

$$\mathrm{Im}[Z_{in}] = -\mathrm{Im}[Z_s] \tag{3.19}$$

$$\mathrm{Re}[Z_{in}] = \mathrm{Re}[Z_s] \tag{3.20}$$

Step-by-Step Design process

1) **For a given Z_s,**
2) **Choose C_{gs}(or W) that satisfies Re[Z_{opt}] = Re[Z_s]**
3) **Choose L_s that satisfies Im[Z_{opt}] = Im[Z_s]**
4) **Choose V_{GS} that satisfies Re[Z_{in}] = Re[Z_s]**
5) **Given L_s satisfies Im[Z_{in}^{*}] ≈ Im[Z_{opt}] automatically**
6) **→ $Z_{opt} = Z_{in}^{*} = Z_s$**
7) **If Z_s is not equal to Z_s', add matching circuit**
8) **→ Noise/input matched simultaneously for given Z_s**

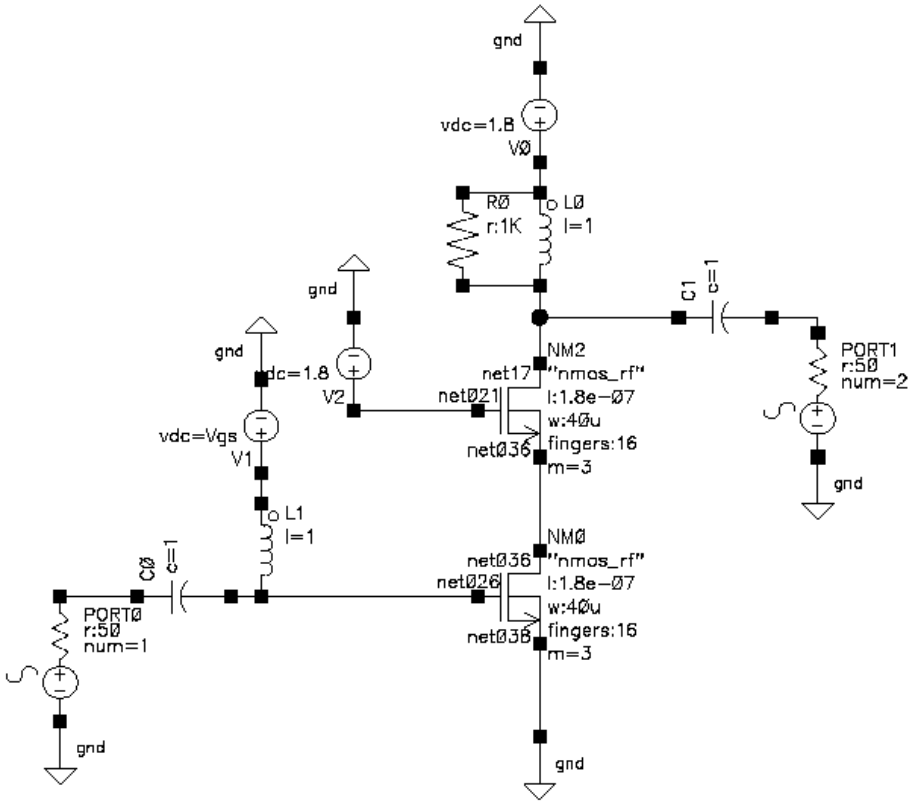
3.2.3. Design Process

The following steps describe the procedure how to design LNA based on cascode topology. Since there is no guideline how to choose the cascode transistor to obtain the best performances such as NF, Power gain, and Linearity. Assume that the size of cascode transistor is chosen to be equal to the input transistor. And also assume that the gate bias of the cascode transistor is V_{dd}.

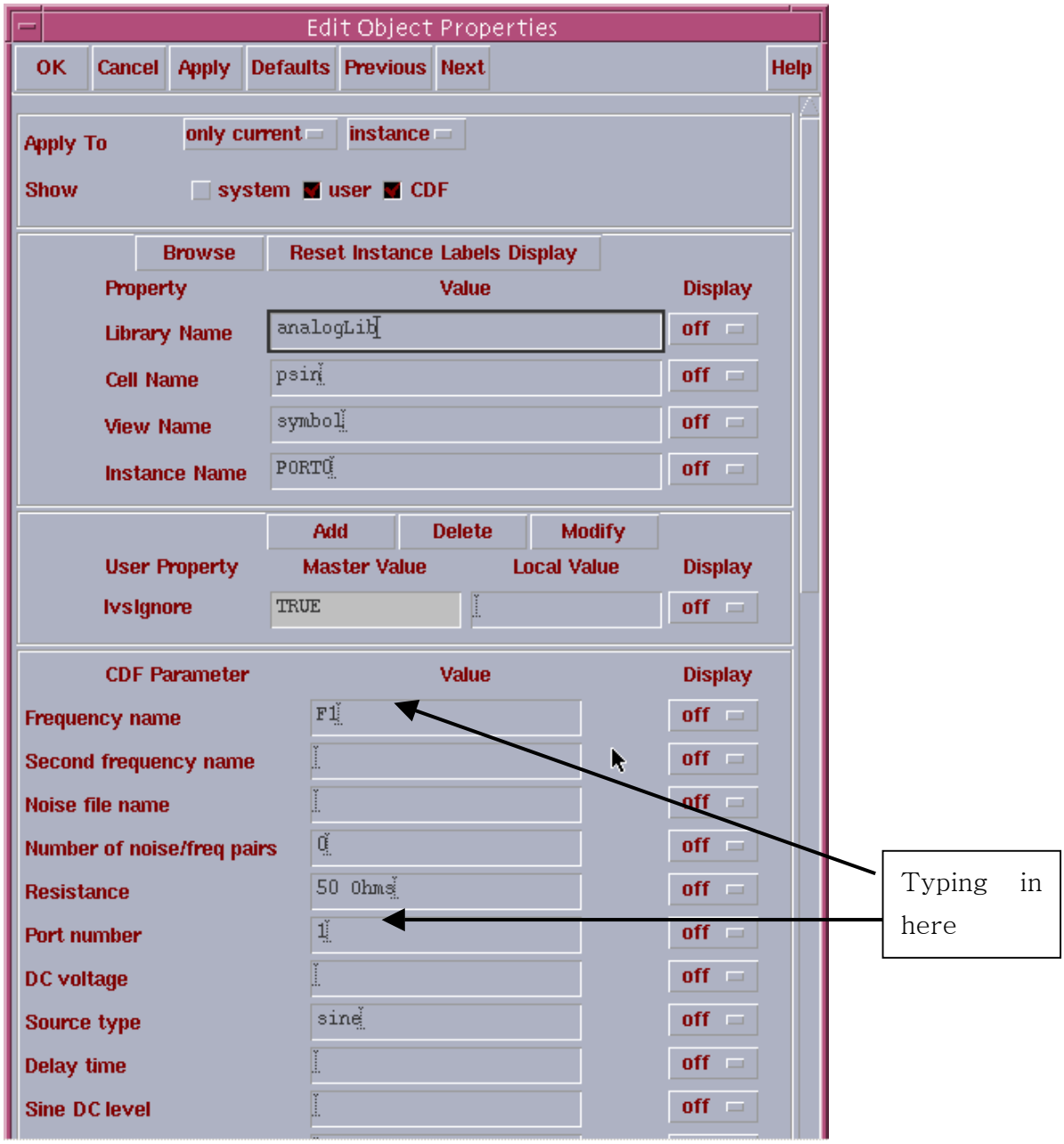
1) Choose V_{GS}

a) Setup Environment

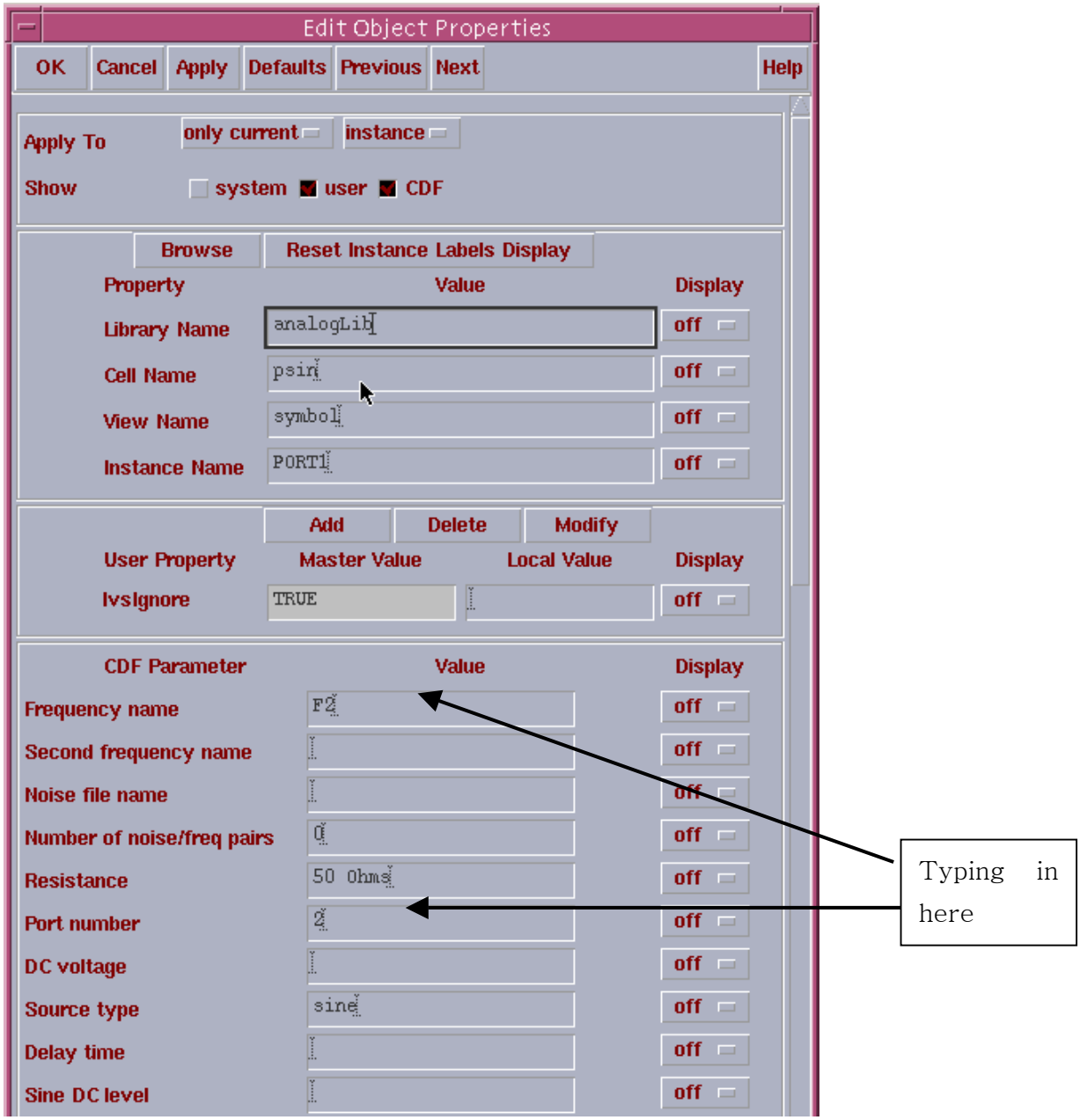
In the library named as LNA example, open new cell view named as Choose V_{GS}. Based on the knowledge conducted in the “Basis cadence lecture”, build the circuit as below.



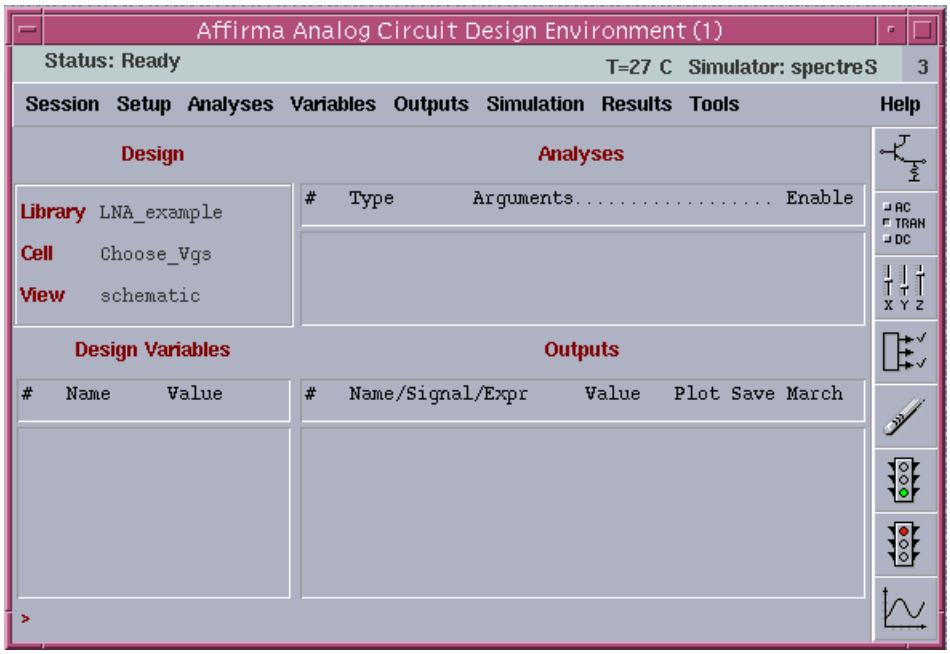
- Highlight *input port* and modify it as



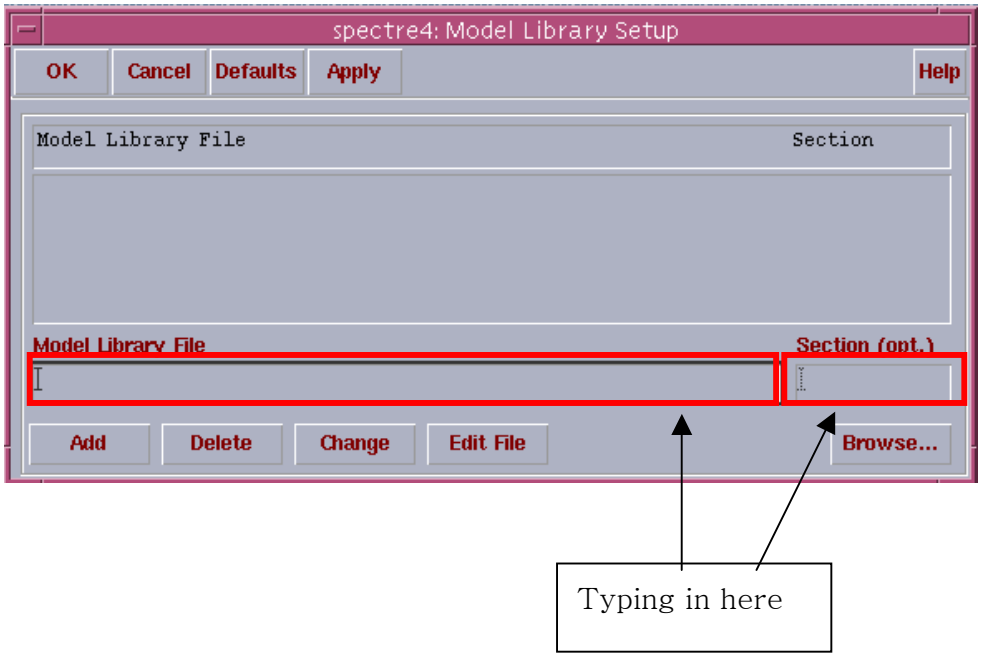
- Highlight *Output port* and modify it as



- From the schematic window select: *Tool- Analog Environment*



- On the Analog Circuit Design Environment, Click *Setup-Model libraries*



- In the *Model Library File* and *Section* fields typing as following

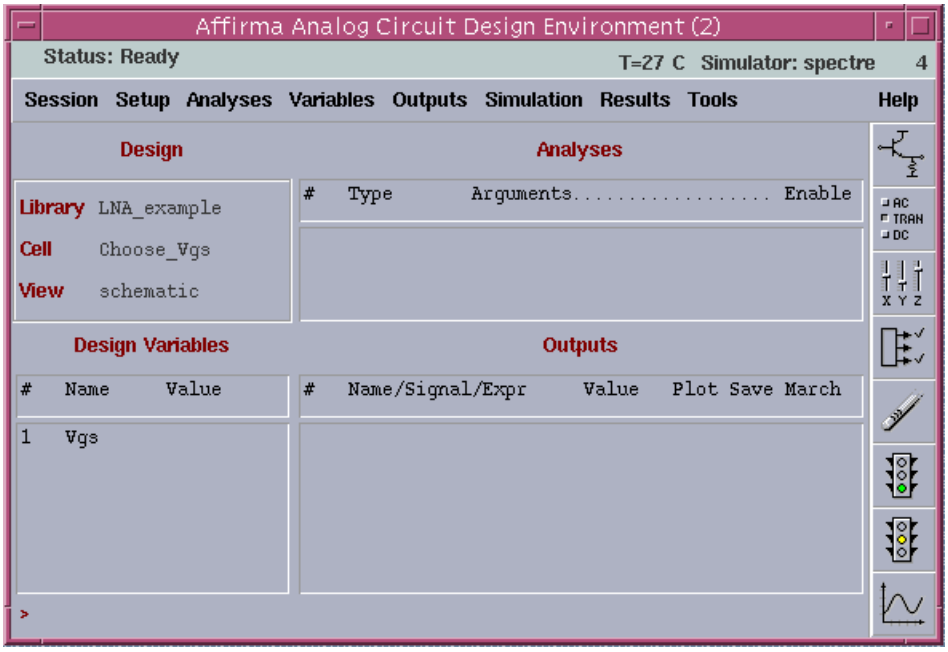
Model Library File	Section (opt.)
/data1/RACS/DC_project/Tsmc18/models/mm018.scs	tt
/data1/RACS/DC_project/Tsmc18/models/mm018.scs	tt_3v
/data1/RACS/DC_project/Tsmc18/models/mm018.scs	tt_na
/data1/RACS/DC_project/Tsmc18/models/mm018.scs	tt_3vna
/data1/RACS/DC_project/Tsmc18/models/mm018.scs	tt_m
/data1/RACS/DC_project/Tsmc18/models/mm018.scs	tt_3m
/data1/RACS/DC_project/Tsmc18/models/mm018.scs	ees
/data1/RACS/DC_project/Tsmc18/models/mm018.scs	tt_bip
/data1/RACS/DC_project/Tsmc18/models/mm018.scs	tt_bip3
/data1/RACS/DC_project/Tsmc18/models/mm018.scs	dio
/data1/RACS/DC_project/Tsmc18/models/rf018.scs	tt_rfmos
/data1/RACS/DC_project/Tsmc18/models/ResModel.scs	res_t

➢ You can Click *Browse* and go up to the directory, which contain the model library of the technology you would like to use. Or instructors will introduce the path of model library

- Notice: After you finish typing one section, press *Add* icon. If you make some mistakes, you can delete by click *Delete* icon

- On the Analog Environment Window, Click *Variable-Copy from cell view*.

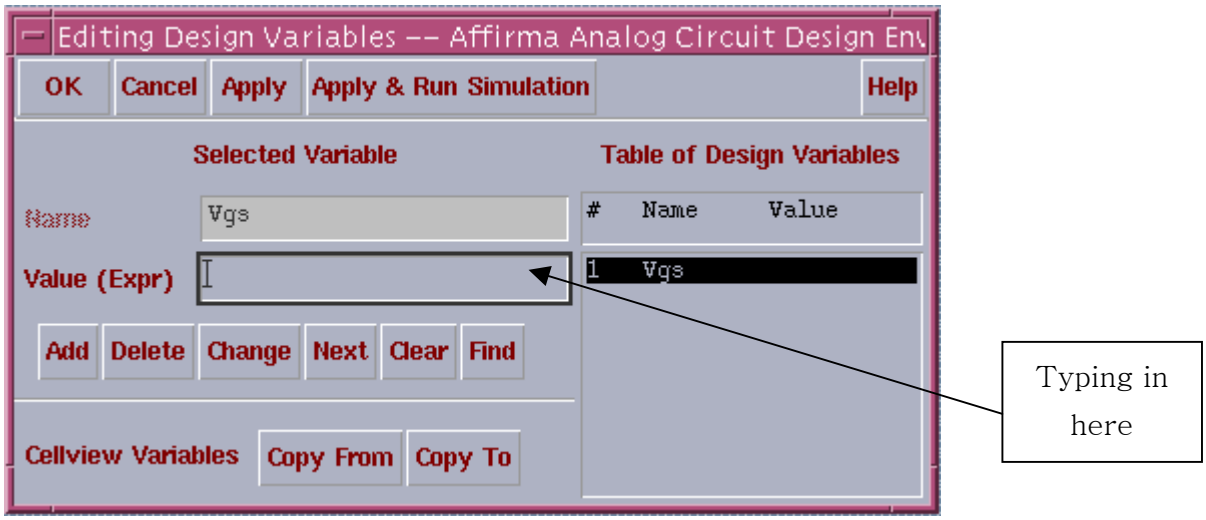
➢ Analog Environment window looks like



- Click edit variable icon on the right hand side 

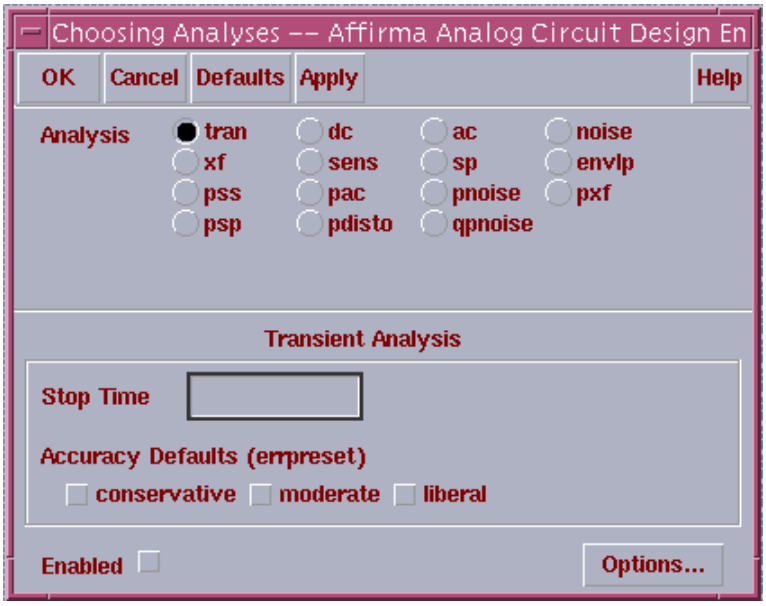
The following window will appear.

- Highlight V_{GS} and typing its primary value (any value)

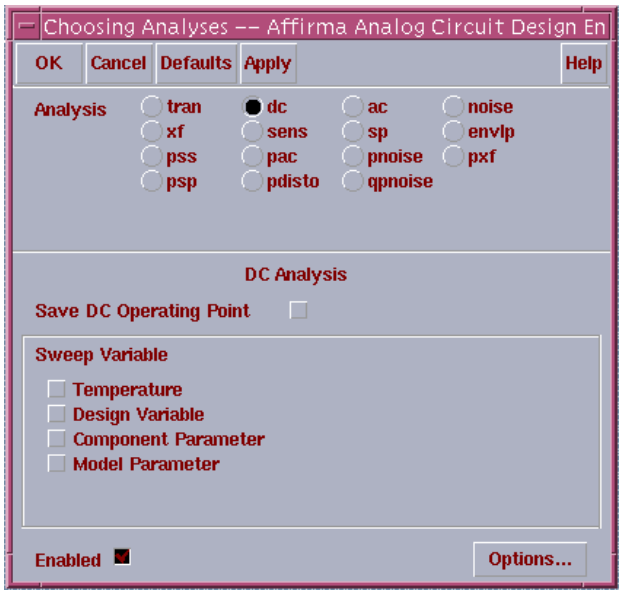


- On the Analog Circuit Design Environment, select *Analyses – Choose*.

  The window will appear as

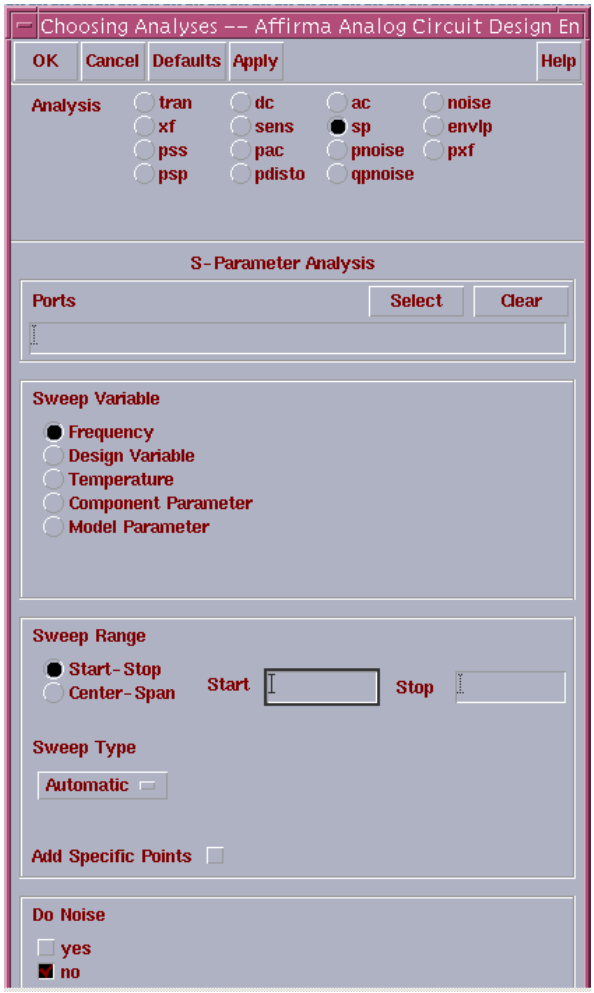


- On the choosing Analyses window, highlight *DC* simulator and modify the field as

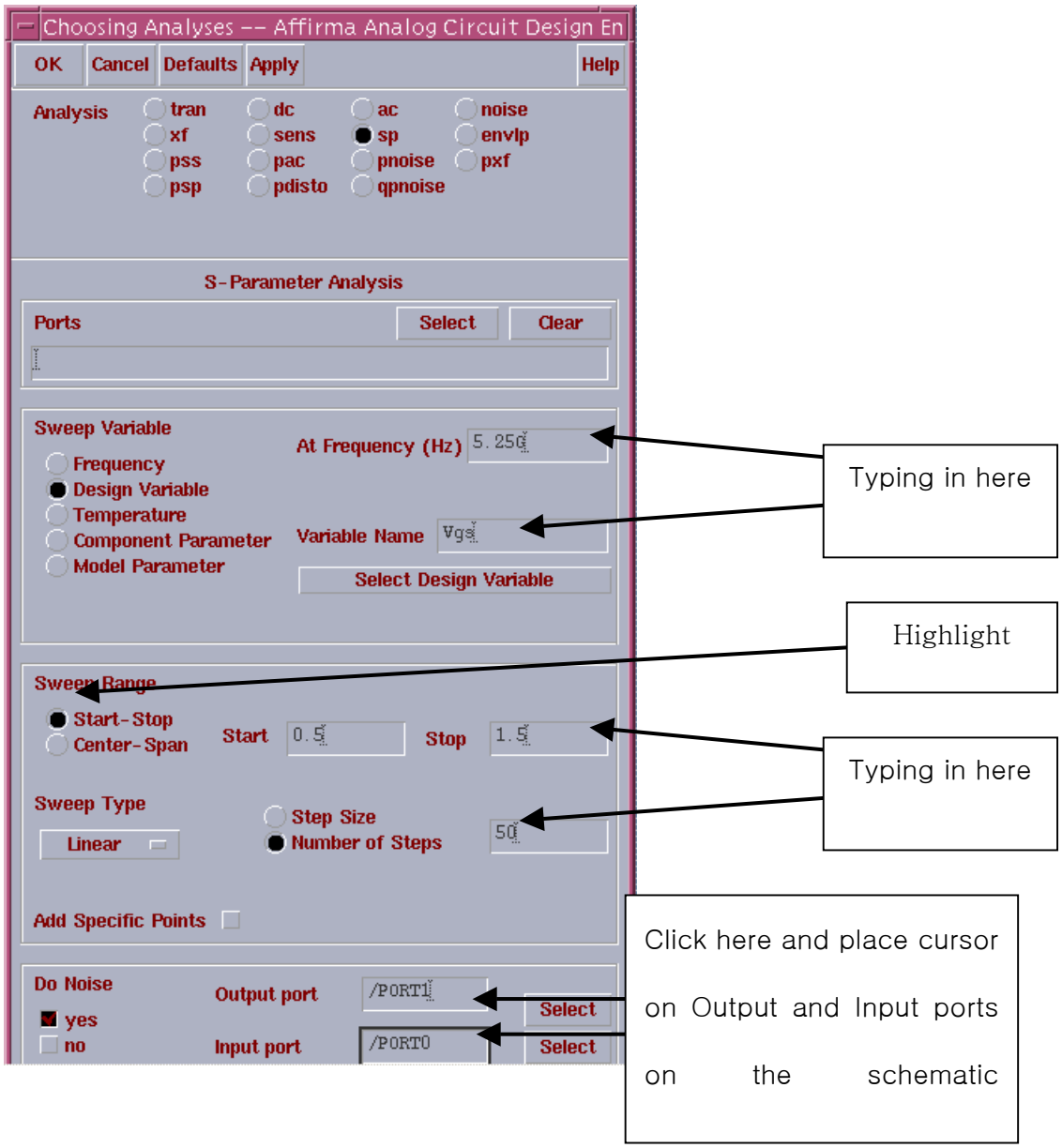


- Click *Apply* icon.

- Choose *SP* Simulator, the window appear as



- Modify your window to become as follows

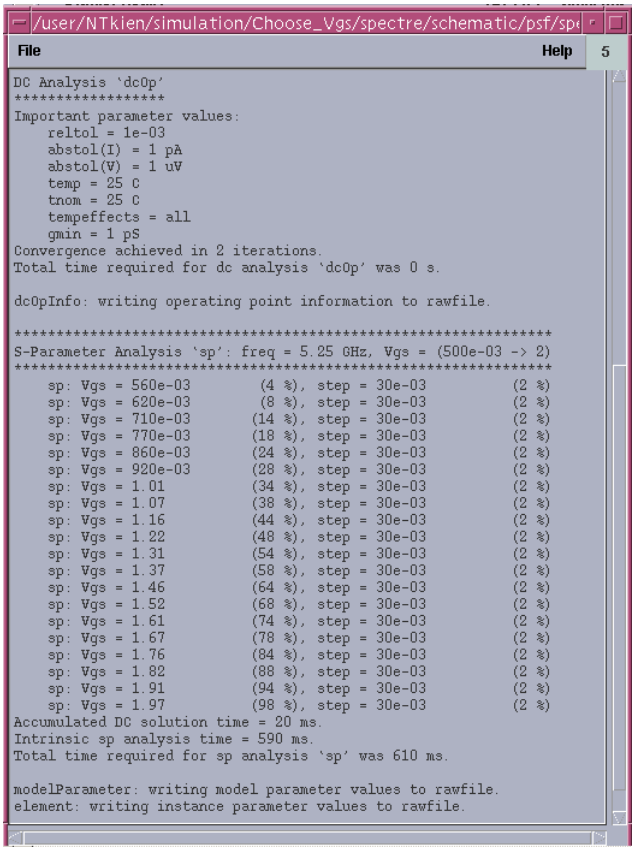

Choosing Analyses -- Affirma Analog Circuit Design En
OK
Cancel
Defaults
Apply
Help
Analysis
tran
dc
ac
noise
xf
sens
sp
envlp
pss
pac
pnoise
pxf
psp
pdisto
qpnoise
S-Parameter Analysis
Ports
Select
Clear
Sweep Variable
At Frequency (Hz)
5.25G
Frequency
Design Variable
Temperature
Component Parameter
Model Parameter
Variable Name
Vgs
Select Design Variable
Sweep Range
Start-Stop
Center-Span
Start
0.5
Stop
1.5
Sweep Type
Linear
Step Size
Number of Steps
50
Add Specific Points
Do Noise
yes
no
Output port
/PORT1
Input port
/PORT0
Select
Select
Typing in here
Highlight
Typing in here
Click here and place cursor on Output and Input ports on the schematic

- Click *OK*

b) Run simulation

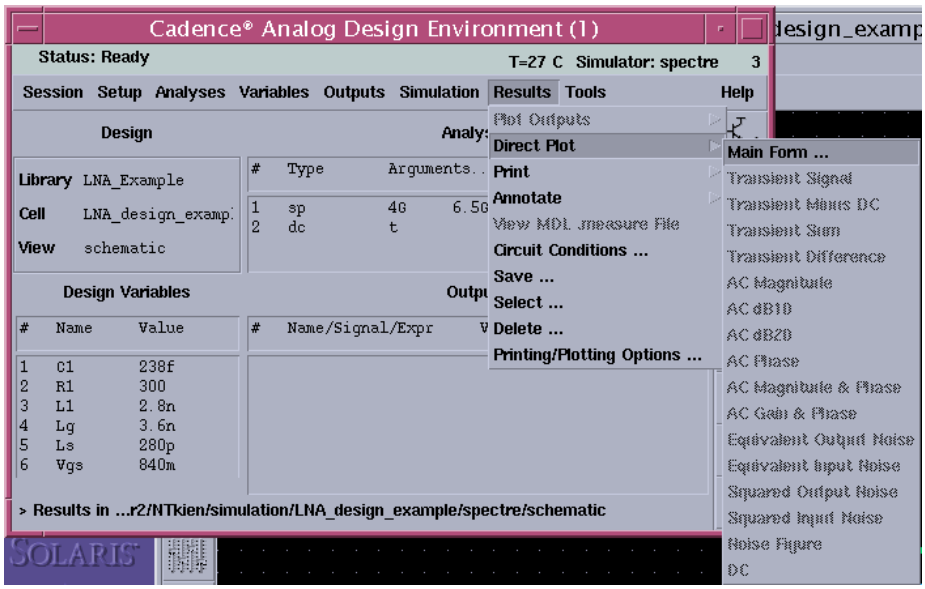
- Click *Netlist and Run* icon 

- After simulation is finished you can see the window looks like



c) Plotting Results

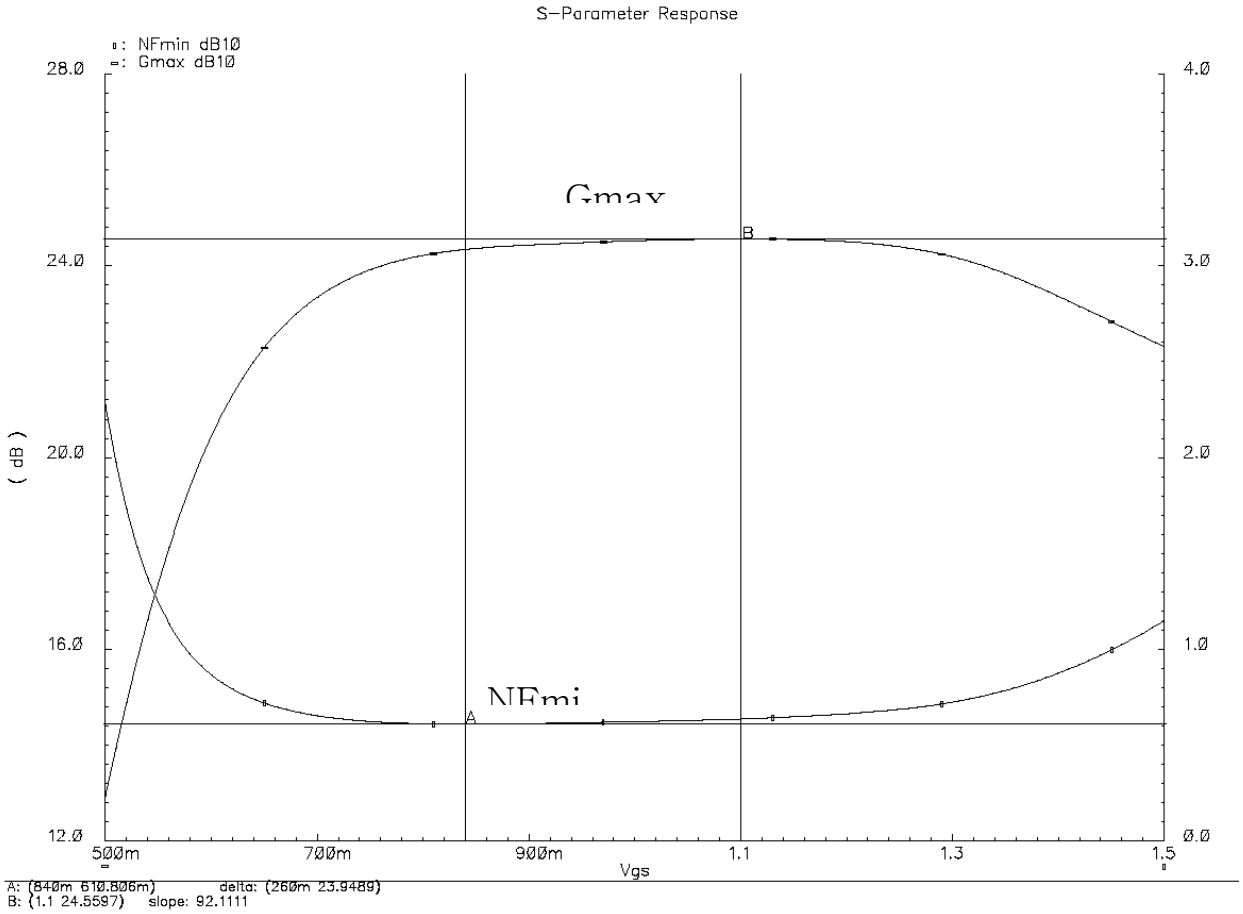
- In the Simulation window, select *Results → Direct Plot → Main* Form.



- The window will appears as

- On the *SP-Parameters Result Form*, do following

- Highlight *Append* for *Plot Mode*
- Highlight *Gmax* for *Function*
- Highlight *Rectangular* for *Plot Type*
- Highlight *dB10* for *Modifier*
- Click *Plot*
- Choose *NFmin* for *Function*
- Highlight Rectangular for *Plot Type*
- Highlight *dB10* for *Modifier*
- Click *Plot*



From above figures, we can determine the value of V_{gs} that gives the minimum

NF and maximum available gain. As can be seen in this figure, we choose V_{gs} = 840 mV.

2) Choose Size of Transistor

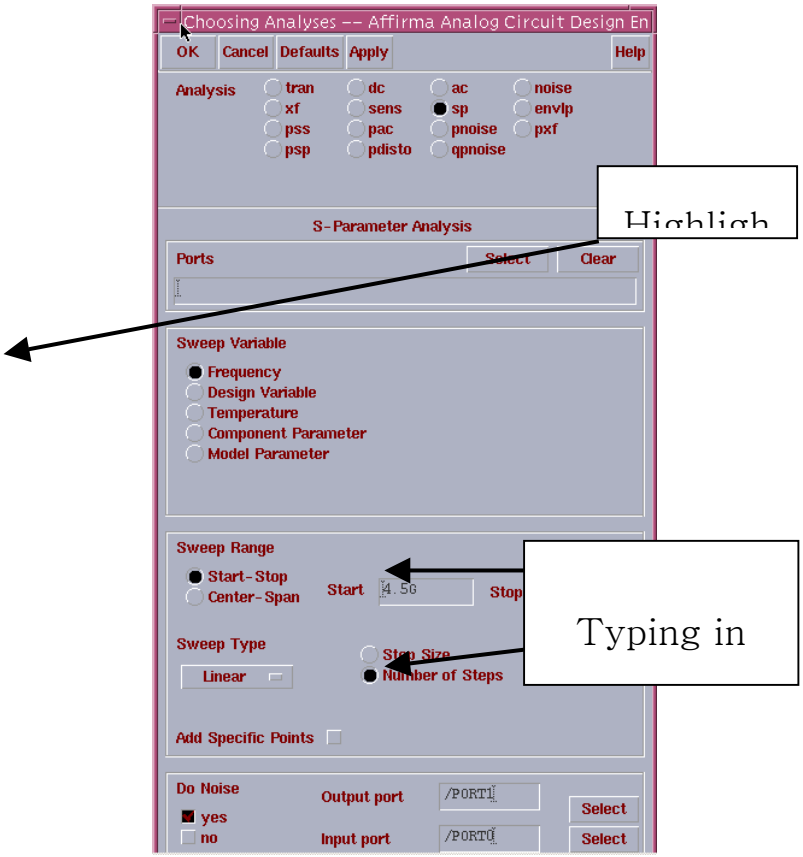
❖ Choose the size of transistor by simulating Γ_{opt} = 50 Ω factor

a) Setup environment

We can set the multiplier factor of transistor as a variable and do the simulation to find the optimum value. But in this process the multiplier cannot be a variable therefore we have to do some simulation steps to find the optimum value of multiplier factor.

➢ Setting the simulation window as

- Setting V_{gs} = 840 mV.
- Modify SP simulator as below.



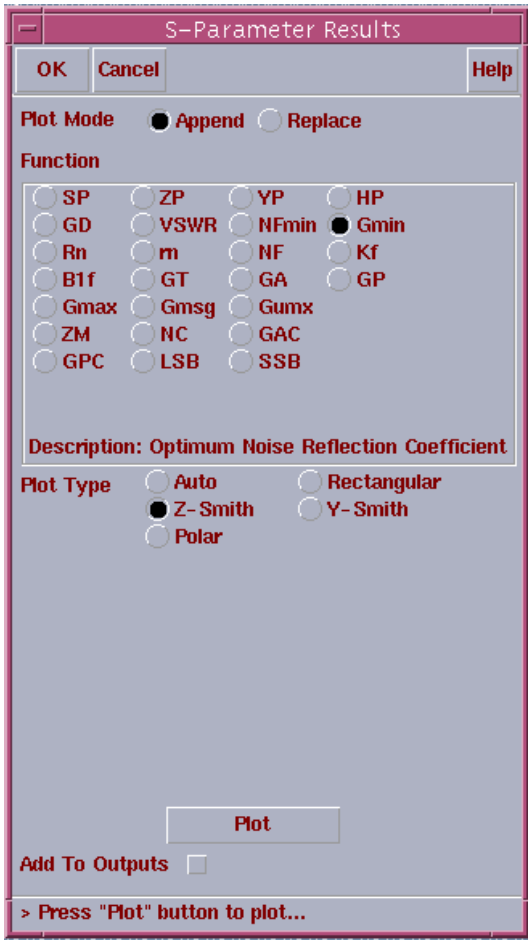
- Click *OK*

b) Run Simulation

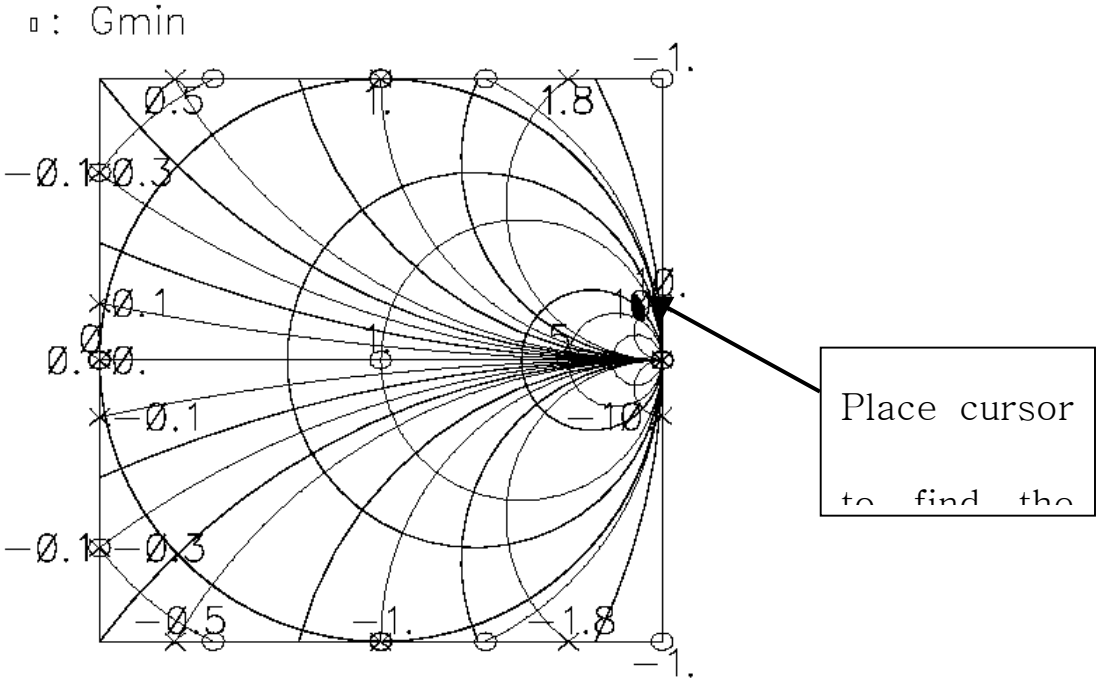
- Click *Run* simulation icon

c) Plotting Results

- After simulation finish click *Results → Main For → S-parameters.*
- On the *S-Parameter* Results window do following
  - Choose *Gmin* (Optimum noise Reflection Coefficient) for *Function*
  - Choose *Z-Smith* for *Plot Type*


S-Parameter Results
OK
Cancel
Help
Plot Mode
Append
Replace
Function
SP
ZP
YP
HP
GD
VSWR
NFmin
Gmin
Rn
m
NF
Kf
B1f
GT
GA
GP
Gmax
Gmsg
Gumx
ZM
NC
GAC
GPC
LSB
SSB
Description: Optimum Noise Reflection Coefficient
Plot Type
Auto
Rectangular
Z-Smith
Y-Smith
Polar
Plot
Add To Outputs
> Press "Plot" button to plot...

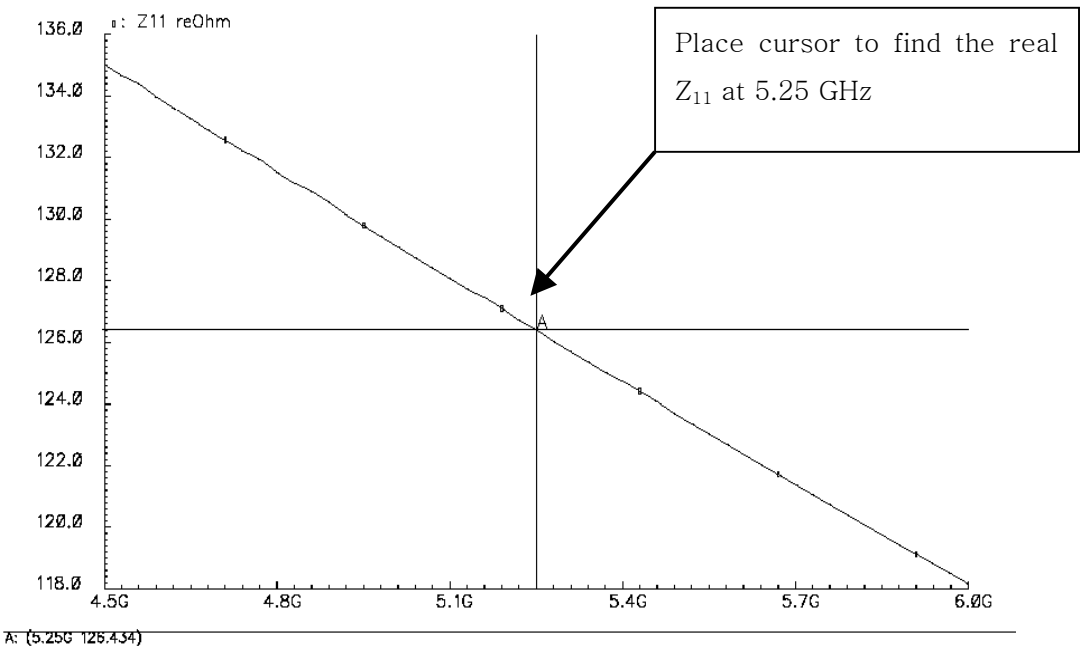
- Click *Plot*


: Gmin
Place cursor

Another way to see the result

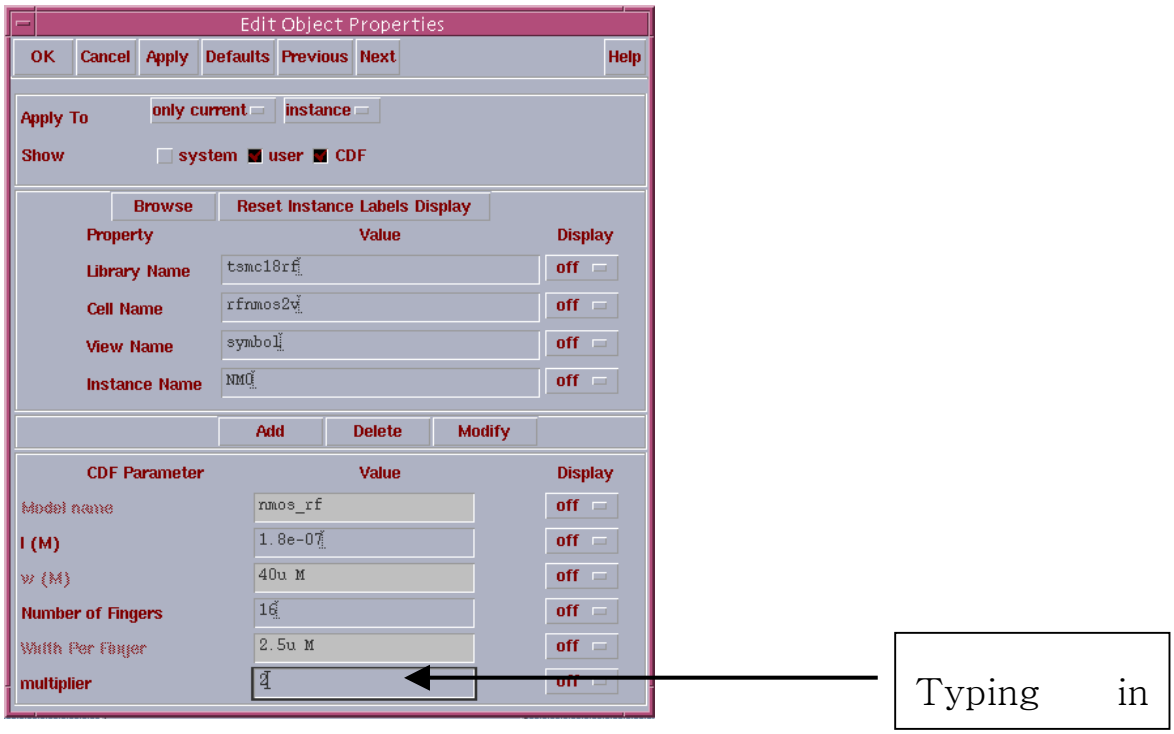
- On the Analog Circuit Design Environment, do following
  - Highlight *ZP* (Z parameters) for *Function*
  - Highlight *Rectangular* for *Plot Type*
  - Highlight *Real* for *Modifier*

- Click *Z11* we can see the results as below



➢ On the Schematic window do following

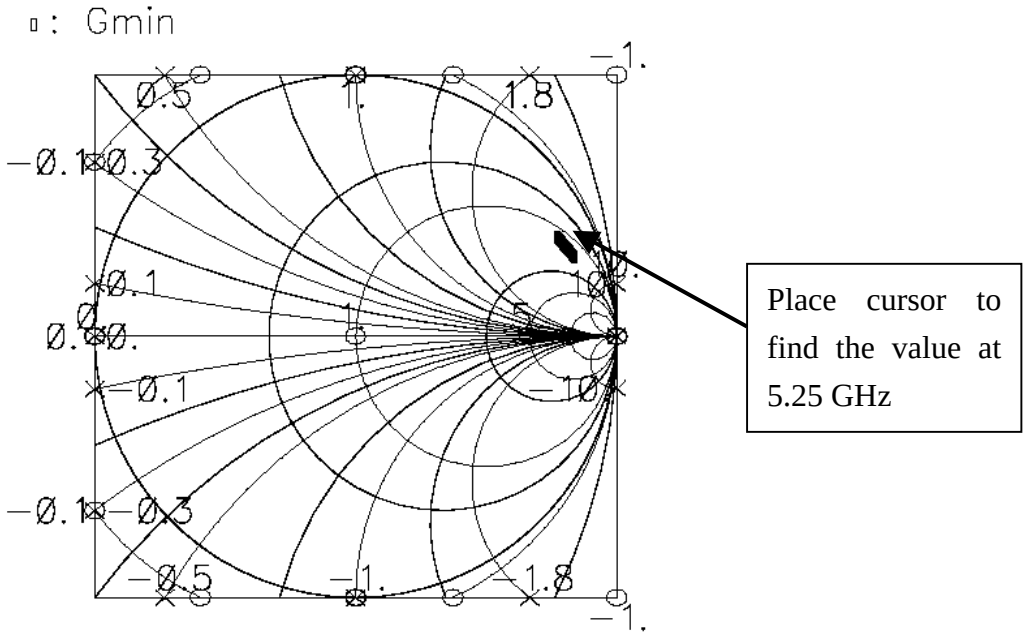
- Highlight *NMOS* transistor by press *Q*
- On the properties window, change *multiplier* = 2.



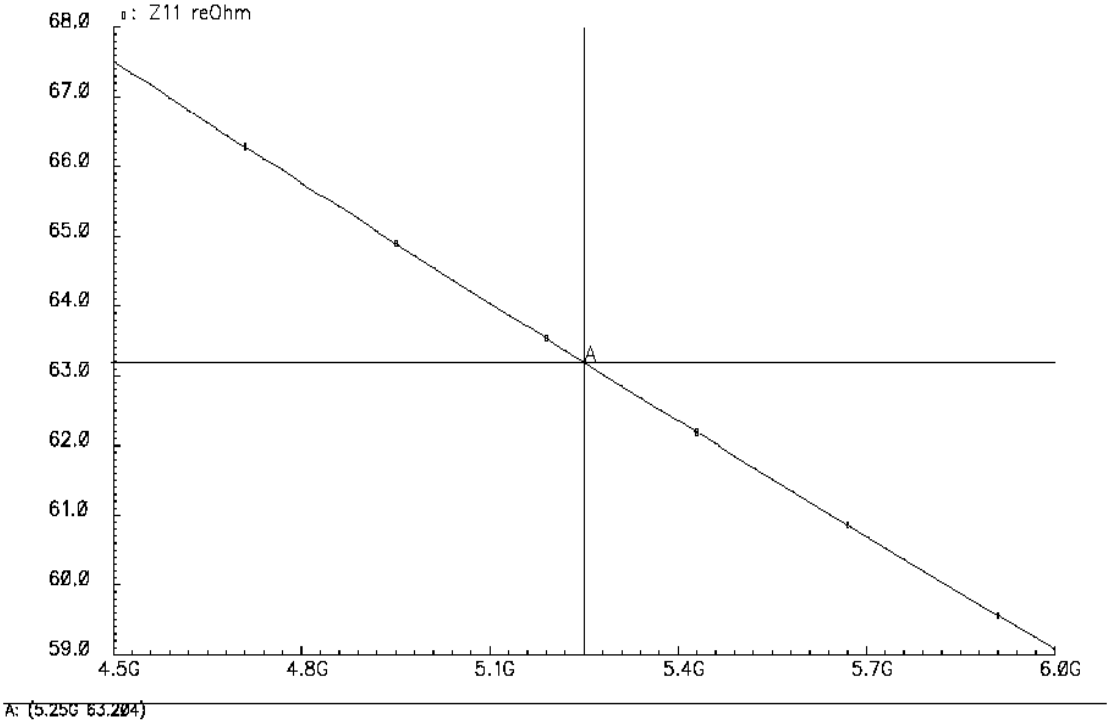
- Press *OK*

- Press *Save and Check* icon

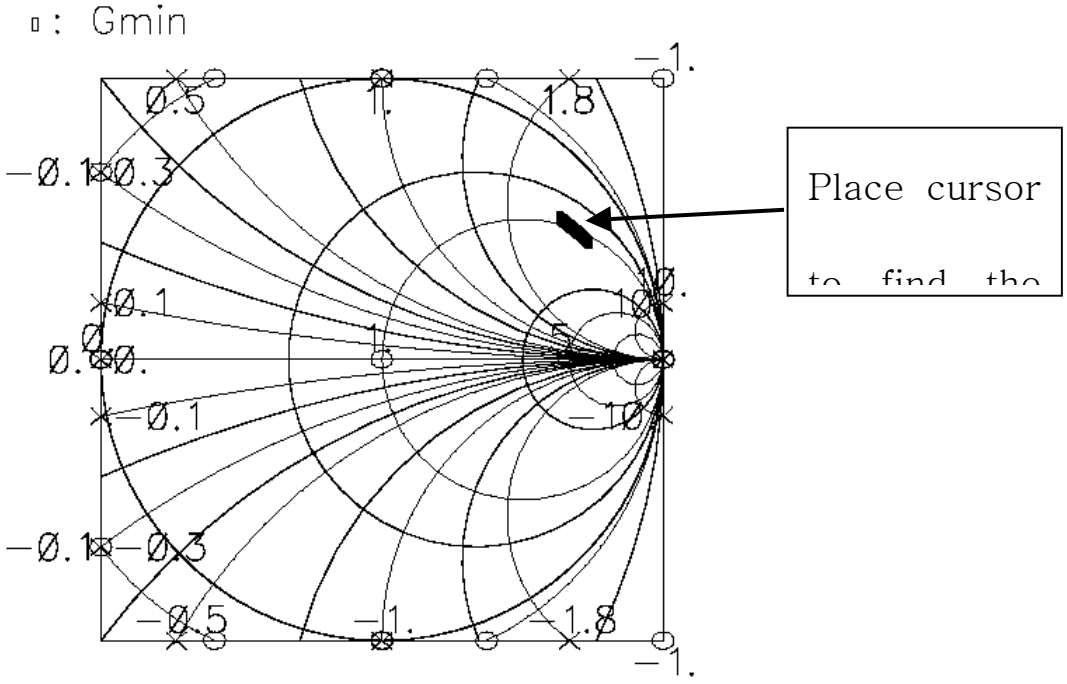
Run simulation and plot result (do the same steps as previous)

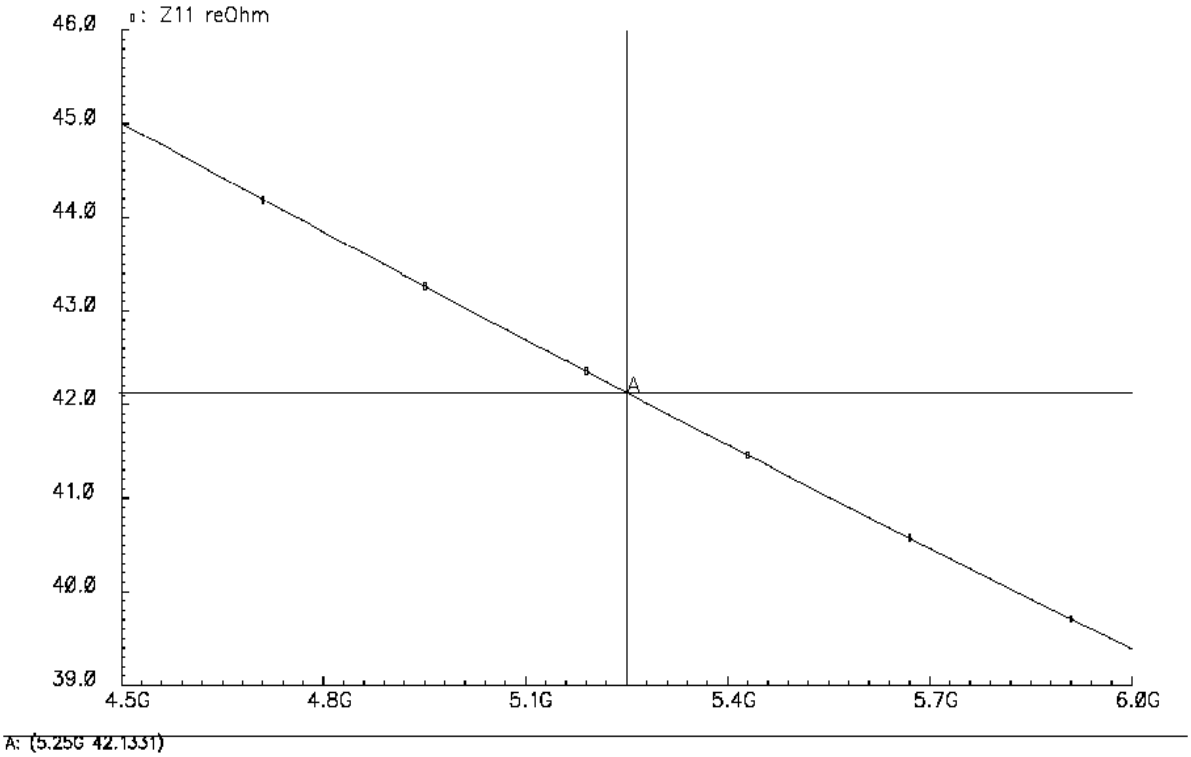


- Do the same step to plot the *Z11*

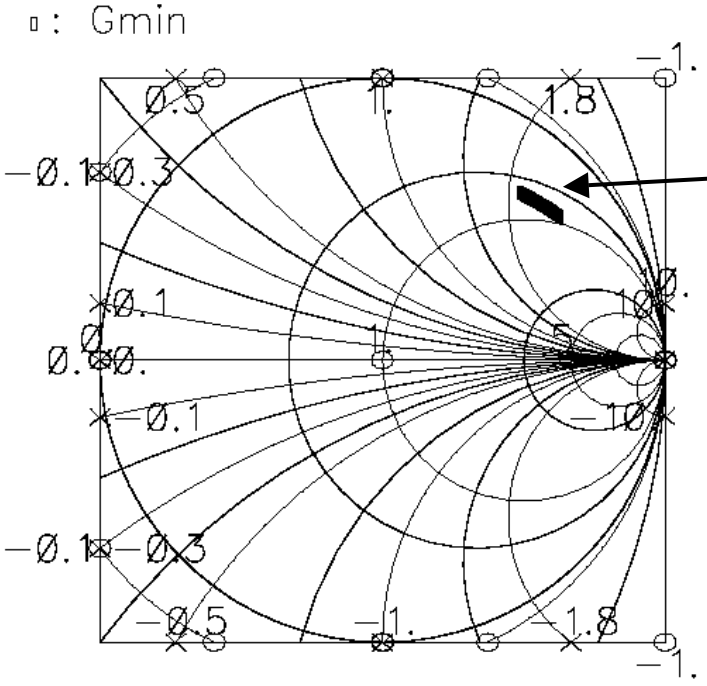


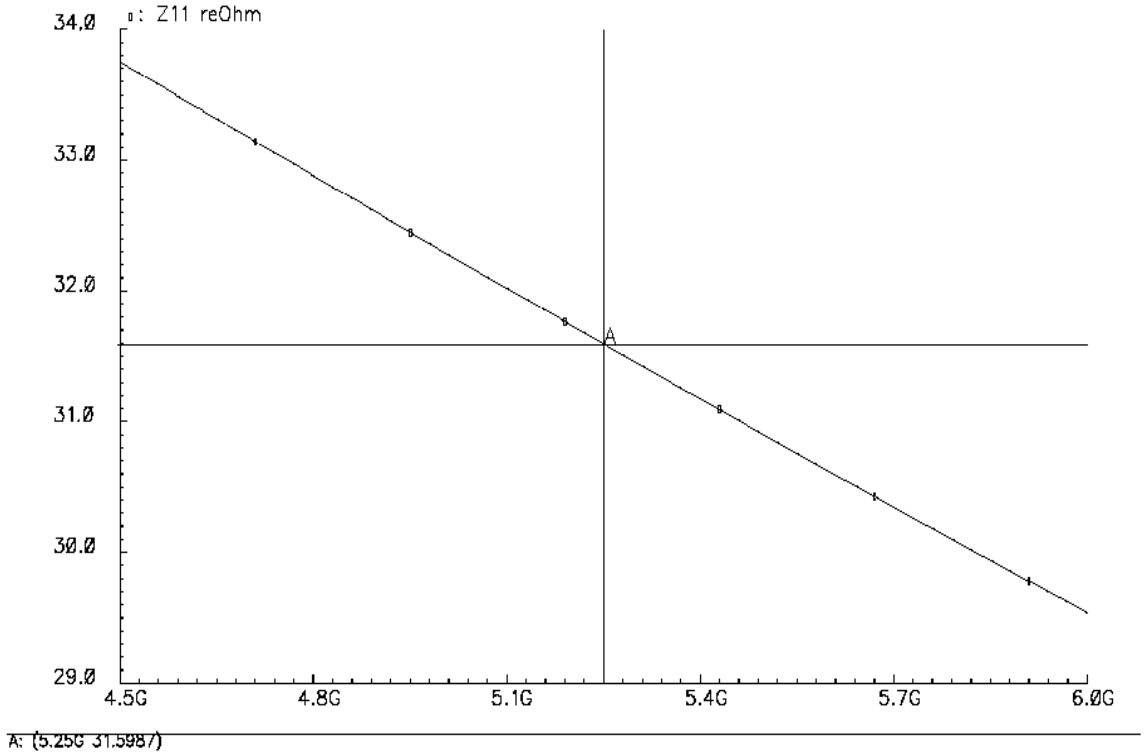
- Do the same above steps for *multiplier* = 3, you obtain the result as





- Do the same above steps for *multiplier* = 4, you obtain the result as





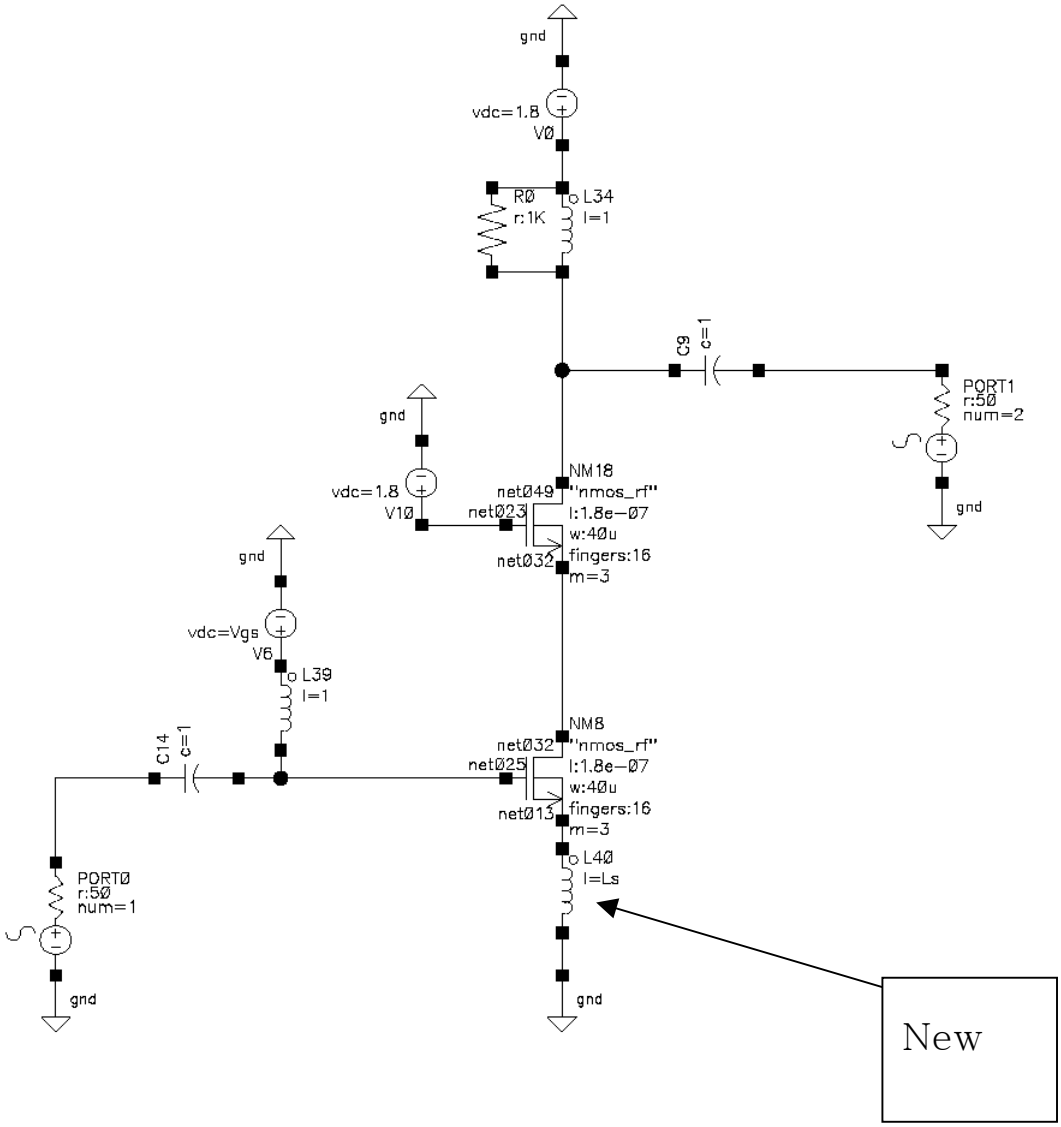
As can be seen from above figures, when multiplier factor = 3, the real part of G_{min} = 1.

3) Choose L_s (Inductor Degeneration)

This step is to choose the value of L_s that makes the real part of S_{11} = 1

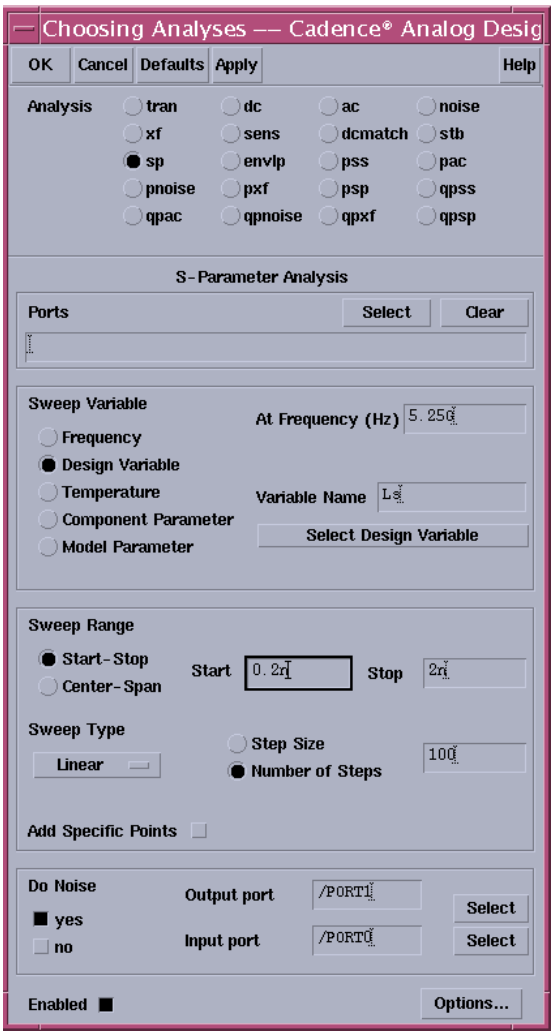
a) Setup Environment

- In the schematic window, insert new inductor as below



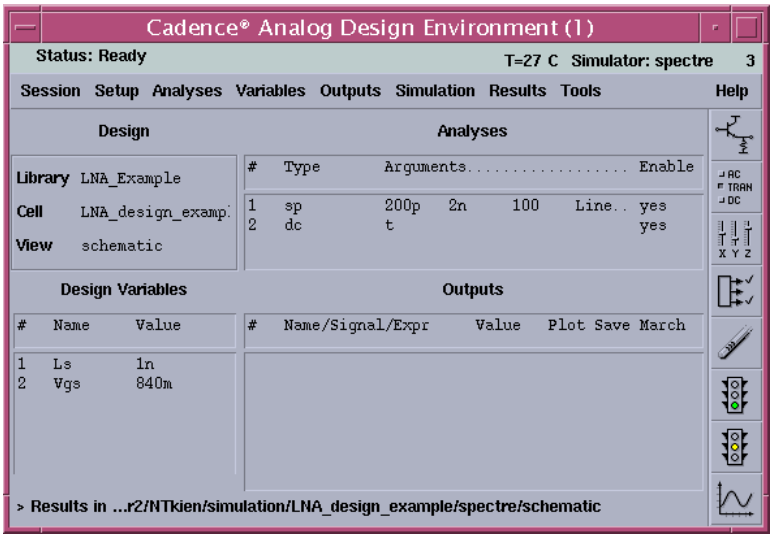
- A new inductor has inductance value as Ls
- On the Analog Circuit Design Environment do the following
  - Select Variables – Copy From Cell View
  - Setting primary value of Ls (any value)

- Modify *SP* simulation looks like



- Click *OK*

- Now your Circuit Design Environment looks like



b) Run Simulation

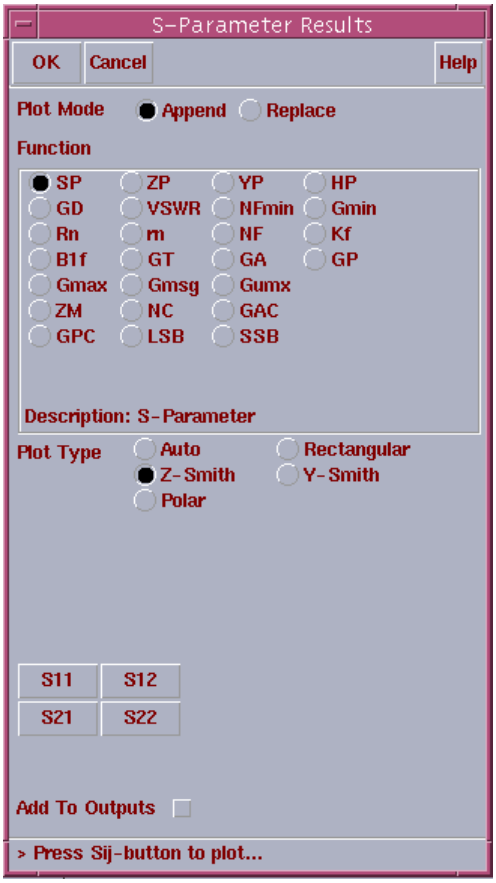
➢ Click *Netlist and Run* icon

c) Plotting Results

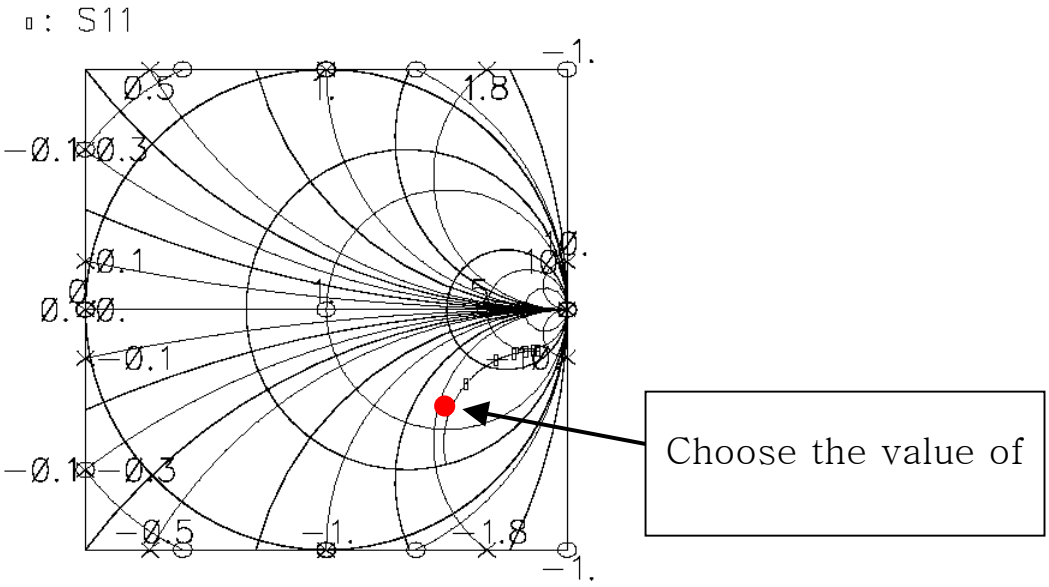
➢ After finish simulation, select *Results → Direct Plot → Main Form*

➢ On the *S-Parameter Results* window do following

- Highlight *SP* (S parameters) for *Function*
- Highlight *Z-Smith* for *Plot Type*



➢ Click *S11*, you can see the result as below

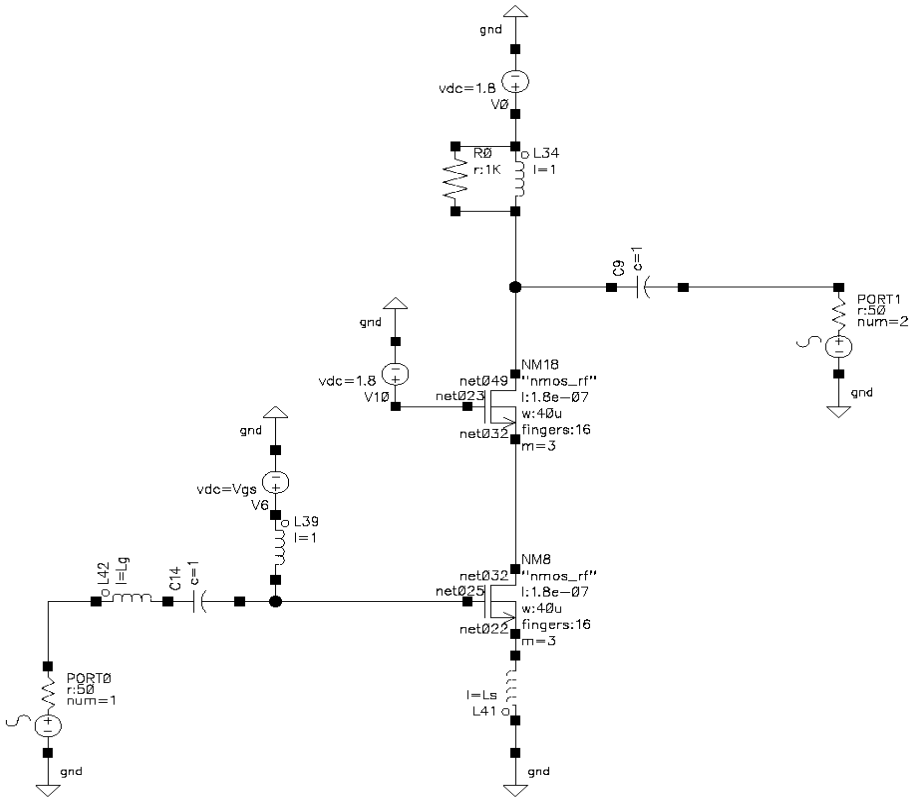


From this figure, you obtain the value of L_s = 0.28 nH

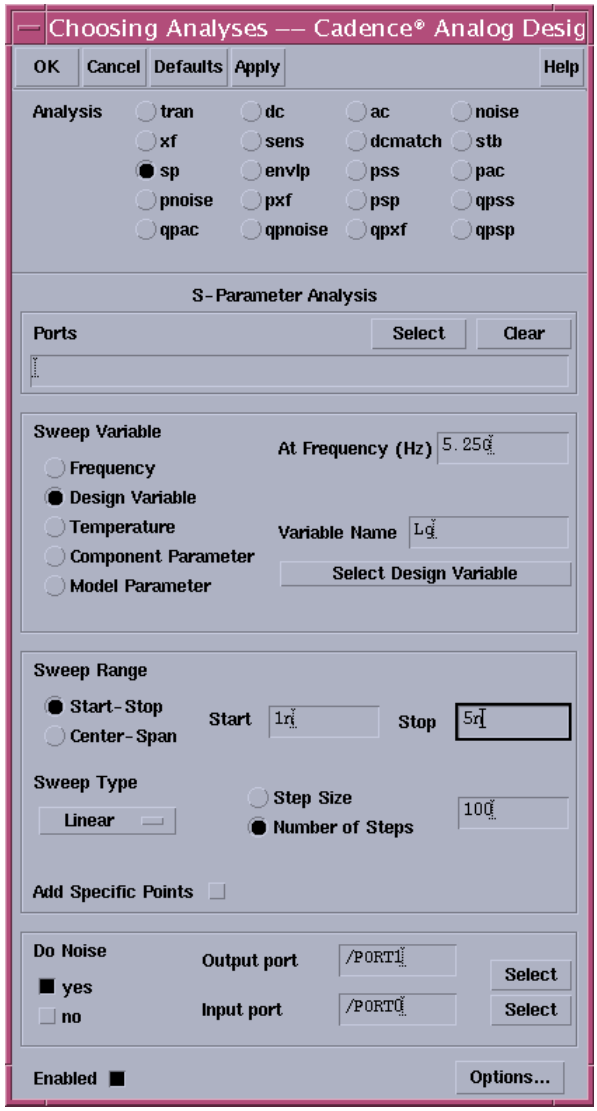
4) Choose the series gate inductance

a) Setup environment

- Insert new inductor which has the inductance value = Lg.

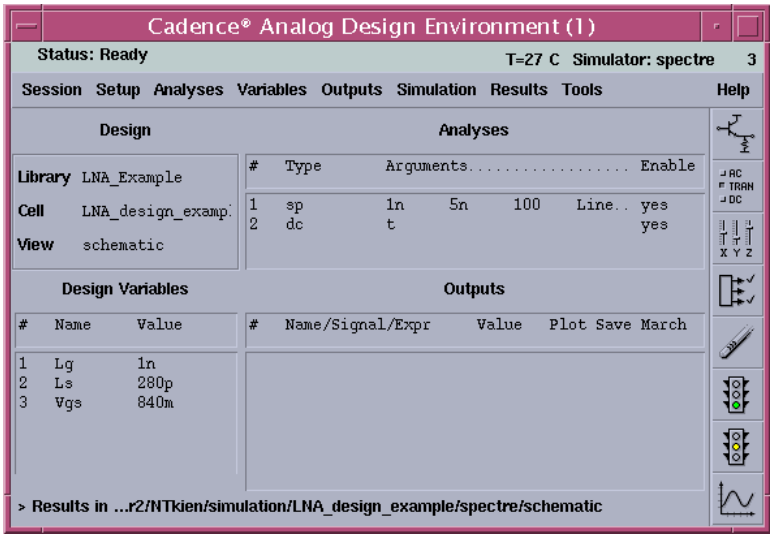


- On the *Analog Circuit Design Environment*, do the following
  - Change the value of L_s = 0.28 nH.
  - Select *Variable – Copy From Cell View*.
  - Set the primary value of Lg (any value)
  - In the Analog Circuit Design Environment, double click on the SP simulation and modify as



- Click *OK*

- Now the Analog Circuit Design Environment becomes as below

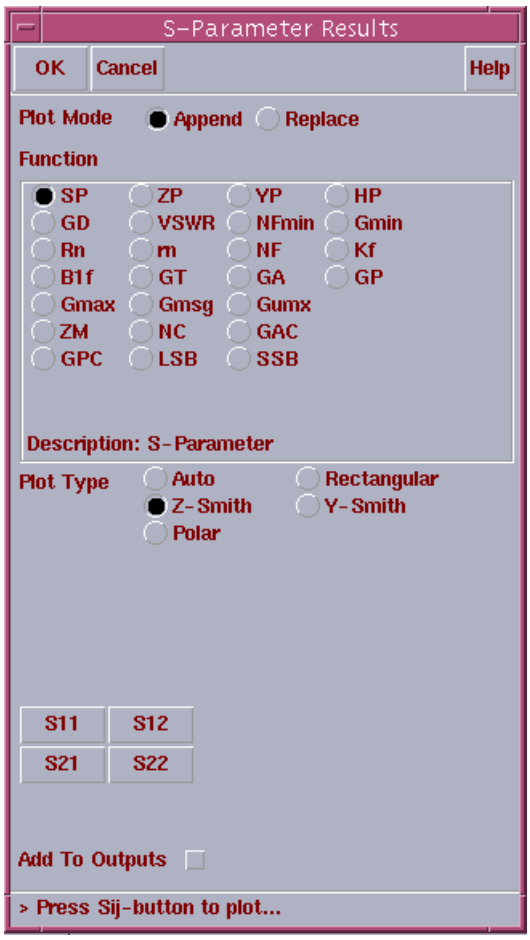


b) Run Simulation

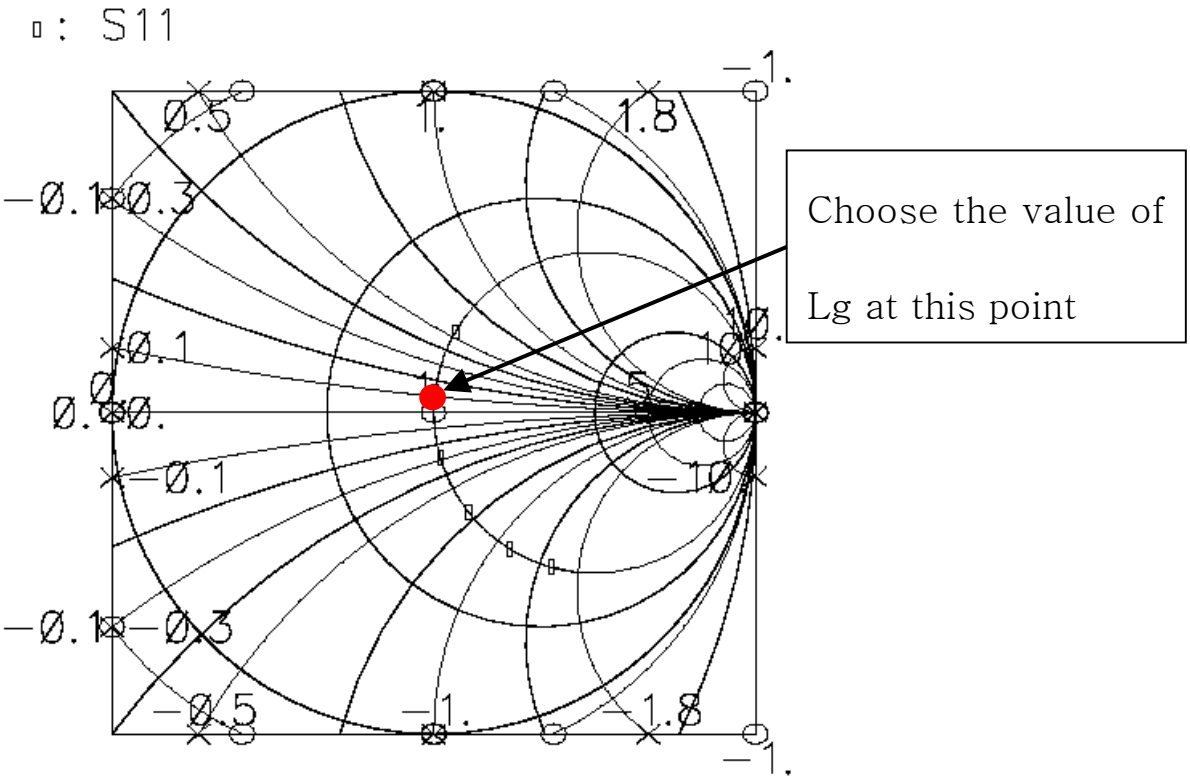
- Click *Nestlist and Run* icon

c) Plotting Results

- After finish simulation, select *Results → Direct Plot → Main Form → S-parameters.*
- On the *S*-Parameter *Results* window do following
  - Highlight *SP* (S parameters) for *Function*
  - Highlight *Z-Smith* for *Plot Type*



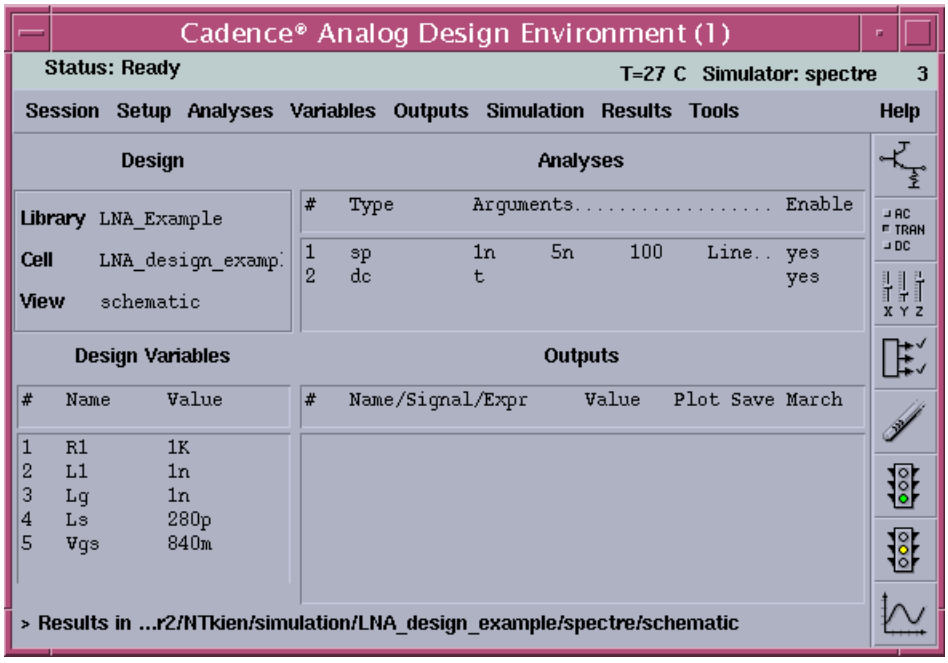
- Click *S11*, you can see the result as below



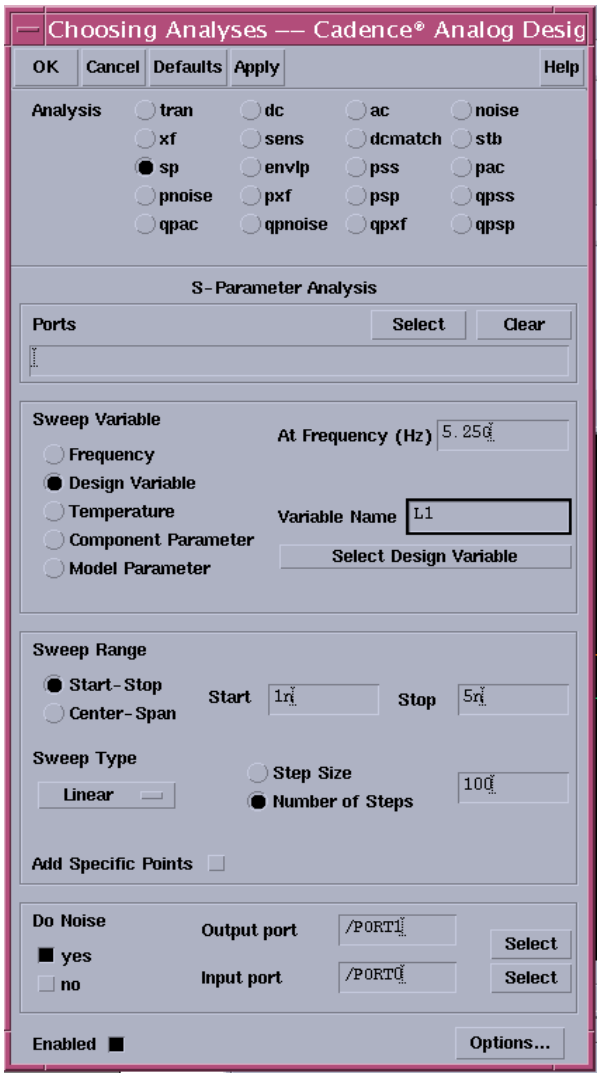
5) Output Matching: Choose load inductance and load resistance

a) Setup environment

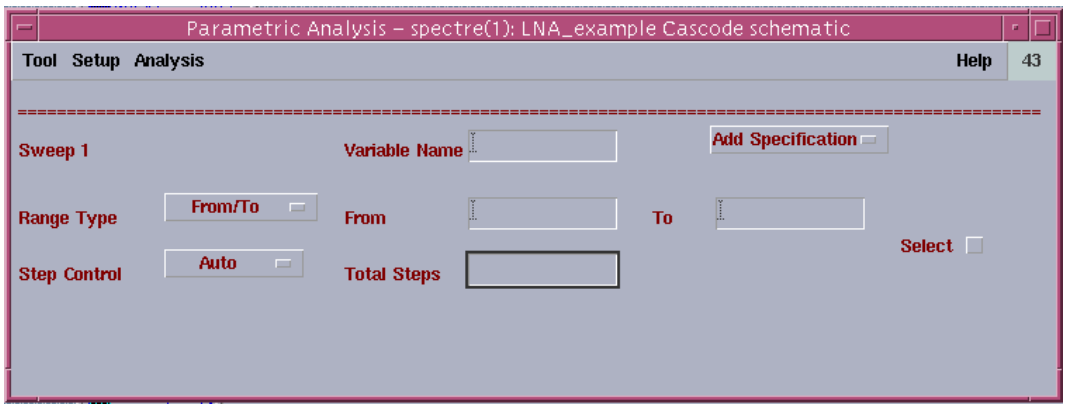
- On the Schematic Window do following steps
  - Change the value of the load resistor to become R1
  - Chang the value of the load inductor to become L1
- On the *Analog Circuit Design Environment* do following
  - Click *Variables → Copy From Cell View*
  - Set the *primary value* of L1 and R1 (any value)
  - The Analog Design Environment look like



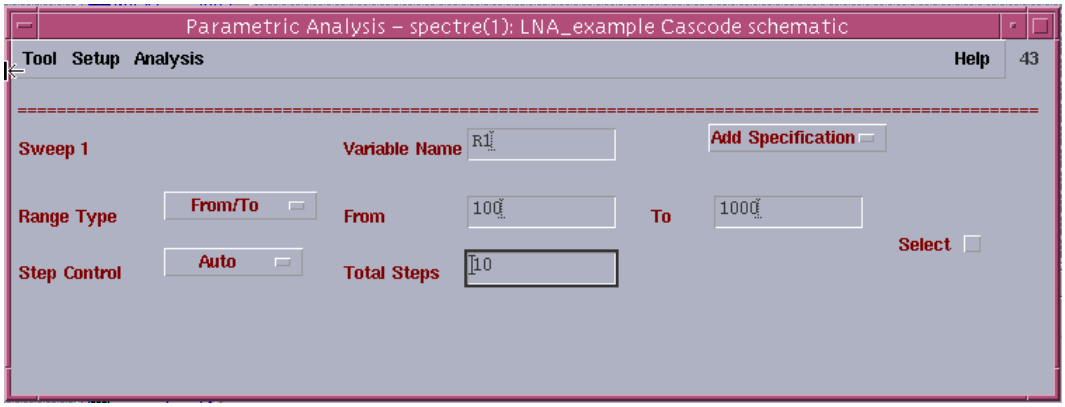
- Double Click on the SP simulator and modify it as



➢ Select *Tools – Parametric Analysis*, the following window appears



➢ Modify the window as below



b) Run Simulation

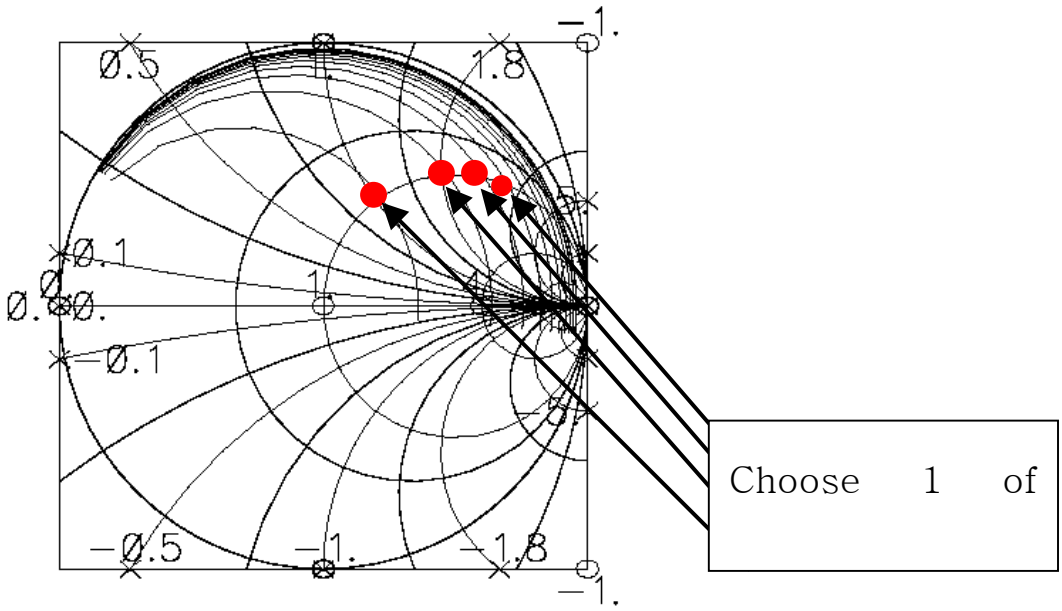
- On the Parametric Analysis window, select *Analysis – Start*

c) Plotting Results

- After simulation is finished, Plotting result

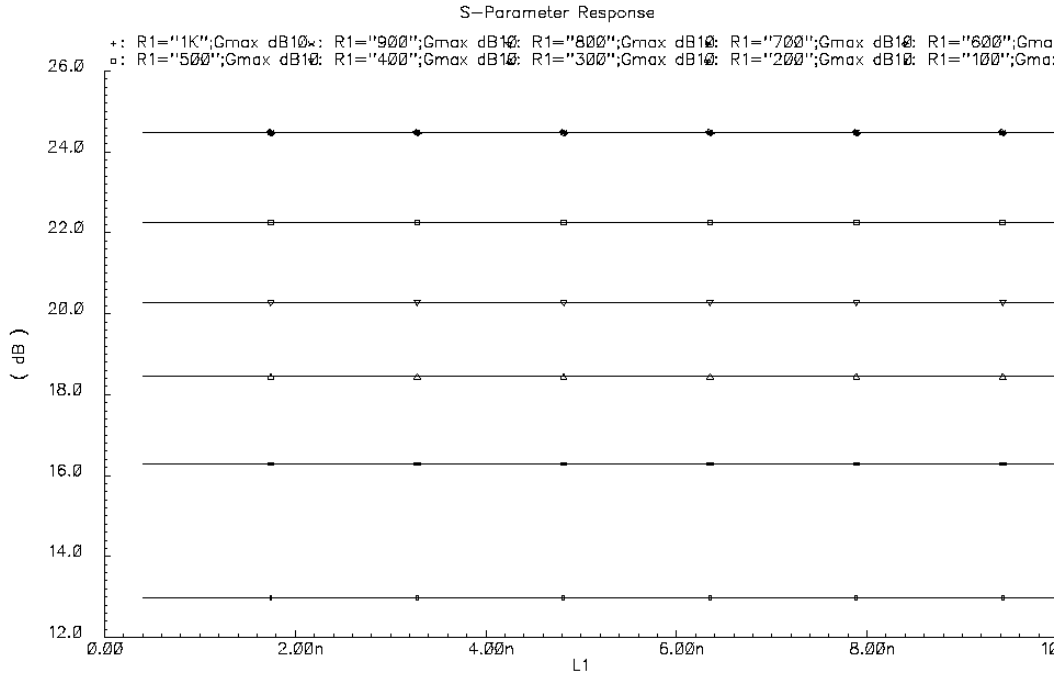
➢ On the Analog Circuit Design Environment, choose: *Results → Direct Plot → Main Form → S-parameters*, the *SP-Parameters* window will appear

- Highlight *SP* for *Function*
- Highlight Z-Smith for Plot Type
- Click *S22* button



You can choose 1 of the ten values that is shown in above figure, however, you should consider about the maximum available gain at each value.

- On the *Analog Circuit Design Environment*, plotting *Gmax* as the function of *R1* and *L1*

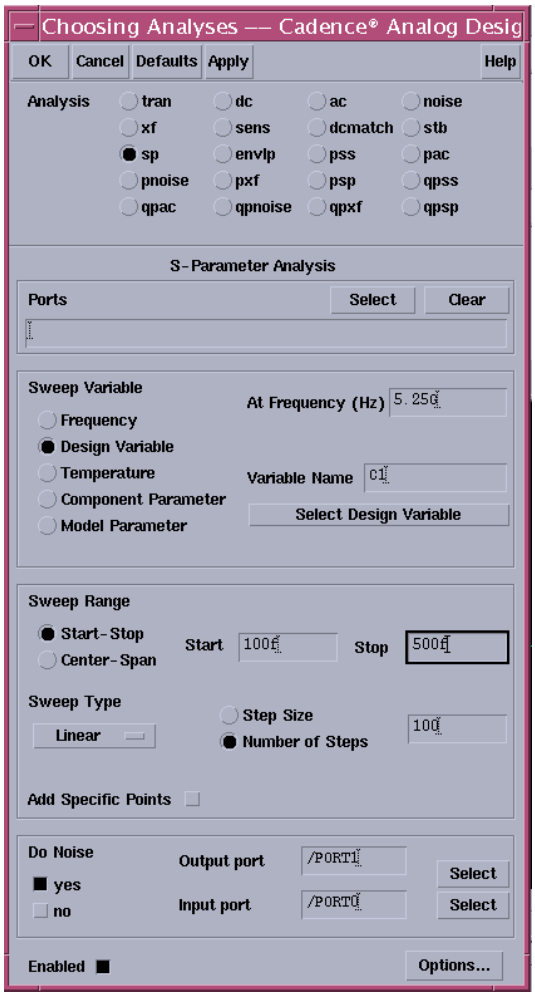


- Based on above figure, assume that you decide to design LNA has gain around 18, so result shows the value of R1 = 300 Ohm.
- See in the Smith chart, when the R1 = 300 Ohm → L1 = 2.8 nH

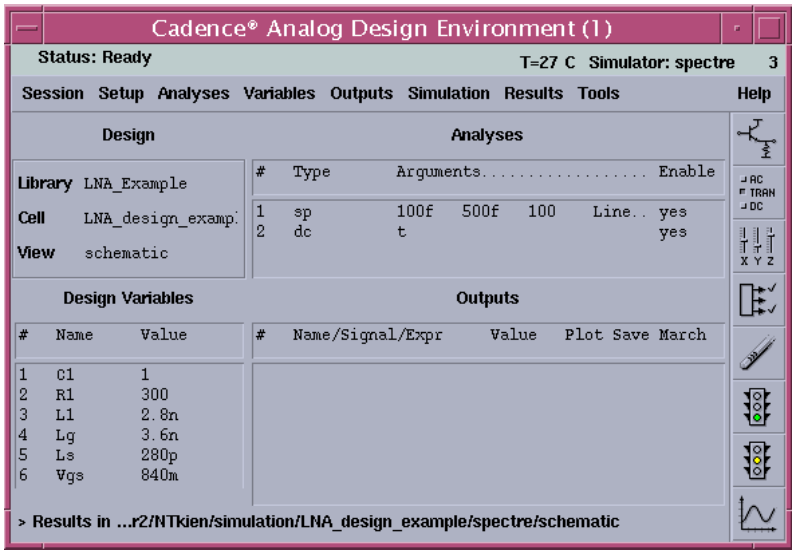
6) Output Matching: choose output capacitance

a) Setup environment

- On the schematic window, *highlight* capacitor named *C1* and setting its *capacitance* value = C1.
- On the Analog Circuit Design Environment, do following
    - Select *Variable – Copy From Cell View*.
    - Set the primary value of C1 (any value)
    - Change the value of L1 = 2.8 nH (this result is obtained in the previous simulation step)
    - On the *Analog Circuit Design Environment* window, double click on the SP simulation and modify as



➢ Now your Analog Circuit Design Environment looks like below



b) Run simulation

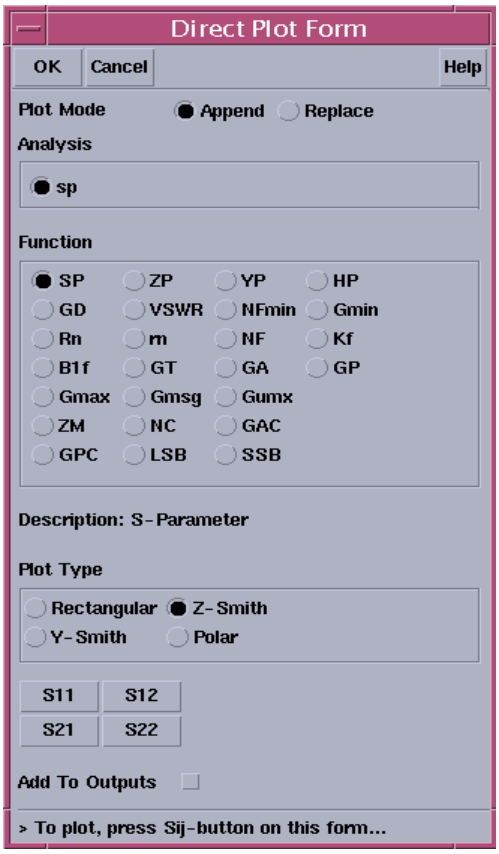
➢ Click *Netlist and Run* icon

c) Plotting result

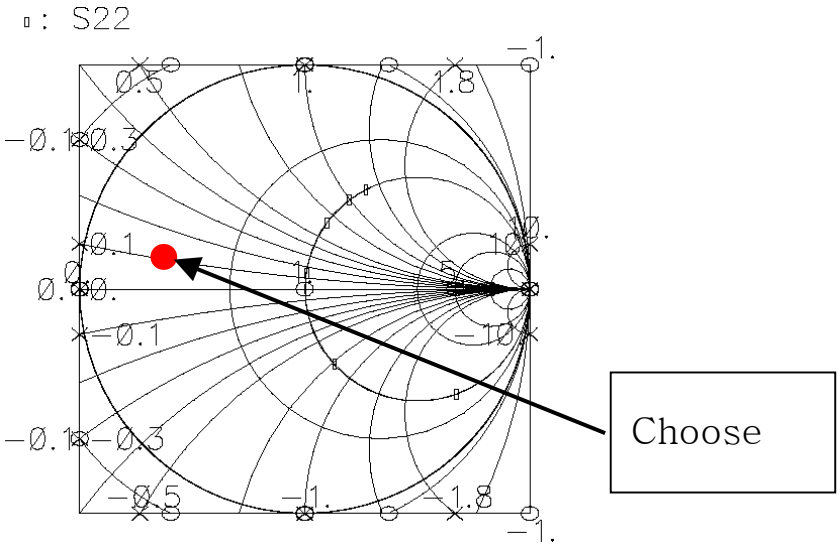
➢ After finish simulation, select *Results* → *Direct Plot* → *Main Form* → S Parameters

➢ On the *S-Parameter Results* window do following

- Highlight *SP* for *Function*
- Highlight *Z-Smith* for *Plot Type*



➢ Click *S22* button, you can see the result as below

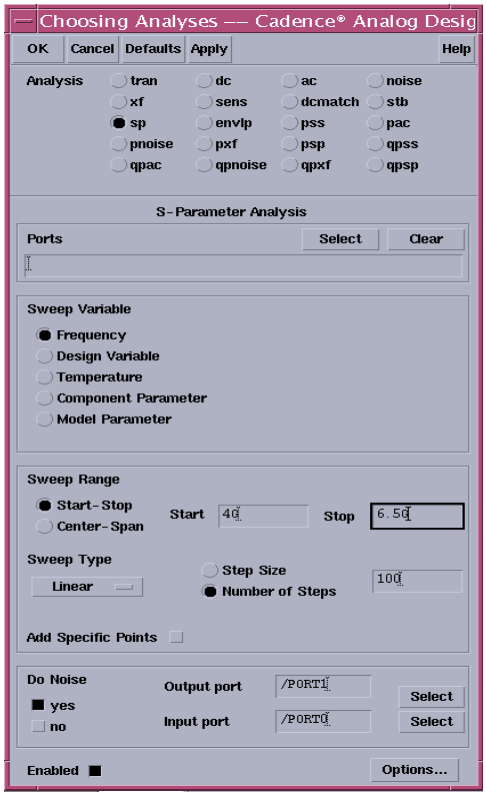


7) Running S-Parameters and NF Simulation

a) Setup Environment

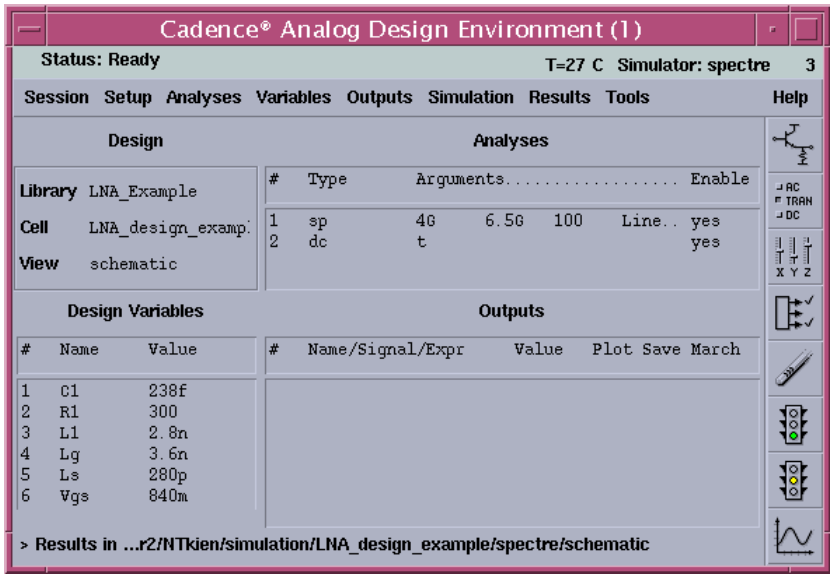
➢ On the Analog Circuit Design Environment window, do following

- Change the value of C1 = 238 fF
- Double click on SP simulator and modify it as



Click *OK*

➢ Now the Analog Circuit Design Environment looks like below



b) Run simulation

Click The *Netlist and Run* icon to run the simulation

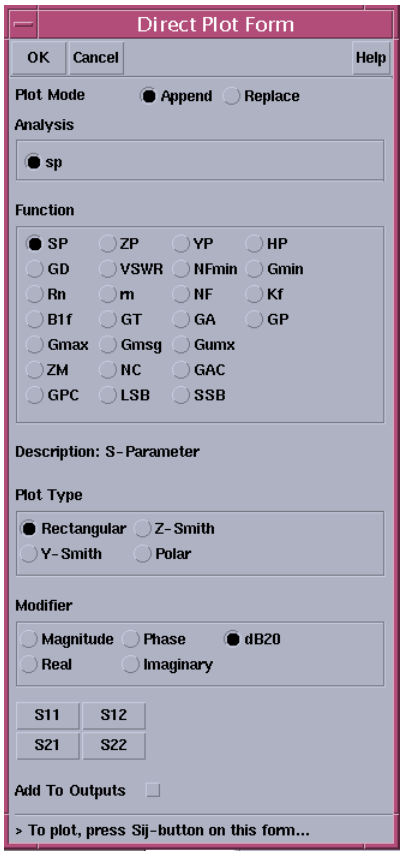
c) Plotting Results

❖ *Plot S parameters:*

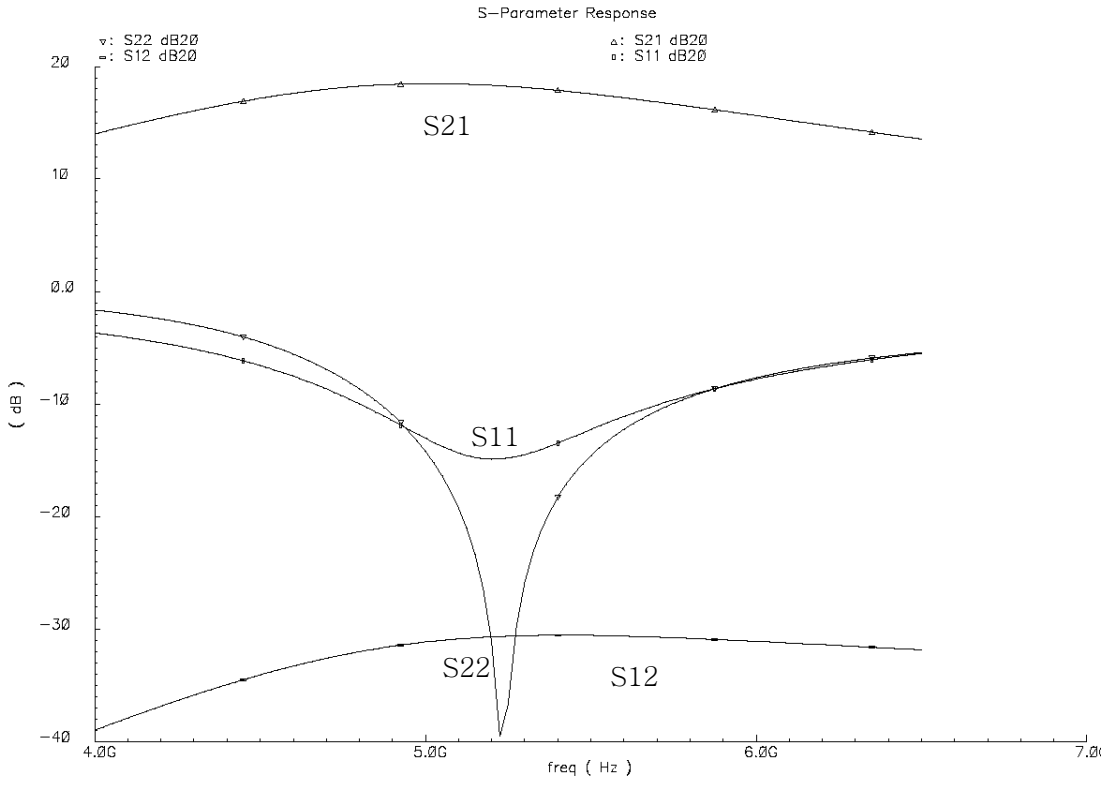
On the Analog Design Environment window

➢ Click *Results →Direct Plot → Main Form → S Parameters*

➢ Modify *Direct Plot Form* window as follows



➢ Click on S11, S22, S21, and S12 separately, the results are shown as follows



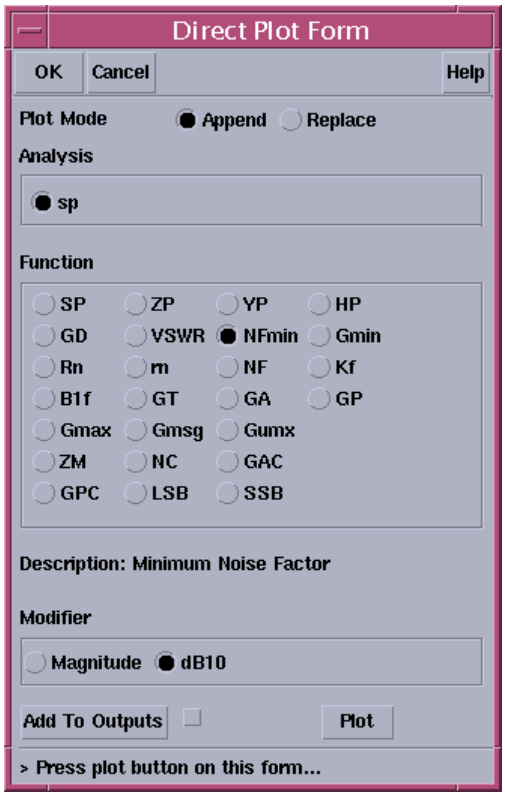
As can be seen in above Fig., the value of S11 is high because the limitation of the isolation between output and input. However, the value of S11 = 15 dB, it can be accepted. If the value of S11 is higher than –15dB, the designer might have to do some simulation steps.

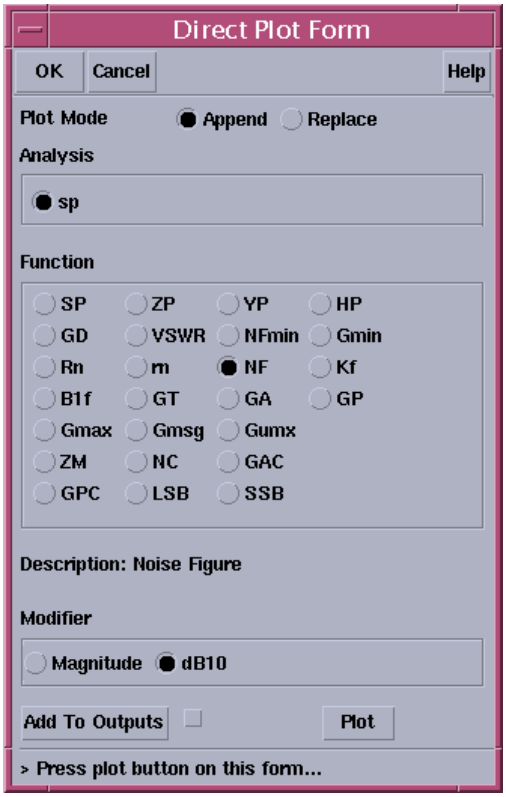
- Keep the output matching as the condition which is found at step (5) & (6)
- Find the value of Ls as the step (3).
- Find the value of Lg as the step (4)

❖ *Plot NF and NFmin of LNA*

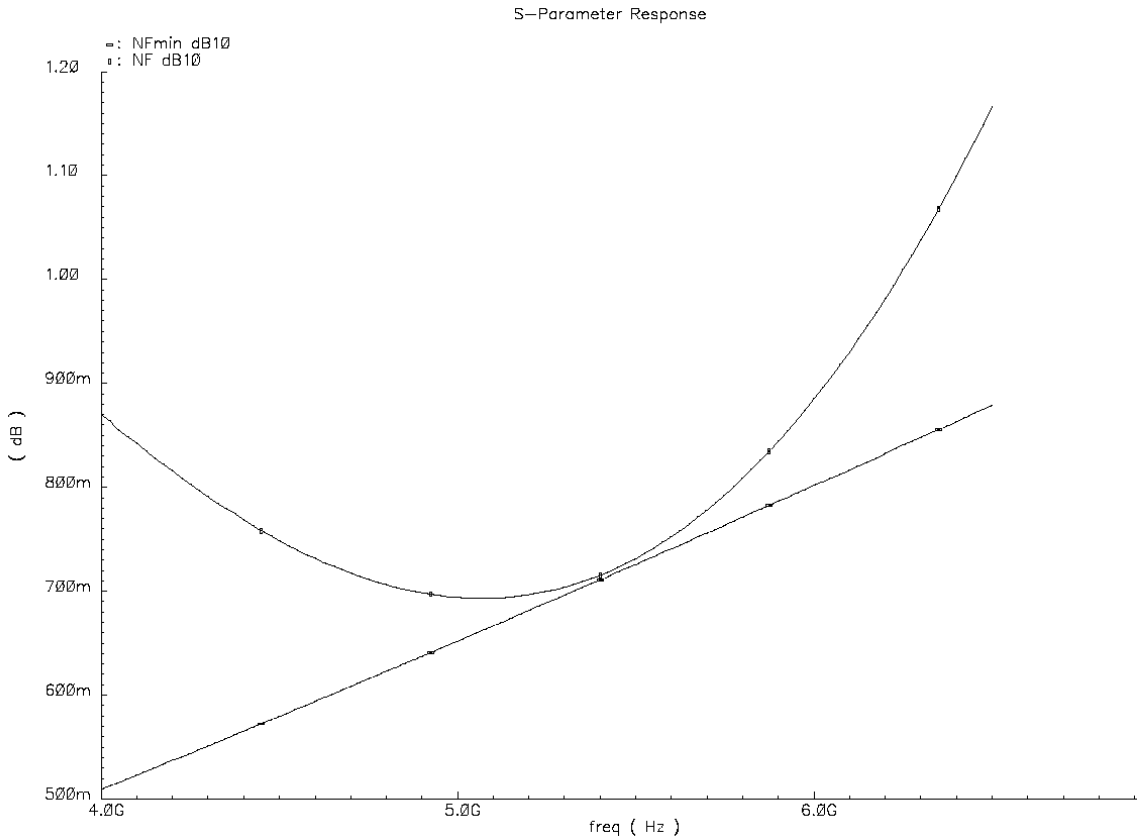
On the Direct Plot Form

- Highline *NFmin* (or *NF*) at the function field
- Highline *dB10* for Modified


Direct Plot Form
OK
Cancel
Help
Plot Mode
Append
Replace
Analysis
sp
Function
SP
ZP
YP
HP
GD
VSWR
NFmin
Gmin
Rn
rn
NF
Kf
B1f
GT
GA
GP
Gmax
Gmsg
Gumx
ZM
NC
GAC
GPC
LSB
SSB
Description: Minimum Noise Factor
Modifier
Magnitude
dB10
Add To Outputs
Plot
> Press plot button on this form...


Direct Plot Form
OK
Cancel
Help
Plot Mode
Append
Replace
Analysis
sp
Function
SP
ZP
YP
HP
GD
VSWR
NFmin
Gmin
Rn
rn
NF
Kf
B1f
GT
GA
GP
Gmax
Gmsg
Gumx
ZM
NC
GAC
GPC
LSB
SSB
Description: Noise Figure
Modifier
Magnitude
dB10
Add To Outputs
Plot
> Press plot button on this form...

The results are shown as follows



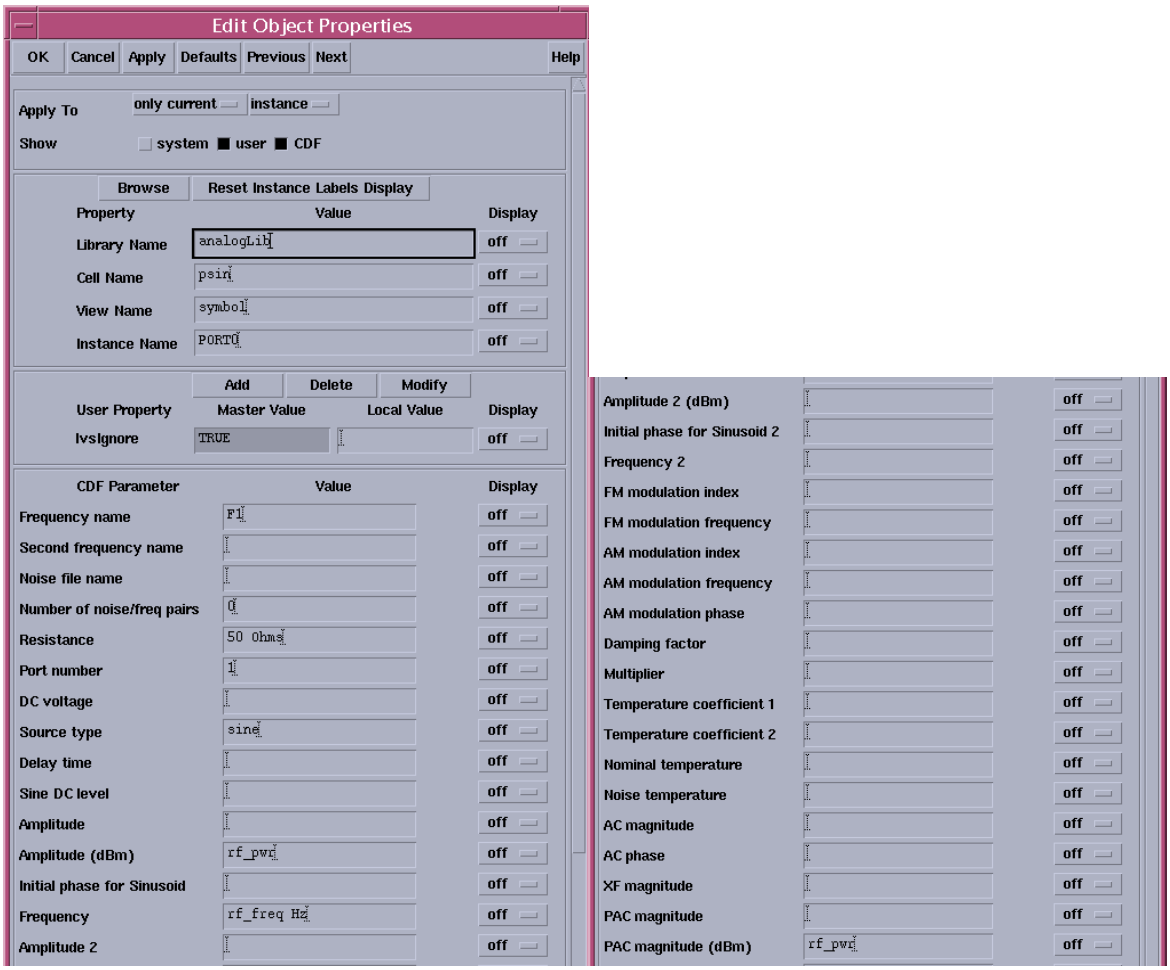
As can be in above Figures, the value of the NF is slightly higher than NF_{min} of the given topology. The reason is the size of the input transistor cannot be chosen properly.

(See the choosing transistor size step, *step (2)*)

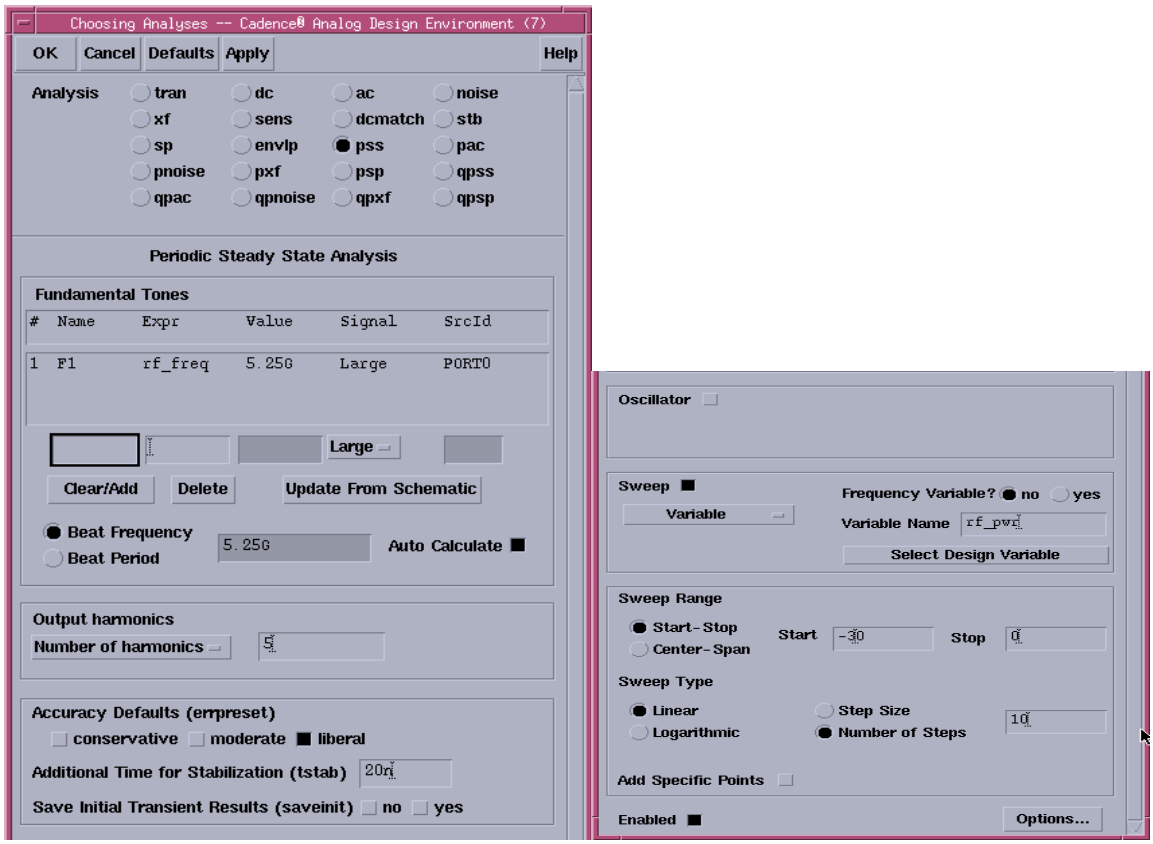
8) Linearity simulation (IIP3 and 1 dB compression Point)

a) Setup environment

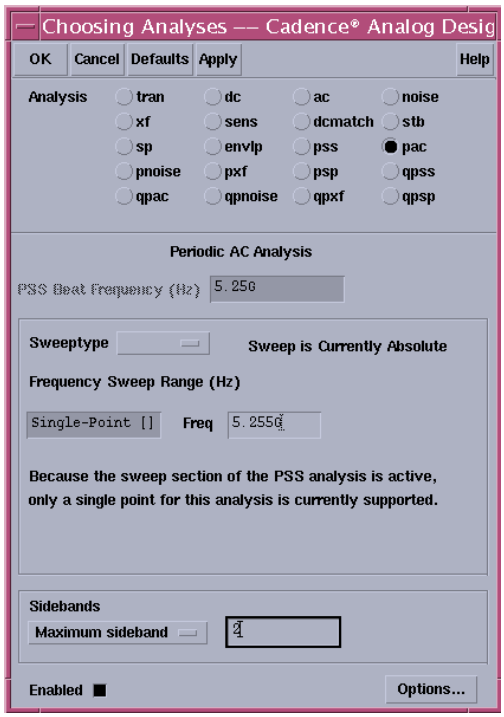
- On the schematic window, highlight *input Port* and *modify* it as



- On the Analog Circuit Design Environment do following
- *Select Variable – Copy From Cell View*
- Setting the primary value of *rf_freq* and *rf_pwr* to be *5.25 G* and *-40*
- Select *Analyses – Choose*
- Highlight *PSS* and *modify* it as below

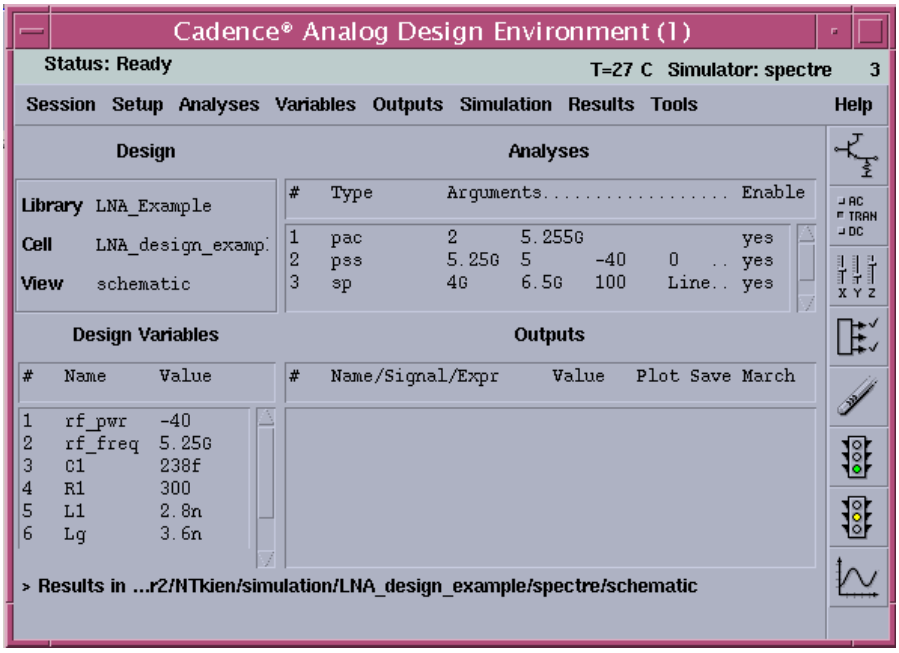


➢ Highlight *PAC* on the *Choosing Analyses* window an modify it as



➢ Click *OK* on the *Choosing* Analyses window.

- Your Analog Circuits Design Environment looks like



b) Run simulation

➢ To run SP analysis, click *Netlist and Run* icon

➢ Look in the output log file to be sure the simulation is completed successfully.

c) Plotting Results

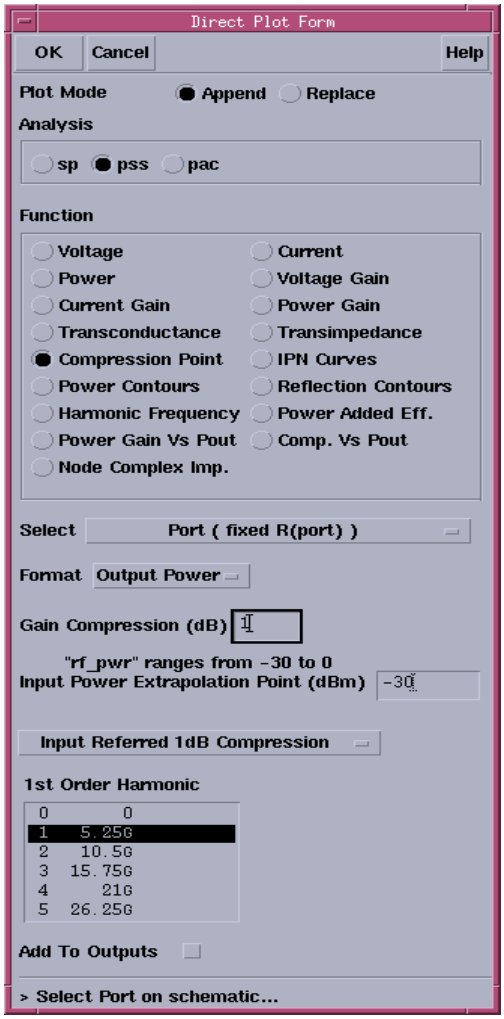
❖ *Plotting 1 dB compression point*

➢ In the simulation window, choose *Results* → *main Plot* → *PSS*. The Waveform window and PSS results form appear.

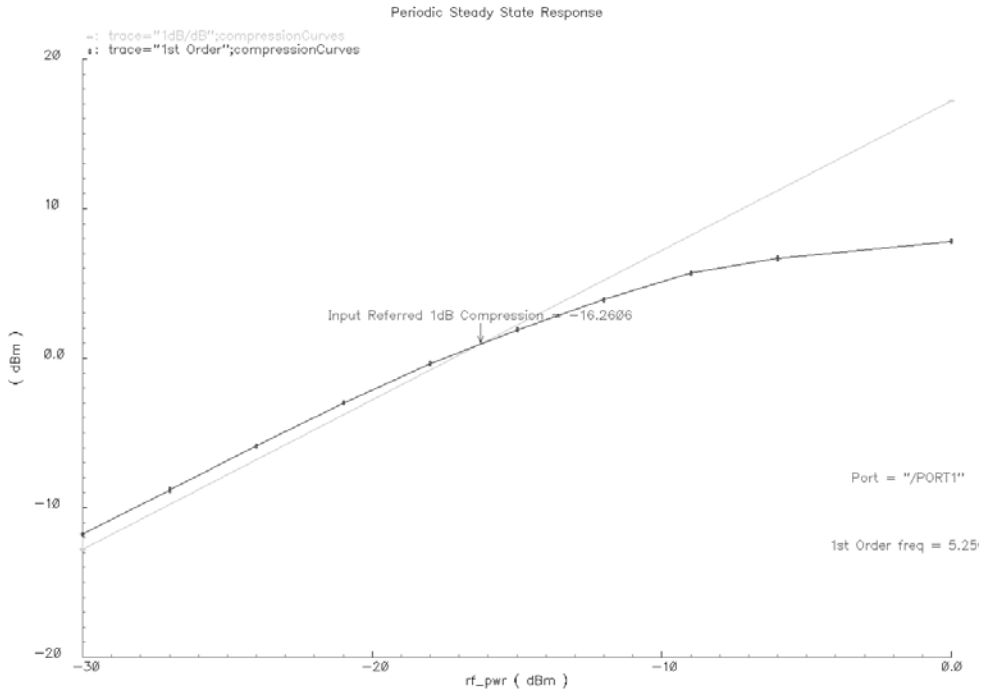
➢ In the PSS results, highlight *PSS* for *Analysis Type*

➢ In the PSS results, highlight *Compression* point for *Function*

➢ Highlight *Variable Sweep* for circuit input power

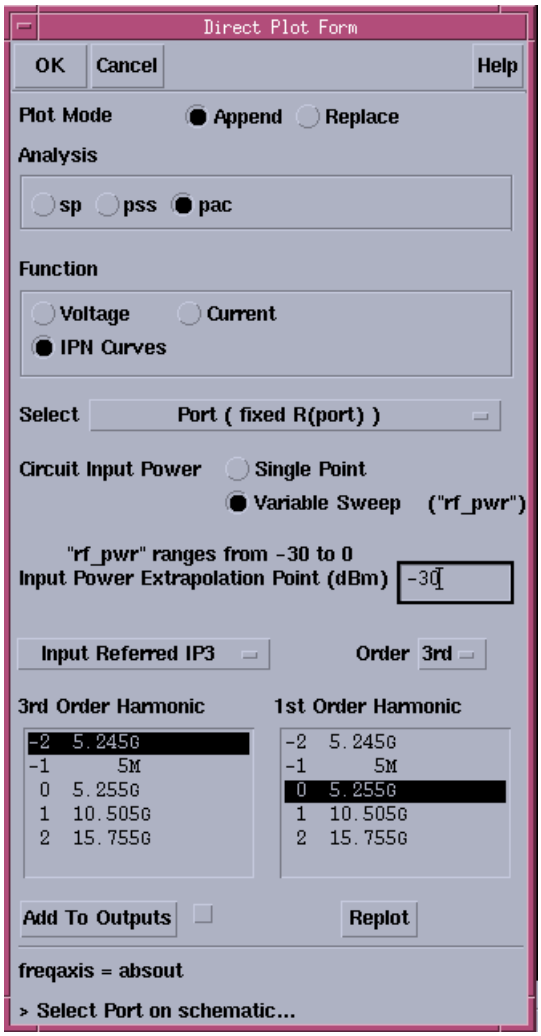


➢ Place cursor in the schematic window and click on the output port.

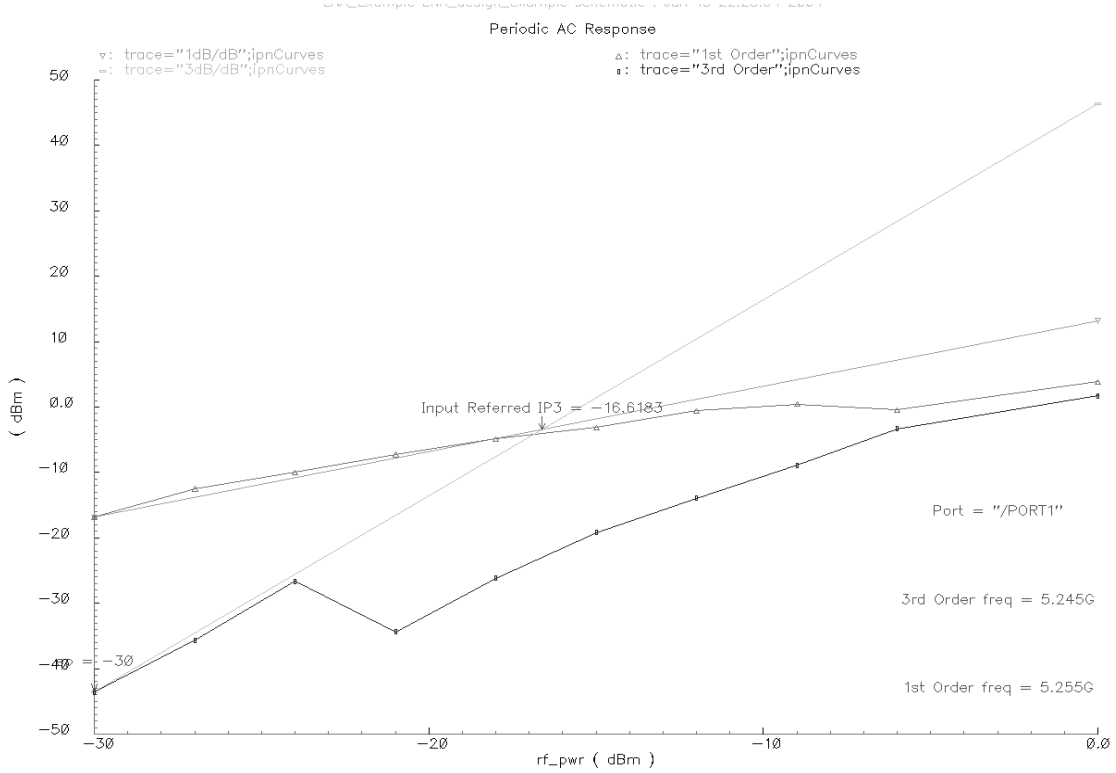


❖ *Plotting IIP3*

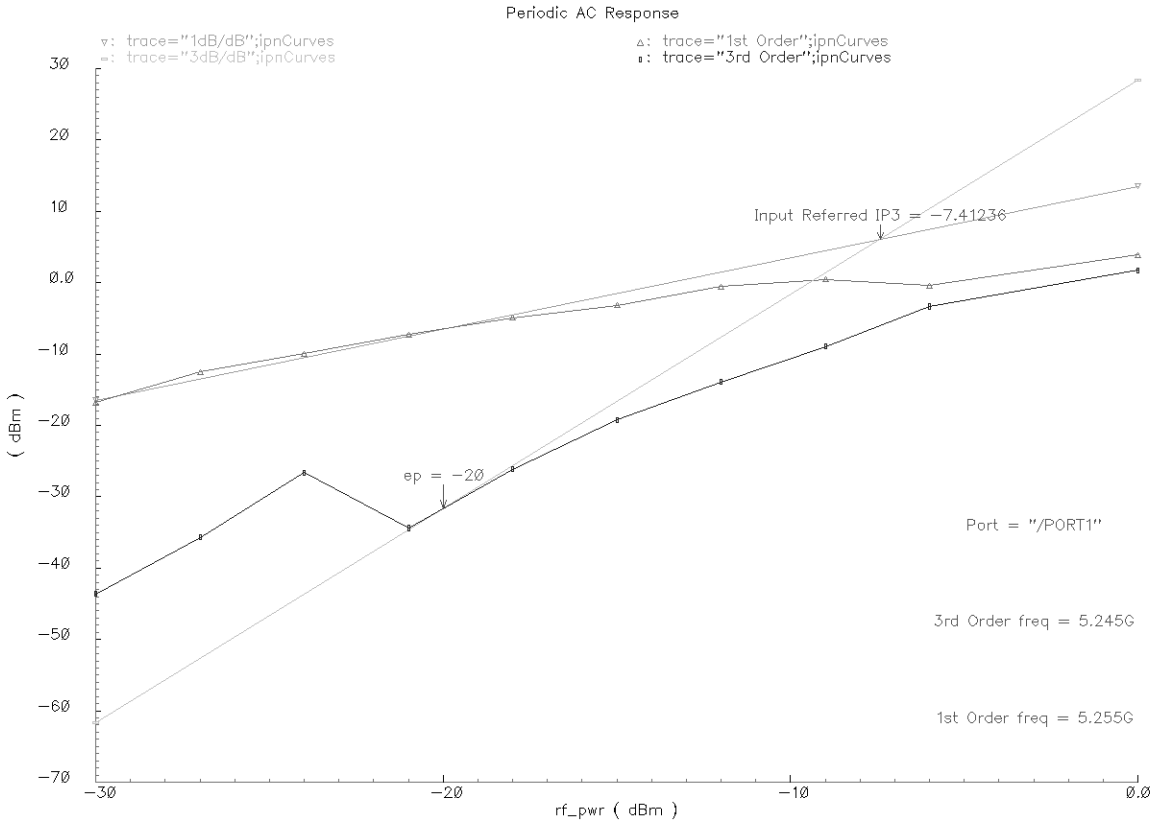
- On the *Analog Circuit Design Environment* window, choose: *Results* → *Direct Plot* → *PSS*. The waveform window and the PSS results appear
- Highlight *PAC* and modify it as



- Place cursor on the output port in the schematic window, you will see the result as



➢ If we choose the Extrapolation value is −20, then we obtain the following Fig.



✓ **SNIM technique is applicable for any Z_s with assuming**

$$R_n = R_n^o = \frac{\gamma}{\alpha}\cdot\frac{1}{g_m} \quad , \quad Z_{opt} = Z_{opt}^o - sL_s$$

$$F_{min} = F_{min}^o = 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\gamma\delta(1-|c|^2)}$$

Stays valid with large W, high P_D and ω

✓ **Problem occurs with small W (low P_D) and low ω**

→ **increase Re[Z_{opt}] → requires high Re[Z_{in}^*] = Re[Z_{opt}]**

→ **requires high L_s → makes the expression for F_{min} invalid**

→ **F_{min} increase significantly above F_{min}^o**

✓ **Even with small W, low P_D, and low ω, possible to achieve $Z_S = Z_{in}^*$ with L_s but NF > F_{min}^o**

✓ **SNIM technique is not applicable for W, ω, and P_D where Re[Z_{opt}] becomes greater than Re[Z_{in}] for the maximum value of L_s ($L_{s,\max}$) where F_{min} of the LNA is not degraded**

✓ **$L_{s,max}$ can be identified by monitoring F_{min} vs. L_s**

✓ **There exists an optimum W that provides minimum NF (> F_{min}^o) → Power-Constrained Noise Optimization Technique**

3.3. Power Constrained Noise Optimization Technique

- ✓ **Under fixed drain current, there exist a transistor size where the NF become minimum [Shaeffer].**

$$W_{opt} \approx \frac{1}{3\omega C_{ox} R_s Q_{in,opt}} \tag{3.21}$$

$$Q_{in,opt} = |c|\sqrt{\frac{5\gamma}{\delta}}\left[1+\sqrt{1+\frac{3}{|c|^2}\left(1+\frac{\delta}{5\gamma}\right)}\right] \tag{3.22}$$

- ✓ **The minimum NF of this case is given by**

$$F_{min\,P} \approx 1 + 2.4\frac{\gamma}{\alpha}\left[\frac{\omega}{\omega_T}\right] \tag{3.23}$$

- ✓ **Compare to Eq. (12), F_{minP} is higher than F_{min}.**

$$F_{min\,P} \approx 1 + 2.4\frac{\gamma}{\alpha}\left[\frac{\omega}{\omega_T}\right]$$

$$F_{min} = F_{min}^{o} = 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\gamma\delta(1-|c|^2)}$$

- ✓ **The reason is mismatch between Z_s and Z_{opt} and/or higher of L_s leads to higher F_{min}**
- ✓ **PCNO technique will eventually converge to the SNIM technique as the power consumption increases (satisfy Eqs. (17), (18), and (20))**

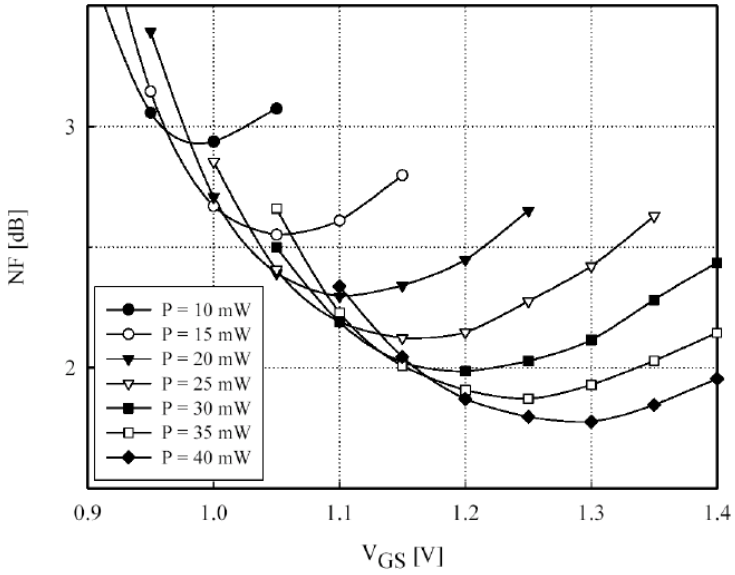


Fig. 3.3. The simulation of *NF* vs V_{GS} at various transistor size at 2 GHz based on 0.8 um CMOS

3.4. Power-Constrained Simultaneous Noise and Input Matching Technique

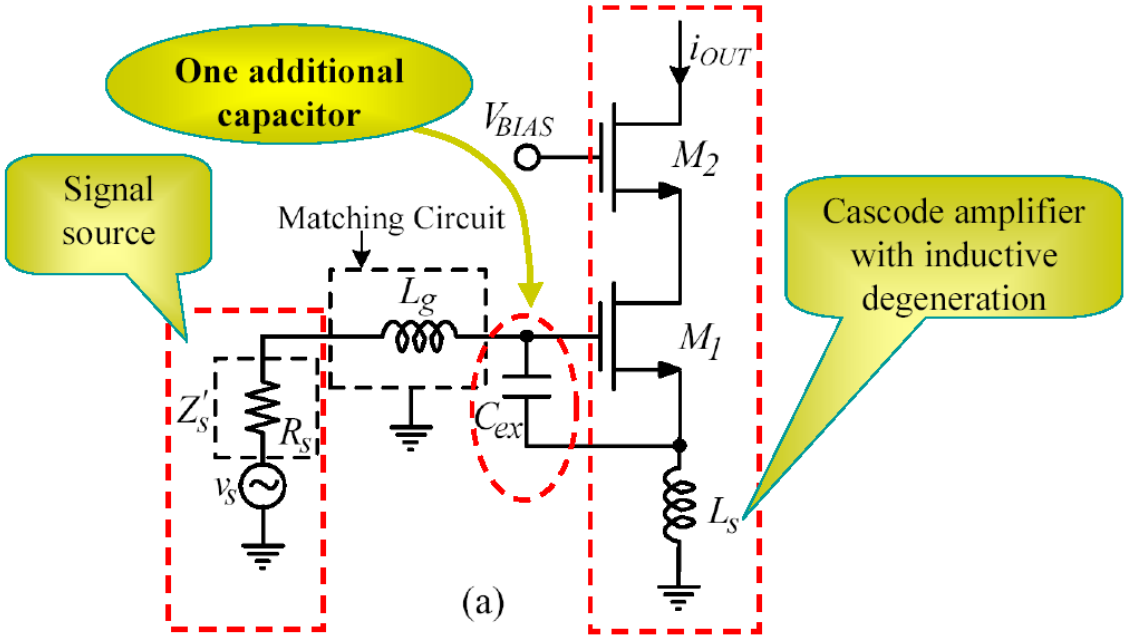
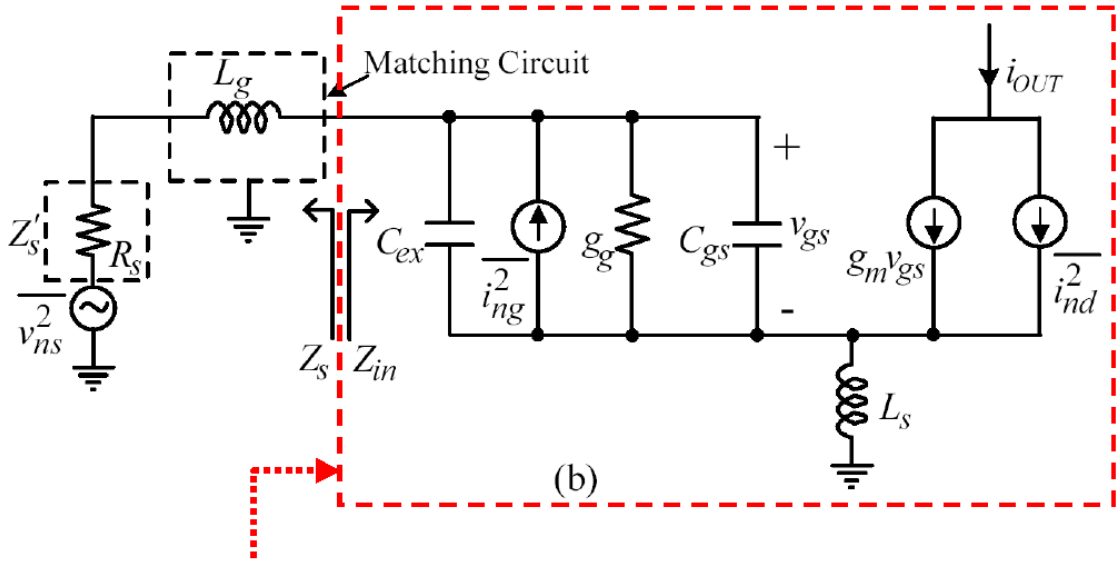


Fig. 3.4. (a) The schematic of cascode topology apply to adopt PCSNIM technique and (b) Small signal equivalent circuit

Assume inductors are lossless, and matching circuit is implemented by a series inductor, but results are valid for arbitrary matching circuits.



Obtain noise parameters by applying KCL/KVL

The noise parameters are given by [Appendix]

$$F = 1 + \frac{1}{g_m^2 R_s} \cdot \left\{ \begin{array}{l} \gamma g_{d0} \cdot \left\{ \begin{array}{l} \left[1 + sC_t(sL_g + sL_s)\left(1 + |c|\alpha\sqrt{\frac{\delta_{eff}}{5\gamma}} \right) \right]^2 \\ -(sC_t R_s)^2 \left(1 + |c|\alpha\sqrt{\frac{\delta_{eff}}{5\gamma}} \right)^2 \end{array} \right. \\ -\frac{\alpha\delta_{eff}}{5}(1-|c|^2) g_m (sC_t)^2 (R_s^2 - sL_g^2) \end{array} \right. \quad \textbf{(3.25)}$$

✓ **The mean-square gate-induce noise now is given by**

$$\overline{i_{ng}^2} = 4kT\delta_{eff}\frac{\omega^2 C_t^2}{5g_{do}}\Delta f \quad \textbf{(3.24)}$$

where

$$\delta_{eff} = \delta.\left(C_{gs}^2 / C_t^2\right)$$

$$C_t = C_{gs} + C_{ex}$$

✓ **Apply the same derivation method as SNIM technique (See Appendix)→ The noise parameters are given by**

✓ **Noise Resistance**

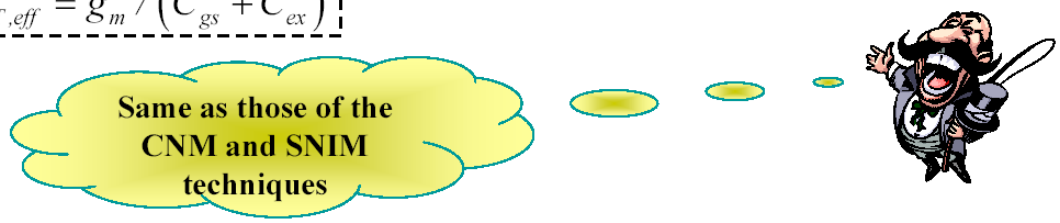
$$R_n = \frac{\gamma}{\alpha} \cdot \frac{1}{g_m} \tag{3.26}$$

✓ **Minimum Noise Figure**

$$F_{min} = 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_{T,eff}} \sqrt{\gamma \delta_{eff} (1 - |c|^2)} \tag{3.27}$$

$$= 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\gamma \delta (1 - |c|^2)}$$

$\omega_{T,eff} = g_m / (C_{gs} + C_{ex})$



✓ **Optimum Noise Impedance**

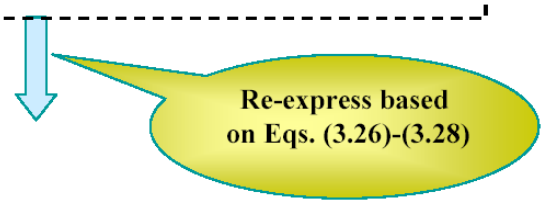
$$Z_{opt} = \frac{\alpha \sqrt{\frac{\delta}{5\gamma(1-|c|^2)}} + j\left(\frac{C_t}{C_{gs}} + \alpha |c| \sqrt{\frac{\delta}{5\gamma}}\right)}{\omega C_{gs} \left\{ \frac{\alpha^2 \delta}{5\gamma(1-|c|^2)} + \left(\frac{C_t}{C_{gs}} + \alpha |c| \sqrt{\frac{\delta}{5\gamma}}\right)^2 \right\}} - sL_s \tag{3.28}$$

✓ **From Fig. 4 (b), the input impedance is given by**

$$Z_{in} = sL_s + \frac{1}{sC_t} + \frac{g_m L_s}{C_t} \tag{3.29}$$

The condition for the simultaneous noise and input matching

$$Z_{opt} = Z_{in}^{*} \begin{cases} \mathrm{Re}[Z_{opt}] = \mathrm{Re}[Z_s] \quad \mathrm{Im}[Z_{in}] = -\mathrm{Im}[Z_s] \\ \mathrm{Im}[Z_{opt}] = \mathrm{Im}[Z_s] \quad \mathrm{Re}[Z_{in}] = \mathrm{Re}[Z_s] \end{cases}$$



$$\frac{\alpha\sqrt{\dfrac{\delta}{5\gamma(1-|c|^2)}}}{\omega C_{gs}\left\{\dfrac{\alpha^2\delta}{5\gamma(1-|c|^2)}+\left(\dfrac{C_t}{C_{gs}}+\alpha|c|\sqrt{\dfrac{\delta}{5\gamma}}\right)^2\right\}} = \mathrm{Re}[Z_s] \tag{3.30}$$

$$\frac{j\left(\dfrac{C_t}{C_{gs}}+\alpha|c|\sqrt{\dfrac{\delta}{5\gamma}}\right)}{\omega C_{gs}\left\{\dfrac{\alpha^2\delta}{5\gamma(1-|c|^2)}+\left(\dfrac{C_t}{C_{gs}}+\alpha|c|\sqrt{\dfrac{\delta}{5\gamma}}\right)^2\right\}} - sL_s = \mathrm{Im}[Z_s] \tag{3.31}$$

$$sL_s + \frac{1}{sC_t} = -\mathrm{Im}[Z_s] \tag{3.32}$$

$$\frac{g_m L_s}{C_t} = \mathrm{Re}[Z_s] \tag{3.33}$$

✓ **Like SNIM technique, Eq. (3.31) ~ Eq. (3.32) → Eq. (3.32) can be dropped (for advanced technologies)**

✓ **The design parameters that can satisfy Eqs. (3.30), (3.31), (3.33) are V_{GS}, W, L_s , and C_{ex}**

→ Eqs. (3.30), (3.31), (3.33) can be solved when power dissipation is fixed since three equations are provided by four unknowns

→ the simultaneous noise and input matching can be achieved at any level of power dissipation

Step-by-Step Design process

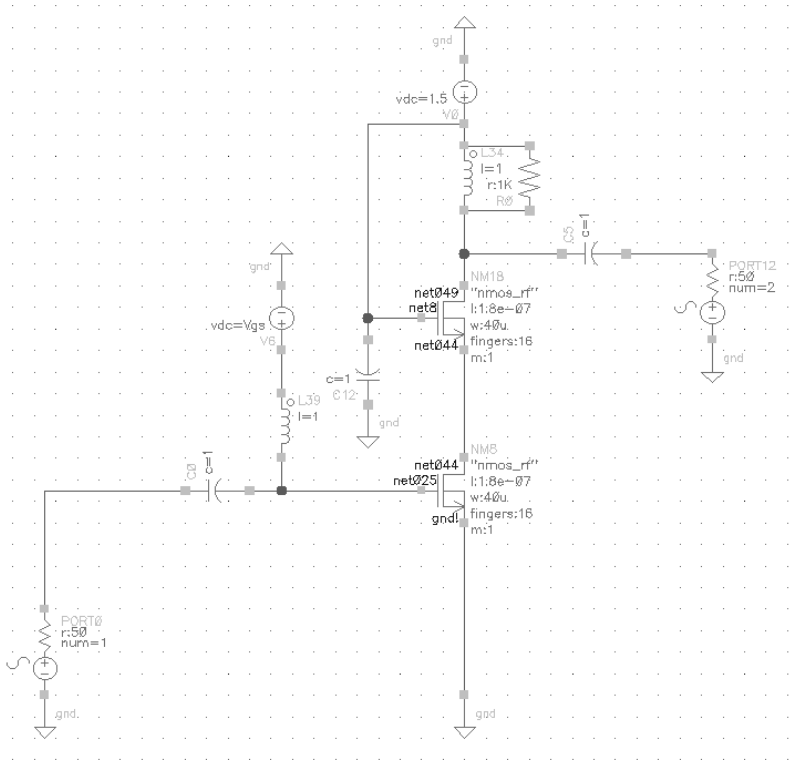
1) **For a given P_D (power dissipation),**
2) **Choose V_{GS} from F_{min} vs. V_{GS} curve for an arbitrary transistor size (choose optimum F_{min})**
3) **Choose C_{gs}(or W) to satisfy P_D → determines Re[Z_{opt}]**
4) **Choose C_{ex} and L_s to satisfy Re[Z_{in}] = Re[Z_{opt}]**
5) **Given L_s satisfies Im[Z_{in}^*] ≈ Im[Z_{opt}] automatically**
6) **→ $Z_{opt} = Z_{in}^*$**
7) **Insert matching circuit to make $Z_{opt} = Z_{in}^* = Z_s$**
8) **Noise/input matched simultaneously at given P_D**

1) Power Constrained

➢ Assume that we design LNA consuming 1 mW under supply voltage of 1.8 V.

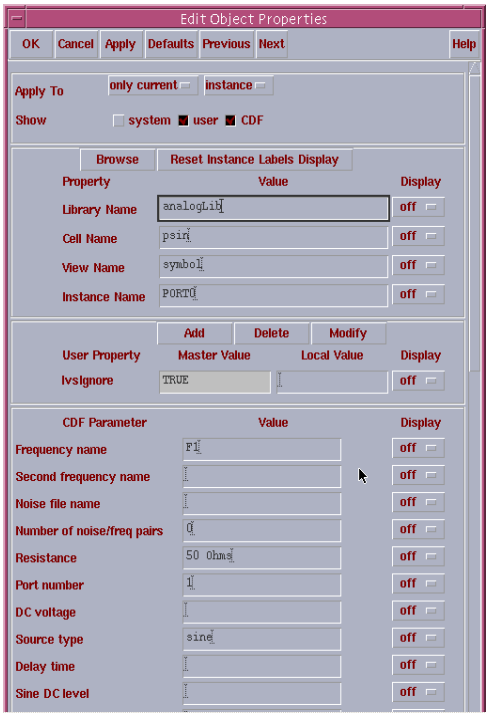
1.1) Setup Environment

Draw Circuit as below

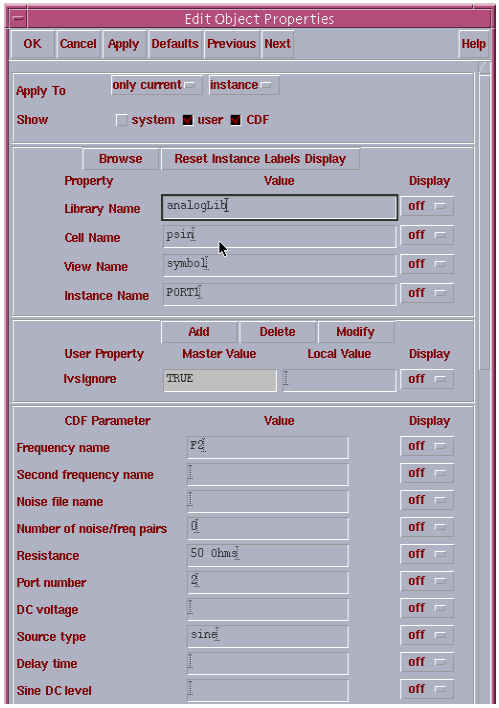


➢ Modify *Input Port* and *Output Port* as follows

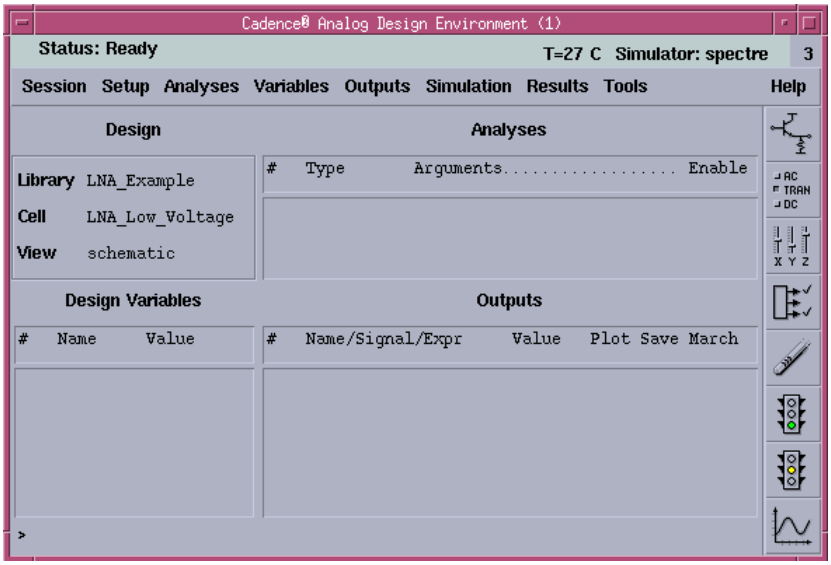
Input Port



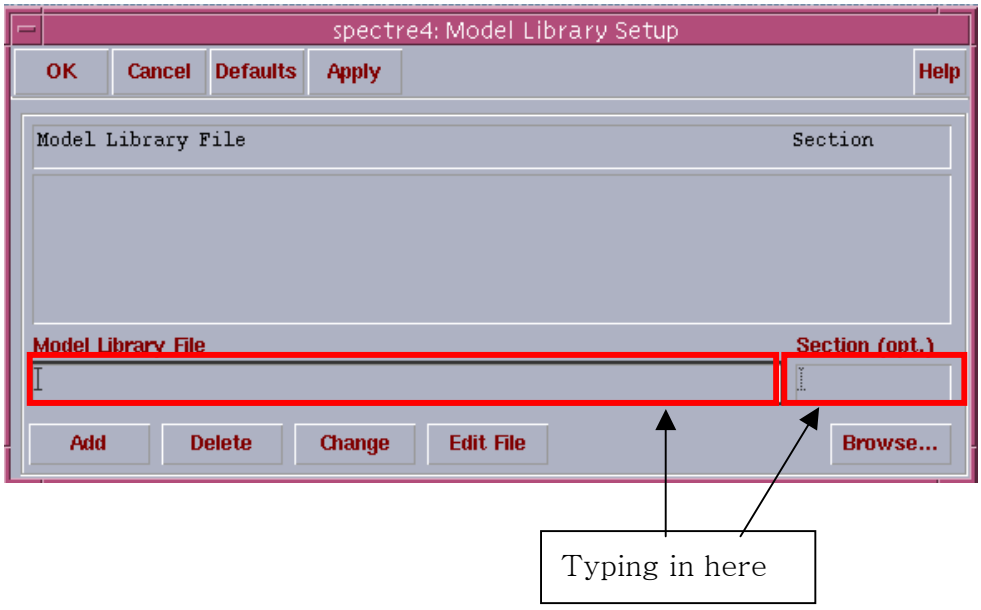
Output Port



➢ From the schematic window select: *Tool- Analog Environment*



➢ On the Analog Circuit Design Environment, Click *Setup-Model libraries*



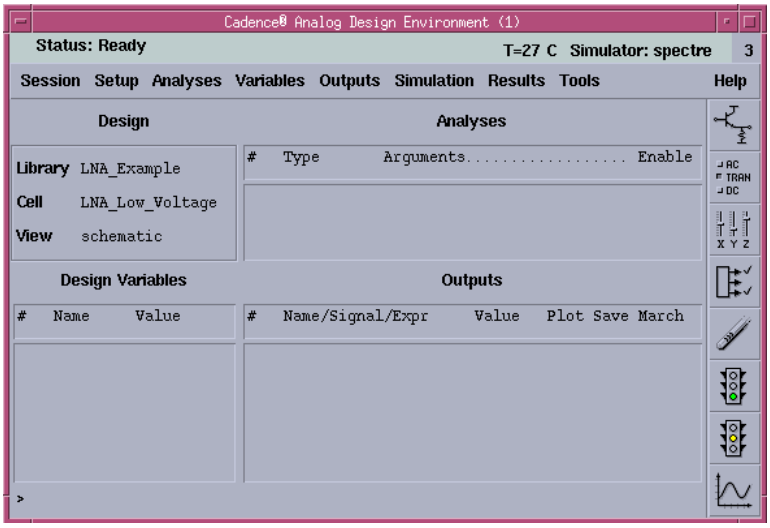
➢ In the *Model Library File* and *Section* fields typing as follows

Model Library File	Section (opt.)
/data1/RACS/DC_project/Tsmc18/models/mm018.scs	tt
/data1/RACS/DC_project/Tsmc18/models/mm018.scs	tt_3v
/data1/RACS/DC_project/Tsmc18/models/mm018.scs	tt_na
/data1/RACS/DC_project/Tsmc18/models/mm018.scs	tt_3vna
/data1/RACS/DC_project/Tsmc18/models/mm018.scs	tt_m
/data1/RACS/DC_project/Tsmc18/models/mm018.scs	tt_3m
/data1/RACS/DC_project/Tsmc18/models/mm018.scs	ees
/data1/RACS/DC_project/Tsmc18/models/mm018.scs	tt_bip
/data1/RACS/DC_project/Tsmc18/models/mm018.scs	tt_bip3
/data1/RACS/DC_project/Tsmc18/models/mm018.scs	dio
/data1/RACS/DC_project/Tsmc18/models/rf018.scs	tt_rfmos
/data1/RACS/DC_project/Tsmc18/models/ResModel.scs	res_t

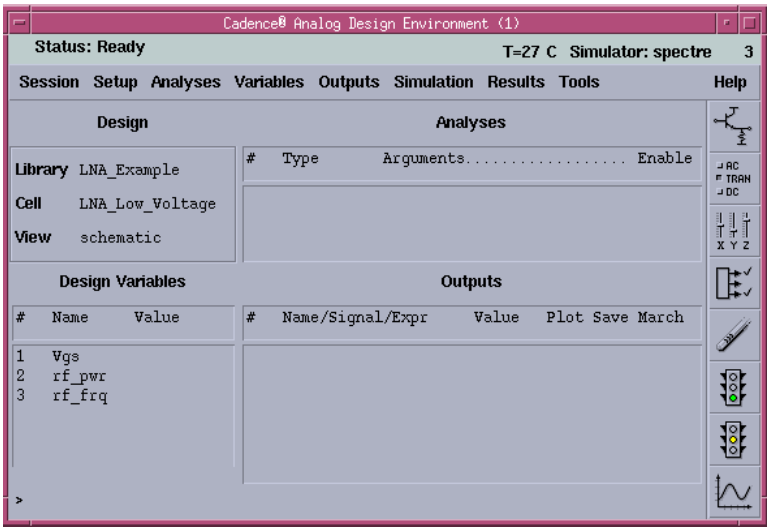
➢ You can Click *Browse* and go up to the directory, which contain the model library of the technology you would like to use. Or instructors will introduce the path of model library

- Notice: After you finish typing one section, press *Add* icon. If you make some mistakes, you can delete by click *Delete* icon
- On the Analog Environment Window, Click *Variable-Copy from cell view*.

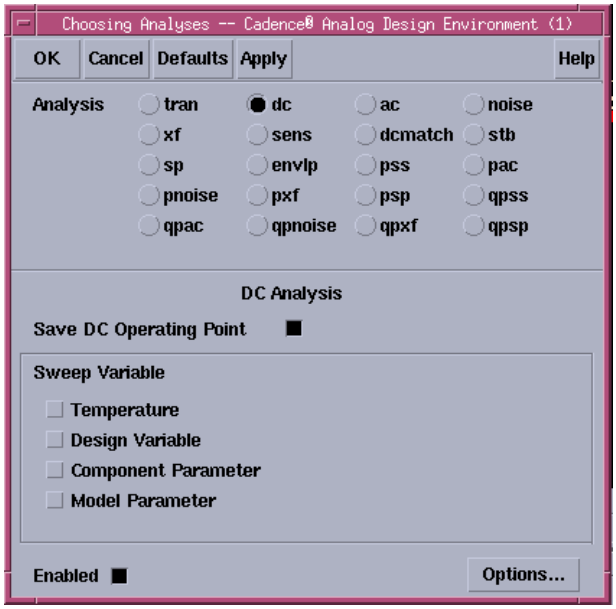
➢ Analog Environment window looks like



➢ Choose *Variable → Copy From Cell View*, Analog Environment window becomes



➢ On the Analog Environment Window, Click *Analysis-Choose,* following windown will appear



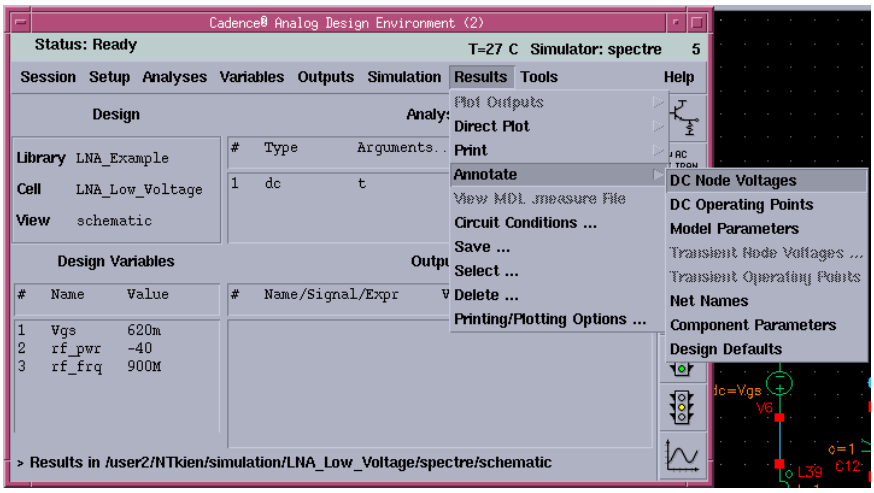
- Choose DC analysis
- Click on Save DC Operating Point
- Make sure that *Enable icon* is on

1.2. Run Simulation

- Click *Netlist and Run* icon

1.3. Plot Results

From Analog Design Enviroment Windown, Click, *Results→ Annotate→ DC Node Voltage /DC Operating Points*

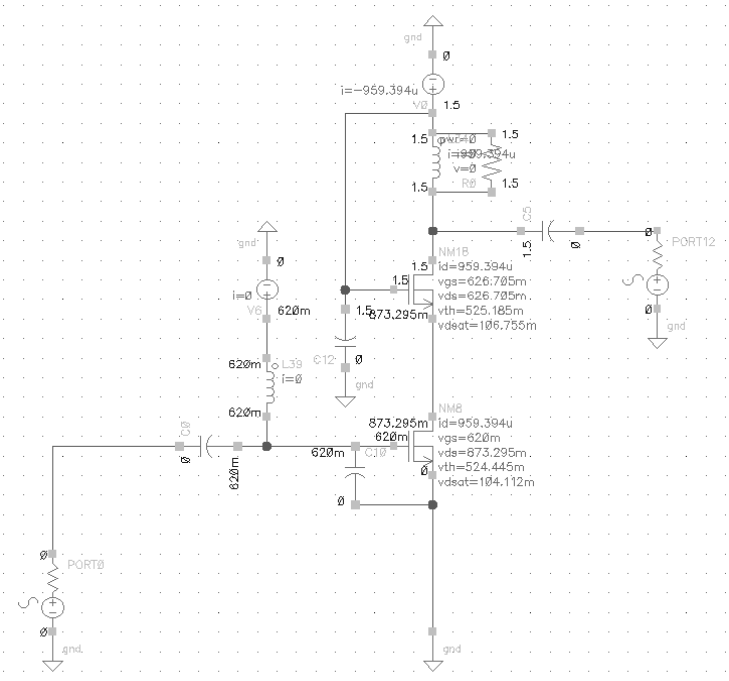


We can see the DC current dissipation of the circuit

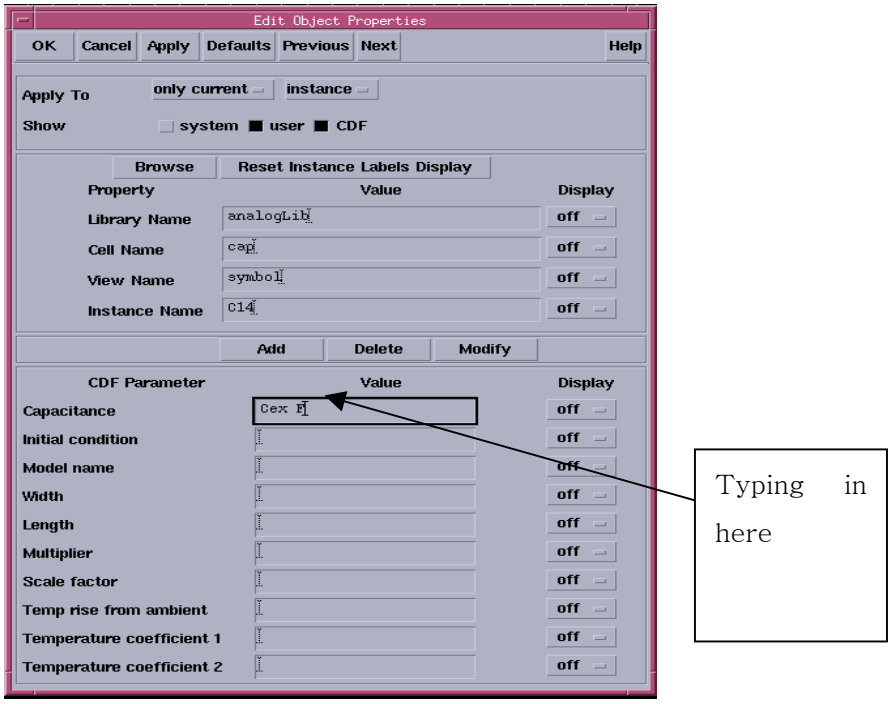
2) Choose the extral capacitor

a) Setup Inviroment

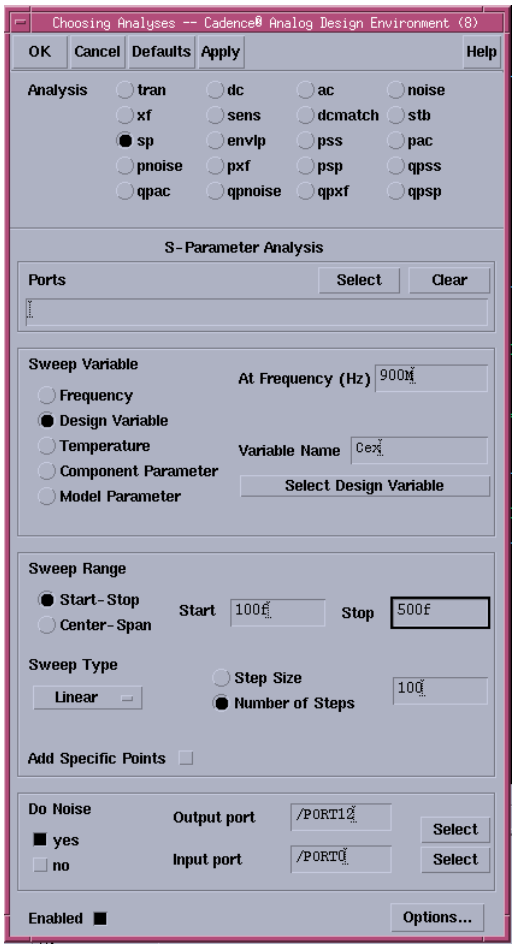
- From the previous step, we choose the value of V_{GS} is equal to 620 mV
- Insert one additional capacitor in parallel with Gate-Source capacitor of input transistor. The LNA schematic now becomes as folows



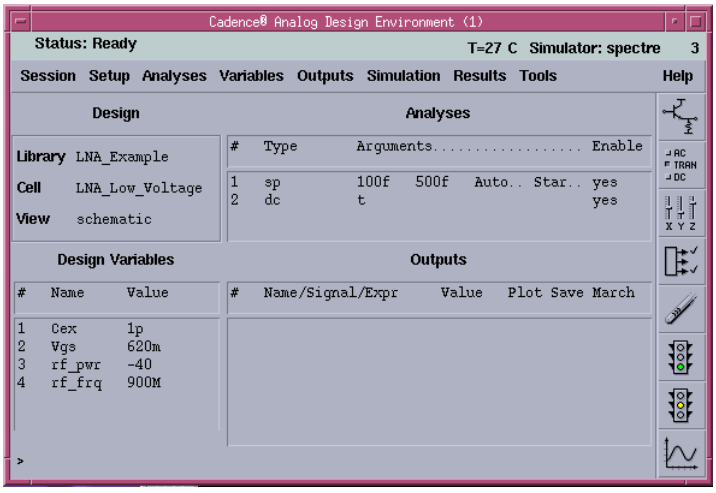
➢ Highline this additional capacitor and modify it as follows

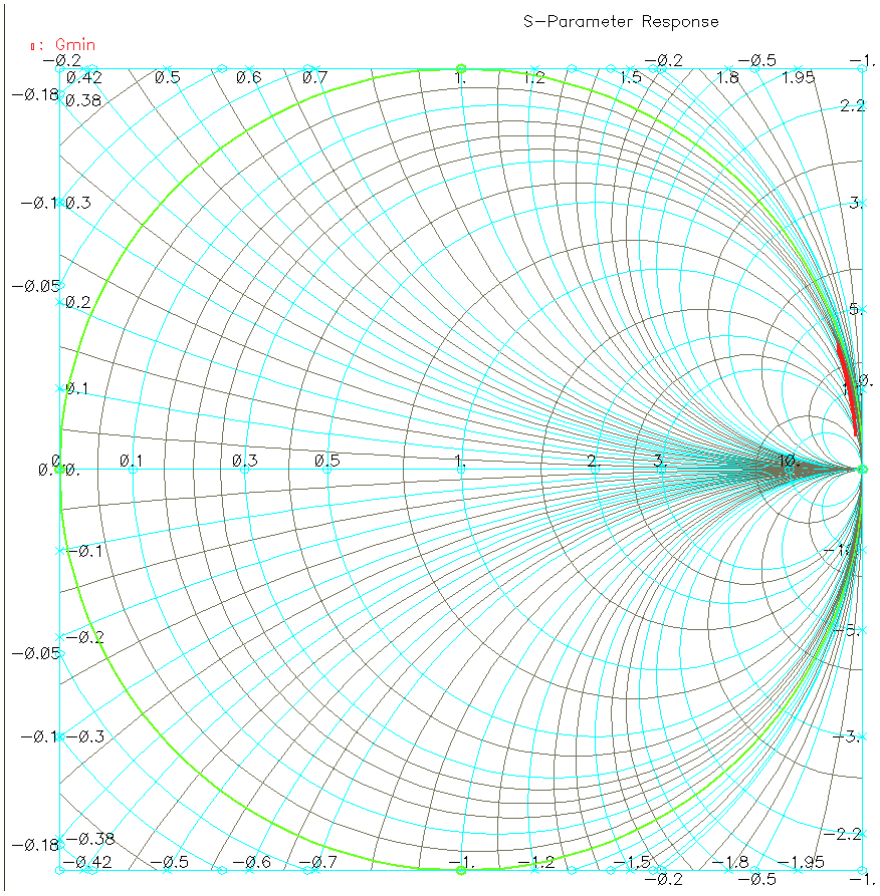


➢ From Analog Design Invirоment, click Analysis → Choose, the Choosing Analyses windown will appear, then modify it as follows



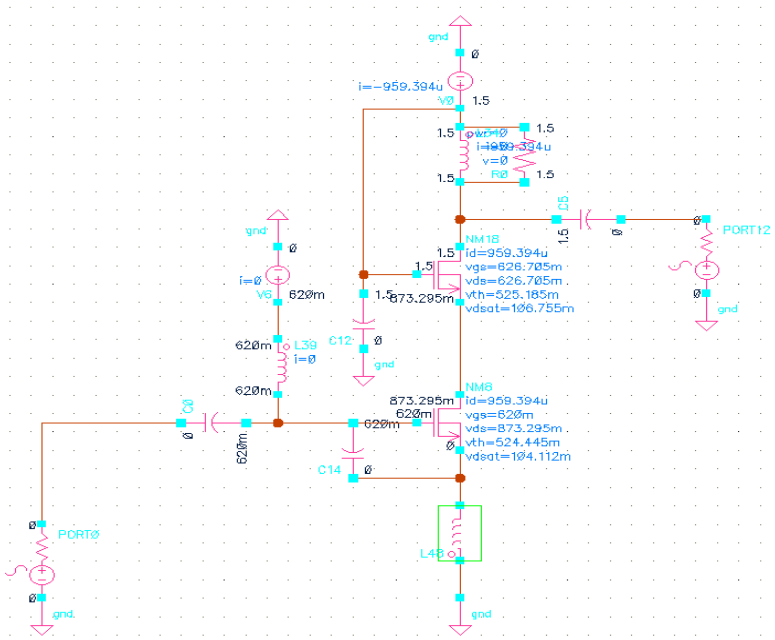
➢ Click *Apply* and *OK*, then the Analog Design Enviroment windown becomes as follows

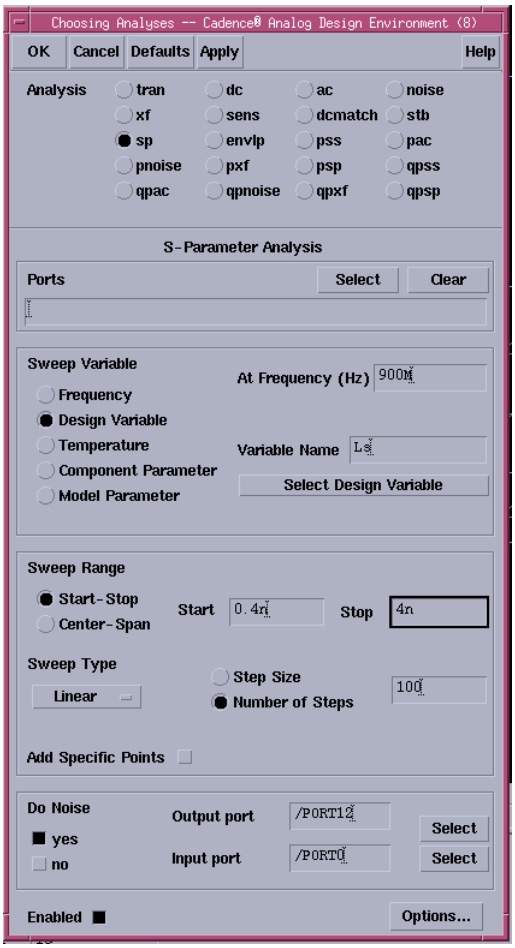


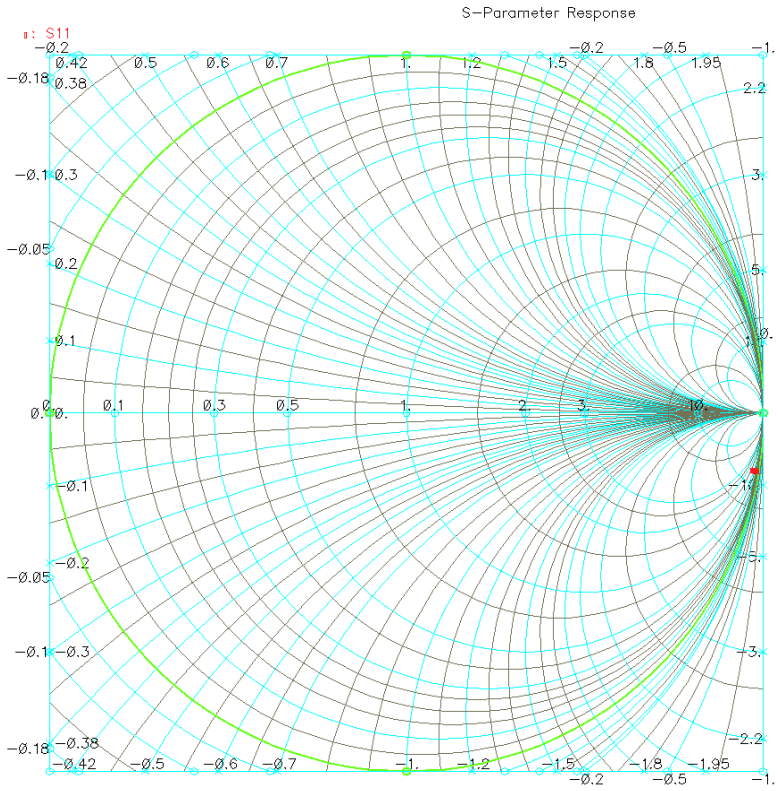


➢ From above Fig., we can choose the value of C_{ex} = 210f in order to obtain the Real value of Γopt equal to 1.

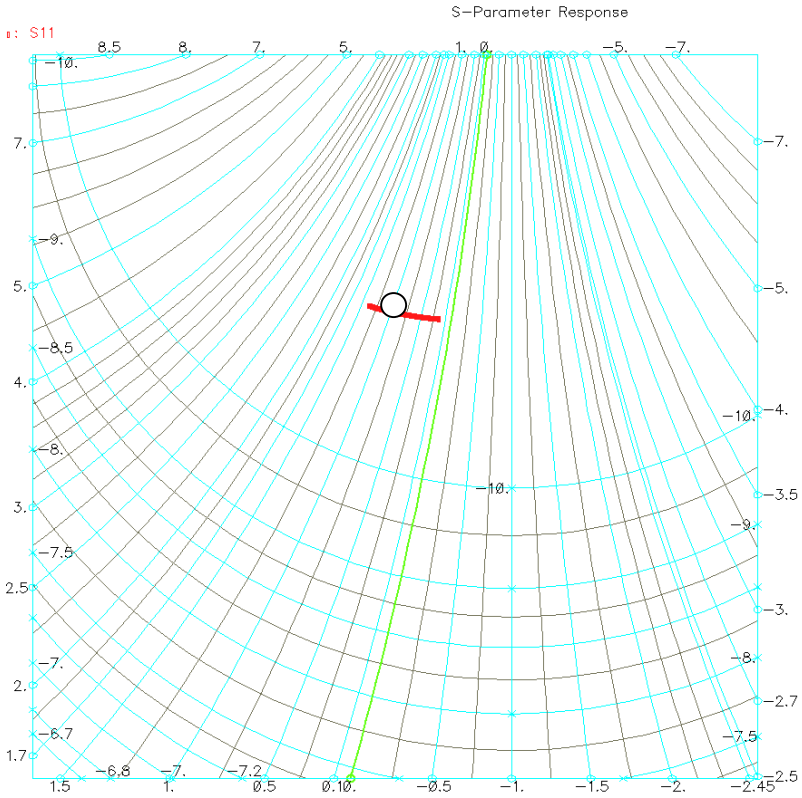
Insert inductive degeneration




Choosing Analyses -- Cadence® Analog Design Environment (8)
OK
Cancel
Defaults
Apply
Help
Analysis
tran
dc
ac
noise
xf
sens
dcmatch
stb
sp
envlp
pss
pac
pnoise
pxf
psp
qpss
qpac
qpnoise
qpxf
qpsp
S-Parameter Analysis
Ports
Select
Clear
Sweep Variable
Frequency
Design Variable
Temperature
Component Parameter
Model Parameter
At Frequency (Hz)
900M
Variable Name
Ls
Select Design Variable
Sweep Range
Start-Stop
Center-Span
Start
0.4n
Stop
4n
Sweep Type
Linear
Step Size
Number of Steps
100
Add Specific Points
Do Noise
yes
no
Output port
/PORT12
Input port
/PORT0
Select
Select
Enabled
Options...

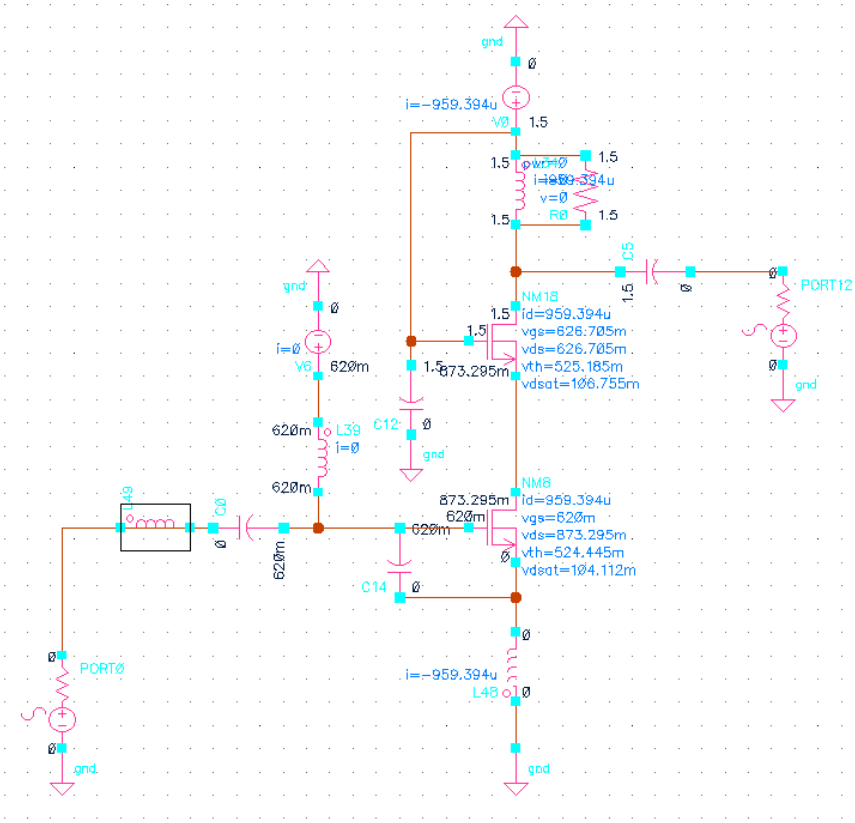


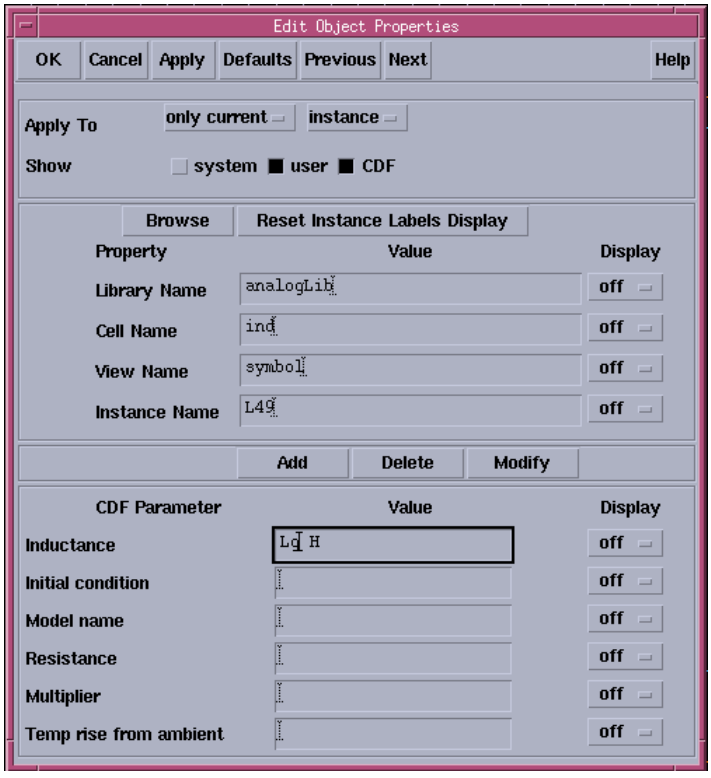
Zoom in

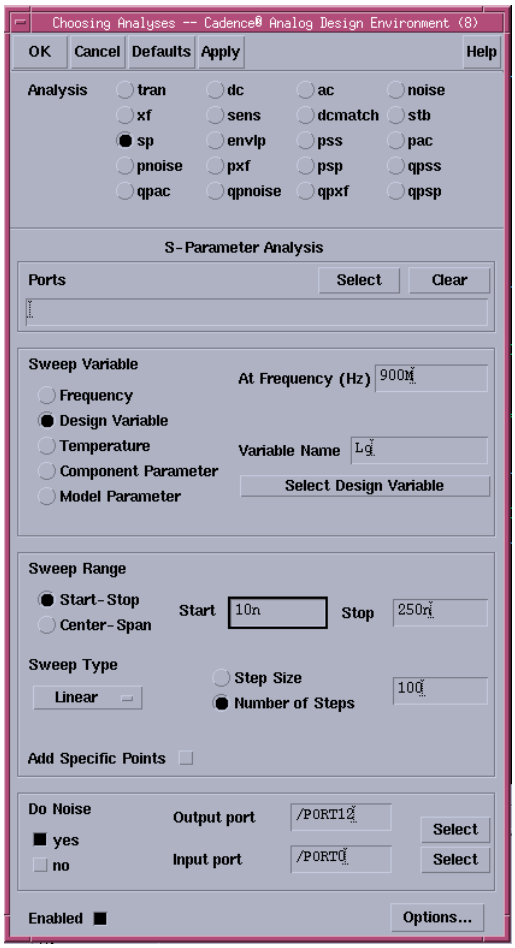


Choose L_s = 1.4n

Insert series gate inductor






Choosing Analyses -- Cadence® Analog Design Environment (8)
OK
Cancel
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Apply
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sens
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sp
envlp
pss
pac
pnoise
pxf
psp
qpss
qpac
qpnoise
qpxf
qpsp
S-Parameter Analysis
Ports
Select
Clear
Sweep Variable
At Frequency (Hz)
900M
Frequency
Design Variable
Temperature
Component Parameter
Model Parameter
Variable Name
Lg
Select Design Variable
Sweep Range
Start-Stop
Center-Span
Start
10n
Stop
250n
Sweep Type
Linear
Step Size
Number of Steps
100
Add Specific Points
Do Noise
yes
no
Output port
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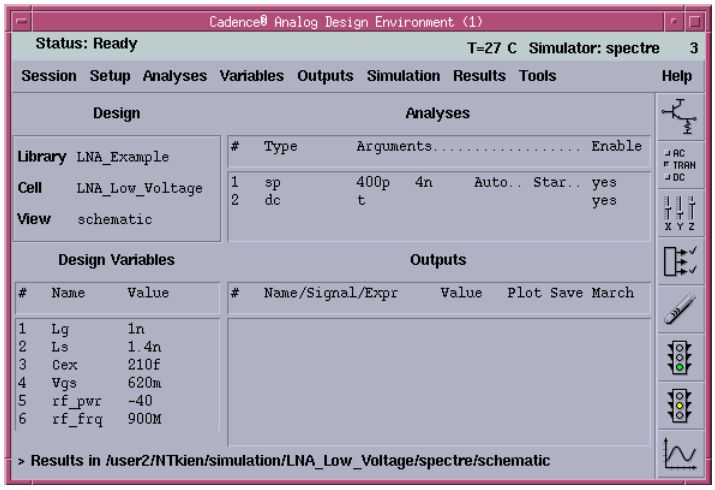
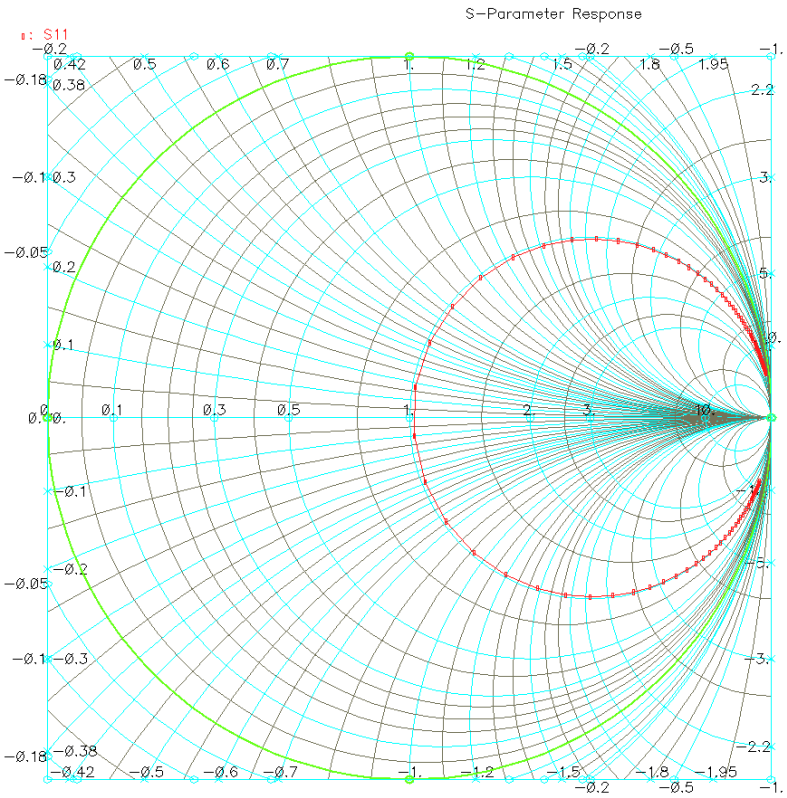
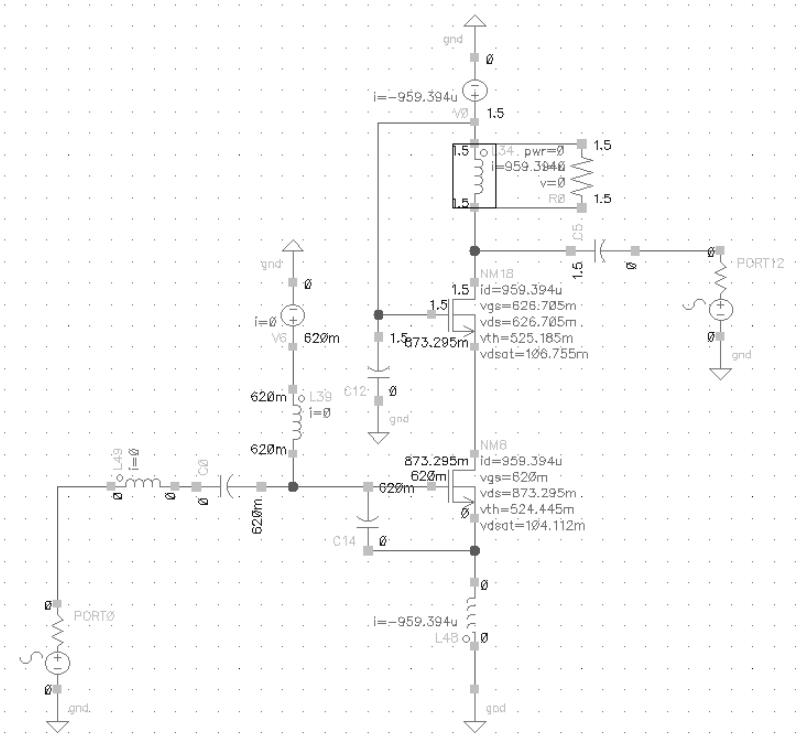
Input port
/PORT0
Select
Select
Enabled
Options...

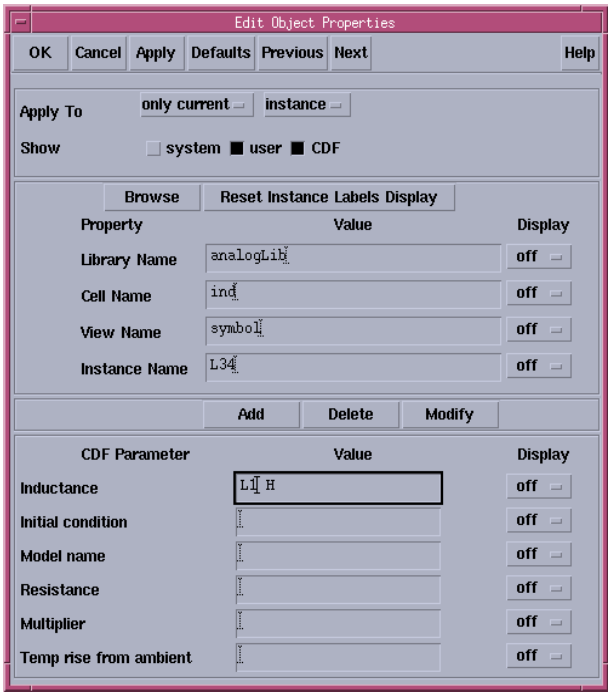

Cadence® Analog Design Environment (1)
Status: Ready
T=27 C Simulator: spectre 3
Session Setup Analyses Variables Outputs Simulation Results Tools Help
Design
Library LNA_Example
Cell LNA_Low_Voltage
View schematic
Analyses
Type Arguments Enable
1 sp 400p 4n Auto.. Star.. yes
2 dc t yes
Design Variables
Name Value
1 Lg 1n
2 Ls 1.4n
3 Cex 210f
4 Vgs 620m
5 rf_pwr -40
6 rf_frq 900M
Outputs
Name/Signal/Expr Value Plot Save March
> Results in /user2/NTkien/simulation/LNA_Low_Voltage/spectre/schematic

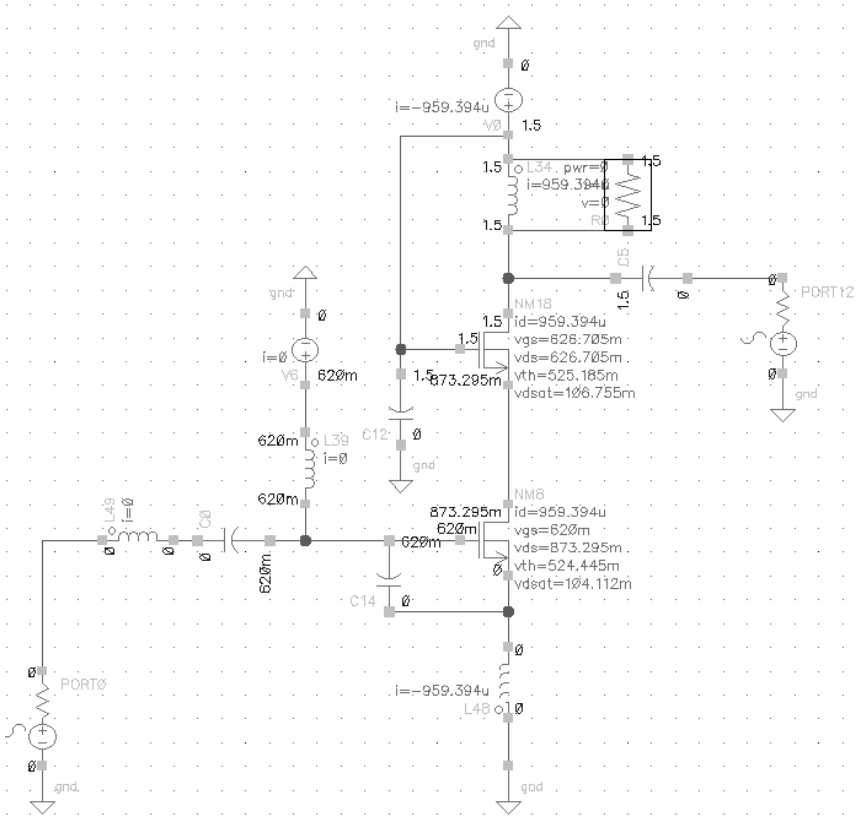


Choose L_g = 107 nH

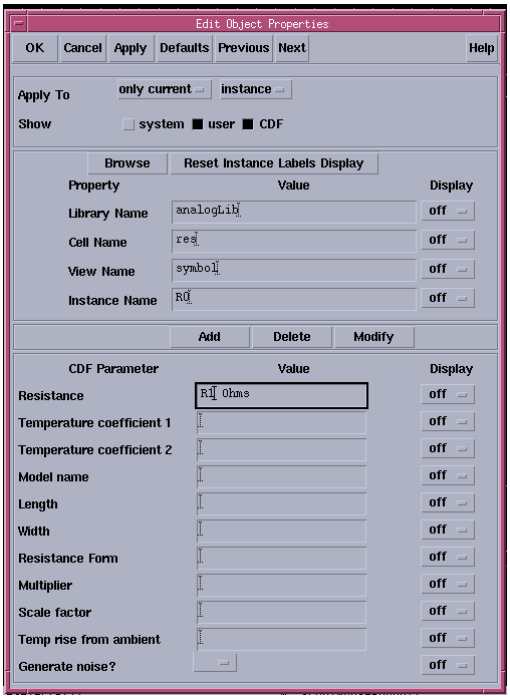


Highlight the output inductor and typing in the inductance field as L1

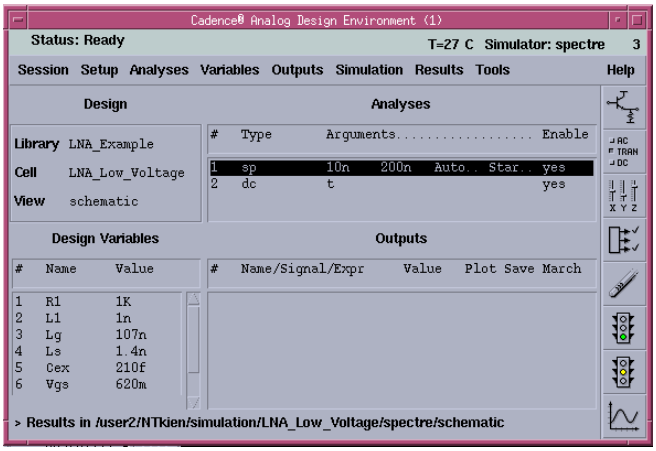


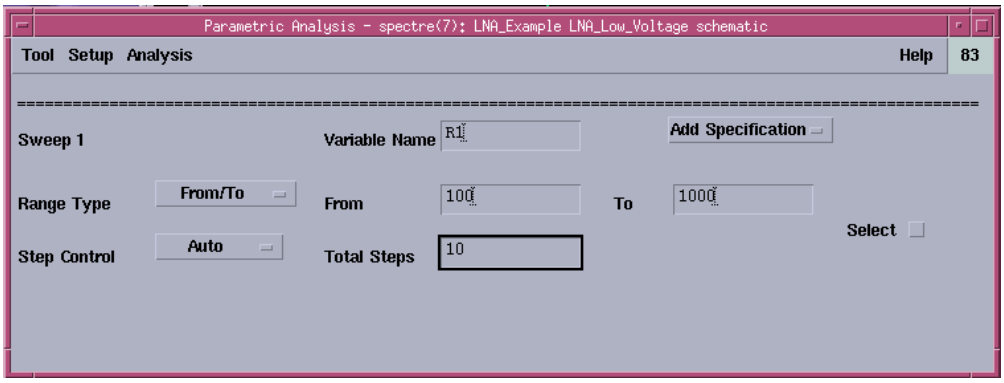


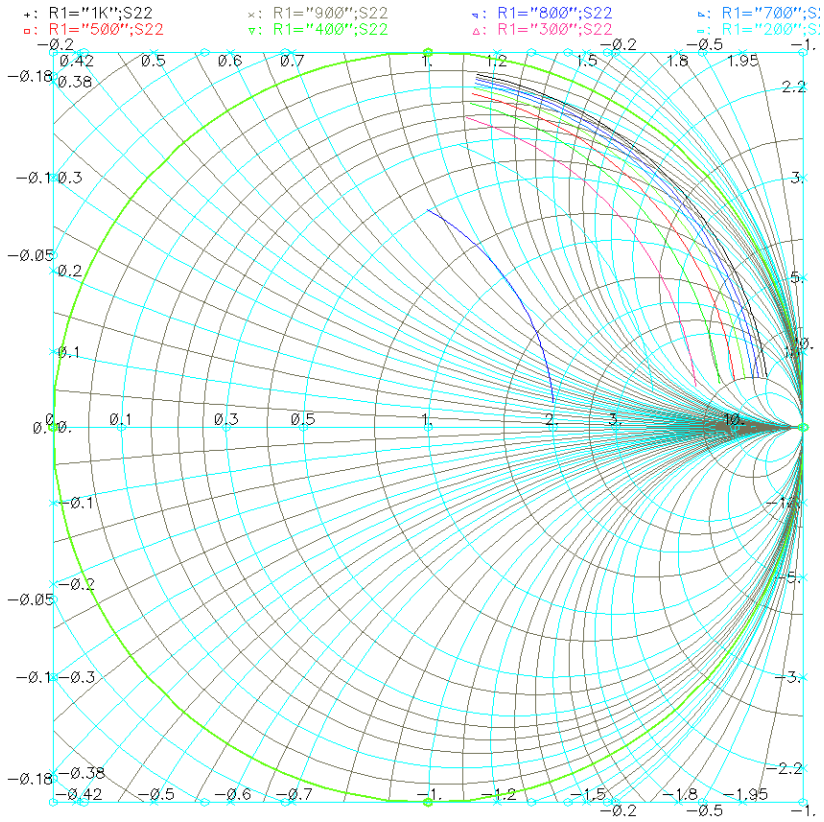
Highlight the output resistor and typing in the resistance field as L1

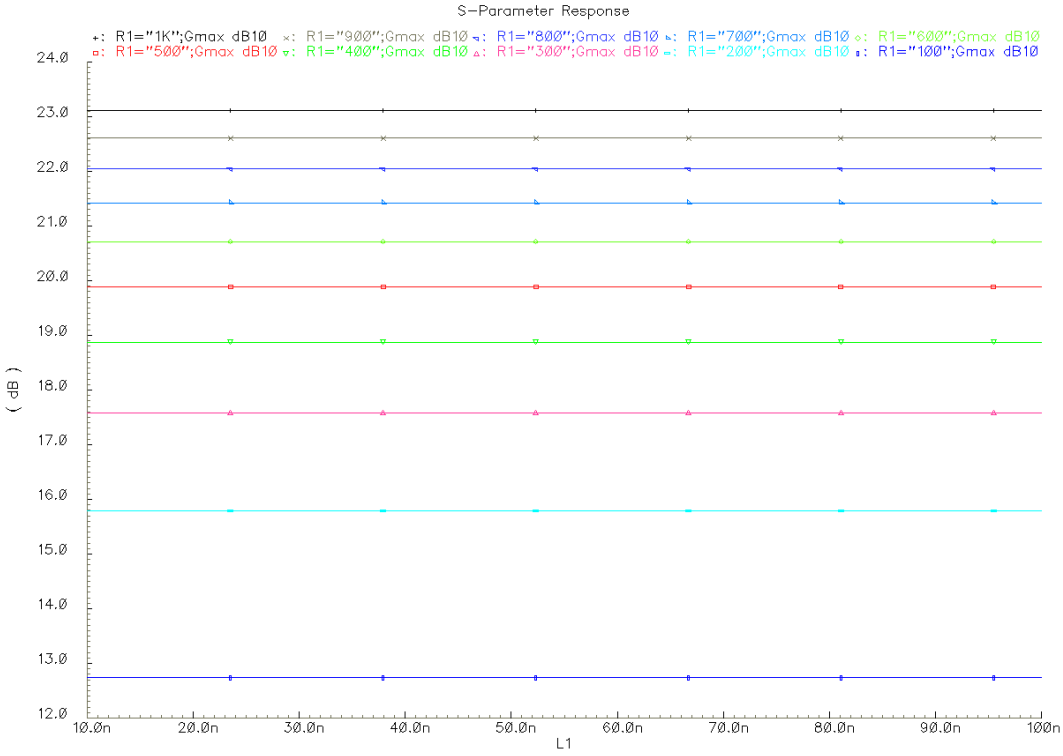


- On the Analog Design Enviroment, click Variable → Copy from cell view, and then typing the primalry value of L1 and R1 (any value).
- The Analog Design Enviroment windown becomes



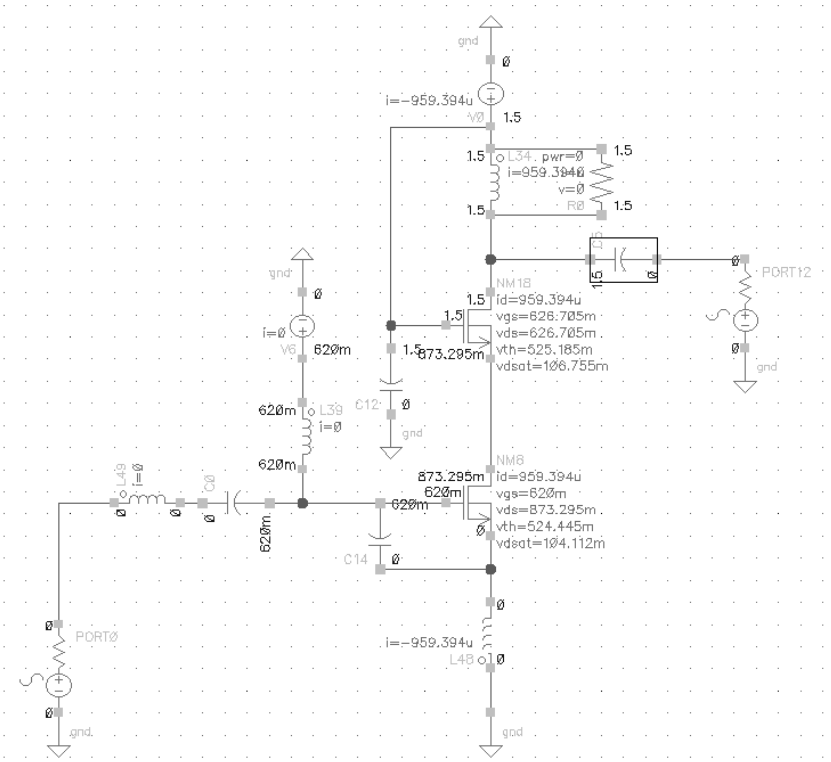

Parametric Analysis - spectre(7): LNA_Example LNA_Low_Voltage schematic
Tool Setup Analysis
Help
83
Sweep 1
Variable Name
R1
Add Specification
Range Type
From/To
From
100
To
1000
Select
Step Control
Auto
Total Steps
10

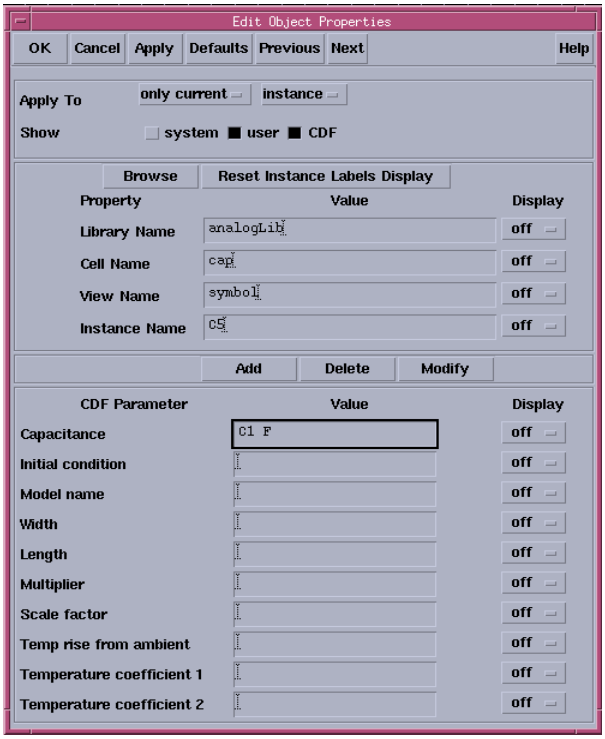

+: R1="1K";S22
×: R1="900";S22
◥: R1="800";S22
◣: R1="700";S
□: R1="500";S22
▽: R1="400";S22
△: R1="300";S22
▱: R1="200";S

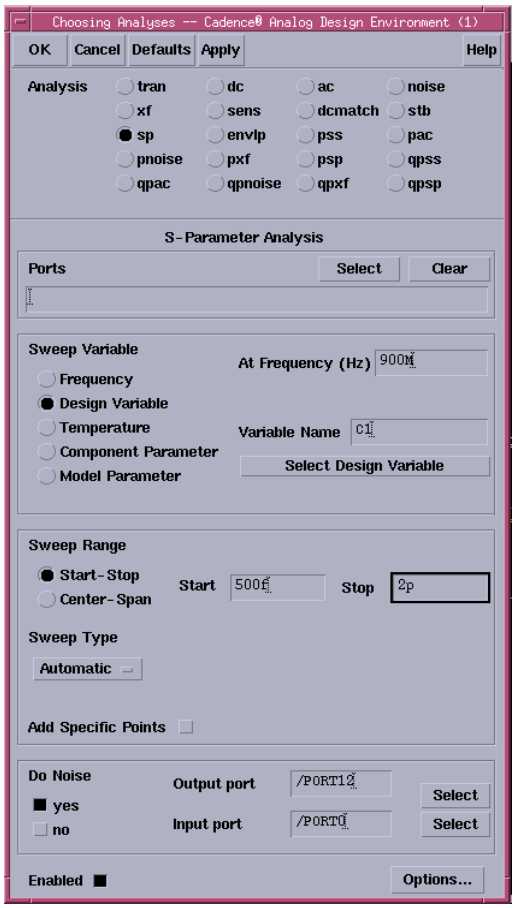


Choose R1 = 400 ohm, L1 = 26 nH

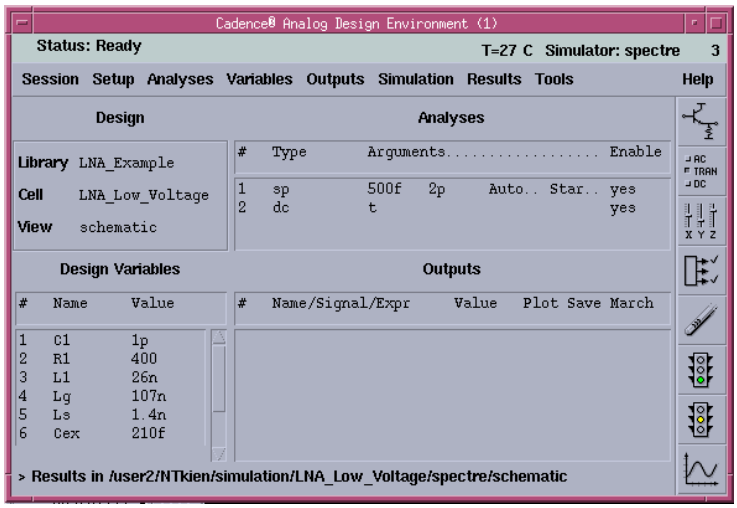
Highline output capacitance

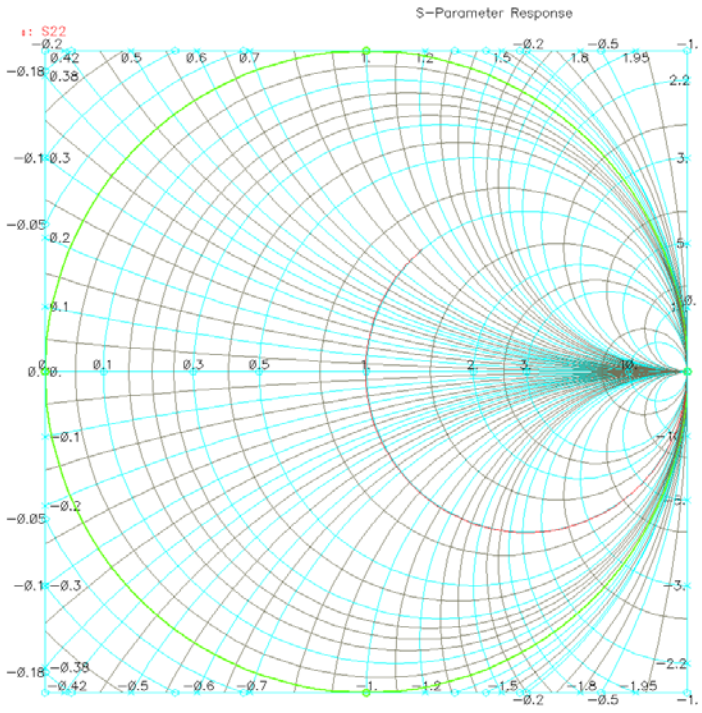



Edit Object Properties
OK
Cancel
Apply
Defaults
Previous
Next
Help
Apply To
only current
instance
Show
system
user
CDF
Browse
Reset Instance Labels Display
Property
Value
Display
Library Name
analogLib
off
Cell Name
cap
off
View Name
symbol
off
Instance Name
C5
off
Add
Delete
Modify
CDF Parameter
Value
Display
Capacitance
C1 F
off
Initial condition
off
Model name
off
Width
off
Length
off
Multiplier
off
Scale factor
off
Temp rise from ambient
off
Temperature coefficient 1
off
Temperature coefficient 2
off


Choosing Analyses -- Cadence® Analog Design Environment (1)
OK
Cancel
Defaults
Apply
Help
Analysis
tran
dc
ac
noise
xf
sens
dcmatch
stb
sp
envlp
pss
pac
pnoise
pxf
psp
qpss
qpac
qpnoise
qpxf
qpsp
S-Parameter Analysis
Ports
Select
Clear
Sweep Variable
At Frequency (Hz)
900M
Frequency
Design Variable
Temperature
Component Parameter
Model Parameter
Variable Name
C1
Select Design Variable
Sweep Range
Start-Stop
Center-Span
Start
500f
Stop
2p
Sweep Type
Automatic
Add Specific Points
Do Noise
yes
no
Output port
/PORT12
Input port
/PORT0
Select
Select
Enabled
Options...

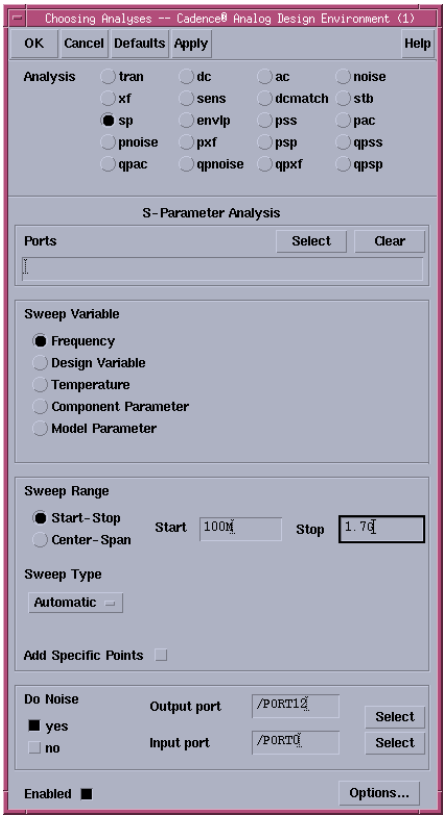
Analog Design Environment becomes



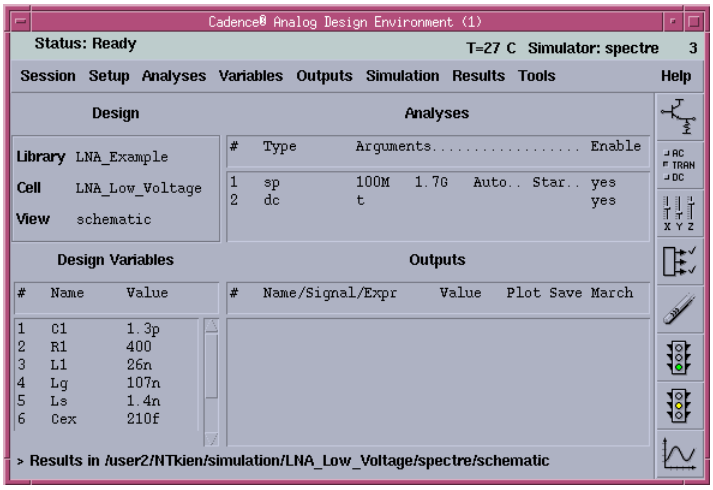


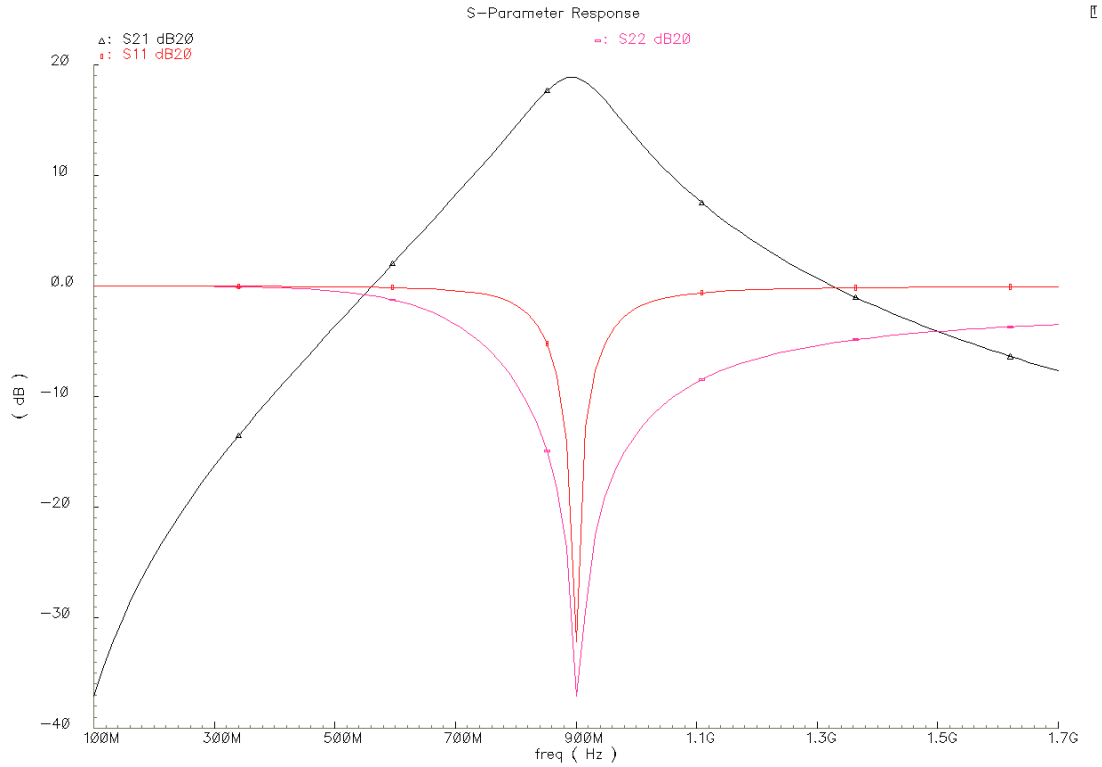
Choose C1 = 1.3 pF

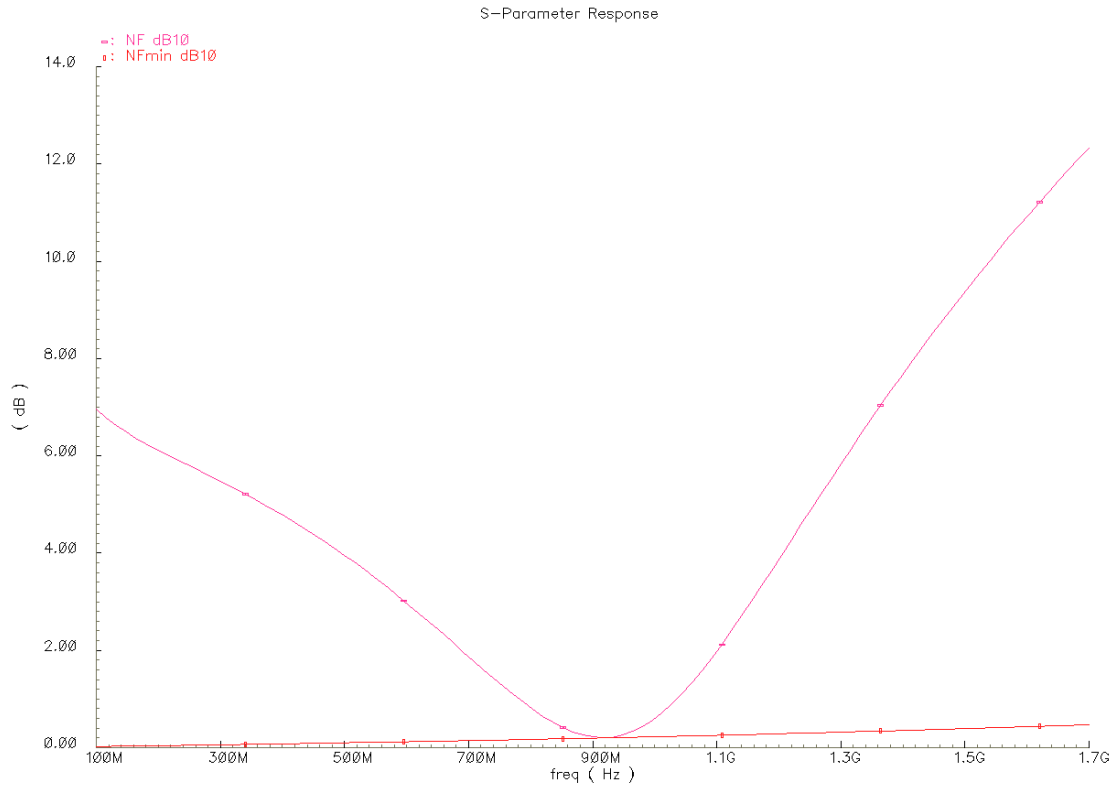
Run S-Parmeters Simulation



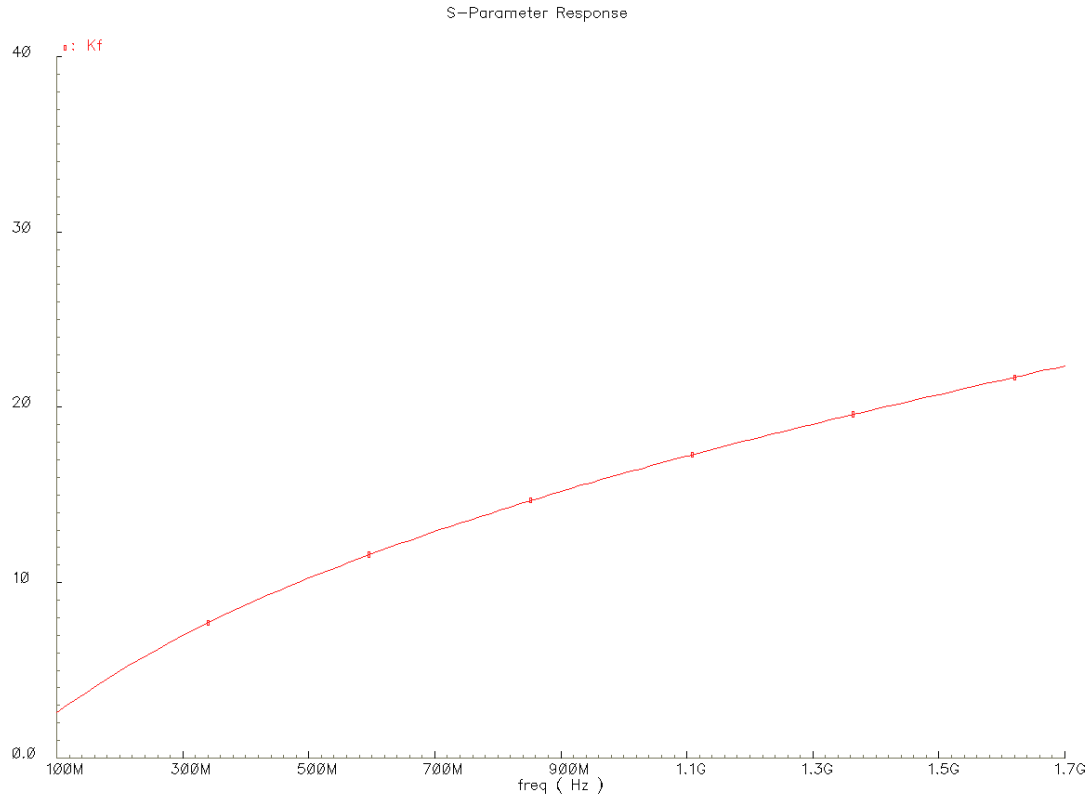
Analog Design Environment becomes




S-Parameter Response
S21 dB20
S11 dB20
S22 dB20
20
10
0.0
-10
-20
-30
-40
(dB)
100M
300M
500M
700M
900M
1.1G
1.3G
1.5G
1.7G
freq (Hz)


S-Parameter Response
NF dB10
NFmin dB10
14.0
12.0
10.0
8.00
6.00
4.00
2.00
0.00
(dB)
100M
300M
500M
700M
900M
1.1G
1.3G
1.5G
1.7G
freq (Hz)

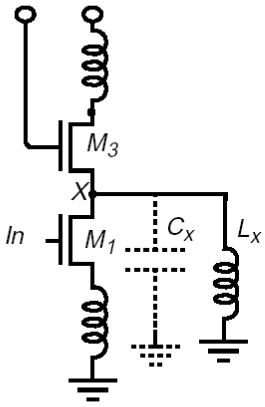
Stability factor

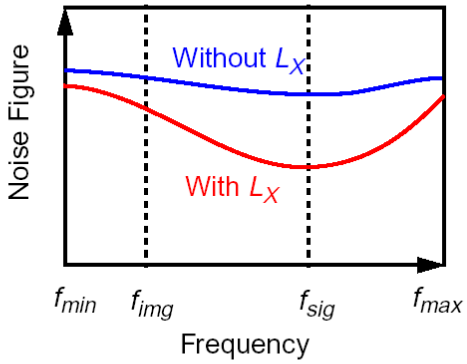


1. Image Rejection LNA

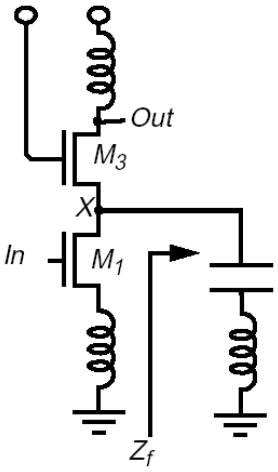
1.1 Circuit Descriptions

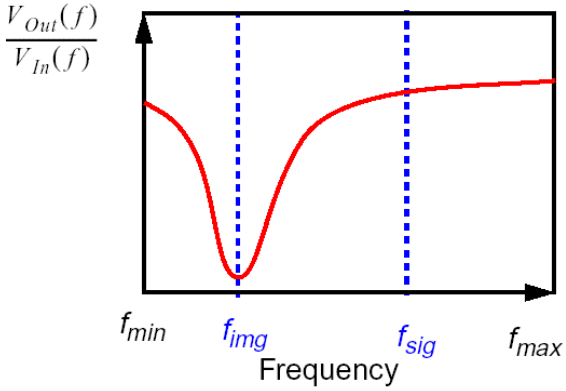
Parasitic capacitance C_X degrades the noise performance.



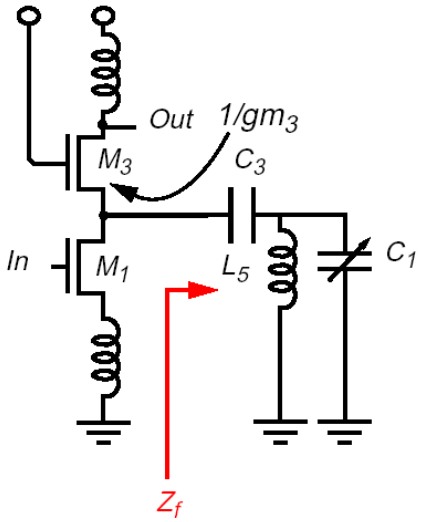


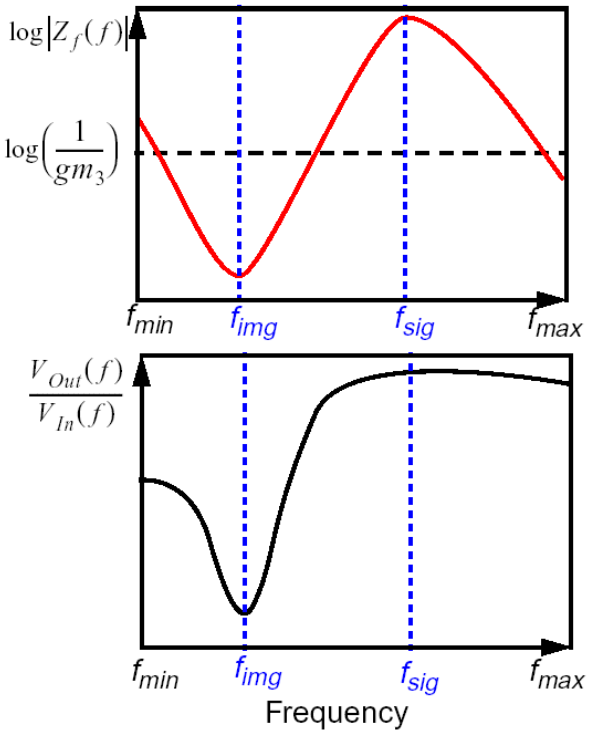
- Parallel resonance @f_{Sig}→ improves noise figure





- Series resonance @f_{Img}→ improves image rejection



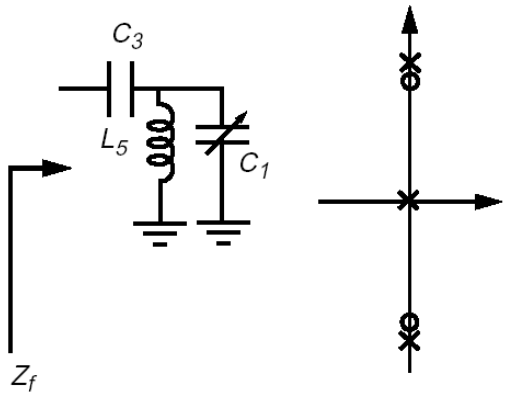


$$Z_f(s) = \frac{L_5 \cdot (C_3 + C_1) \cdot s^2 + 1}{C_1 \cdot C_3 \cdot L_5 \cdot s^3 + C_3 \cdot s}$$

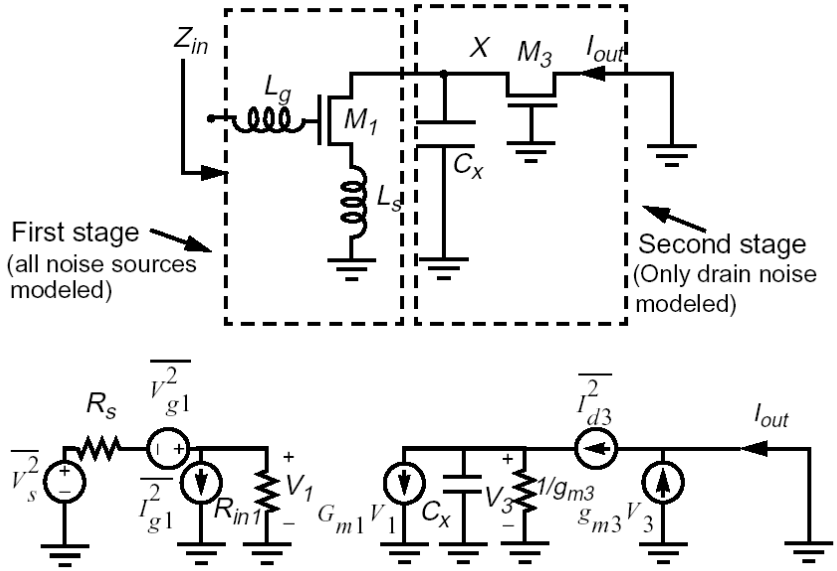
$$\omega_p = 0$$

$$\omega_p = \pm \frac{1}{\sqrt{L_5 \cdot C_1}}$$

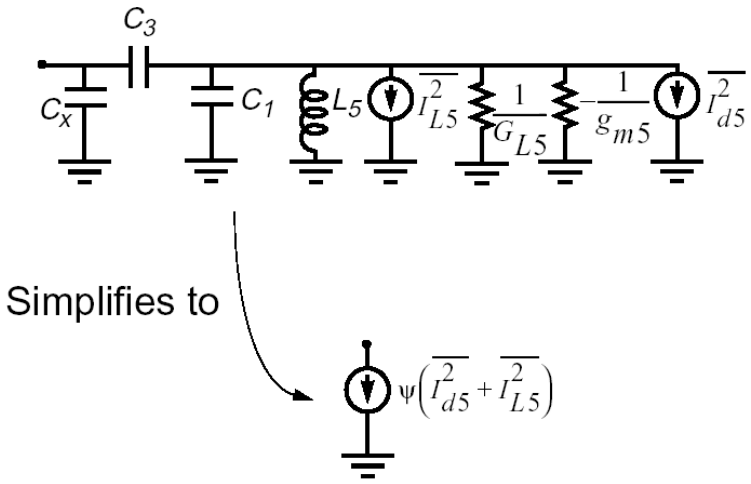
$$\omega_z = \pm \frac{1}{\sqrt{L_5 \cdot (C_3 + C_1)}}$$



Equivalent Noise Circuit for the LNA



Filter Noise Model



Noise Formulas

$$F_{no-filter} = F_1 + 4R_s\gamma_3 g_{do3}\left(\frac{\omega_0^2}{\omega_T^2}\right)\left(\frac{C_x^2}{g_{m3}^2}\omega_0^2\right)$$

- Overall NF of LNA/Filter is

$$F_{tot} = F_1 + \psi \cdot 4R_s(\gamma_5 g_{do5} + G_{L5})\left(\frac{\omega_0^2}{\omega_T^2}\right)$$

$$\text{Where } \psi = \frac{C_3^2 \cdot \omega_0^2}{\left(\frac{C_3^2}{C_x + C_3}\right)^2 \cdot \omega_0^2 + (G_{L5} - g_{m5})^2},$$

$$F_1 = 1 + \frac{1}{g_m^2 R_s} \cdot \left\{ \begin{array}{l} \gamma g_{d0} \cdot \left\{ \begin{array}{l} \left[1 + s^2 C_{gs}\left(L_g + L_s\right)\left(1 + |c|\alpha\sqrt{\frac{\delta}{5\gamma}}\right)\right]^2 \\ -\left(sC_{gs}R_s\right)^2\left(1 + |c|\alpha\sqrt{\frac{\delta}{5\gamma}}\right)^2 \end{array} \right\} \\ -\frac{\alpha\delta}{5}\left(1 - |c|^2\right) g_m \left(sC_{gs}\right)^2\left(R_s^2 - sL_g^2\right) \end{array} \right\}$$

- Note that the impedance of the filter at the frequency of the pole is high enough → $F_{total} = F_1$

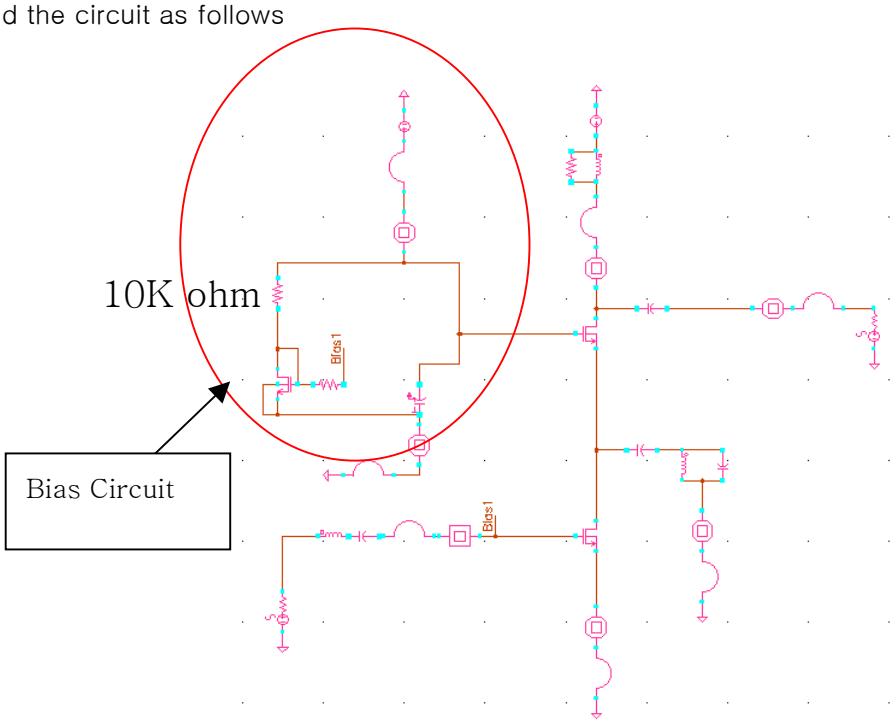
1.2 Circuit Implementation

1.2.1 Setup Environment

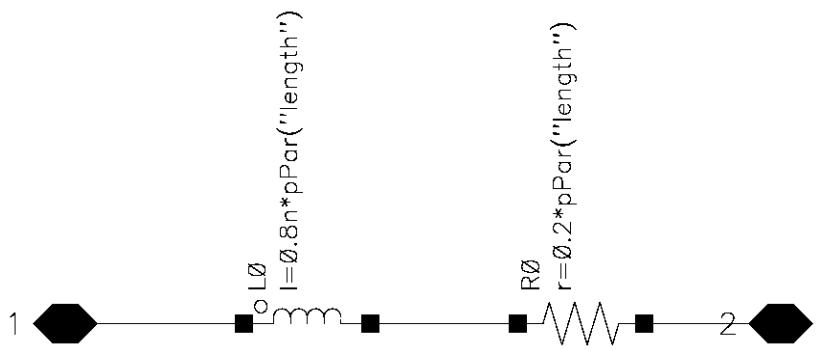
Assume that we design the image rejection LNA operating at 5 GHz with the image signal equal to 5.5 Ghz → Based on Eq. We can calculate the value of each component of the image rejection circuit as follows:

L1 (image rejection filter) = 2.2 nH, C1 (Image Rejection Filter) = 100f, C3 (Image Rejection Filter) = 300f

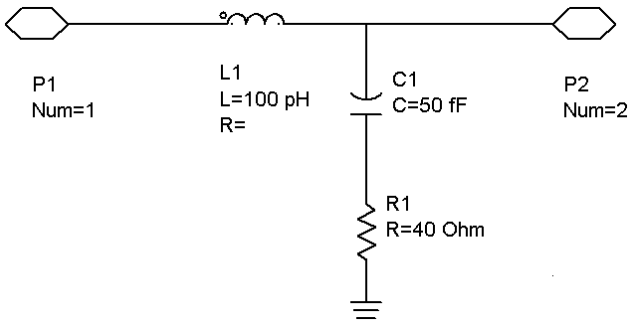
Build the circuit as follows



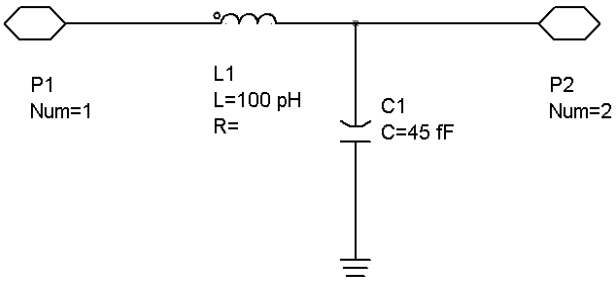
- The model of bond-wire is shown in below



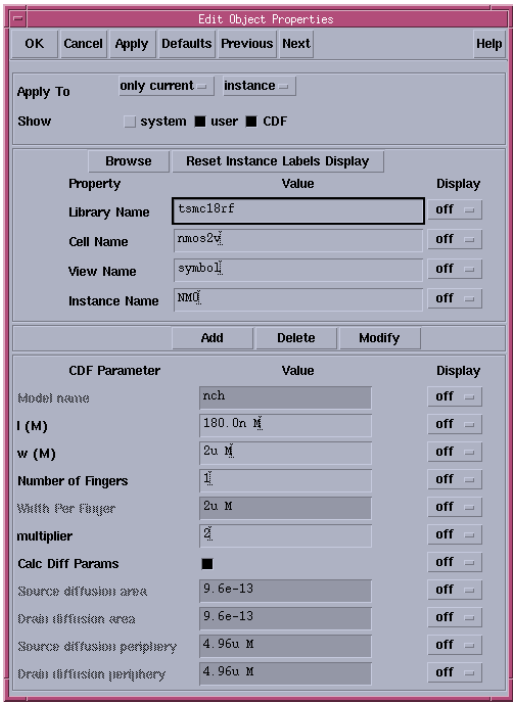
- The model of bond pad power is shown in below



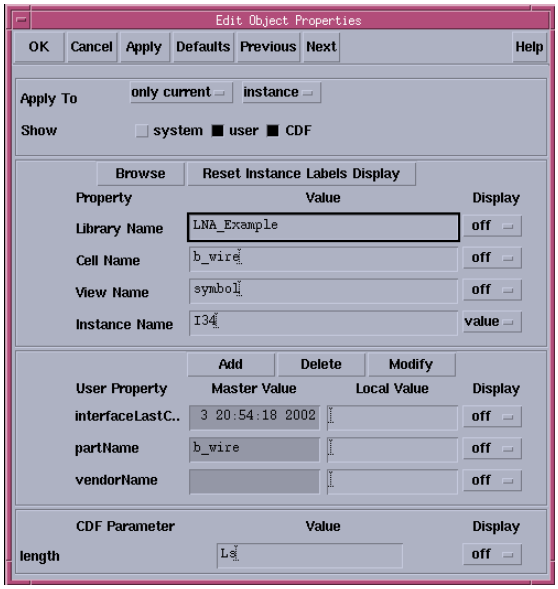
- The model of bond pad shield is shown in below



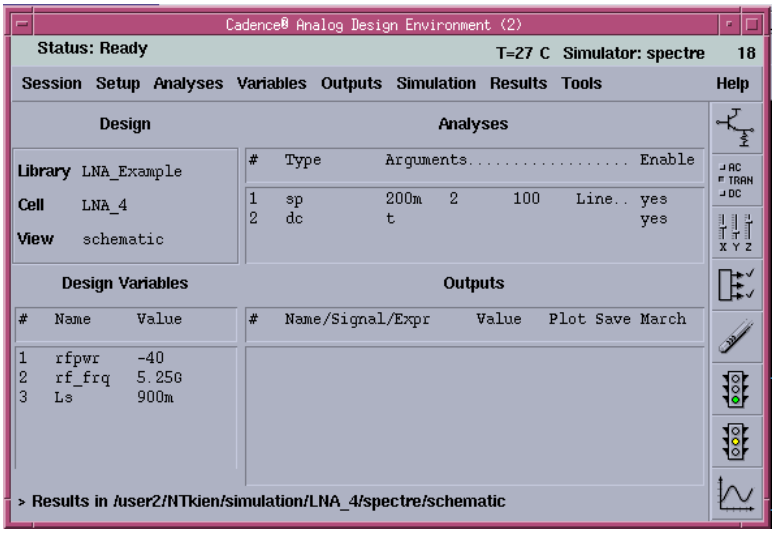
Size of bias transistor



The way to find the value of input and output matching are the same as the Low Noise Amplifier 1: Theory. However, the step to determine the value of Ls is different because now the degeneration inductor is made by bonding wire instead of using onchip inductor.



Sweep the value of Ls

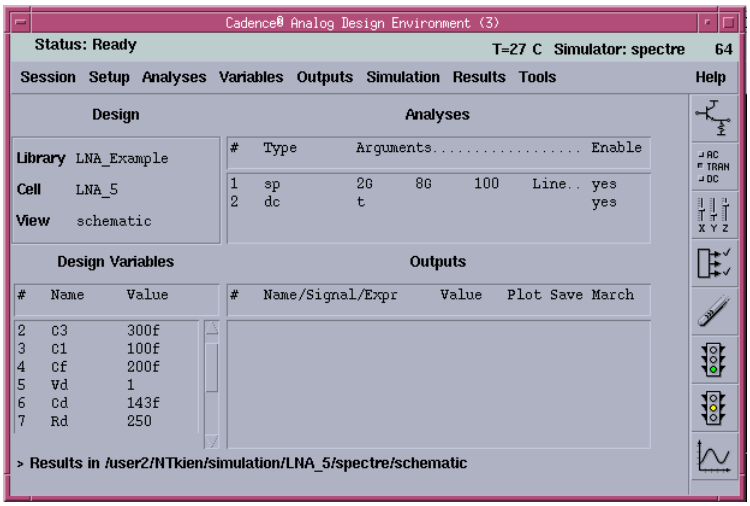


Finally, we obtain the value of each component as follows

Ls = 0.3m, Lg = 2.5 nH, Ld (output inductance) = 2.3 nH, Rd (Output resistance) = 250 ohm

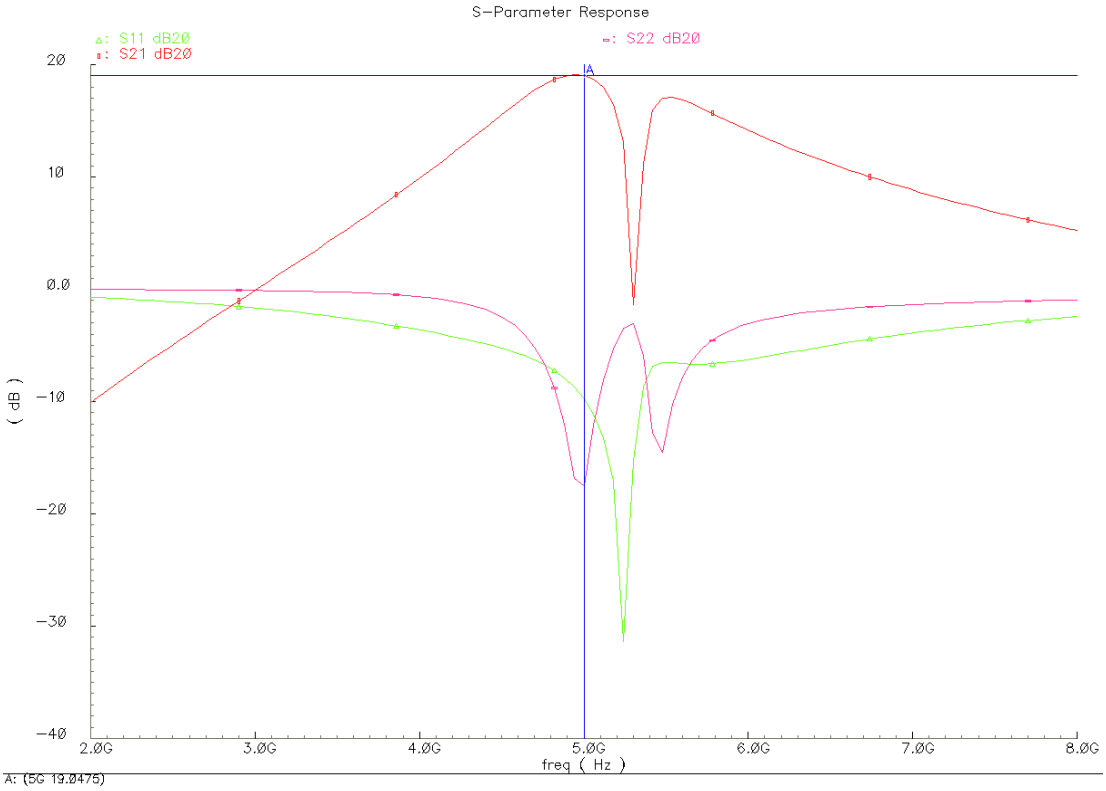
Cd (Ouput capacitance = 1443 fF

1.2.2 Run S-parameters simulation

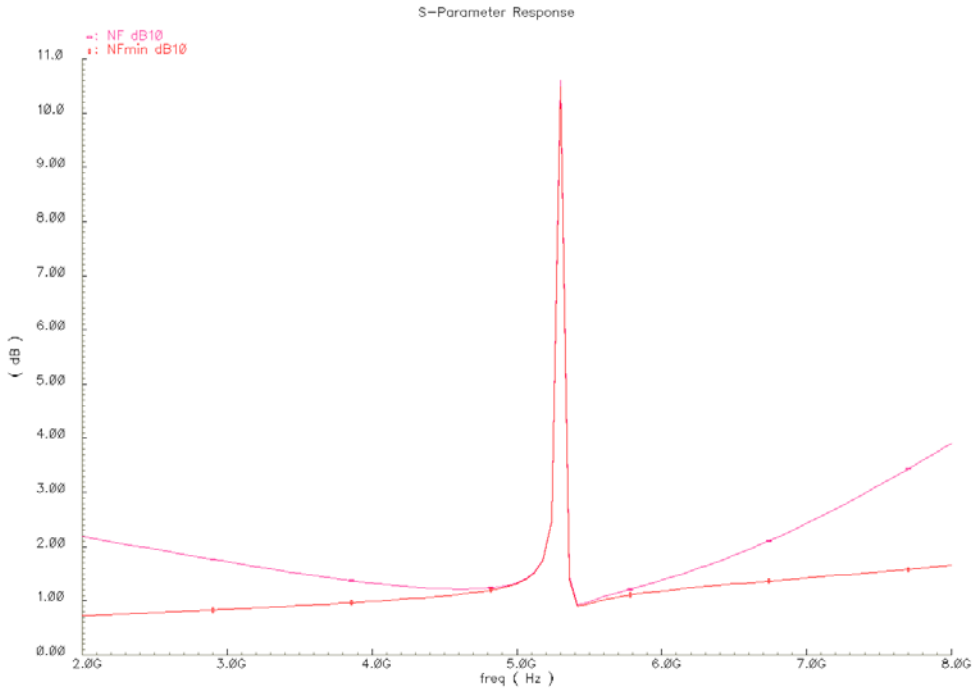


1.2.3 Plot Results

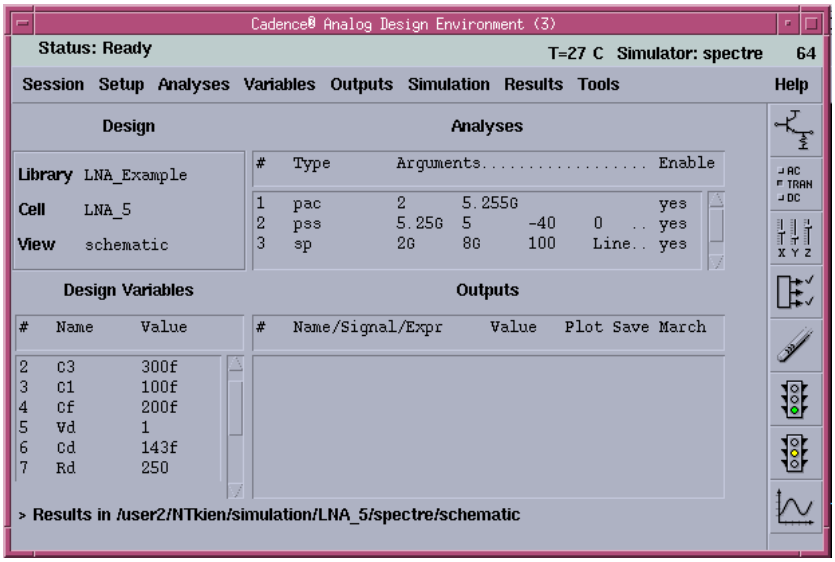
1) S-Parameters



2) NF and NFmin

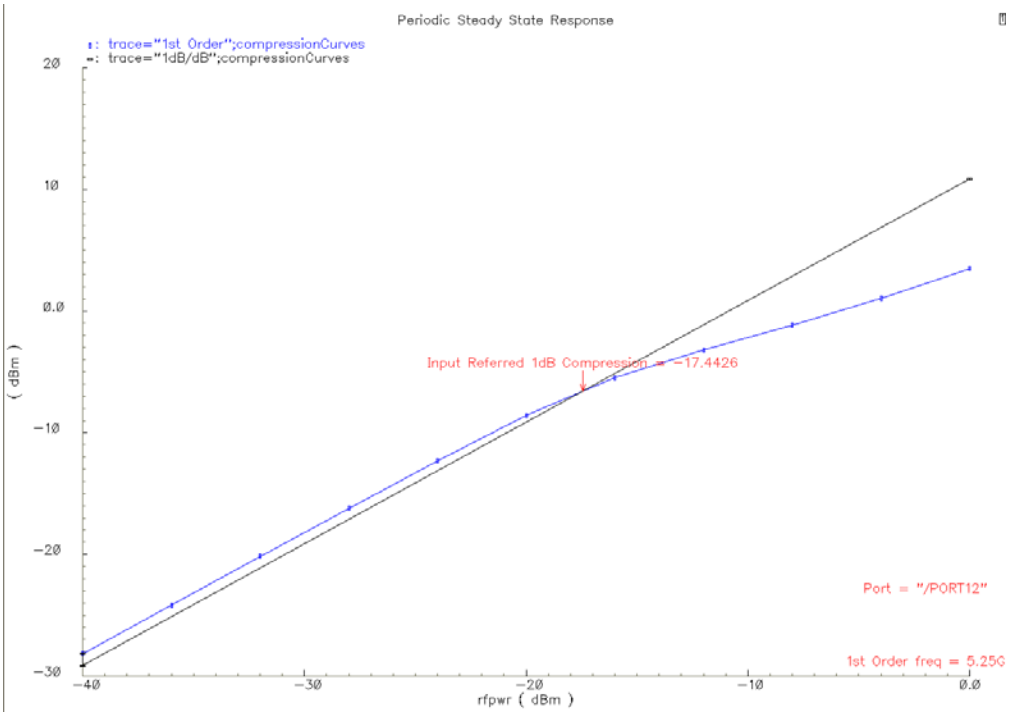


1.2.4. Check Linearity

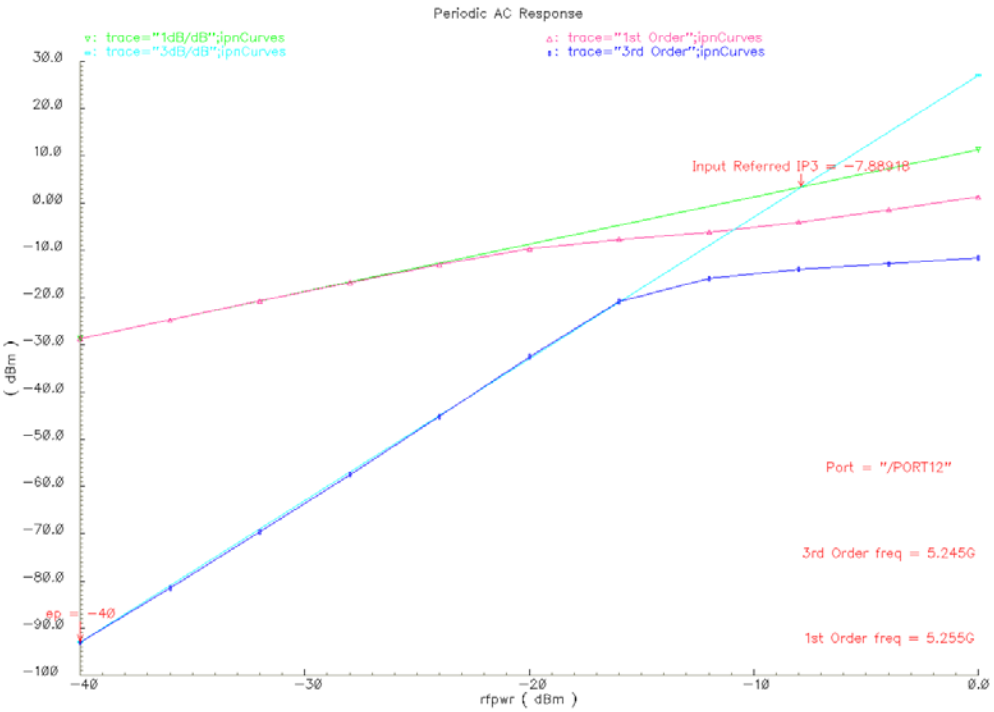


1.2.5. Plot Results

1) 1dB compression point

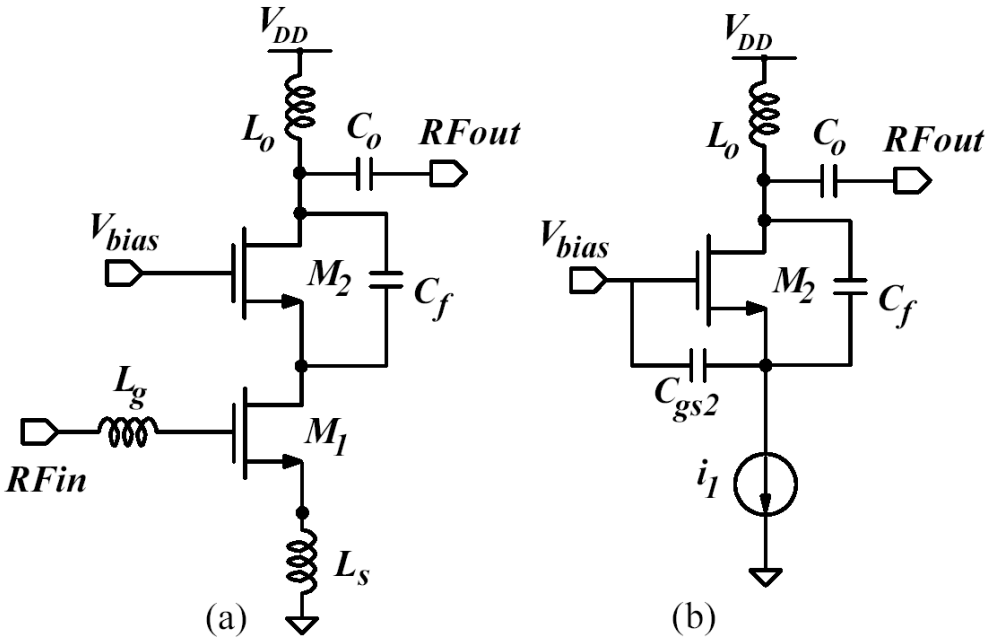


2) IIP3



2. Gain Enhancement Technique Using Positive Feedback

2.2.1 Circuit Descriptions



- The positive feedback is realized by C_f
- This phenomenon can be understood by another point of view as the form of oscillator. C_{gs1}, C_f, and M_1 constitute an oscillator topology with inductive termination at the output.
- The gain of amplifier without C_f is given by

$$A_v = g_{m1} Q_{in} \frac{1}{G_{tot}} = G_{eff} \frac{1}{G_{tot}} \tag{5.1}$$

- g_m is the transconductance of M_1,
- Q_{in} is the quality factor of the input circuit
- G_{eff} is the effective transconductance of the amplifier
- G_{tot} is the total transconductance at the drain of M_2 and is dominated by the equivalent parallel conductance of the inductor (G_P).

$$G_P = \frac{1}{Q_L^2 R_{L_o}} \tag{5.2}$$

- R_{Lo} is the series resistance of the inductor

➢ Low Q_L lead to high G_P → high G_{tot} → Limit the A_v of the amplifier

➢ From (5.1) → Gain of amplifier can be improved by larger G_{eff} or larger L_o → larger power consumption or an impracticably larger value for the inductor

➢ The Q of the amplifier without C_f is given by

$$Q = \frac{1}{G_{tot}} \sqrt{\frac{C_{tot}}{L_o}} \tag{5.3}$$

- C_{tot} is the total capacitance at the drain of M_2.

➢ From (5.2) and (5.3): Low Q_L will also limit the Q of amplifier

➢ Assume that $\omega << g_{m2} / \left(C_{gs2} + C_f \right)$, from Fig.-b, the negative conductance (G_N) is generated by C_f is

$$G_N = \frac{\omega^2 C_{gs2}\left(C_N + C_{gd2}\right)}{g_{m2}} \tag{5.4}$$

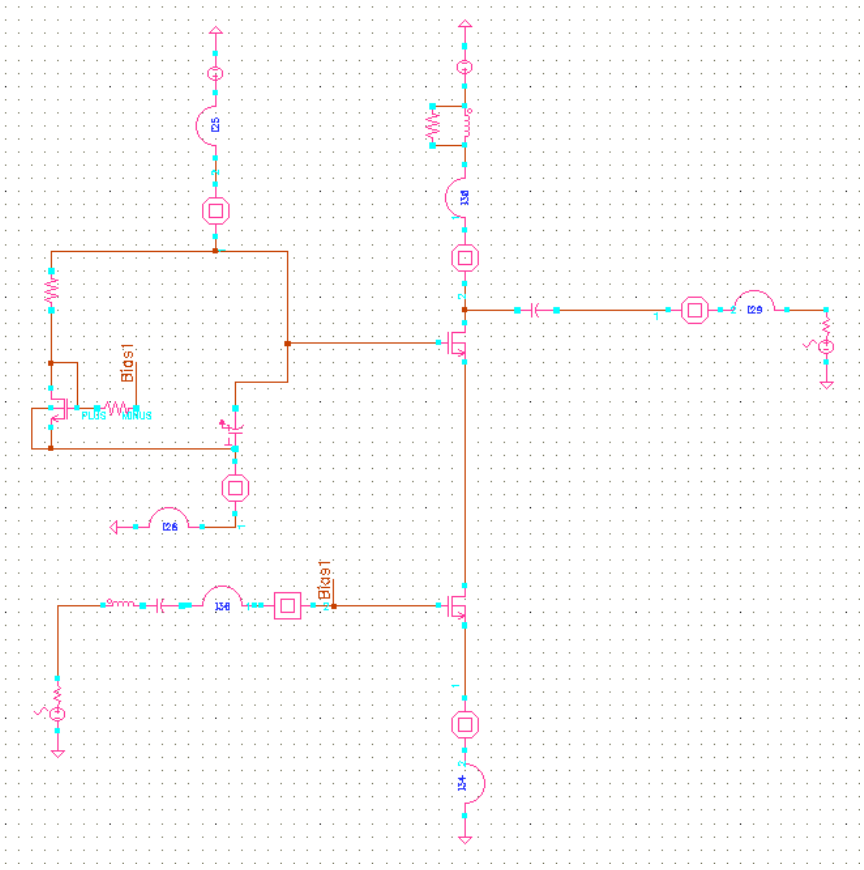
- The total conductance now is given by

$$G_{tot} = G_P - G_N \tag{5.5}$$

- From (5.5) by using C_f, the total conductance is reduced→ improve gain of LNA
- Note that no additional active is used therefore no more DC power dissipated and no noise contributed.
- The limit to amount of feedback is governed by stability consideration. To ensure the stability condition, G_{tol} must always positive.

2.2.2 Ciruit Implementation

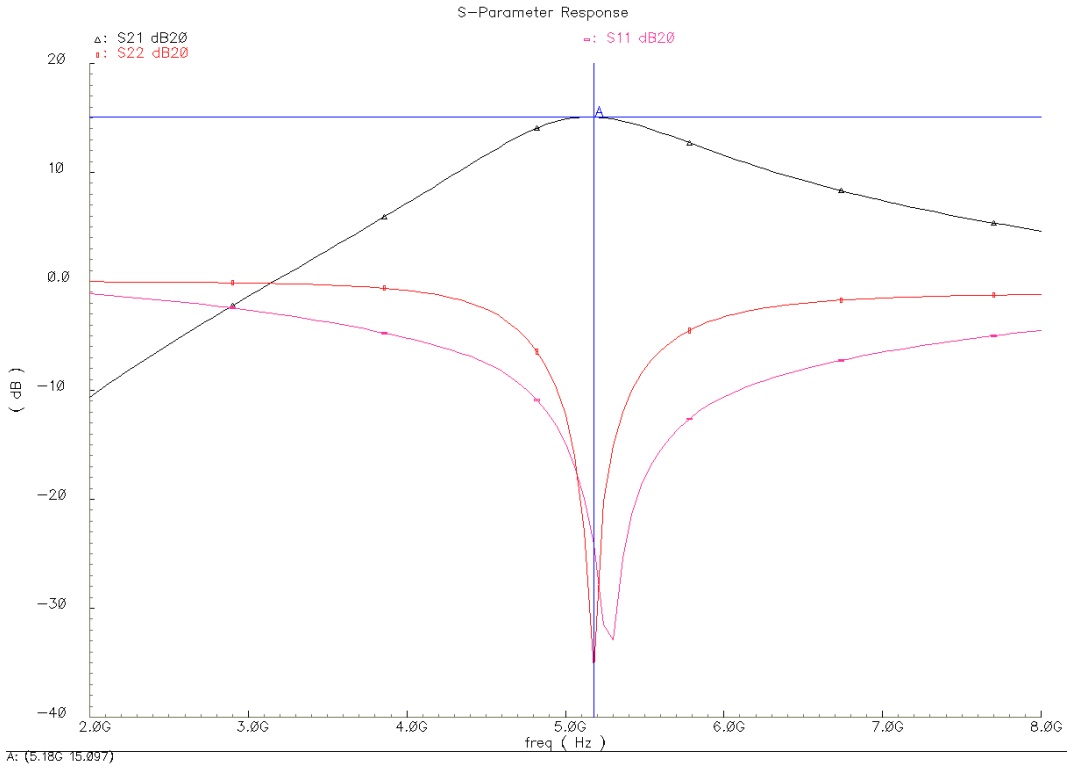
2.2.1 Setup Environment

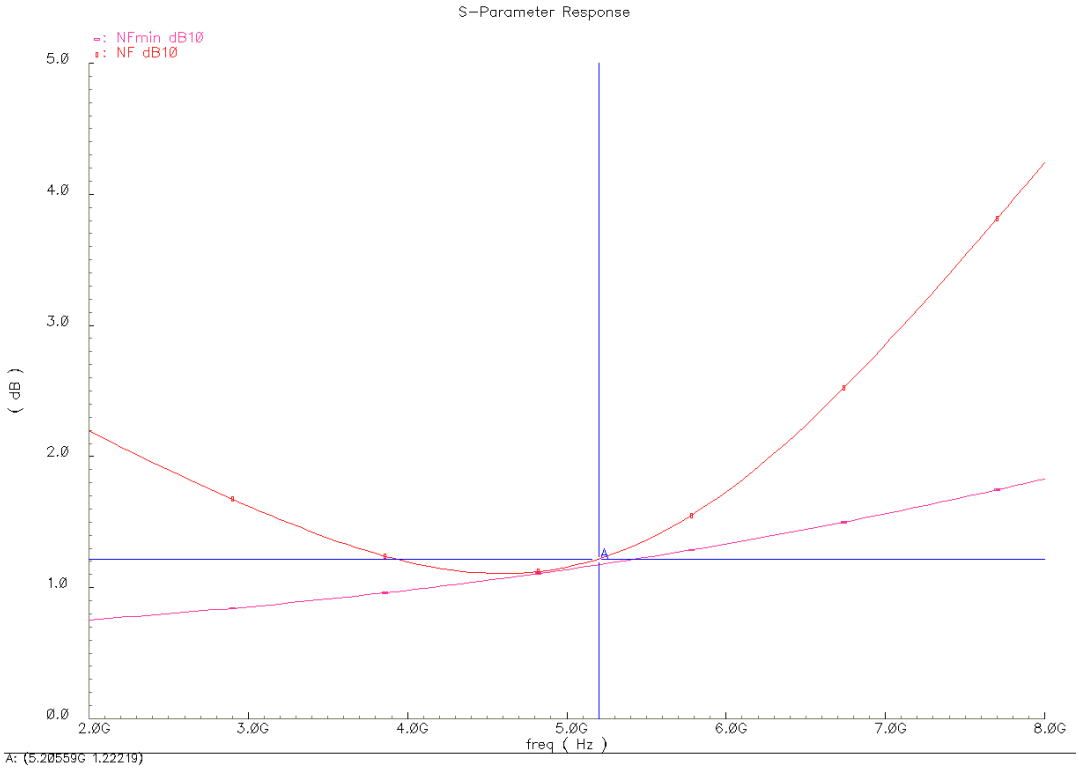


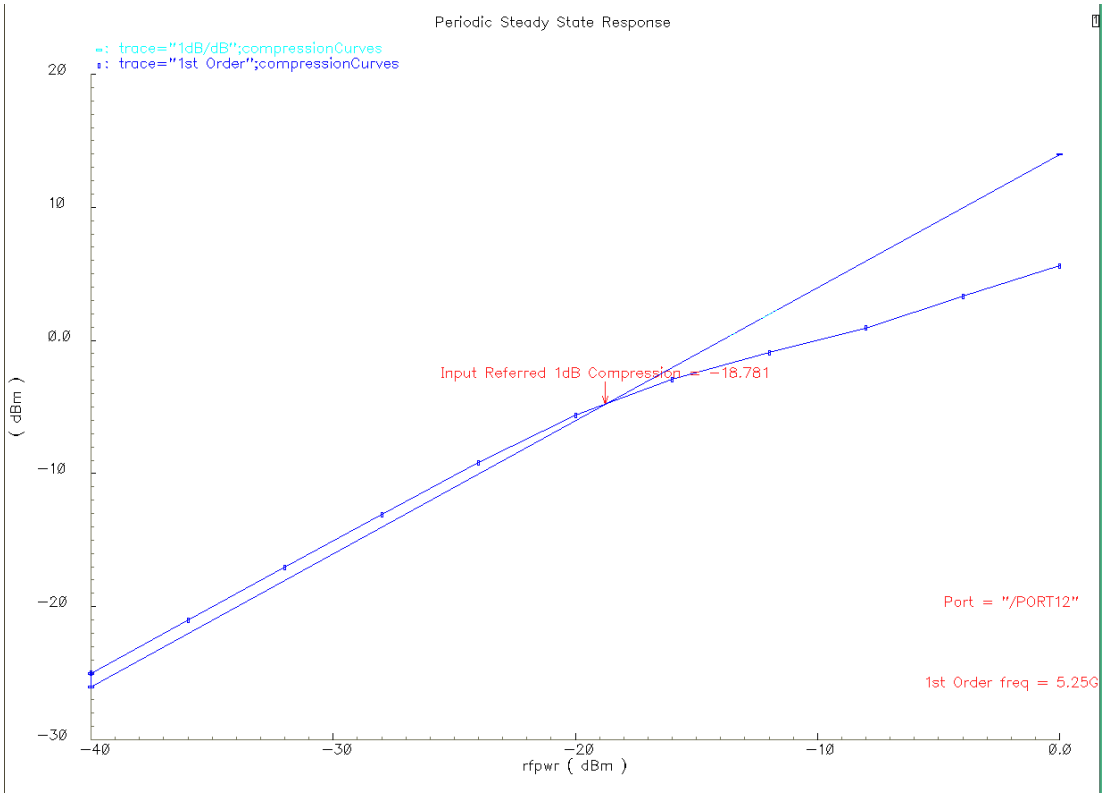
The value of component of matching network: Ls = 530 mm, Lg = 2.6 nH

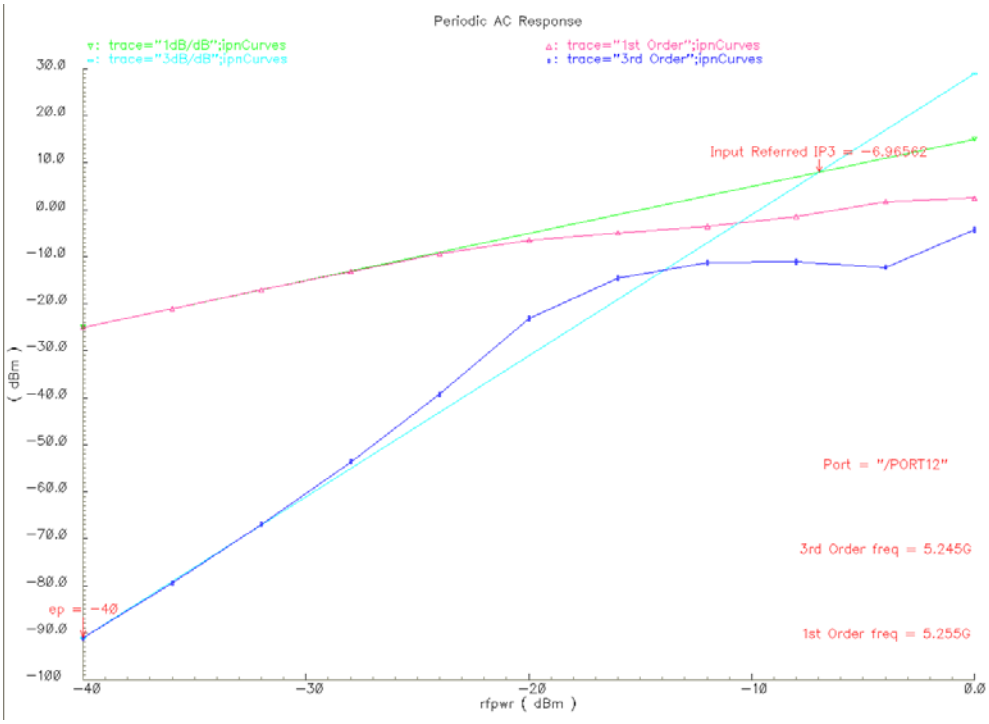
The value of output matching network: L1, R1 va C1 are:

2.2.2 Runsimulation



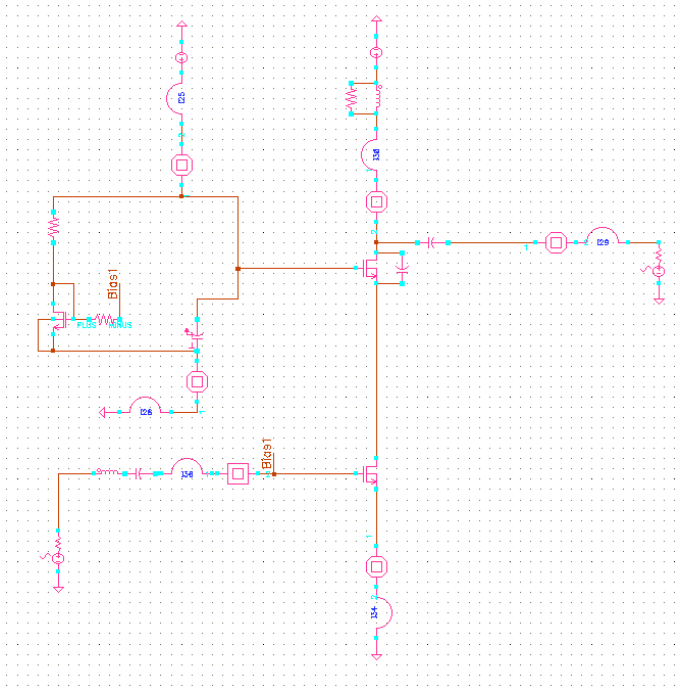




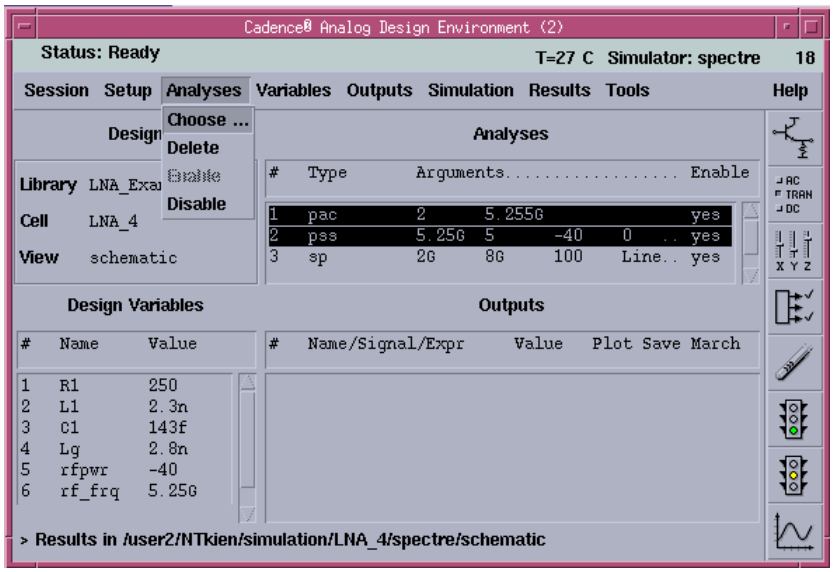


Insert additional capacitor connected to drain and source terminal of the cascode transistor

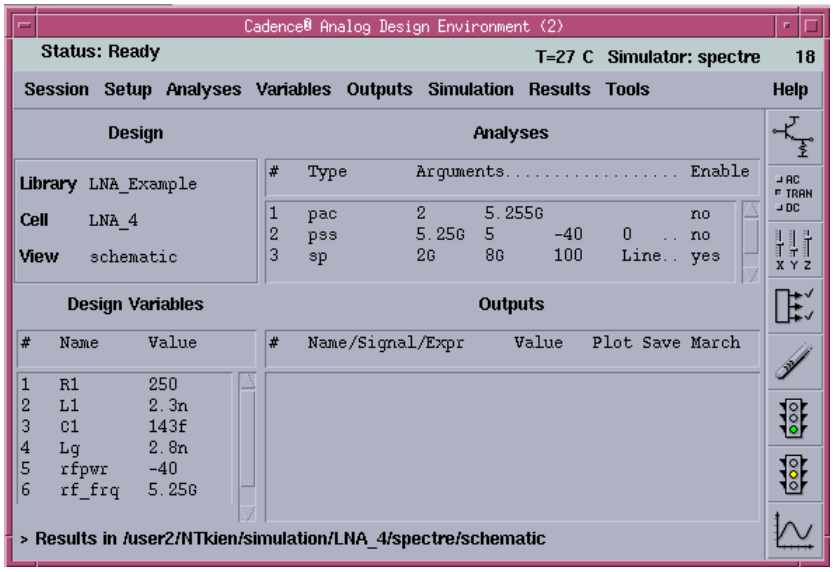
- Highline this capacitor and as set its capacitance as variable C_f



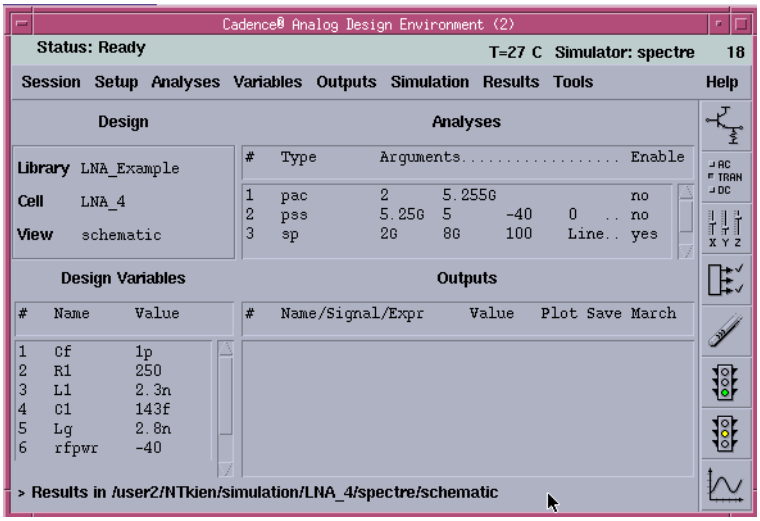
On the Anallog Design Inviroment windown, invisible PSS and PAC analyses by doing as follows



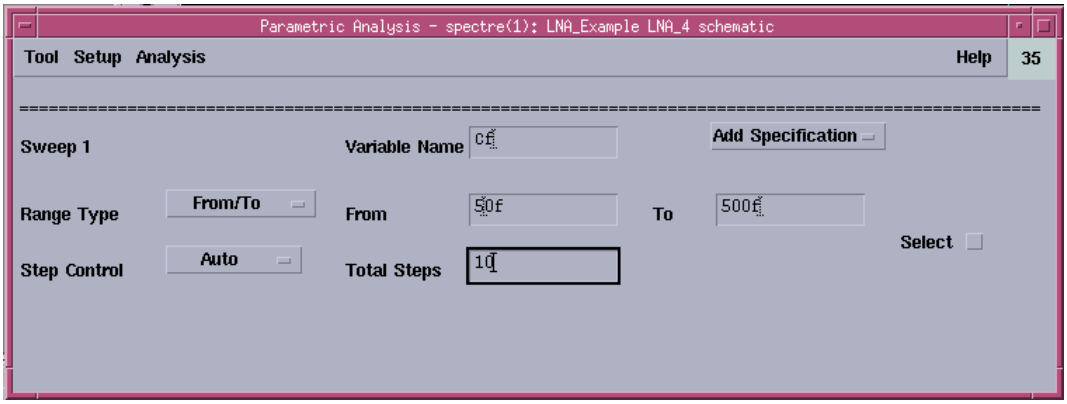
➢ Anallog Design Inviroment windown becomes



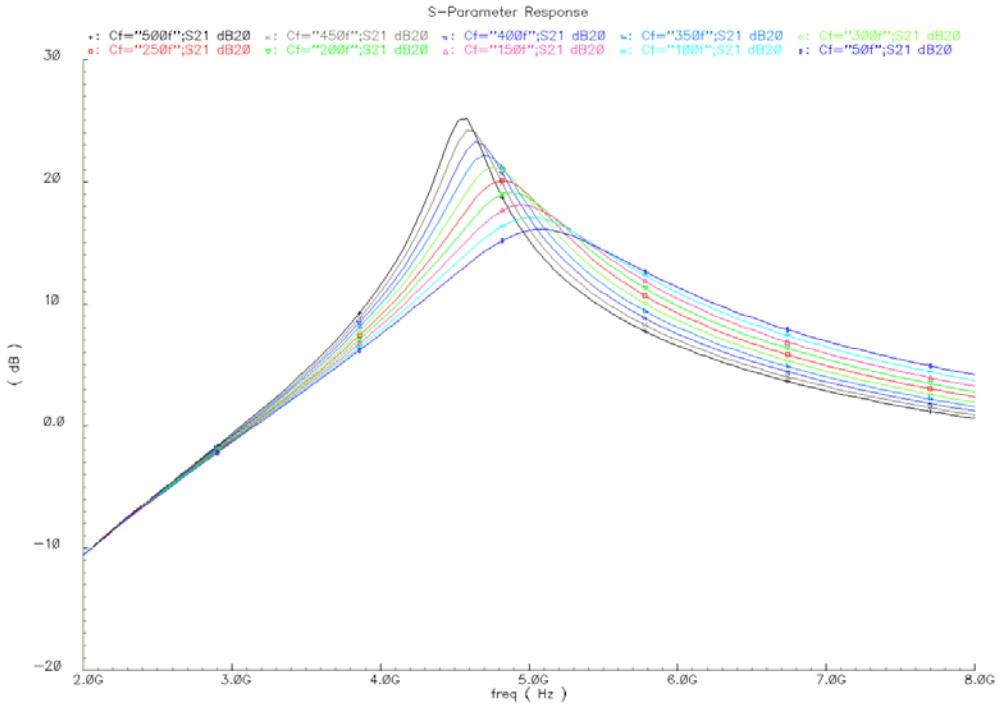
Click Variable→ Copy from cell view



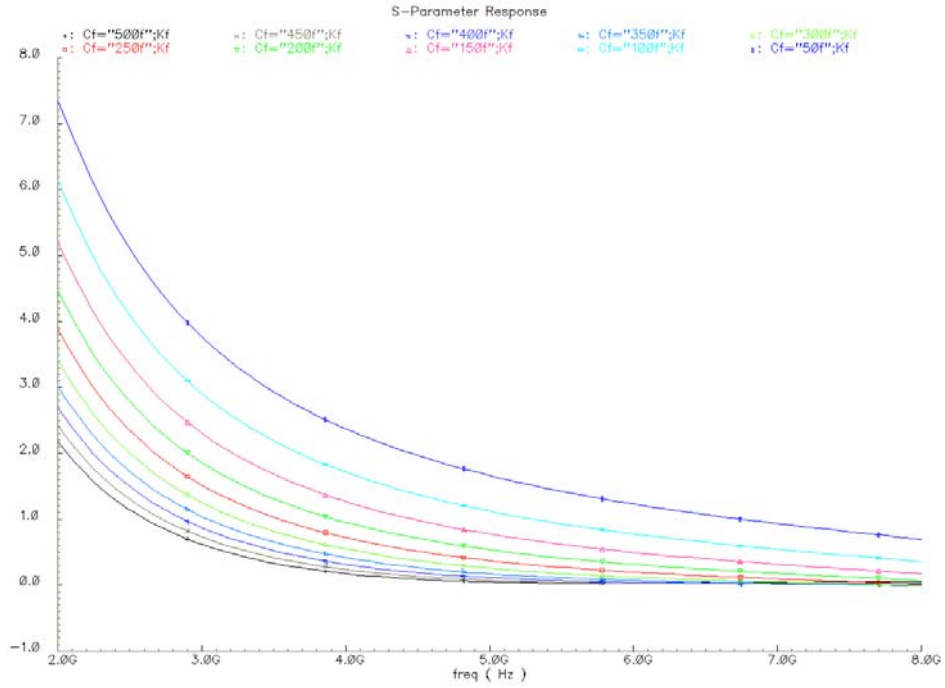
Click *tool* the Parametric Analysis windown will appear. After that we modify it as follows



Click Analysis → Start in order to run the simulation. After simulation, Plot S21, and K-factor we can obtain results as follows



K factor



Considering the value of K factor → choose value of C_f.