目　　录

第一部分. 前　　言

本实验为微电子系专业选修课程《模拟CMOS集成电路设计》的配套实验。本实验围绕如何实现一个给定性能参数要求的简单差分运算放大器而展开。

通过该实验，使得学生能够建立模拟集成电路设计的基本概念，了解设计的基本方法，熟悉模拟CMOS集成电路设计的典型流程，了解在每一个流程中所应用的EDA工具，并能较熟练地使用每个流程对应的设计工具。通过让学生自己分析每个流程中所出现的问题，把课程所学知识联系实际，从而增强学生分析问题、解决问题的能力。

本实验的内容以教材一至十章内容为基础，因此，该实验适合在开课学期的后半部分时间开展。

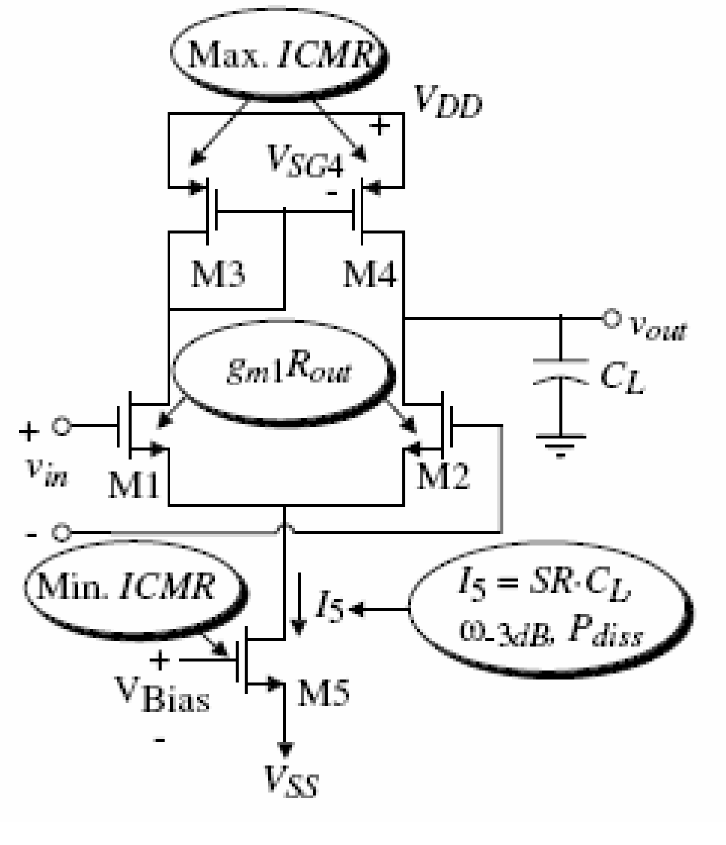
本实验讲义内容安排如下，首先是前言，其次是基础知识，接下来是实际实验内容，具体分成四个过程，最后是附录。建议在实际实验开始之前依次浏览三个附件文档。

第二部分．实验的基础知识

该实验内容所涉及的基础知识包括两部分：电路方面、流程方面和EDA设计工具使用方面。

1．电路有关的基础知识。

该实验是围绕如何实现基于 SMIC 0.18um 工艺下，一个给定性能参数要求的简单差分运算放大器而展开，因此，以电流镜做负载的基本五管差分运算放大器的性能分析是该实验的理论基础。具体内容在讲义以及课件相关章节中有详细介绍。以下用一张图简单重述该电路的有关性能与各元件参数之间的关系分析结论。



相关的设计公式如下：

$$R_{out}=\frac{2}{\left(\lambda_N+\lambda_P\right)I_{SS}}$$

$$A_V=g_{m1}R_{out}$$

$$\varpi_{-3dB}=1/R_{out}C_L$$

$$V_{IC}(\max)=V_{DD}-V_{SG3}+V_{TN1}$$

$$V_{IC}(\min)=V_{SS}+V_{DS5}(sat)+V_{GS1,2}$$

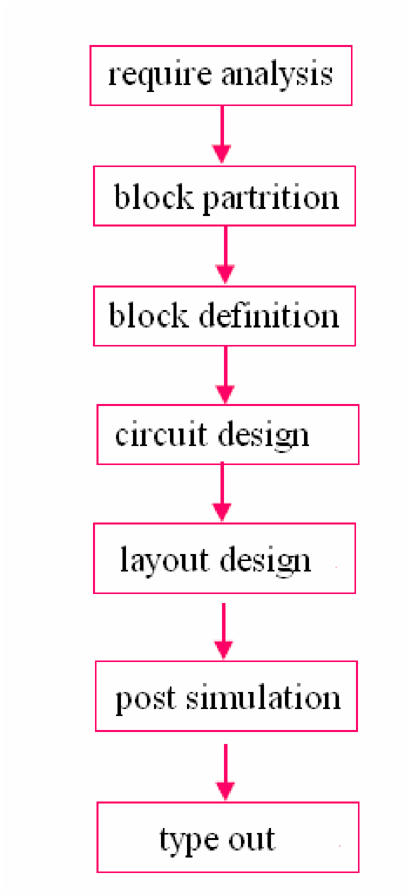
$$SR=I_{SS}/C_L$$

$$P_{diss}=\left(V_{DD}+\left|V_{SS}\right|\right)\times I_D$$

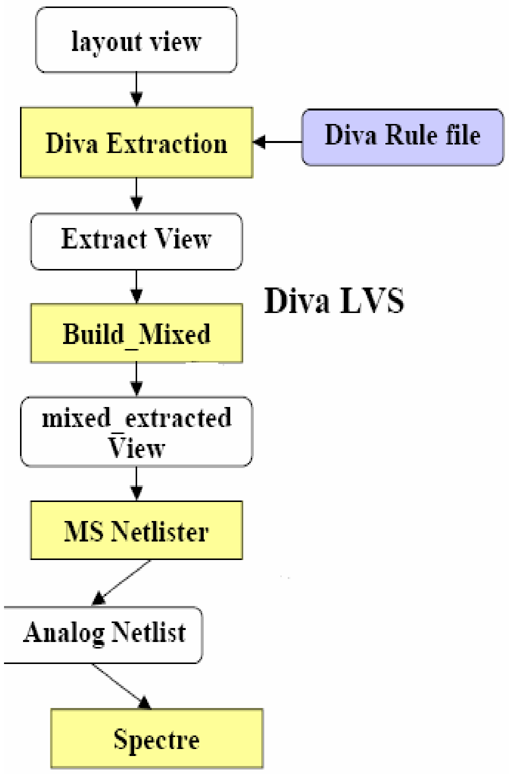
2．流程方面有关的基础知识。

首先，在流程方面，需要掌握基本的流程。针对该实验，简单描述如下。在给定的性能参数要求下，实现以电流镜做负载的基本五管差分运算放大器，首要的任务就是找到每个放大器的性能参数与电路中元件参数之间的关系表达式，根据各个参数之间的关系以及相应表达式，在适当折衷之后，根据给定的参数，逐个确定元件参数，重点是 MOS 管的宽度、长度和偏置电压。然后利用设计工具（实验中采用 cadence virtuoso composer）绘制相应的电路图，检查无误后，生成网表，利用仿真器，进行电路性能的前端仿真（实验中采用 cadence virtuoso analog environment)，保证性能仿真正确；接下来，利用技术文档，在 cadence virtuoso layout editor 环境下进行版图设计，版图设计结束后，进行 DRC(设计规则检查)、ERC(电学规则检查)、Extract(电路图抽取)、LVS(版图与电路图的对比)、寄生参数提取；最后，利用提取的寄生参数，反标到原有电路中，进行再次的性能仿真，通过后 type out。整个流程，描述如下图所示：

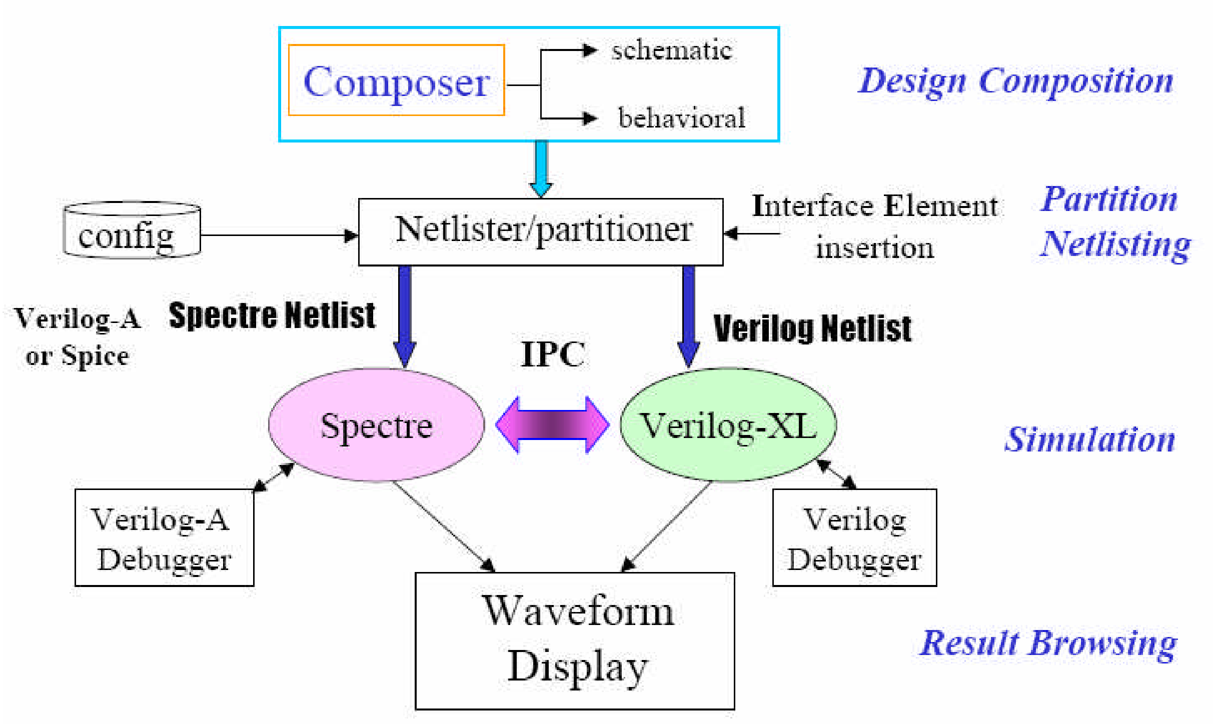
（1）整体：



（3） 后仿真：



（2） 电路设计

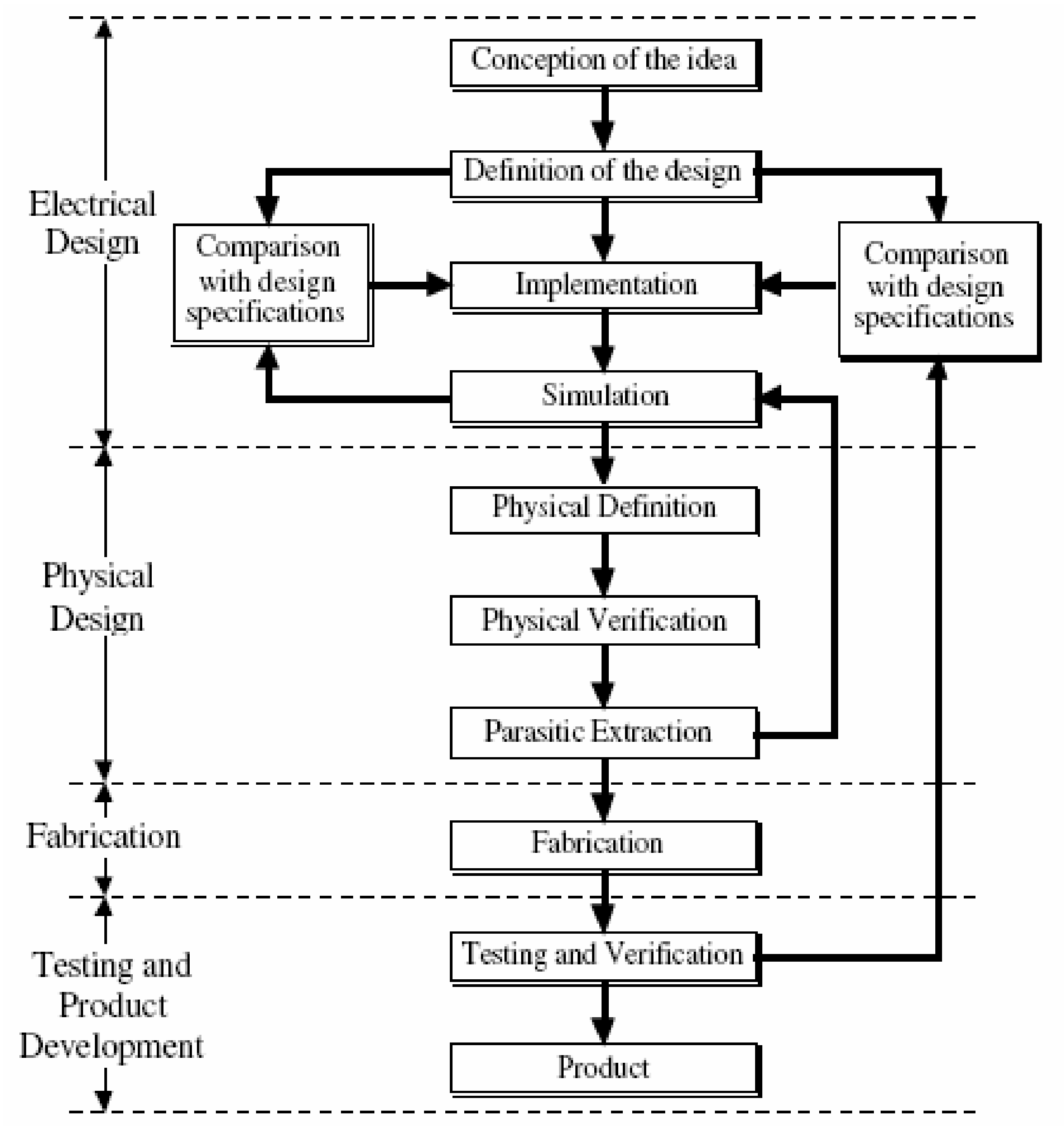


（4）设计整体流程见下一页。

3．EDA 工具使用方面的知识

在设计的每一个阶段，都有相应的 EDA 设计工具，在使用这些工具之前，需要仔细阅读相关的使用手册。本实验手册以附件的形式，提供每个阶段设计工具的简单使用手册，请参阅相关附件。

模拟集成电路设计整体流程



第三部分．实验内容

（一）

cadence virtuoso schematic 电路图绘制

一．实验目的

1． 进一步理解五管基本差分放大器的性能。

2．掌握电路图绘制工具 cadence virtuoso schematic 的使用。

二．实验内容

1．登陆工作站，启动 cadence custom IC design tools 环境。

具体操作如下：

（1） 用学生密码 55555 登录 PC；

（2） 启动 windows 系统后，双击打开 hummingbird connectivity;

（3） 双击打开 exceed ，出现所有能建立连接的工作站列表；

（4） 选择一个工作站，建立连接；

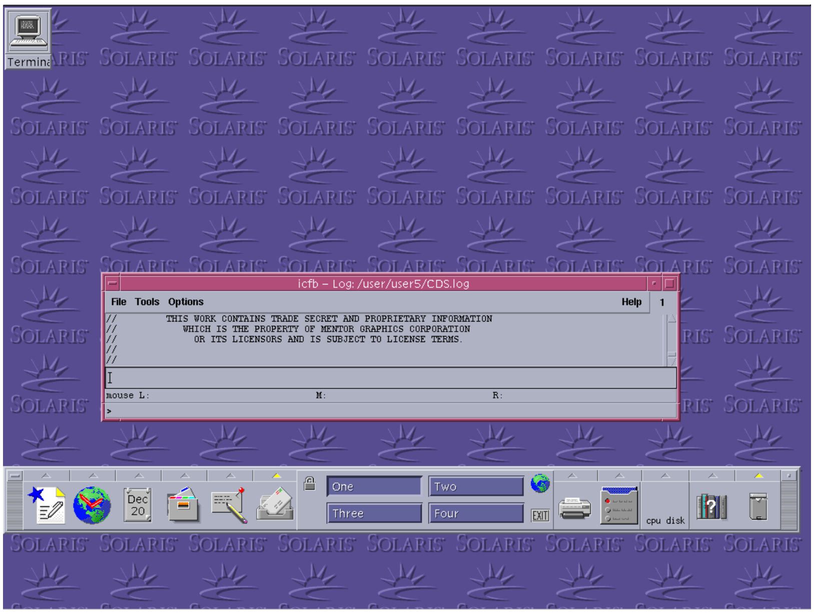
（5） 用 student 帐户和 55555 密码登录 solaris 系统；

（6） 在 solaris 系统 IDE 桌面空白处单击右键，弹出菜单，选择 tools->terminal ；

（7） 在打开的 terminal 中，敲入 cds.setup ，enter；

（8） 敲入 icfb& enter；

（9） Cadence design tools 环境启动，出现 cadence 的 CIW 对话框。 如图



```
//         THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
//            WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION
//             OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.
//
//
mouse L:                          M:                          R:
>
```

2. 运放电路手工设计

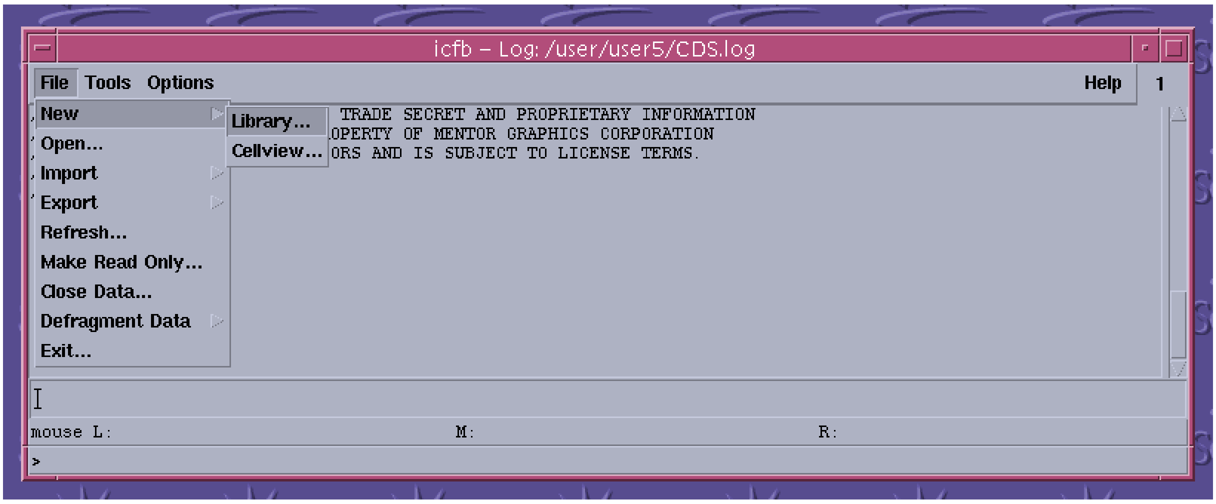
按照给定的性能参数和典型工艺参数，手工计算五管基本差分运算放大器的元件参数，设计好该差分运算放大器。参数要求如下：

（1） 要求实现的参数：gain ,slew rate ,bandwidth ,ICMR ,power dissipation

(2) 已知的典型工艺参数：threshold voltage, channel length, μ_n μ_p C_{ox} ,VDD

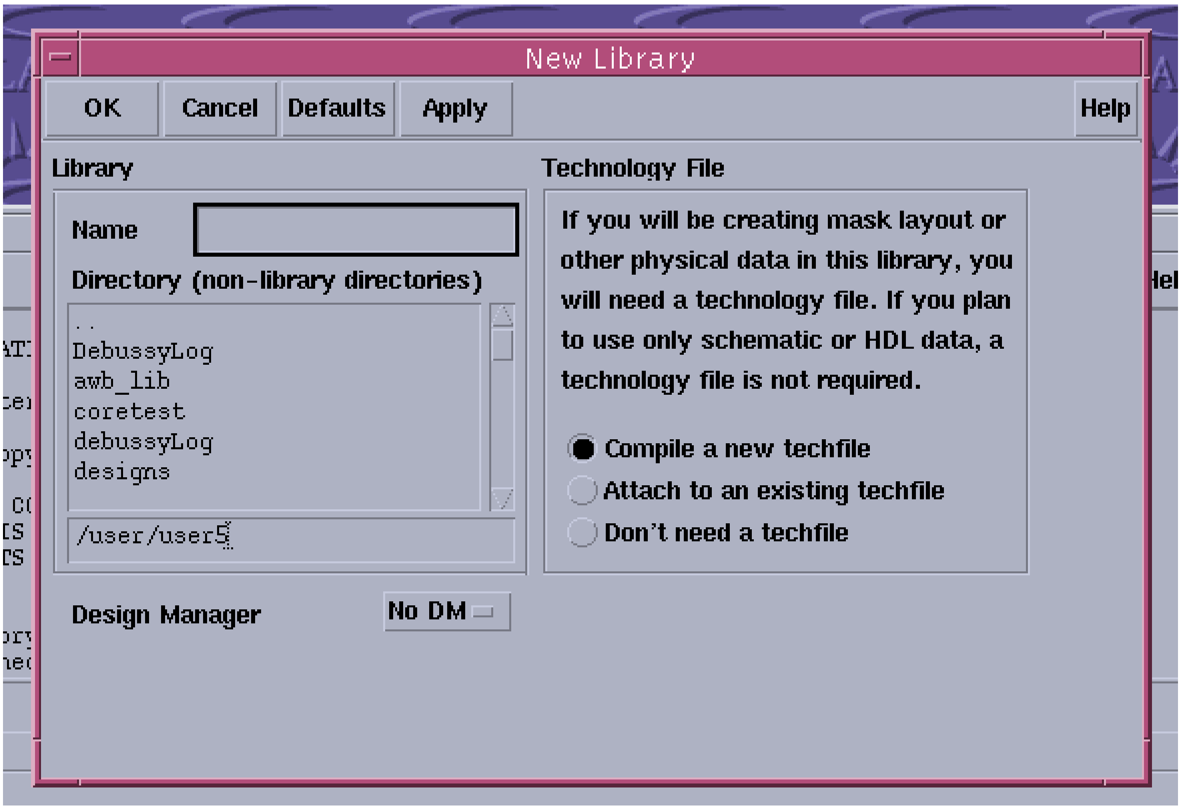
3.电路图绘制前的准备工作

（1）在 cadence CIW 对话框中，创建新的 library，用以保存所有与该设计相关的文档和数据。点击 file->new->library 如图所示：



```
 TRADE SECRET AND PROPRIETARY INFORMATION
OPERTY OF MENTOR GRAPHICS CORPORATION
ORS AND IS SUBJECT TO LICENSE TERMS.
mouse L:                    M:                    R:
>
```

(2)新建 library，在如图所示对话框中填入相应的内容：



Library

Name

Directory (non-library directories)

..
DebussyLog
awb_lib
coretest
debussyLog
designs

/user/user5

Technology File

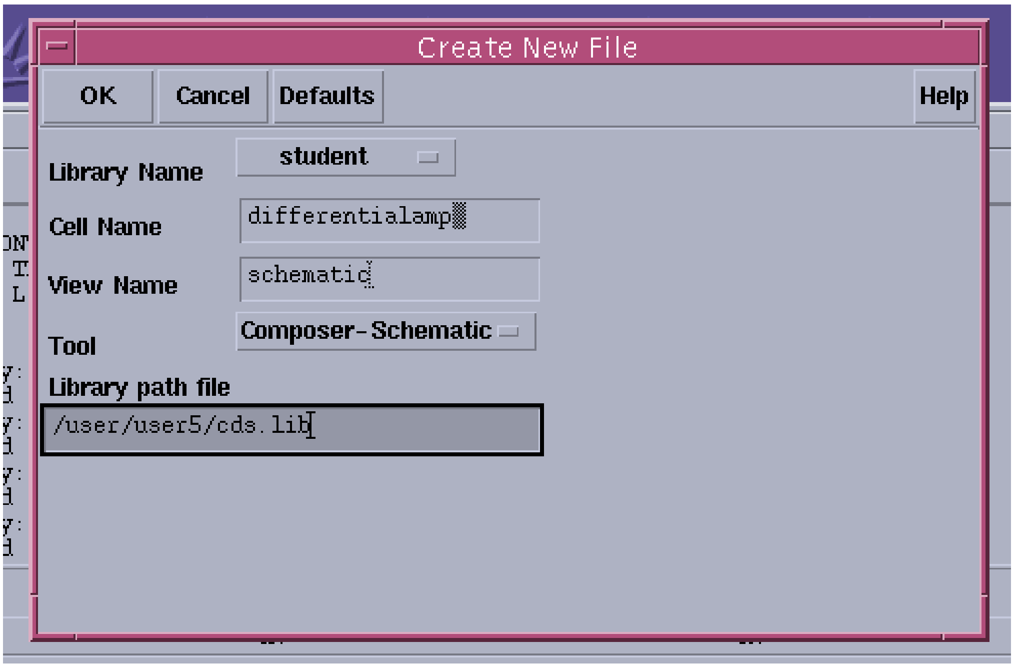
If you will be creating mask layout or other physical data in this library, you will need a technology file. If you plan to use only schematic or HDL data, a technology file is not required.

● Compile a new techfile
○ Attach to an existing techfile
○ Don't need a techfile

Design Manager: No DM

在默认的路径下自己命名 library name，右边技术文件，在这个实验中我们暂时不使用技术文档，选择 “don’t need a techfile”. 点击 ok ,返回到 CIW 对话框；

（3）新建一个 cellview ,单击 file->new->cellview,出现如图所示对话框：



Library Name: student

Cell Name: differentialamp

View Name: schematic

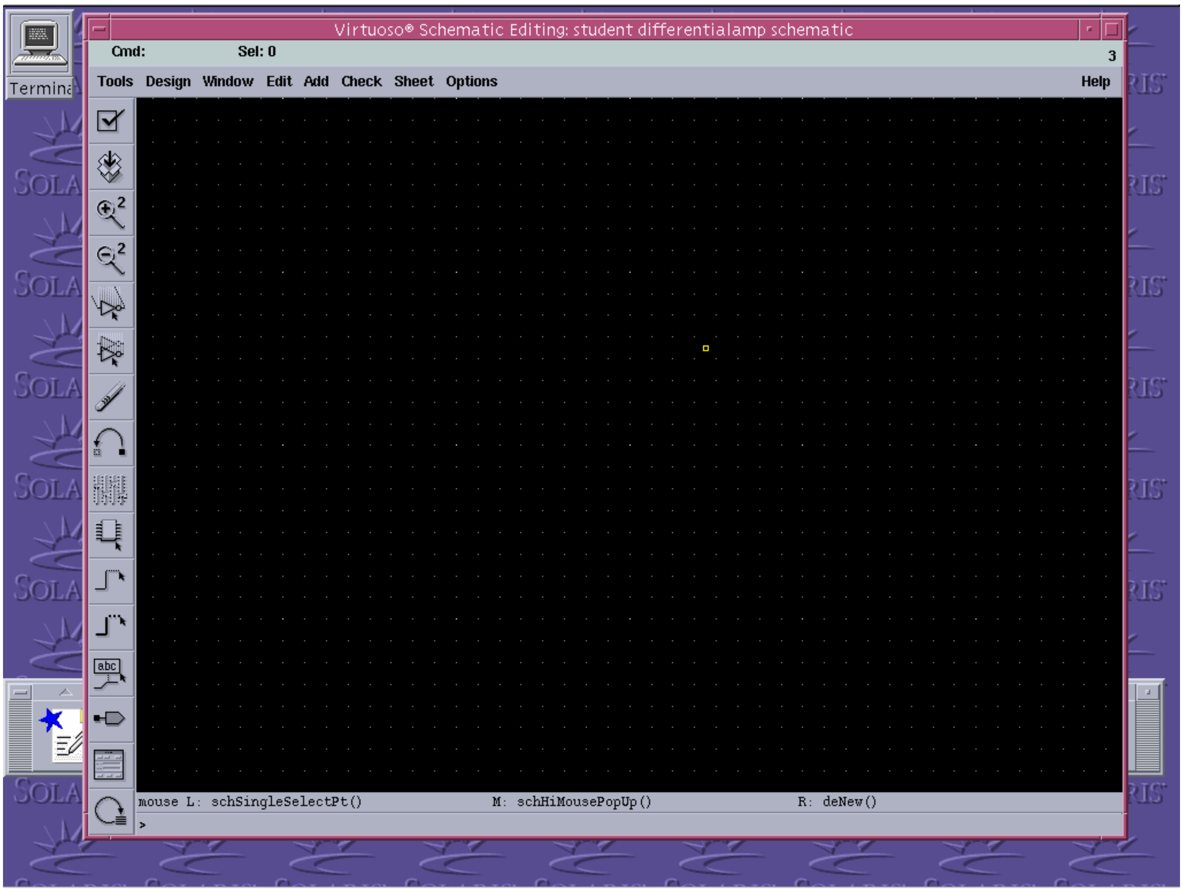
Tool: Composer-Schematic

Library path file

/user/user5/cds.lib

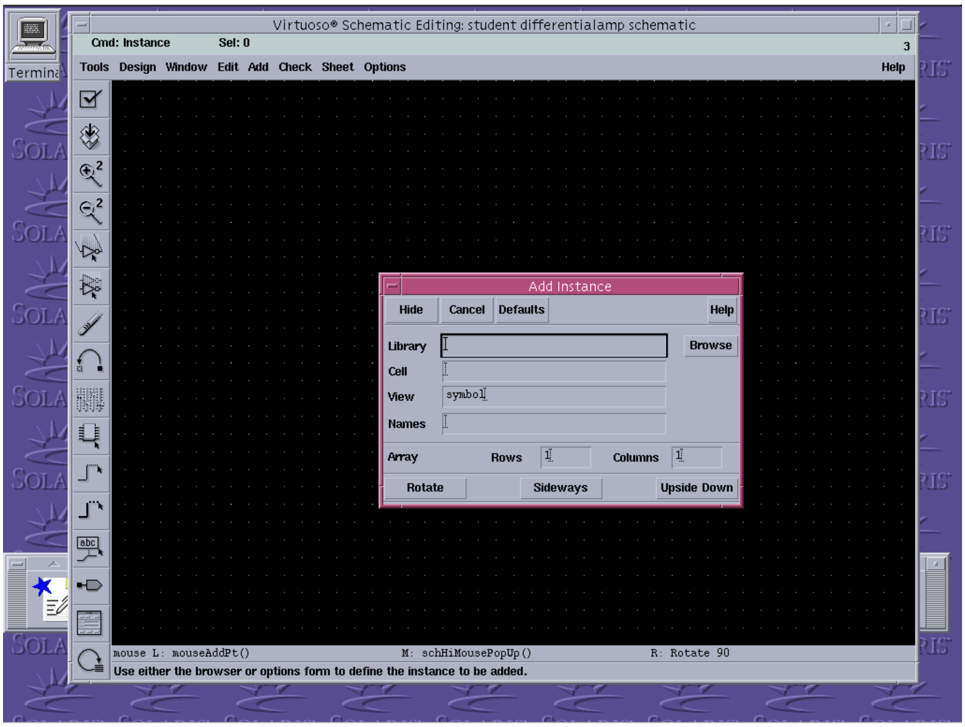
在 library name 选项，选择刚才自己命名的 library ； tool 选项下选择

composer-schematic， 则 view name 自动定义为 schematic，自己命名 cell name ，例如 differentialamp ，点击 ok， 出现 schematic page,如图所示，在此 page 上，即可绘制所设计的电路图。


Virtuoso® Schematic Editing: student differentialamp schematic
Cmd:
Sel: 0
3
Tools Design Window Edit Add Check Sheet Options
Help
Terminal
mouse L: schSingleSelectPt()
M: schHiMousePopUp()
R: deNew()
>

（4）添加 nmos-transistor 和 pmos-transistor

单击 add->instance ,出现如图所示“add instance”对话框。


Virtuoso® Schematic Editing: student differentialamp schematic

Cmd: Instance Sel: 0

Tools Design Window Edit Add Check Sheet Options Help
Add Instance
Hide Cancel Defaults Help
Browse
Rotate Sideways Upside Down

Library

Cell

View symbol

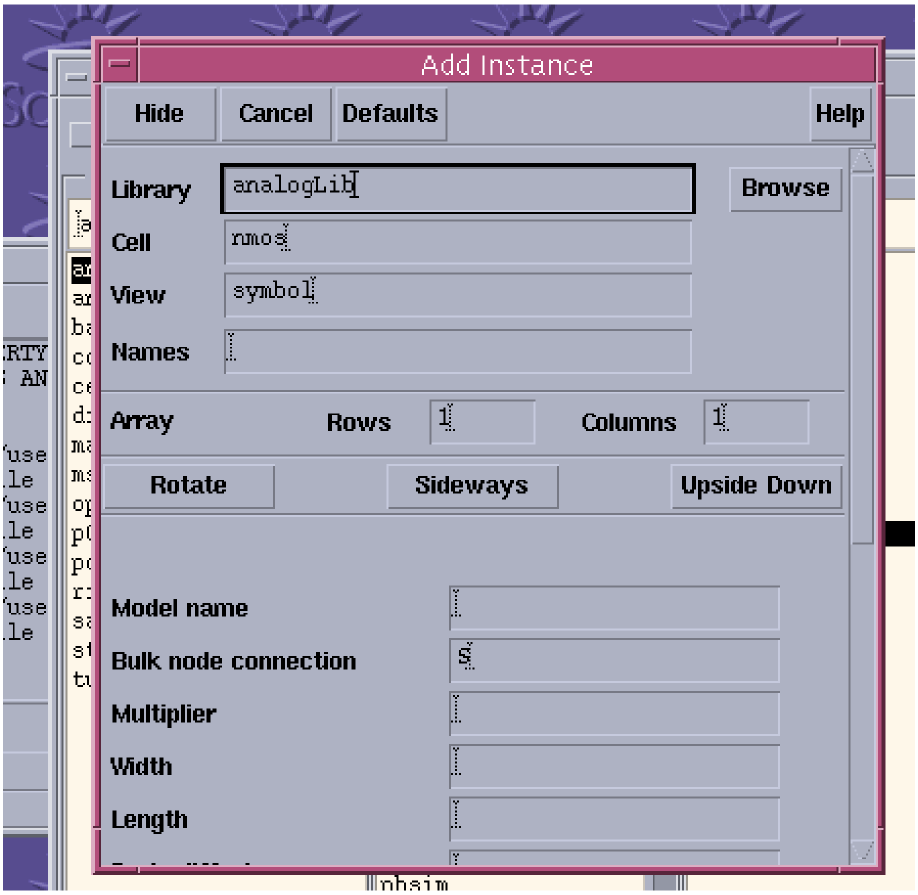
Names

Array Rows 1 Columns 1

mouse L: mouseAddPt() M: schHiMousePopUp() R: Rotate 90

Use either the browser or options form to define the instance to be added.

在此对话框中，选择 library 为 analoglib，cell 为 nmos，view 为 symbol,name 自己定义，之后，对话框自动扩展为如图，在此对话框中，需要确定 length and width.



Library analogLib

Cell nmos

View symbol

Names

Array Rows 1 Columns 1

Model name

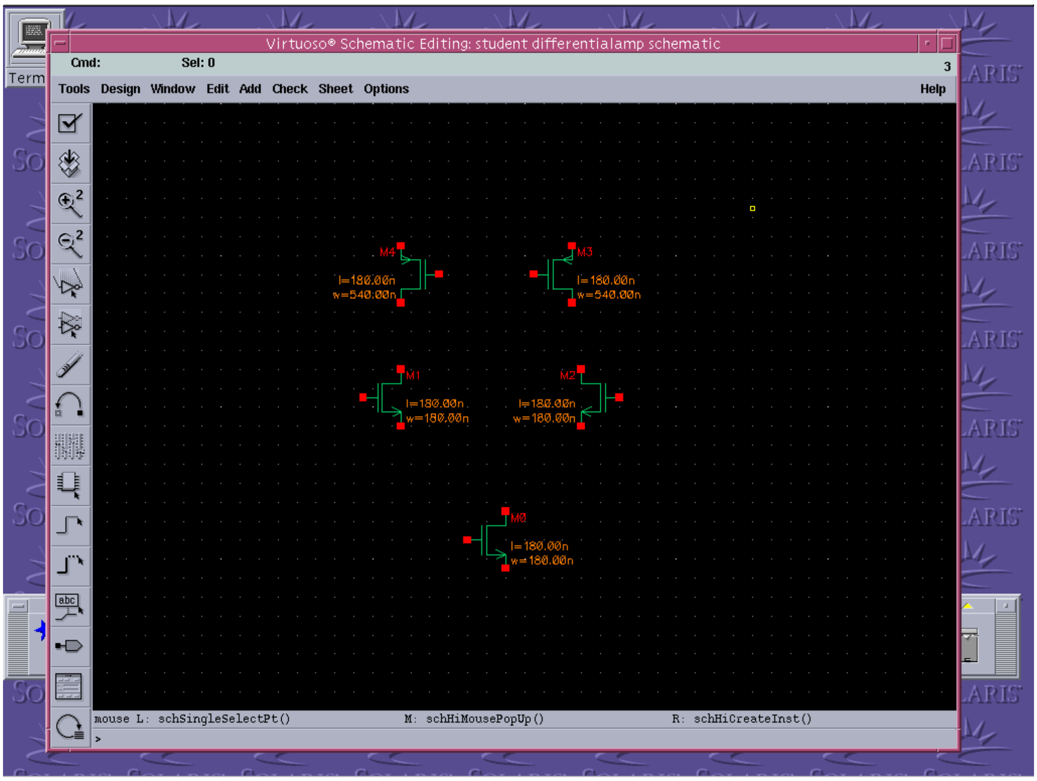
Bulk node connection S

Multiplier

Width

Length

Model name 由性能模拟时采用的 model 文件来决定。SMIC model 文件中定义的 nmos model name 为 n18 ，pmos model name 为 p18 。之后，在 schematic page 上点击，即可把该元件添加到 page 上。如图所示：


Virtuoso® Schematic Editing: student differentialamp schematic

Cmd: Sel: 0 3

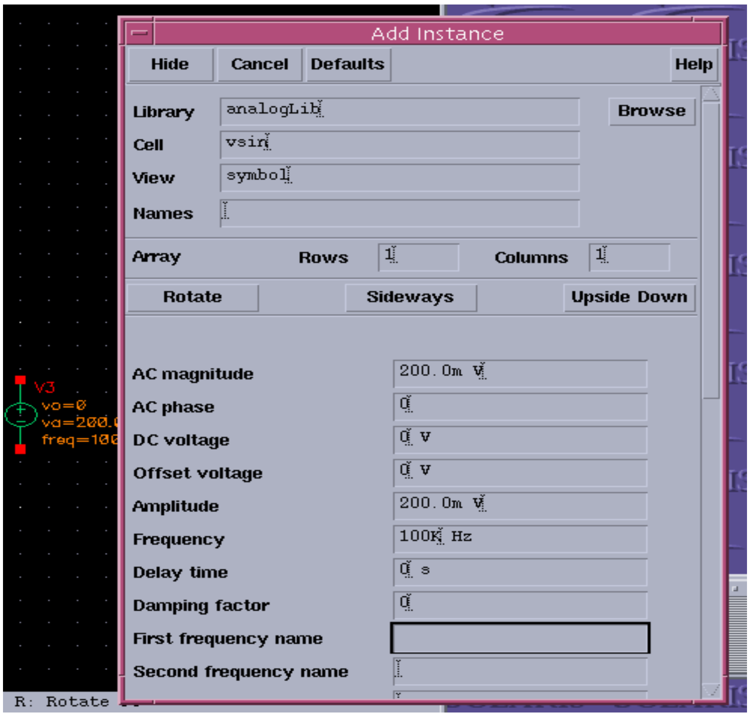
mouse L: schSingleSelectPt() M: schHiMousePopUp() R: schHiCreateInst()

>

（5）添加其他元件

同理，单击 add->instance ,选择所需的元件，即可添加到 page 上，如图所示

添加正弦驱动信号，



Library analogLib

Cell vsin

View symbol

Names

Array Rows 1 Columns 1

AC magnitude 200.0m V

AC phase 0

DC voltage 0 V

Offset voltage 0 V

Amplitude 200.0m V

Frequency 100K Hz

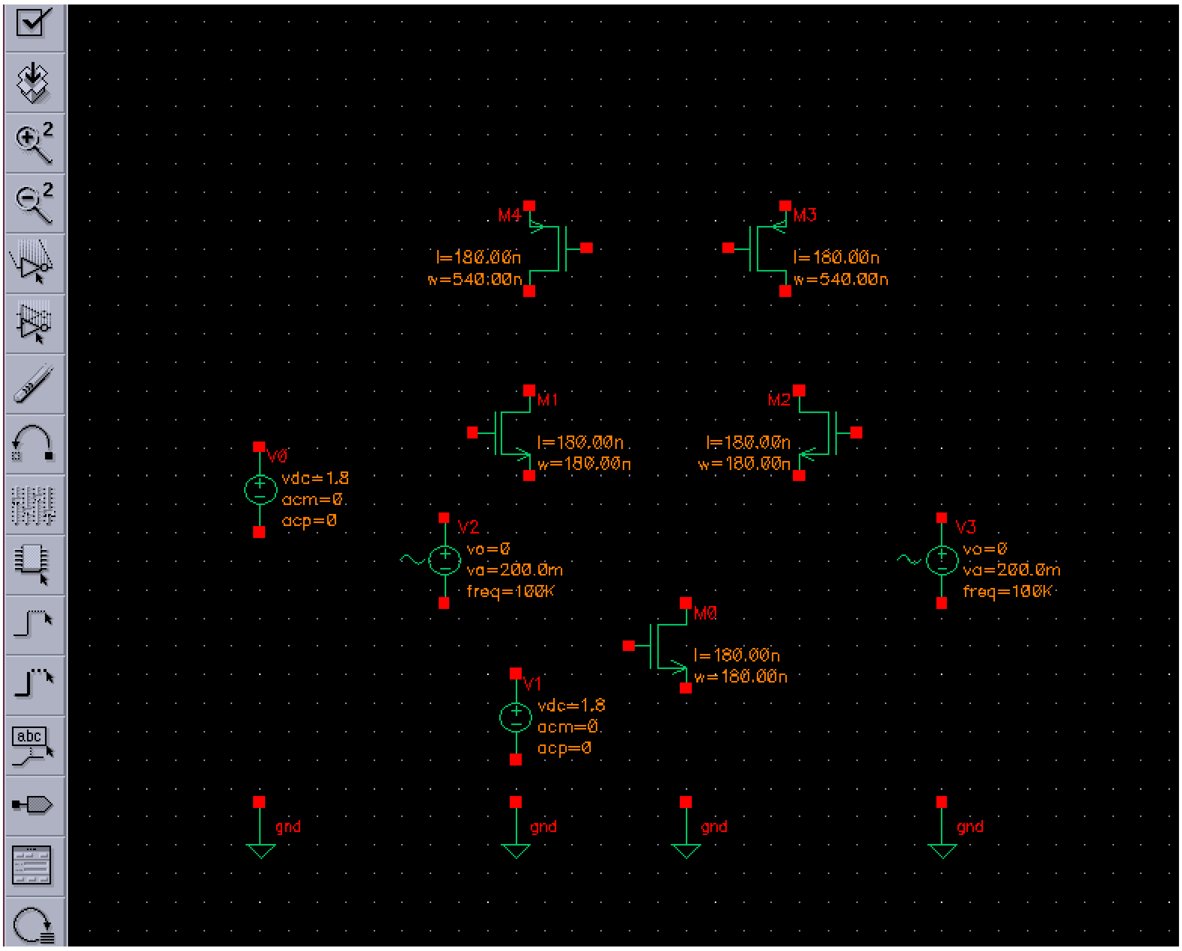
Delay time 0 s

Damping factor 0

First frequency name

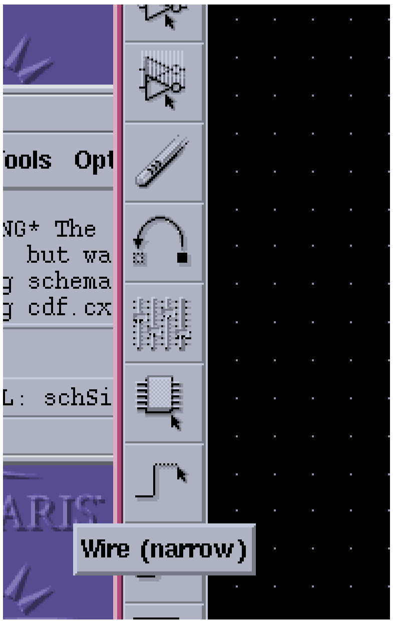
Second frequency name

添加直流电源，添加参考地。完成之后如图所示。

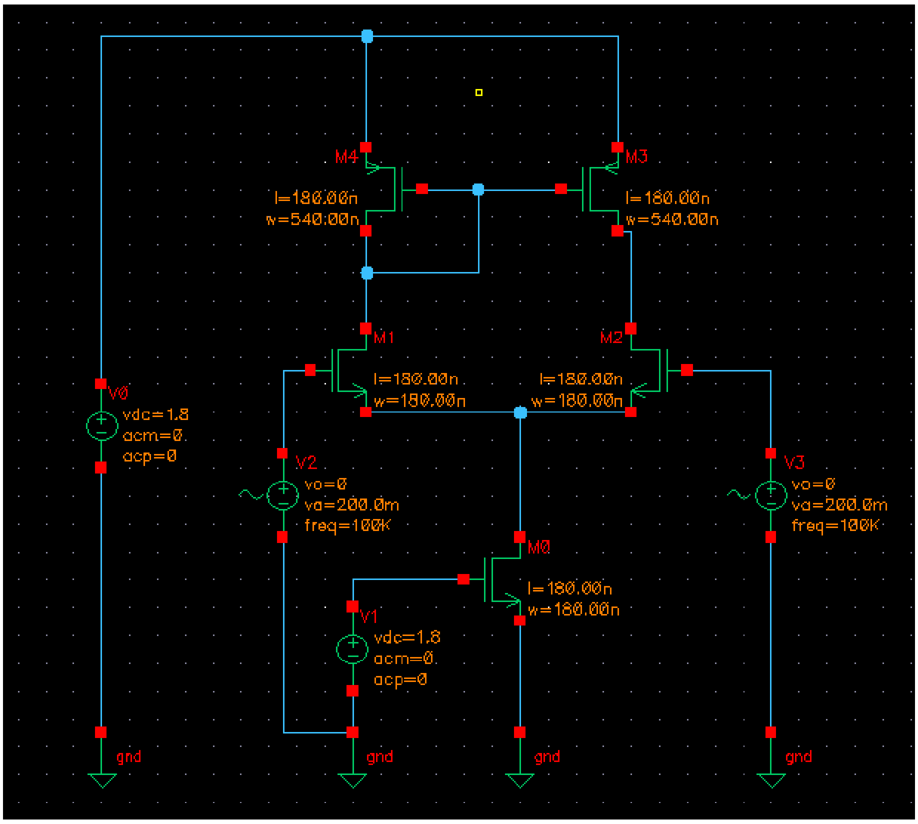


（6）连接元器件

单击左边工具栏中的细连线

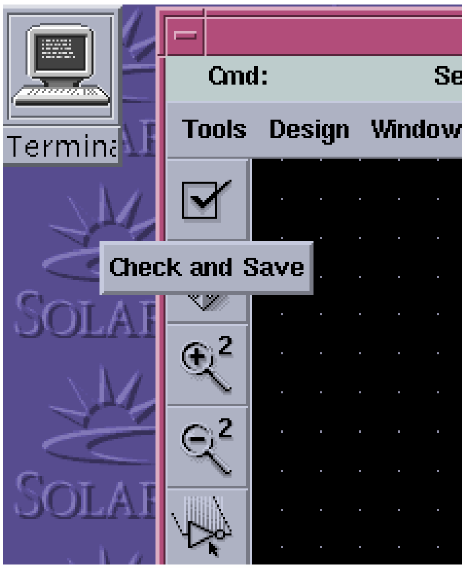


按照所设计的电路，连接各个元件。完成连接后的电路如图所示：



（7）检查连接，并且保存设计

单击左边工具栏里“ check and save”，如图所示：



至此，所设计的五管简单差分运算放大器的电路绘制结束。

三．思考题

1．电路图绘制中，GND 的物理意义是什么？

2．如何把实验中差放的输入信号替换成管脚？

3．电路图绘制后，check and save 命令执行后出现错误，从哪儿可以得到错误的相关信息？

第三部分 实验内容

（二）

利用 Spectre /HSpice 进行性能模拟

一．实验目的

1．掌握电路性能仿真工具 Spectre /HSpiceD 的使用。

2．进一步理解五管基本差分放大器的性能。

二．实验内容

1．模型文件的准备

Spectre 仿真器所用的 MOS 模型文件后缀名为.scs；hspice 仿真器所用的 MOS 模型文件后缀名为.mdl。现有的 SMIC 库中提供的是用于 hspice 的模型文件，并且提供了“TT、FF、SS”三种，实验中采用 TT。实验中该模型文件所在位置的绝对路径如下：/data/smic/ms018_v1p6.mdl

2.打开实验一中的电路图

（1）登陆到工作站 solaris 系统之下，

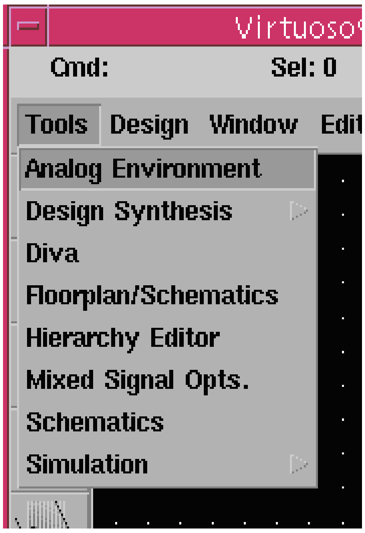
（2）运行 icfb& ,enter,进入 cadence 设计环境。

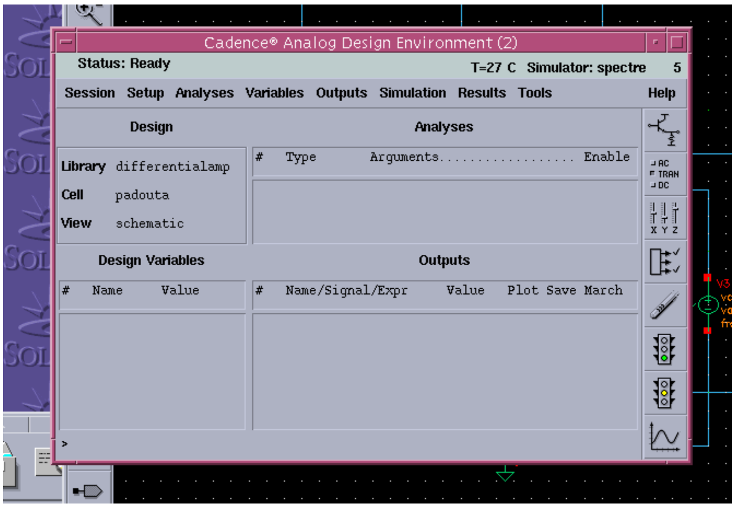
（3）在 CIW 窗口 file->open，选择实验一中设计的电路图，打开。

（4）运行“check and save”,确保没有任何错误。

3．进入性能模拟环境

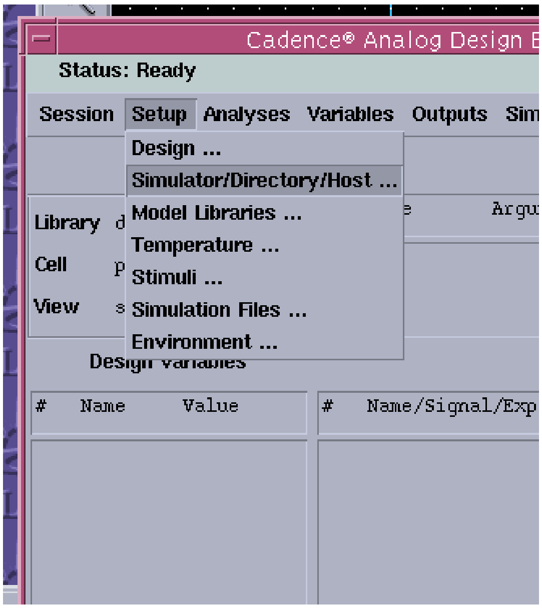
在 schematic page 页面下，单击 tools->analog environment ,出现 cadence analog design environment 性能模拟页面，分别如下图所示:

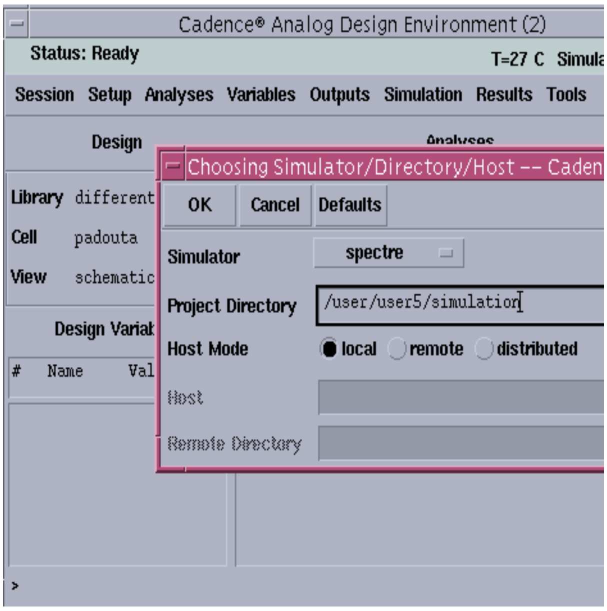




4.选择仿真器

（1）在 cadence analog design environment 页面下，单击 setup -> simulator/directory/host 命令，出现仿真器选择界面，分别如图：





Simulator spectre

Project Directory /user/user5/simulation

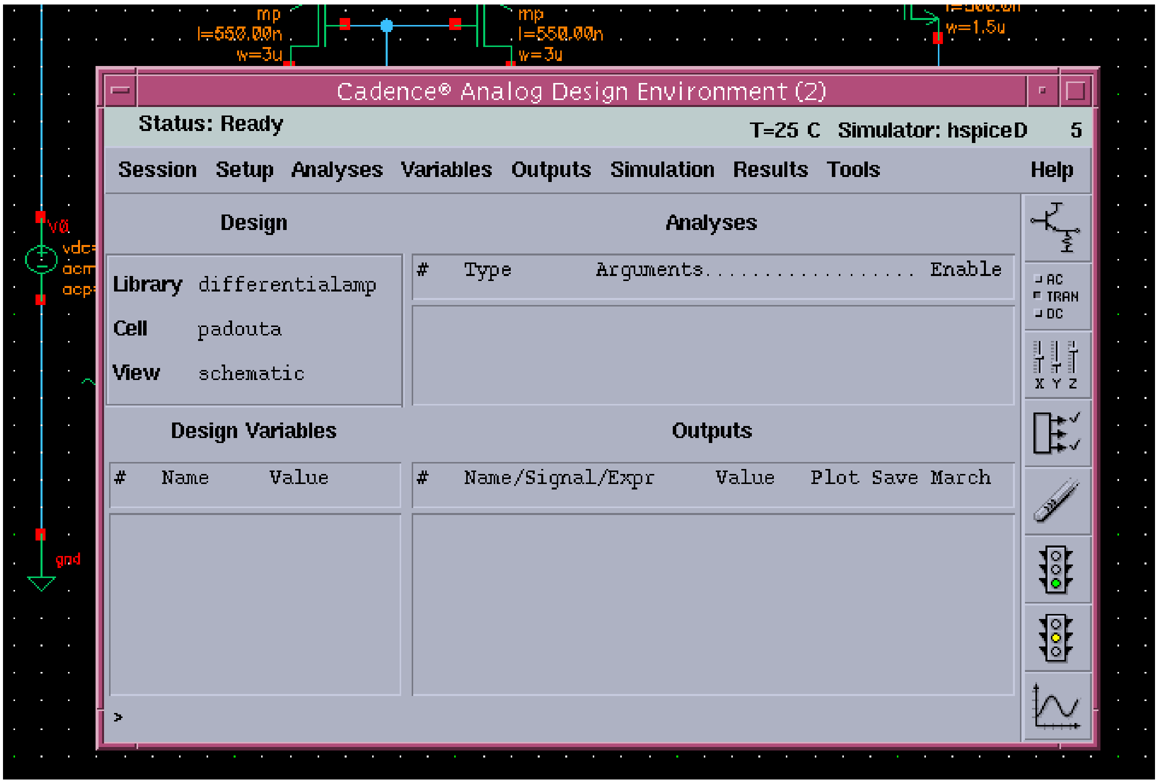
Host Mode ● local ○ remote ○ distributed

Host

Remote Directory

（2）在 simulator 选择项里，罗列了所有能用的仿真器，选择 hspiceD，单击 OK，运行后出现如图所示性能模拟页面。此图表示，目前选择的性能仿真器为 hspiceD，性能模拟的环境温度为 T=25 ℃ 。

（3）仔细察看该页面所描述的相关信息。


Cadence® Analog Design Environment (2)
Session Setup Analyses Variables Outputs Simulation Results Tools Help
Design
Analyses
# Type Arguments................. Enable
Design Variables
Outputs
# Name Value
# Name/Signal/Expr Value Plot Save March
AC
TRAN
DC
X Y Z
mp
l=550.00n
w=3u
w=1.5u
V0
gnd

Status: Ready

T=25 C Simulator: hspiceD 5

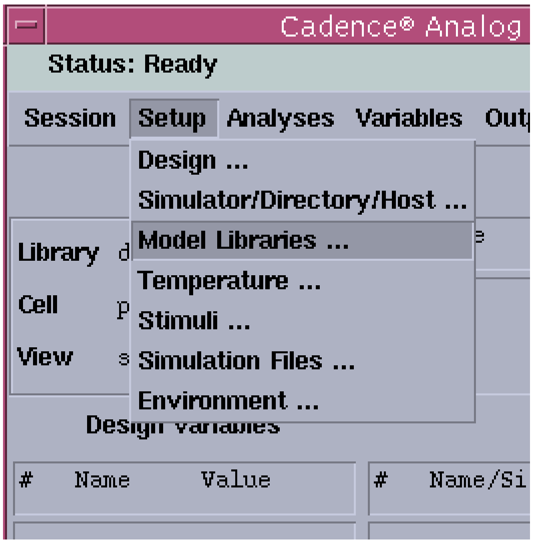
Library differentialamp

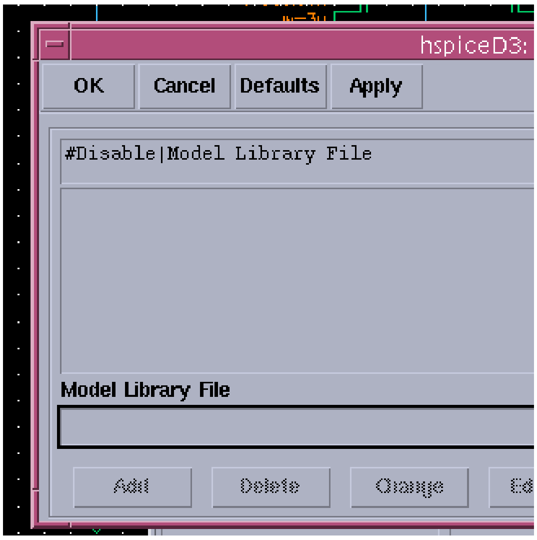
Cell padouta

View schematic

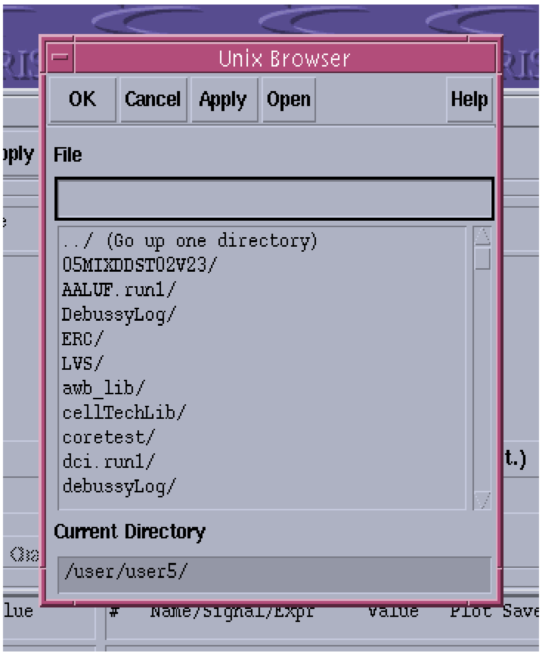
5. 选择电路中元器件的模型

(1)实验中主要是选择 NMOS 和 PMOS 的模型。在上述页面下，单击 setup -> model libraries ，出现模型选择窗口，分别如图所示：





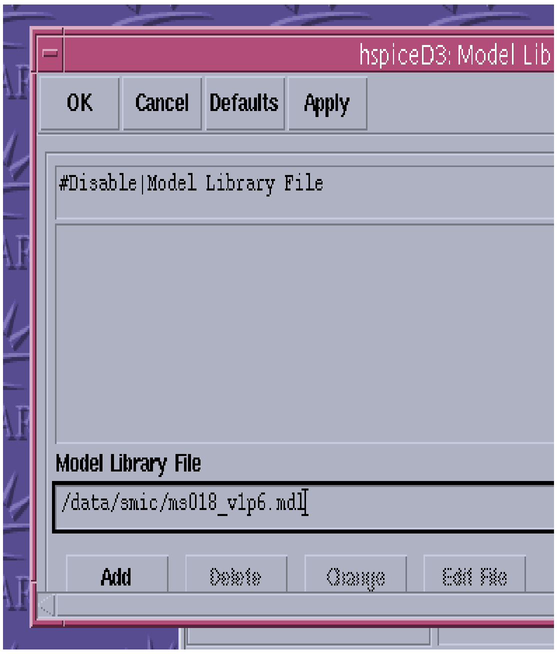
(2)单击模型选择窗口右下角 browse 按钮 ，出现 unix browser 窗口，在该窗口中，找到模型文件位置的绝对路径，/data/smic/ms018_v1p6.mdl 单击 ok，



File

```
../ (Go up one directory)
05MIXDDST02V23/
AALUF.run1/
DebussyLog/
ERC/
LVS/
awb_lib/
cellTechLib/
coretest/
dci.run1/
debussyLog/
```

Current Directory: /user/user5/



#Disable|Model Library File

Model Library File: /data/smic/ms018_v1p6.mdl

（3）依次单击 add — apply - ok，模型文件选择完成，返回到 cadence analog design environment 界面。

6．选择激励源

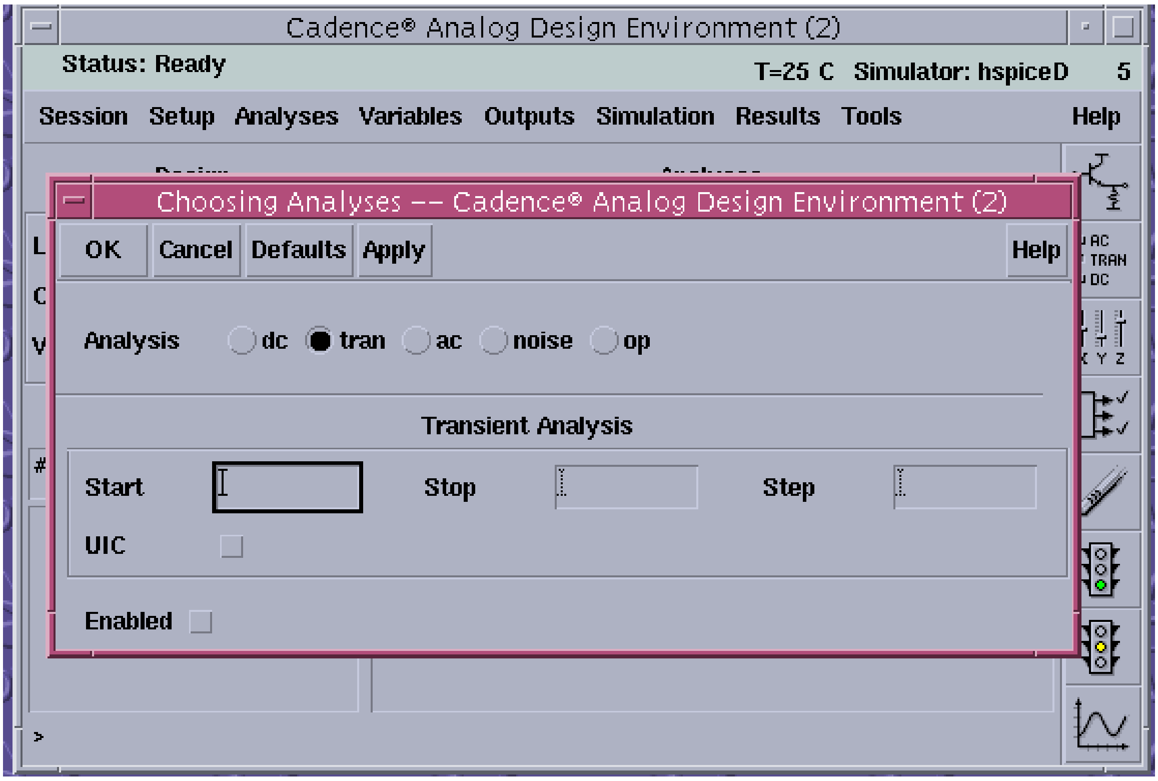
（1） 在 cadence analog design environment 界面，单击菜单 setup-> stimuli 或者单击 setup -> stimuli file ，可以从外部导入激励源，需要注意的是该操作对应于输入信号在 schematic 中是用 input 类型的 pin 表示。

（2）本实验中采用直接在 schematic 中接入输入信号，因此无需在施加激励源。

7．选择性能模拟的类型

（1）在 cadence analog design envrionment 界面下单击菜单 analysis -> choose，出现 hspiceD 所提供的分析类型列表，如图所示

（2）hspiceD 提供了共 5 中分析类型，依次为 dc(直流特性分析)、tran（瞬态响应分析）、ac（交流特性分析）、noise（噪声特性分析）和 op（工作点分析）。期中 op 为每次模拟都必须先完成的性能模拟。



Cadence® Analog Design Environment (2)

Status: Ready T=25 C Simulator: hspiceD 5

Choosing Analyses -- Cadence® Analog Design Environment (2)

Analysis ○ dc ● tran ○ ac ○ noise ○ op

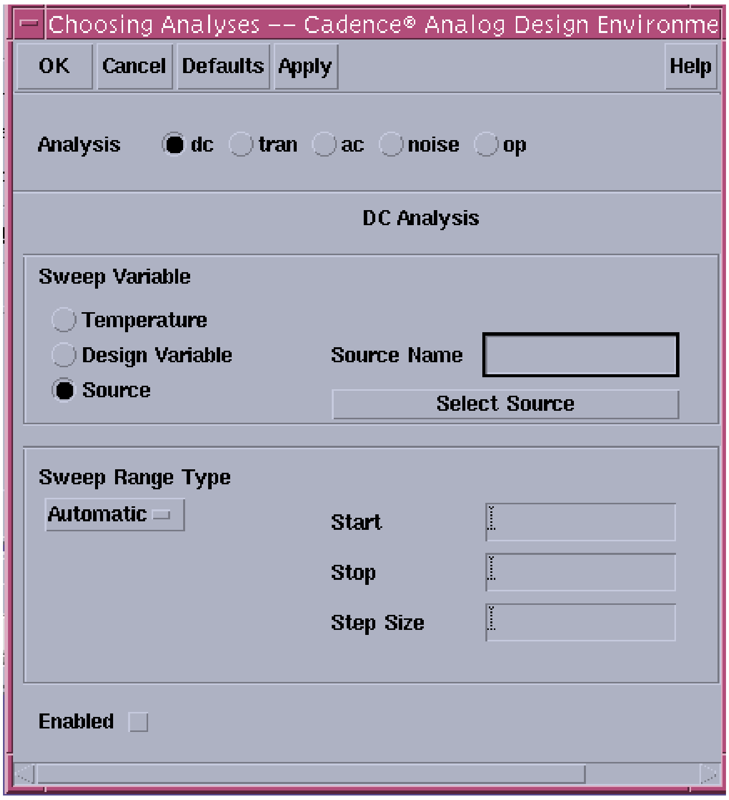
Transient Analysis

Start Stop Step

UIC □

Enabled □

（3）每种分析的窗口以及描述分别图示如下：



Choosing Analyses -- Cadence® Analog Design Environme

Analysis ● dc ○ tran ○ ac ○ noise ○ op

DC Analysis

Sweep Variable

○ Temperature

○ Design Variable

● Source

Source Name

Sweep Range Type

Automatic

Start

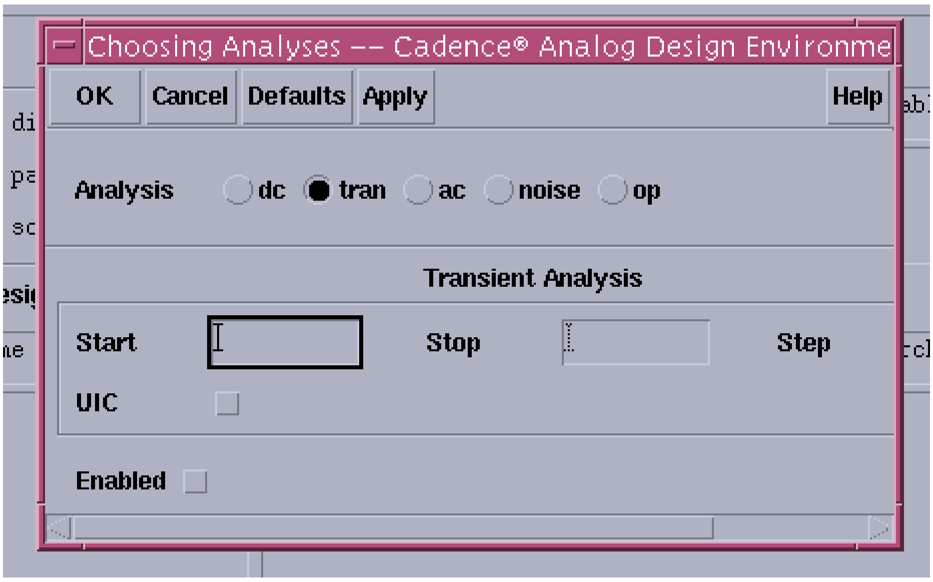
Stop

Step Size

Enabled □

a. 直流分析：包括静态工作点分析以及参数扫描分析。静态点分析由默人包含的 op 分析完成。参数扫描是分析电路某个参数随着电路中某个直流参数变化而变化的一种分析。在该窗口中，可以选择扫描参数的类型、选择要扫描的参数、确定该扫描参数的扫描范围以及扫描的步长。

b. 瞬态响应分析：



Analysis ○ dc ● tran ○ ac ○ noise ○ op

Transient Analysis

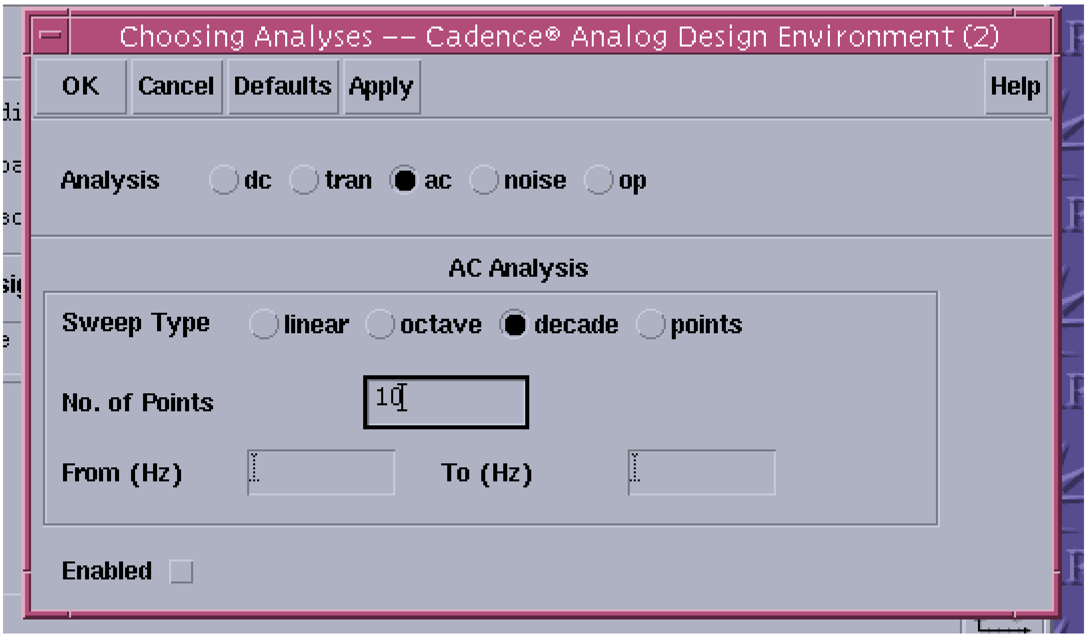
Start Stop Step

UIC □

Enabled □

该类型分析主要是分析电路的性能随着时间如何改变。在该类型的分析中，只需要确定开始时间、终止时间以及时间步长。

c.交流分析



Analysis ○ dc ○ tran ● ac ○ noise ○ op

AC Analysis

Sweep Type ○ linear ○ octave ● decade ○ points

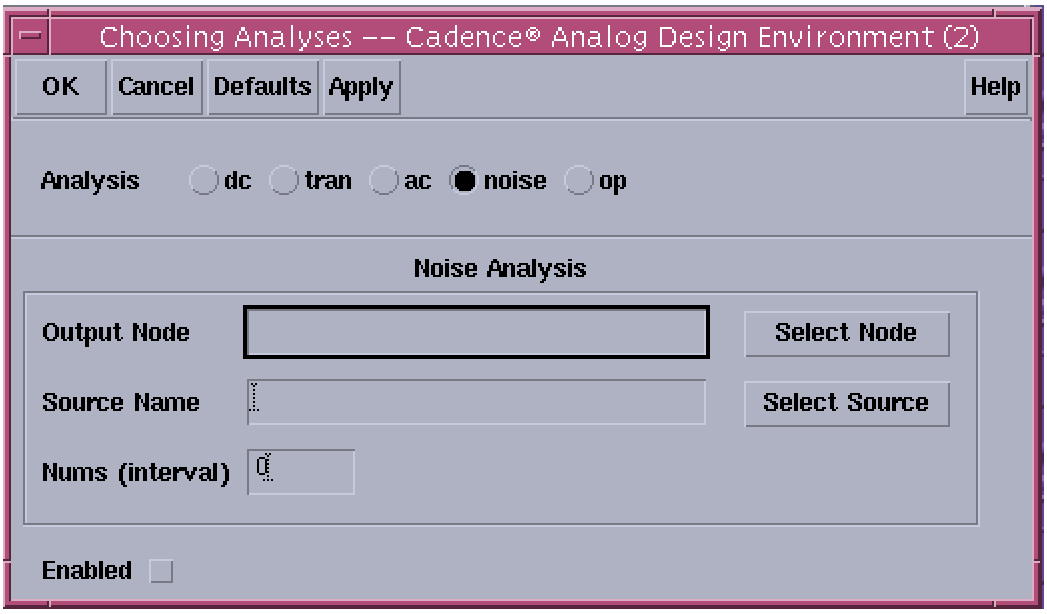
No. of Points 10

From (Hz) To (Hz)

Enabled □

该类型分析是分析电路的性能与交流激励源的频率之间的关系。采用该分析类型时，电路图中必须包含有至少一个交流源。在该类型分析中，首先需要确定扫描的类型，提供类型依次为 频率线性增加、频率八倍程增加、频率十倍程增加和点选；其次需要确定每步长中选取的点的个数；最后，需要确定扫描的开始频率和终止频率。

d. 噪声分析



Analysis ○ dc ○ tran ○ ac ● noise ○ op

Noise Analysis

Output Node

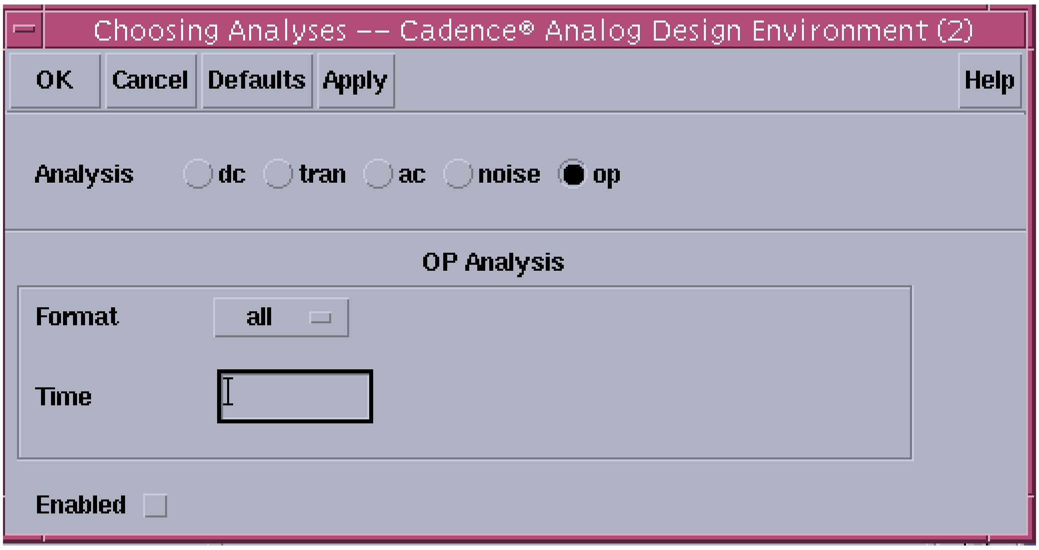
Source Name

Nums (interval) 0

Enabled □

该类型分析中，只需确定输出的节点和确定源即可。

f. 工作点分析



Analysis ○ dc ○ tran ○ ac ○ noise ● op

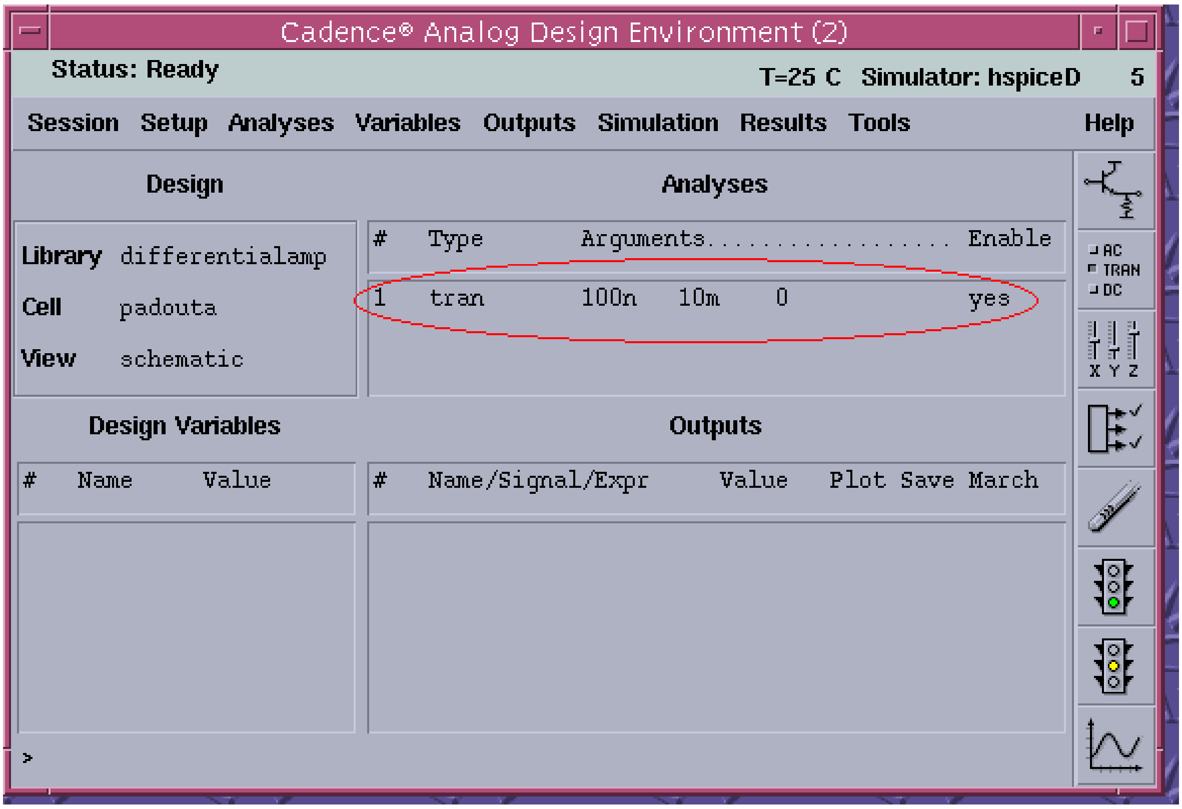
OP Analysis

Format all

Time

Enabled □

（4）在实验中，选择 tran 即瞬态响应分析。并且确定开始时间为 0s，终止时间根据电路中接入的交流信号源的频率来确定，暂时选择 10ms ，步长选择为 100ns。单击 OK，此时该分析类型以及相关设置完成，并且显示在 candece analog design environment 窗口中，如图所示：


Cadence® Analog Design Environment (2)
Status: Ready
T=25 C Simulator: hspiceD 5
Session Setup Analyses Variables Outputs Simulation Results Tools Help
AC
TRAN
DC
X Y Z
>

Design

Library differentialamp

Cell padouta

View schematic

Analyses

#	Type	Arguments.................			Enable
1	tran	100n	10m	0	yes

Design Variables

#	Name	Value

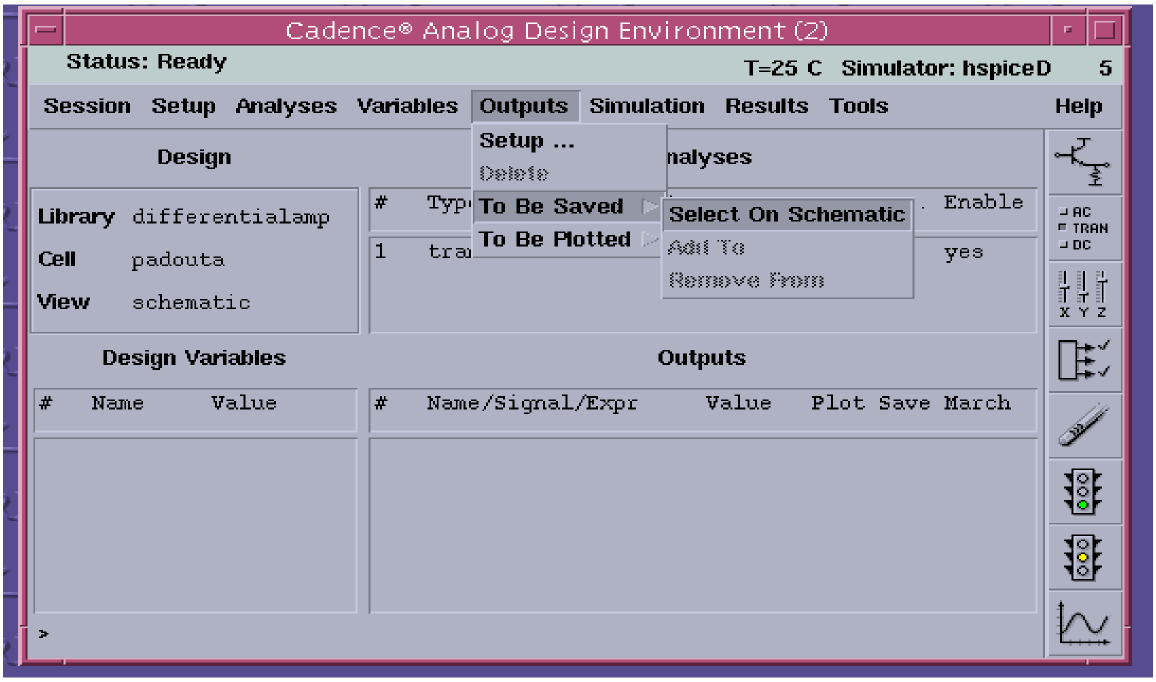
Outputs

#	Name/Signal/Expr	Value	Plot	Save	March

8．确定输出显示变量

（1）选择保存模拟数据的变量

在 cadence analog design environment 窗口中，依次单击 outputs ->to be saved -> select on schematic ，如图


Cadence® Analog Design Environment (2)
Status: Ready
T=25 C Simulator: hspiceD 5
Session Setup Analyses Variables Outputs Simulation Results Tools Help
Setup ...
Delete
To Be Saved
To Be Plotted
Select On Schematic
Add To
Remove From
AC
TRAN
DC
X Y Z
>

Design

Library differentialamp

Cell padouta

View schematic

nalyses

#	Typ	Enable
1	tra	yes

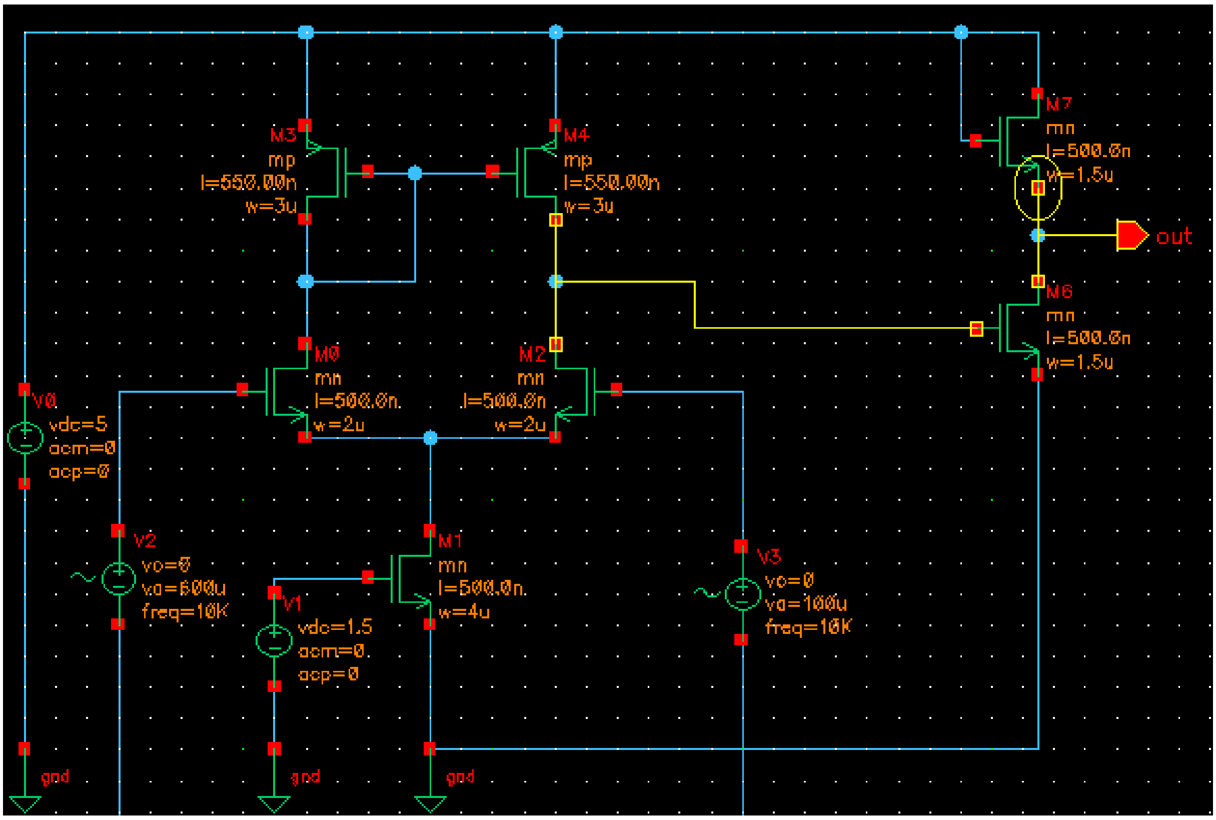
Design Variables

#	Name	Value

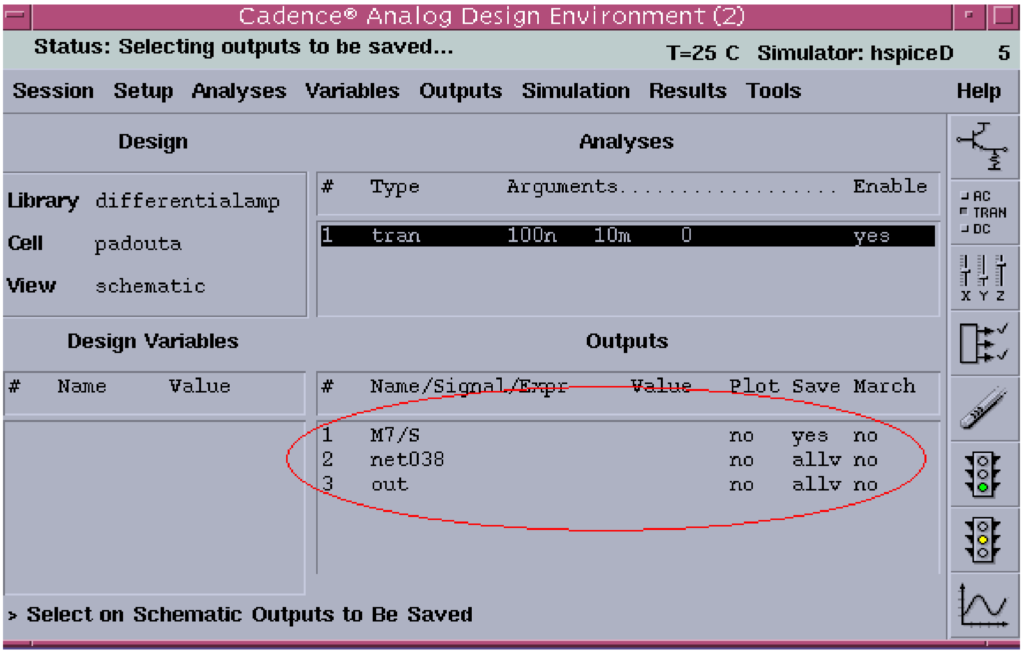
Outputs

#	Name/Signal/Expr	Value	Plot	Save	March

Schematic page 页面被作为当前页面，在该页面上用鼠标右键点选需要保存模拟数据的物理量，需要注意的是：点选电路中的点表示保存该点的电流量；点选电路中的连线（net）表示保存该连线的电压量，选中后分别用黄色圆圈和黄色连线突出显示，如图



选择结束后，自动在 cadence analog design environment 窗口中显示，如图所示：



Status: Selecting outputs to be saved...   T=25 C Simulator: hspiceD   5

Design

Library differentialamp

Cell padouta

View schematic

Analyses

#	Type	Arguments................			Enable
1	tran	100n	10m	0	yes

Design Variables

#	Name	Value

Outputs

#	Name/Signal/Expr	Value	Plot	Save	March
1	M7/S		no	yes	no
2	net038		no	allv	no
3	out		no	allv	no

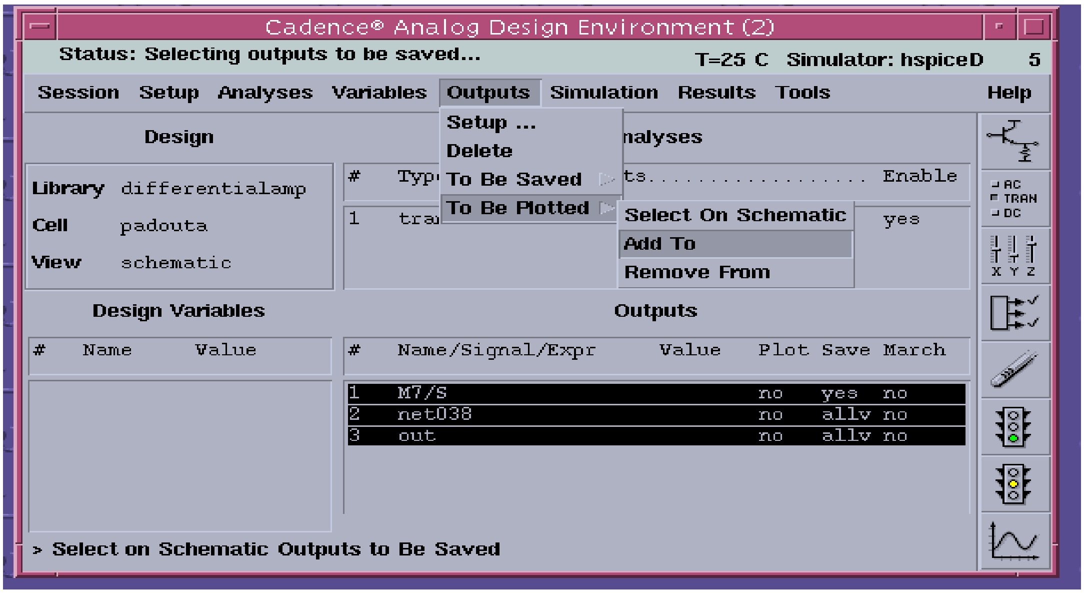
> Select on Schematic Outputs to Be Saved

（2）选择显示模拟数据的变量

有两种方法可以完成

a. 在 cadence analog design environment 窗口中，依次单击 outputs ->to be plotted -> select on schematic ，与选择保存模拟数据的变量的操作相同即可；

b. 若要显示的变量同时也是保存数据的变量，则只需在上图所示的红色圈中，选中要显示的变量，如果有多个需要显示，可以选用 shift 键实现多选，如图，再依次单击 outputs ->to be plotted ->add to ，即可把选中的变量加入到显示变量列表。



Status: Selecting outputs to be saved...   T=25 C   Simulator: hspiceD   5

Design

Library differentialamp
Cell padouta
View schematic

nalyses

#	Typ	ts.................	Enable
1	tra		yes

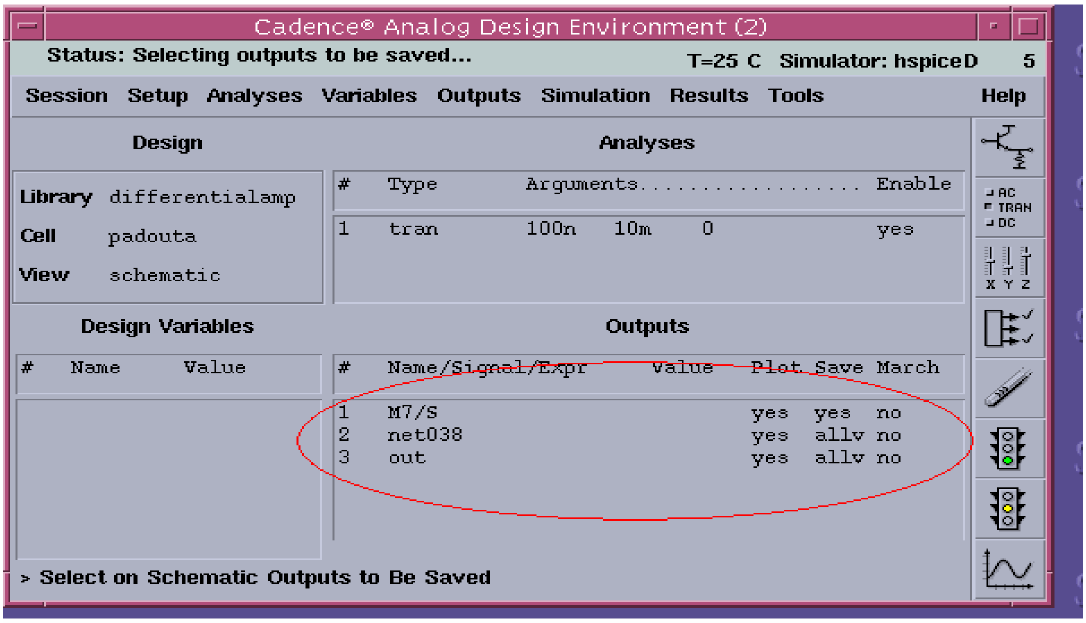
Design Variables

#	Name	Value

Outputs

#	Name/Signal/Expr	Value	Plot	Save	March
1	M7/S		no	yes	no
2	net038		no	allv	no
3	out		no	allv	no

> Select on Schematic Outputs to Be Saved



Status: Selecting outputs to be saved...   T=25 C   Simulator: hspiceD   5

Design

Library differentialamp
Cell padouta
View schematic

Analyses

#	Type	Arguments.................			Enable
1	tran	100n	10m	0	yes

Design Variables

#	Name	Value

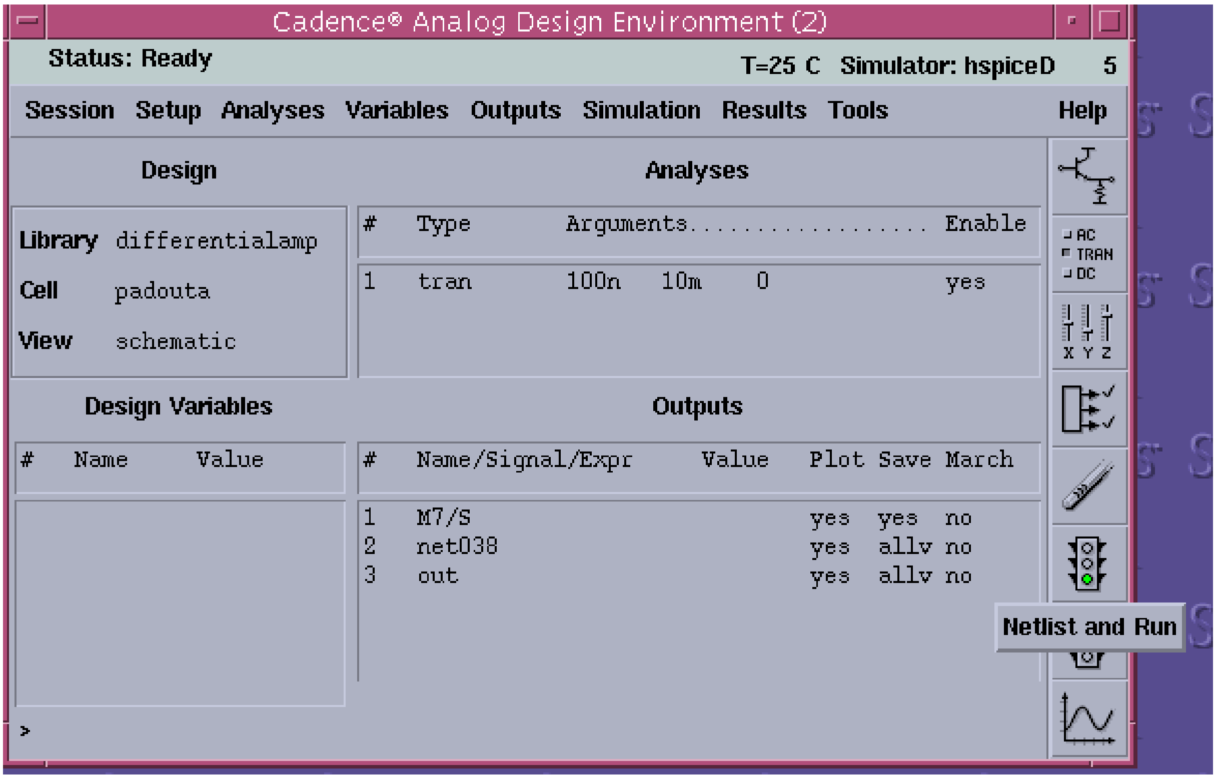
Outputs

#	Name/Signal/Expr	Value	Plot	Save	March
1	M7/S		yes	yes	no
2	net038		yes	allv	no
3	out		yes	allv	no

> Select on Schematic Outputs to Be Saved

9．进行模拟

（1）以上设置完成后，单击右边工具栏中的 netlist and run ,列出网表并且进行模拟，即可进行瞬态响应。



Cadence® Analog Design Environment (2)

Status: Ready   T=25 C Simulator: hspiceD   5

Session Setup Analyses Variables Outputs Simulation Results Tools   Help

Design

Library differentialamp
Cell padouta
View schematic

Analyses

#	Type	Arguments.................			Enable
1	tran	100n	10m	0	yes

Design Variables

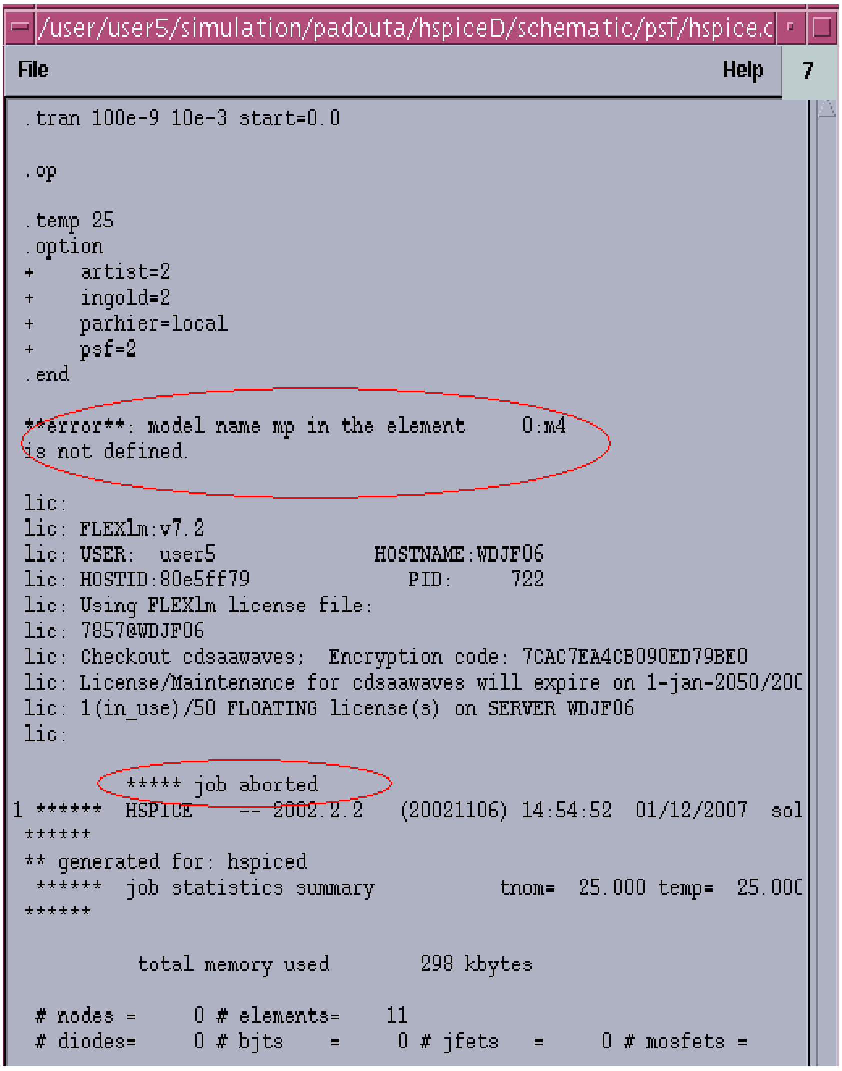
#	Name	Value

Outputs

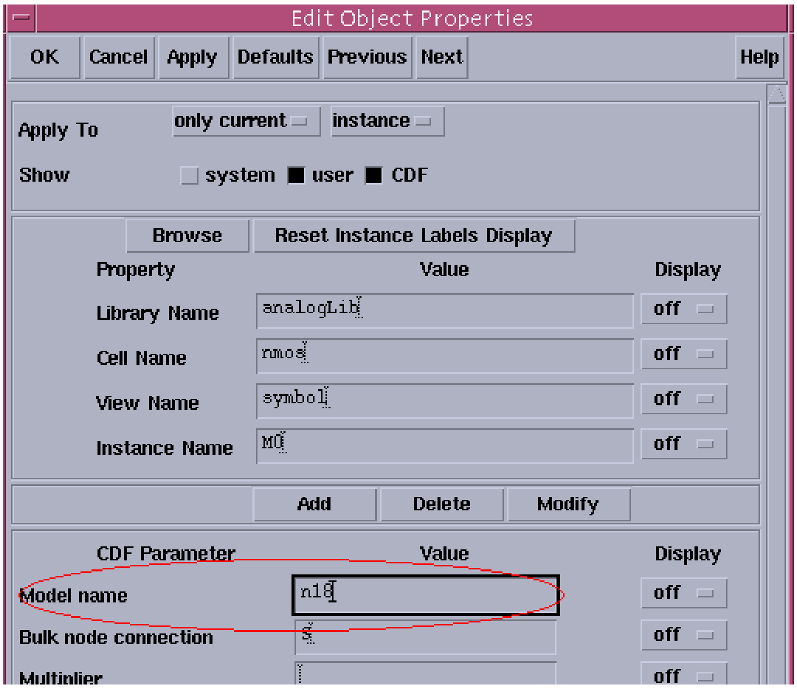
#	Name/Signal/Expr	Value	Plot	Save	March
1	M7/S		yes	yes	no
2	net038		yes	allv	no
3	out		yes	allv	no

（2）在该例子中，由于 MOS 管的名称故意设置错误，因此模拟运行过程中会报错，如图所示 。图中，用红色椭圆突出显示，其一为错误源提示，其二为运行失败提示。由于 SMIC 库中 MOS 管的模型文件中定义的 MOS 名称分别为 n18 和 p18，因此此处 NMOS 的 model name mn 提示为未定义。

（3）接下来修正错误。选择 cadence schematic 窗口为当前窗口，选中 NMOS 管，单击左边工具栏中的 property 图标，显示元器件属性窗口，纠正 model name ，所有 NMOS 为 n18 ，所有 PMOS 为 p18 ，单击 OK，如图所示。


/user/user5/simulation/padouta/hspiceD/schematic/psf/hspice.c
File
Help
7

```
.tran 100e-9 10e-3 start=0.0

.op

.temp 25
.option
+    artist=2
+    ingold=2
+    parhier=local
+    psf=2
.end

**error**: model name mp in the element     0:m4
is not defined.

lic:
lic: FLEXlm:v7.2
lic: USER:   user5               HOSTNAME:WDJF06
lic: HOSTID:80e5ff79                PID:      722
lic: Using FLEXlm license file:
lic: 7857@WDJF06
lic: Checkout cdsaawaves;  Encryption code: 7CAC7EA4CB090ED79BE0
lic: License/Maintenance for cdsaawaves will expire on 1-jan-2050/200
lic: 1(in_use)/50 FLOATING license(s) on SERVER WDJF06
lic:

         ***** job aborted
1 ******  HSPICE   -- 2002.2.2   (20021106) 14:54:52  01/12/2007  sol
******
** generated for: hspiced
 ******  job statistics summary           tnom=  25.000 temp=  25.000
******

          total memory used         298 kbytes

 # nodes =      0 # elements=     11
 # diodes=      0 # bjts    =      0 # jfets    =      0 # mosfets =
```



Apply To: only current, instance

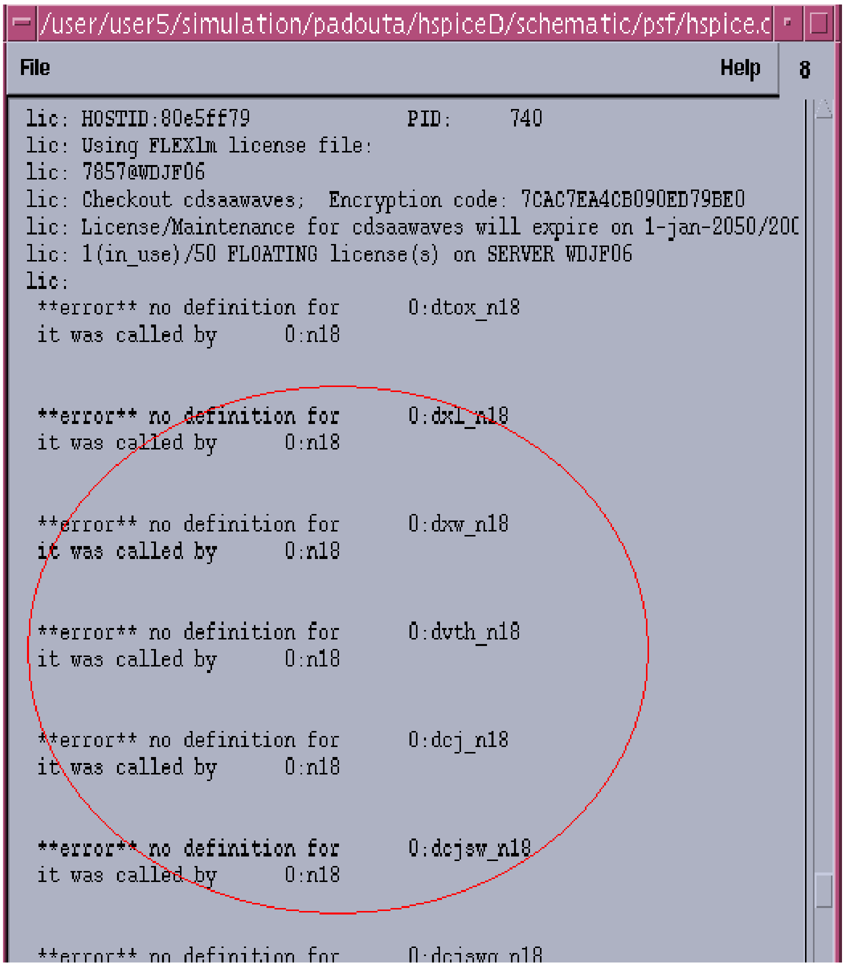
Show: □ system ■ user ■ CDF

Property	Value	Display
Library Name	analogLib	off
Cell Name	nmos	off
View Name	symbol	off
Instance Name	M0	off

CDF Parameter	Value	Display
Model name	n18	off
Bulk node connection	S	off
Multiplier		off

（4）运行 check and save 之后，再次运行 netlist and run ，此时 MOS model name

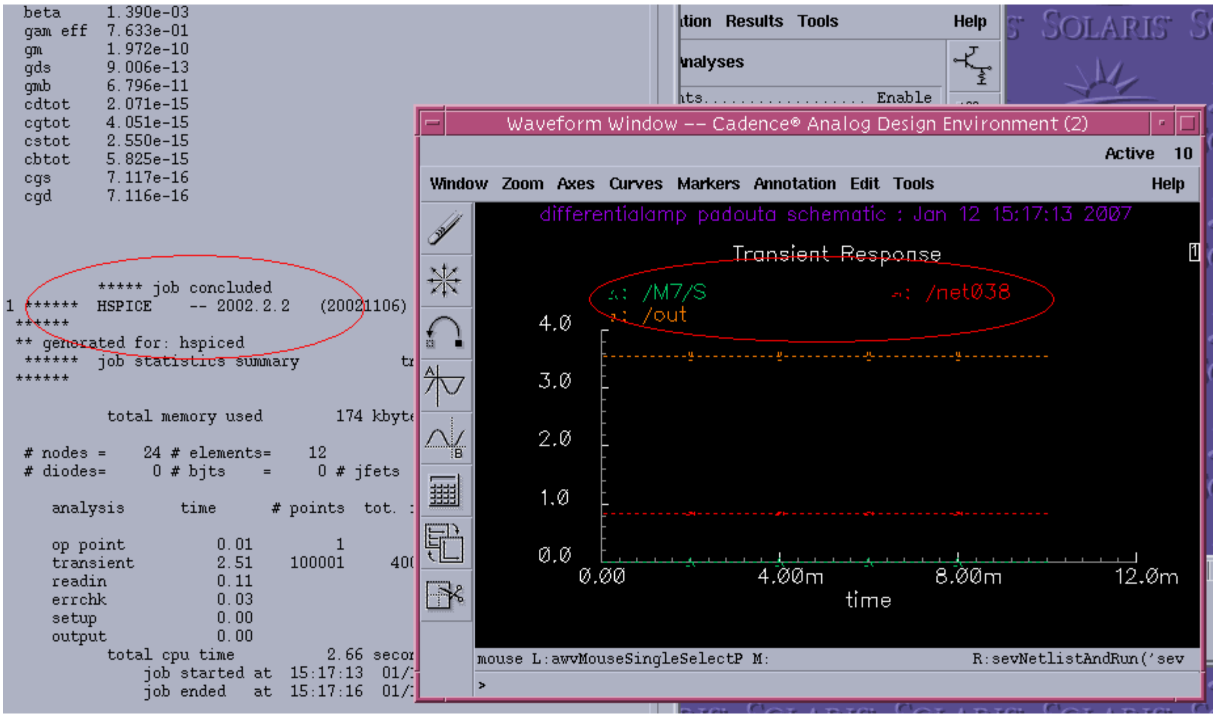
正确无误，但是再次报错，提示如图所示：


/user/user5/simulation/padouta/hspiceD/schematic/psf/hspice.c
File
Help
8

```
lic: HOSTID:80e5ff79               PID:     740
lic: Using FLEXlm license file:
lic: 7857@WDJF06
lic: Checkout cdsaawaves;  Encryption code: 7CAC7EA4CB090ED79BE0
lic: License/Maintenance for cdsaawaves will expire on 1-jan-2050/20C
lic: 1(in_use)/50 FLOATING license(s) on SERVER WDJF06
lic:
 **error** no definition for      0:dtox_n18
 it was called by         0:n18


 **error** no definition for      0:dxl_n18
 it was called by         0:n18


 **error** no definition for      0:dxw_n18
 it was called by         0:n18


 **error** no definition for      0:dvth_n18
 it was called by         0:n18


 **error** no definition for      0:dcj_n18
 it was called by         0:n18


 **error** no definition for      0:dcjsw_n18
 it was called by         0:n18


 **error** no definition for      0:dcjswg_n18
```

该错误提示为所采用的模型文件中，有未定义的参数，通过在 solaris 操作系统下用文本编辑器察看，可以知道是 ms018_v1p6.mdl 中，“TT、FF、SS”没有确定。根据 SMIC 提供的文档，修改该模型文件。

（5）再次运行 netlist and run，过程中无任何报错，所选中的显示变量自动在 plot 窗口中分色显示，如图所示。图中红色椭圆，其一表示模拟完成，其二表示显示的变量。



```
  beta      1.390e-03
  gam eff   7.633e-01
  gm        1.972e-10
  gds       9.006e-13
  gmb       6.796e-11
  cdtot     2.071e-15
  cgtot     4.051e-15
  cstot     2.550e-15
  cbtot     5.825e-15
  cgs       7.117e-16
  cgd       7.116e-16



          ***** job concluded
1 ******  HSPICE    -- 2002.2.2   (20021106)
 ******
 ** generated for: hspiced
  ******  job statistics summary           tr
 ******

           total memory used          174 kbyte

  # nodes =    24 # elements=    12
  # diodes=     0 # bjts    =     0 # jfets

     analysis      time      # points   tot. :

     op point          0.01          1
     transient         2.51     100001      40(
     readin            0.11
     errchk            0.03
     setup             0.00
     output            0.00
           total cpu time          2.66 secor
               job started at  15:17:13  01/:
               job ended   at  15:17:16  01/:
```

tion Results Tools Help
nalyses
nts.................. Enable
SOLARIS
Waveform Window -- Cadence® Analog Design Environment (2)
Active 10
Window Zoom Axes Curves Markers Annotation Edit Tools Help
differentialamp padouta schematic : Jan 12 15:17:13 2007
Transient Response
/M7/S
/net038
/out
4.0
3.0
2.0
1.0
0.0
0.00
4.00m
8.00m
12.0m
time
mouse L:awvMouseSingleSelectP M: R:sevNetlistAndRun('sev

（6）通过单击菜单 axes 可以调整 X、Y 轴的显示范围和显示方式，如下图所示：

至此，该电路的瞬态响应分析基本结束。得到相关变量的波形之后，需要对相关参数进行分析。这一部分内容不作为实验的内容。

三．思考题

1．尝试对该电路进行交流性能分析。

2．如何得到该电路的带宽这一参数？在波形显示上又如何读出该带宽数据？

3.如何得到单个 NMOS 管子的 f_T ？

4.如何得到单个 NMOS 管子的跨导？

第三部分 实验内容

（三）

Cadence virtuoso Layout editor 版图编辑

一．实验目的

通过绘制五管基本差分运算放大器的版图，熟悉 layout editor 的基础操作，能够运用 layout editor 编辑器进行单层电路图版图的手工绘制。

二．实验内容

1.按照之前实验中的操作步骤，登陆工作站。

2．目录准备

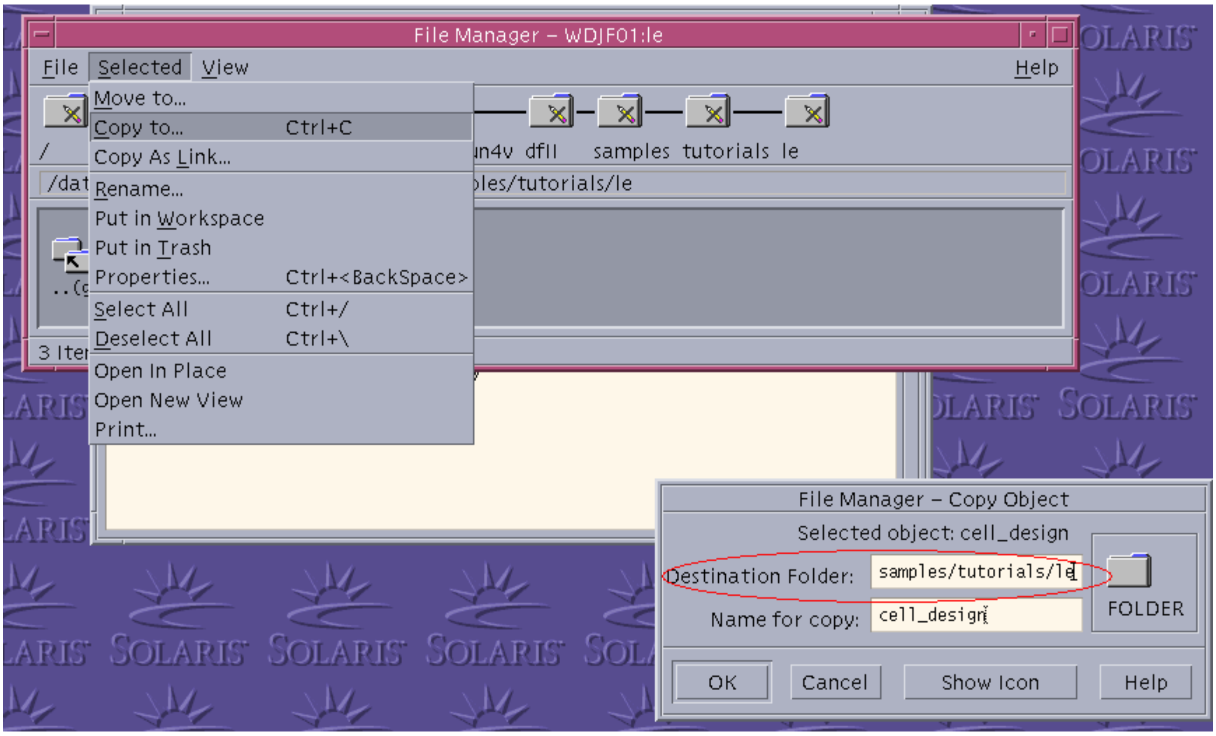
（1）登陆工作站后，进入默认的工作目录 /data/user/student/ ；

（2）进入到自己建立的文档目录中；

（3）在 terminal 当前目录下，键入命令 ls cell_design ，回车，此命令为检查当前工作目录下是否存在名字为 cell_design 的文件夹。因为在实验中，需要用到名称为 cell_design 的软件自带的数据库。若显示“ No such file or directory “，则表明当前工作目录下无该名称的文件夹。若显示存在，则先删除。

（4）进入目录 /data/ap/cadence/IC/tools.sun4v/dfII/samples/tutorials/le ，在此目录下可找到名称为 cell_design 的文件夹 ，选择该文件夹，单击菜单 selected —>copy to ，出现如图对话框，在图中红线画出的地方，敲入需要拷入的文件夹，即 /data/user/student/****，期中****为学生自己建立的工作目录。

（5）进入目录 /data/user/student/****/cell_design



Selected object: cell_design

Destination Folder: samples/tutorials/le

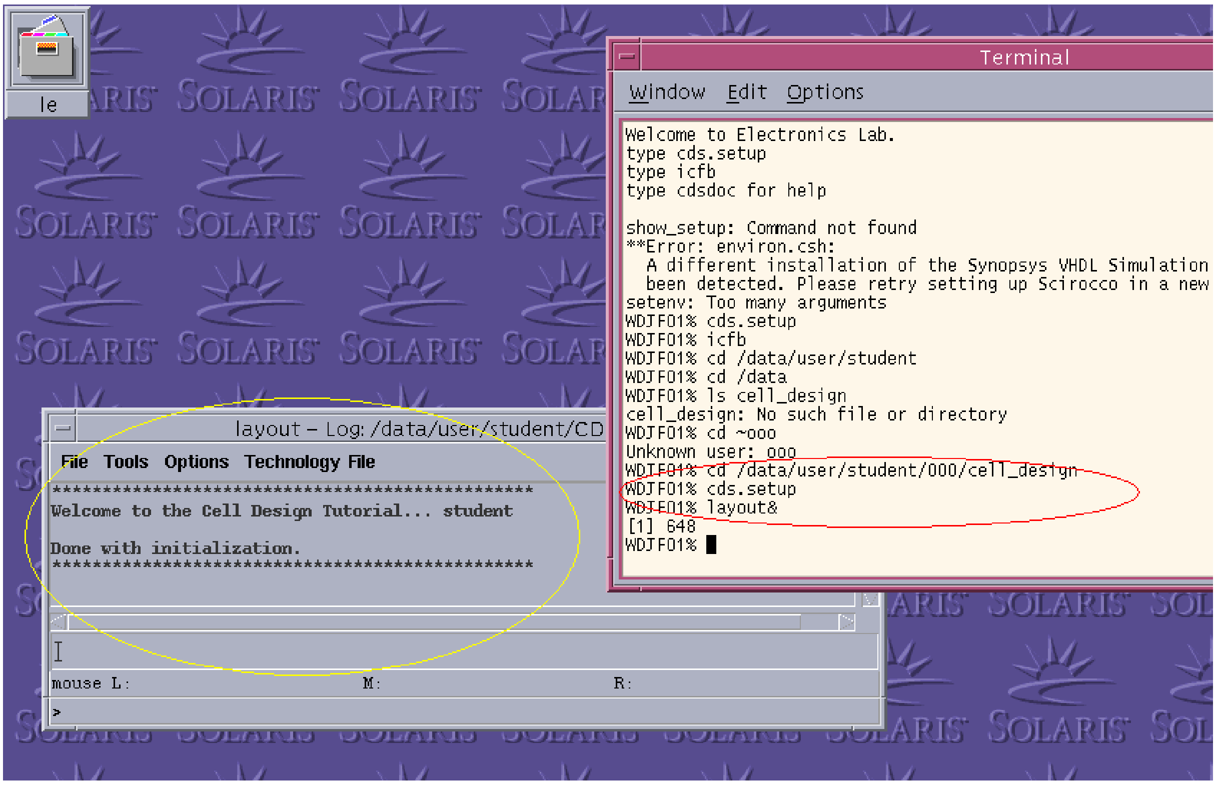
Name for copy: cell_design

(6) 键入命令 cds.setup enter;

(7) 键入命令 layout & ,即可启动 layout editor。

3. 启动 layout editor

按照上述操作，启动 layout editor 之后，如图所示：



```
Welcome to Electronics Lab.
type cds.setup
type icfb
type cdsdoc for help

show_setup: Command not found
**Error: environ.csh:
  A different installation of the Synopsys VHDL Simulation
  been detected. Please retry setting up Scirocco in a new
setenv: Too many arguments
WDJF01% cds.setup
WDJF01% icfb
WDJF01% cd /data/user/student
WDJF01% cd /data
WDJF01% ls cell_design
cell_design: No such file or directory
WDJF01% cd ~ooo
Unknown user: ooo
WDJF01% cd /data/user/student/000/cell_design
WDJF01% cds.setup
WDJF01% layout&
[1] 648
WDJF01% 
```

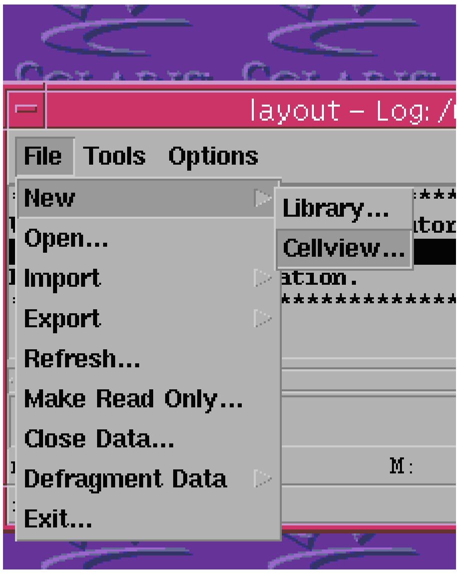
```
****************************************************
Welcome to the Cell Design Tutorial... student

Done with initialization.
****************************************************
```

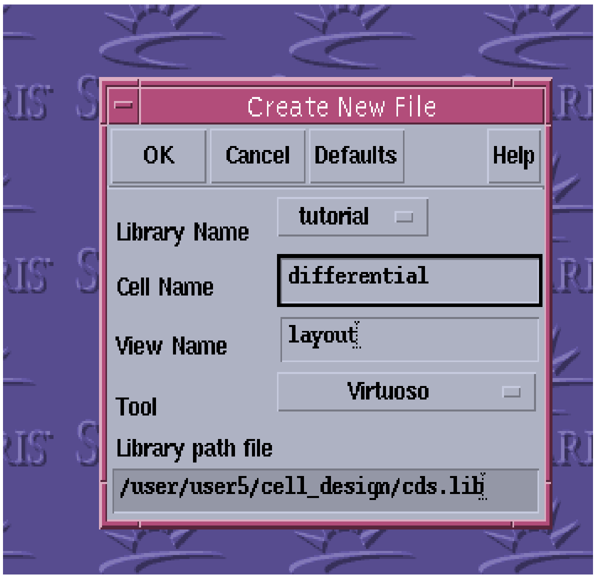
```
mouse L:                    M:                    R:
>
```

红线所示为敲入启动 layout editor 的命令，而黄线所示为启动成功提示信息。

4. 绘制版图

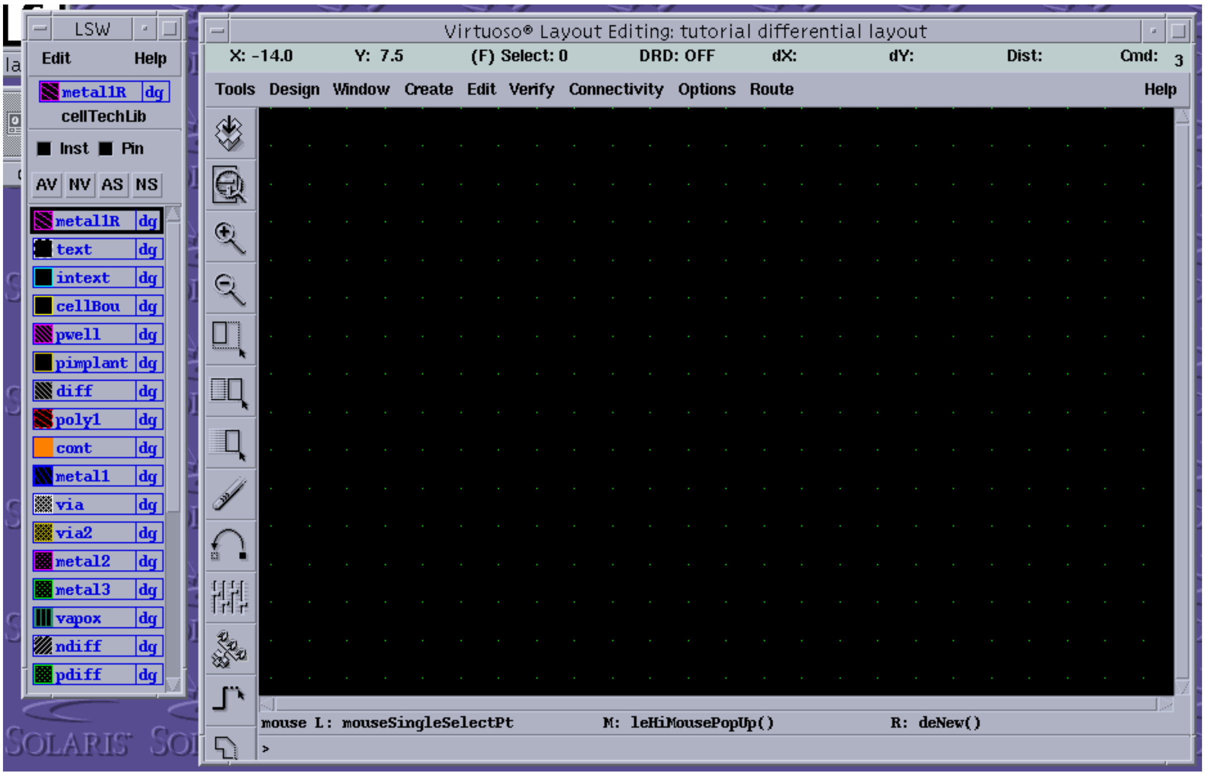
（1）创建 layout view :单击菜单 file -> new ->cell view，如图所示





Library Name: tutorial
Cell Name: differential
View Name: layout
Tool: Virtuoso
Library path file: /user/user5/cell_design/cds.lib

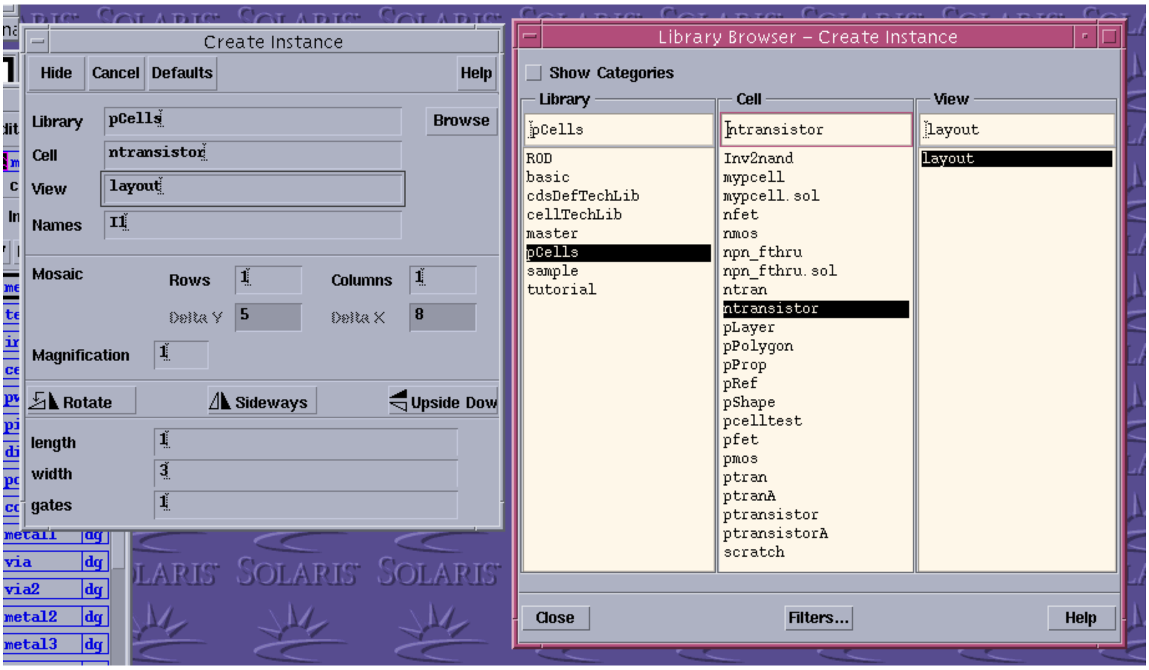
在 library name 一栏选择 tutorial ，cell name 为自己定义，示意中采用 differential ,tool 选择 virtuoso,则 view name 自动转换成 layout，library path file 采用默认即可。单击 OK。出现如图



其中，左侧为层选择窗口（LSW），右侧为版图绘制窗口。

（2）绘制 NMOS 管：

单击绘制窗口菜单 create -> instance，出现左侧 create instance 窗口，



Library pCells
Cell ntransistor
View layout
Names I1

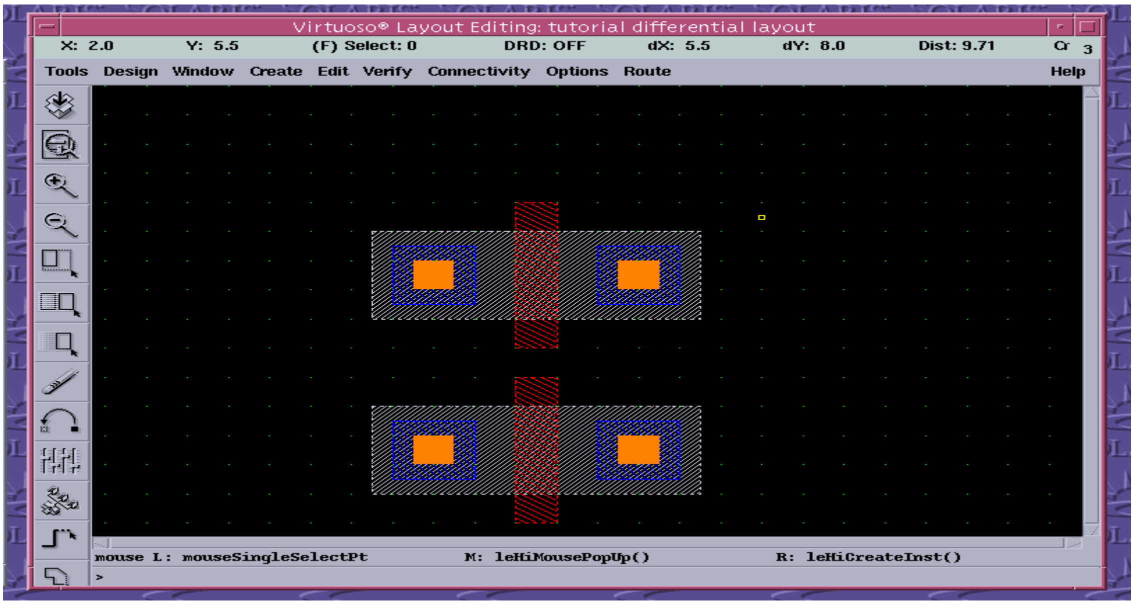
Mosaic Rows 1 Columns 1
Delta Y 5 Delta X 8
Magnification 1

length 1
width 3
gates 1

□ Show Categories

Library	Cell	View
pCells	ntransistor	layout
ROD basic cdsDefTechLib cellTechLib master pCells sample tutorial	Inv2nand mypcell mypcell.sol nfet nmos npn_fthru npn_fthru.sol ntran ntransistor pLayer pPolygon pProp pRef pShape pcelltest pfet pmos ptran ptranA ptransistor ptransistorA scratch	layout

在该窗口中，library 选择时，点击 browse，出现右侧窗口，依次选择 pcells，ntransistor，layout，mosaic 一栏采用默认， 三个按钮 rotate sideways upside down 可根据实际放置的需要选择采用， length，width，gates 填入合适的参数即可，在版图绘制窗口合适位置单击鼠标，即可完成一个 NMOS 管的版图，如图所示：



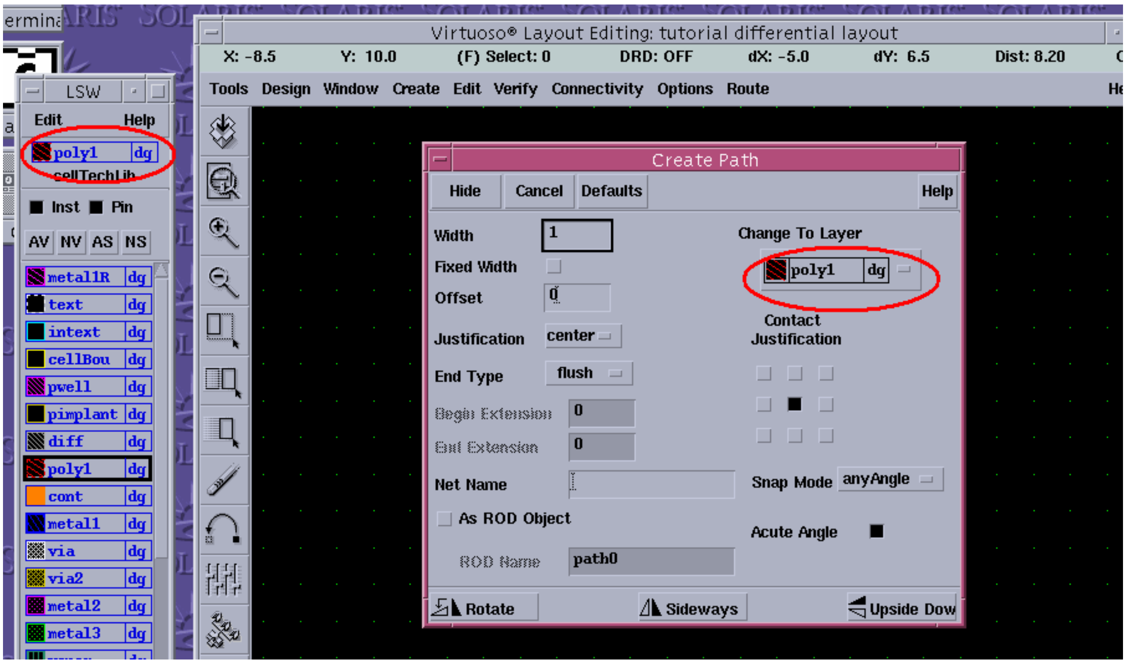
X: 2.0 Y: 5.5 (F) Select: 0 DRD: OFF dX: 5.5 dY: 8.0 Dist: 9.71 Cr 3

mouse L: mouseSingleSelectPt M: leHiMousePopUp() R: leHiCreateInst()

（3）绘制 PMOS 管：类似以上操作，可完成 PMOS 版图的添加。

(4）用 path 连接 MOS 管的栅极:

Path 是一种用中心线和确定宽度来定义的方形连接。用 path 连接晶体管栅极的操作如下。首先单击层选择窗口（LSW）中的 poly1 层，使其成为当前层，单击版图绘制窗口菜单 create -> path，出现如图所示窗口，


Virtuoso® Layout Editing: tutorial differential layout

X: -8.5 Y: 10.0 (F) Select: 0 DRD: OFF dX: -5.0 dY: 6.5 Dist: 8.20

Create Path

Width 1

Fixed Width □

Offset 0

Justification center

End Type flush

Begin Extension 0

End Extension 0

Net Name

□ As ROD Object

ROD Name path0

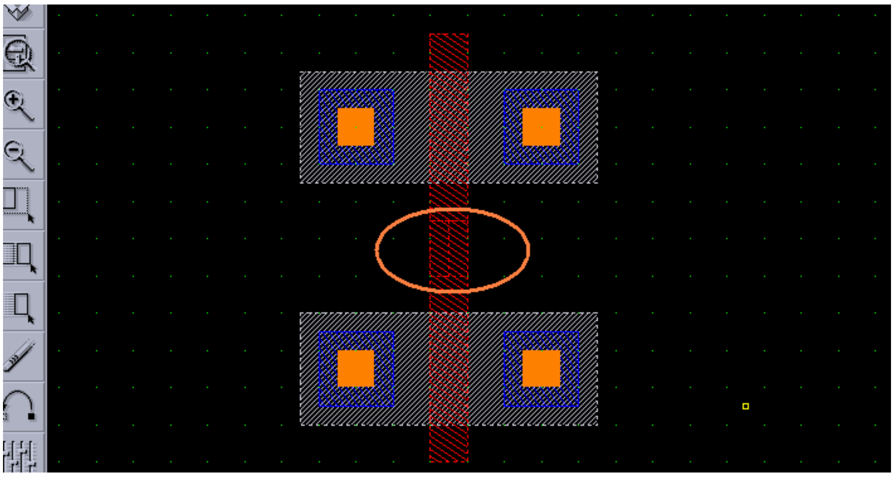
Change To Layer poly1 dg

Contact Justification

Snap Mode anyAngle

Acute Angle ■

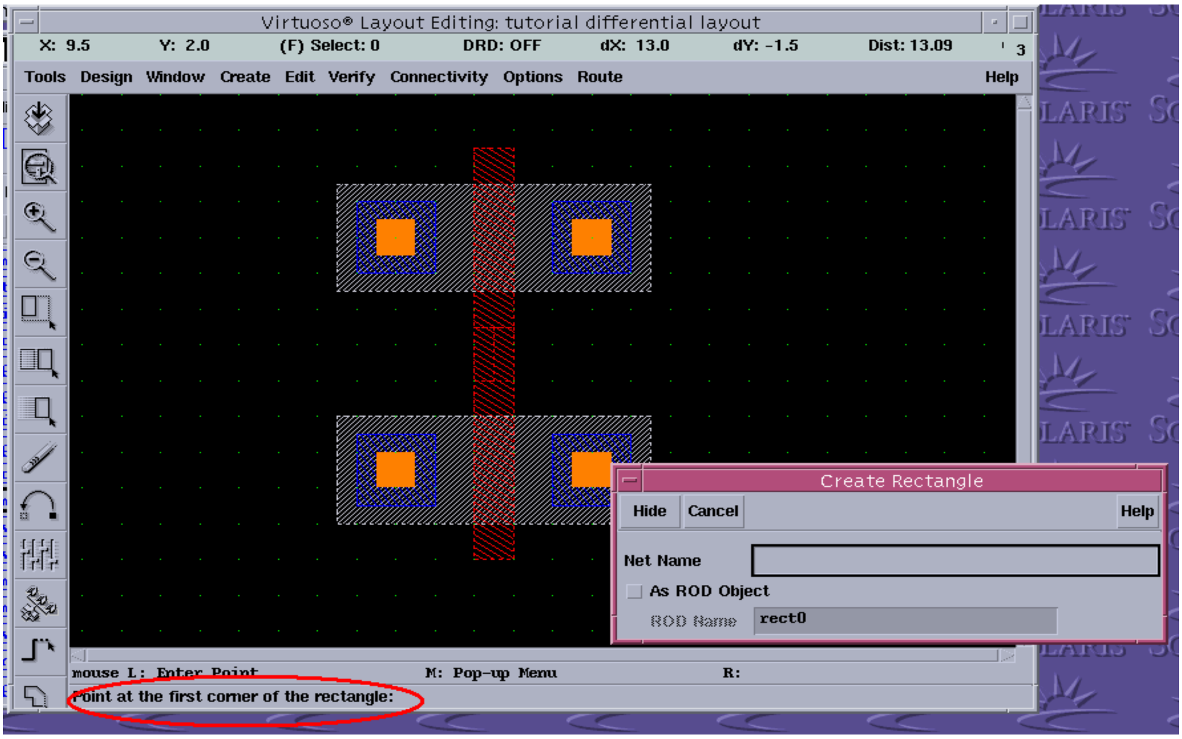
红线所示为当前编辑层，在 create path 窗口中，设置相关的参数即可，这里均采用默认值，完成后在绘制窗口所要连接的两个栅极分别单击，即可完成用 poly-silicon Path 连接两个栅极，如下图



桔黄色所示即为刚完成的 poly-silicon path 。

（5）用 metal rectangle 连接晶体管的源漏

Rectangle 由其连个对角来确定形状。操作如下，首先单击层选择窗口（LSW）中的 metal1 层，使其成为当前层，单击版图绘制窗口菜单 create ->rectangle，出现如图所示窗口，



X: 9.5 Y: 2.0 (F) Select: 0 DRD: OFF dX: 13.0 dY: -1.5 Dist: 13.09 3

Net Name

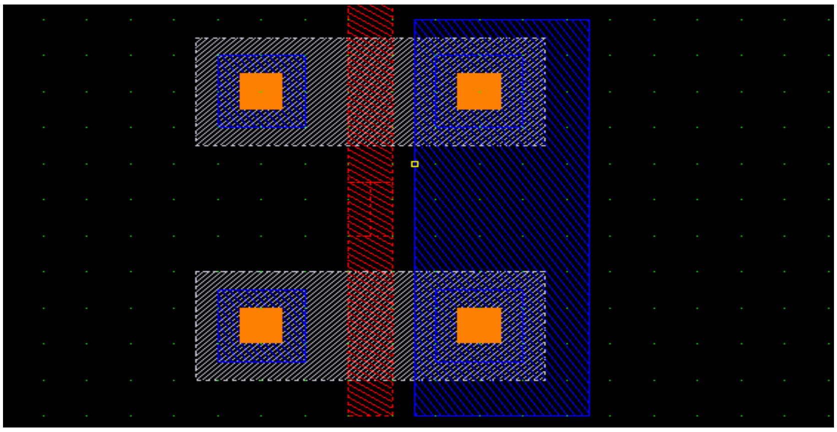
□ As ROD Object

ROD Name rect0

mouse L: Enter Point M: Pop-up Menu R:

Point at the first corner of the rectangle:

图中红线所示为提示确定 rectangle 的第一个点，按照提示，在需要连接的漏源之间，单击合适的位置作为第一个点，接着提示确定 rectangle 的对角点，按照提示操作，完成后的形状如图

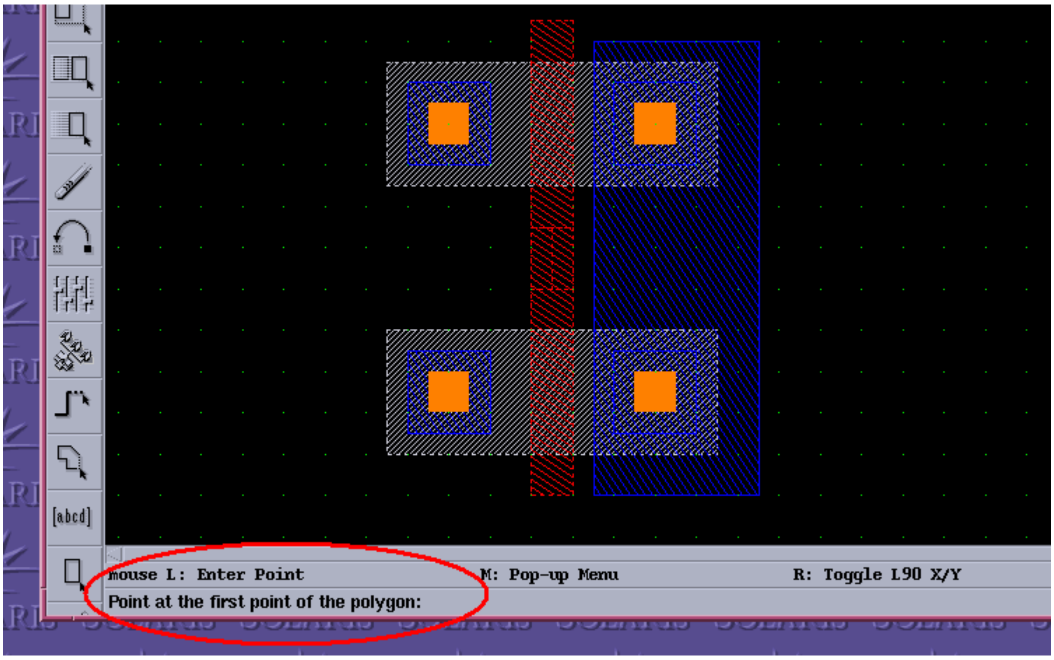


图中蓝颜色所示即为用来连接漏源的金属 rectangle。

（6）重复操作 （4）（5）完成其他元件的连接;

（7）添加 power:

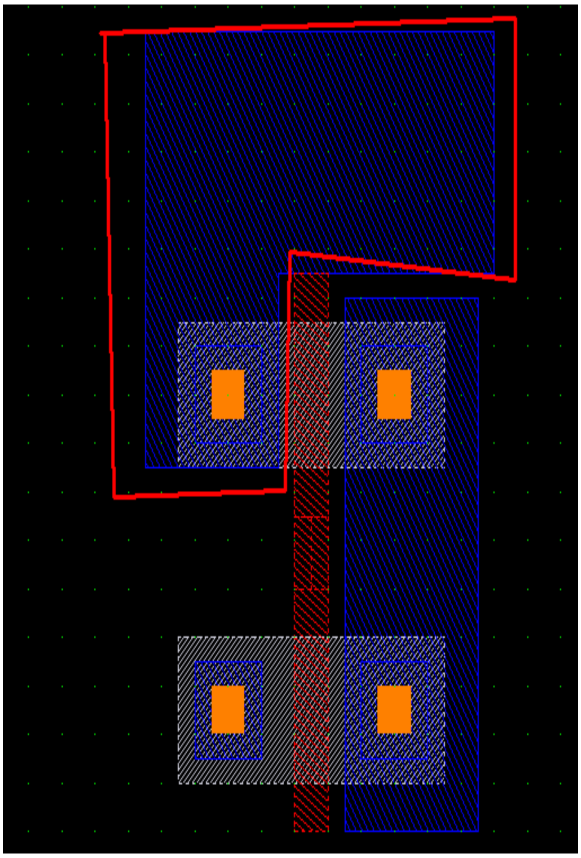
采用 metal polygon 来完成 power 。polygon 是一种由依次经过各个点，并且最后一点回到最初一点构成闭合曲线而形成。操作如下。首先单击层选择窗口（LSW）中的 metal1 层，使其成为当前层，单击版图绘制窗口菜单 create ->polygon，出现如图所示窗口，红线所示为提示确定 polygon 第一个点，依次选择合适的位置作为 polygon 的各个顶点，并且最终回到起点闭合，即可完成 metal polygon 的绘制。完成后如图所示，红线所表示的蓝色区域即为所添加的连接 power 的 metal polygon 。

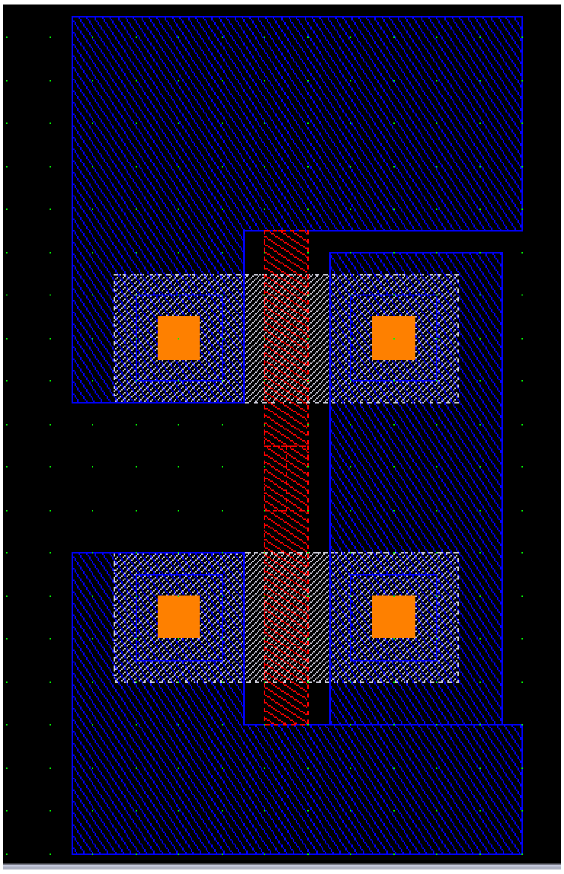


mouse L: Enter Point M: Pop-up Menu R: Toggle L90 X/Y

Point at the first point of the polygon:

（8）采用类似（7）操作，完成 GND 的连接。完成后的示意图如图所示。





（9）单击菜单 create -> label 可以在需要的位置创建图形的标签。

（10）完成所有连接后，单击版图绘制窗口左侧工具栏中的 save，即可。

（11）按照以上操作，独立完成五管基本差分运算放大器的版图绘制。

（12）多层版图设计操作，请参考使用手册。

三. 思考题

1. 源漏连接用的 metal rectangle 和栅连接用的 poly path 有何区别？

2. Power GND 用的 metal polygon 和漏源连接用的 metal rectangle 有何区别？

3. Power GND 的 metal polygon 大小由哪些参数来决定？

第三部分 实验内容

（四）

DRC、LVS EXTRACT 以及后仿真

一．实验目的

通过本实验，掌握对已绘制电路版图进行设计规则检查（DRC)、电学规则检查（ERC)、版图和原电路图的对比（LVS）以及对绘制的电路版图进行寄生参数提取（EXTRA）的基本流程和基本操作。能够利用提取的寄生参数再次对原电路进行性能的模拟。

二．实验内容

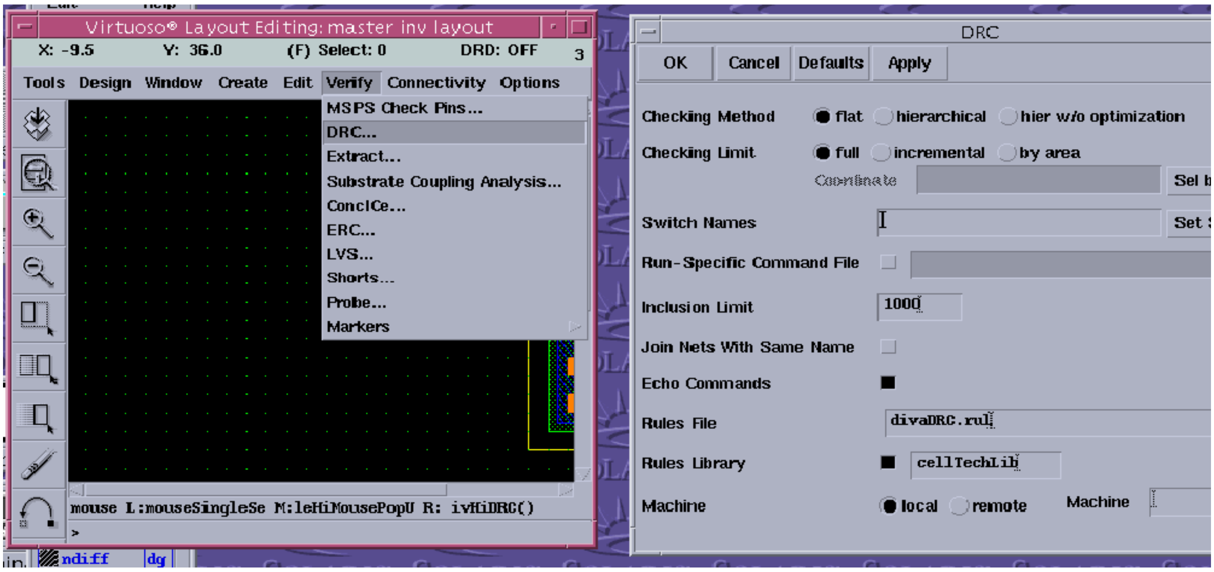
1．仿照实验三中的操作，登陆服务器，进入 cell_design 目录下，键入命令 layout 或者 layout plus，启动 virtuoso layout editor ;

2．单击菜单 file ->open ,打开 master library 下 inv layout 。在本实验中，采用 cell_design tutorial 中 inverter 的 layout 来说明 DRC、ERC、LVS、EXTRAC 等操作。

3．DRC（设计规则检查）

该步骤主要是检查所绘制的版图是否符合设计规则。具体操作如下：

（1）在实验三的最后，保存后，通过单击菜单 verify -> DRC,弹出对话框如下



X: -9.5 Y: 36.0 (F) Select: 0 DRD: OFF 3

mouse L:mouseSingleSe M:leHiMousePopU R: ivHiDRC()

Checking Method ● flat ○ hierarchical ○ hier w/o optimization

Checking Limit ● full ○ incremental ○ by area

Coordinate

Switch Names

Run-Specific Command File □

Inclusion Limit 1000

Join Nets With Same Name □

Echo Commands ■

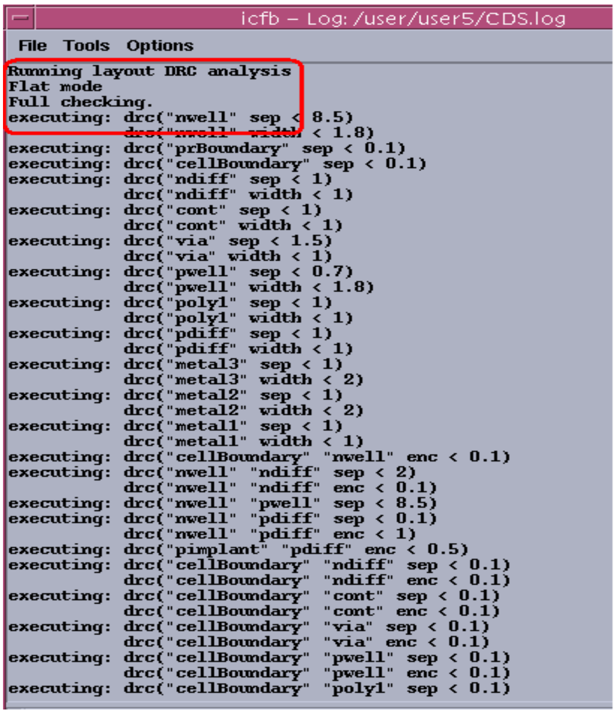
Rules File divaDRC.rul

Rules Library ■ cellTechLib

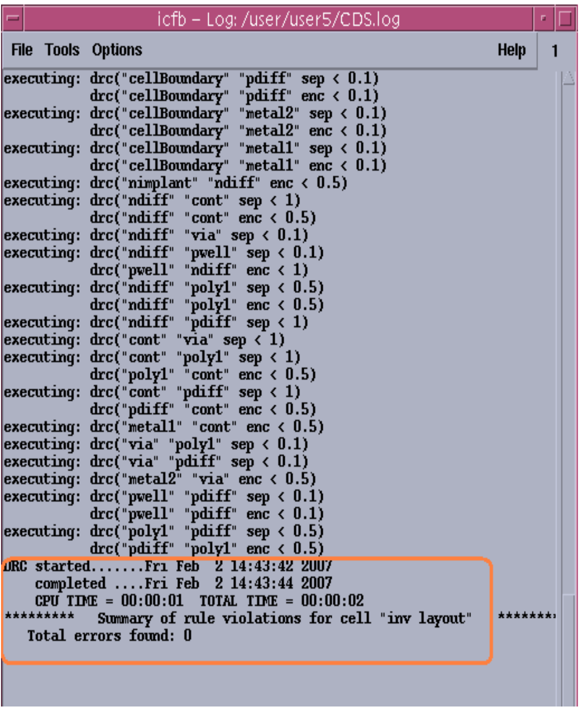
Machine ● local ○ remote Machine

在右边的 DRC 对话框中，包含了诸多内容，这些内容均采用默认值即可，其中重要的内容是规则文件和规则文件所在的库，这里均采用默认值，即 cell_design tutorial 自带的规则文件和库。

（2）设置完成后，单击 ok ，开始进行设计规则检查，结果如图所示



```
Running layout DRC analysis
Flat mode
Full checking.
executing: drc("nwell" sep < 8.5)
           drc("nwell" width < 1.8)
executing: drc("prBoundary" sep < 0.1)
executing: drc("cellBoundary" sep < 0.1)
executing: drc("ndiff" sep < 1)
           drc("ndiff" width < 1)
executing: drc("cont" sep < 1)
           drc("cont" width < 1)
executing: drc("via" sep < 1.5)
           drc("via" width < 1)
executing: drc("pwell" sep < 0.7)
           drc("pwell" width < 1.8)
executing: drc("poly1" sep < 1)
           drc("poly1" width < 1)
executing: drc("pdiff" sep < 1)
           drc("pdiff" width < 1)
executing: drc("metal3" sep < 1)
           drc("metal3" width < 2)
executing: drc("metal2" sep < 1)
           drc("metal2" width < 2)
executing: drc("metal1" sep < 1)
           drc("metal1" width < 1)
executing: drc("cellBoundary" "nwell" enc < 0.1)
executing: drc("nwell" "ndiff" sep < 2)
           drc("nwell" "ndiff" enc < 0.1)
executing: drc("nwell" "pwell" sep < 8.5)
executing: drc("nwell" "pdiff" sep < 0.1)
           drc("nwell" "pdiff" enc < 1)
executing: drc("pimplant" "pdiff" enc < 0.5)
executing: drc("cellBoundary" "ndiff" sep < 0.1)
           drc("cellBoundary" "ndiff" enc < 0.1)
executing: drc("cellBoundary" "cont" sep < 0.1)
           drc("cellBoundary" "cont" enc < 0.1)
executing: drc("cellBoundary" "via" sep < 0.1)
           drc("cellBoundary" "via" enc < 0.1)
executing: drc("cellBoundary" "pwell" sep < 0.1)
           drc("cellBoundary" "pwell" enc < 0.1)
executing: drc("cellBoundary" "poly1" sep < 0.1)
```



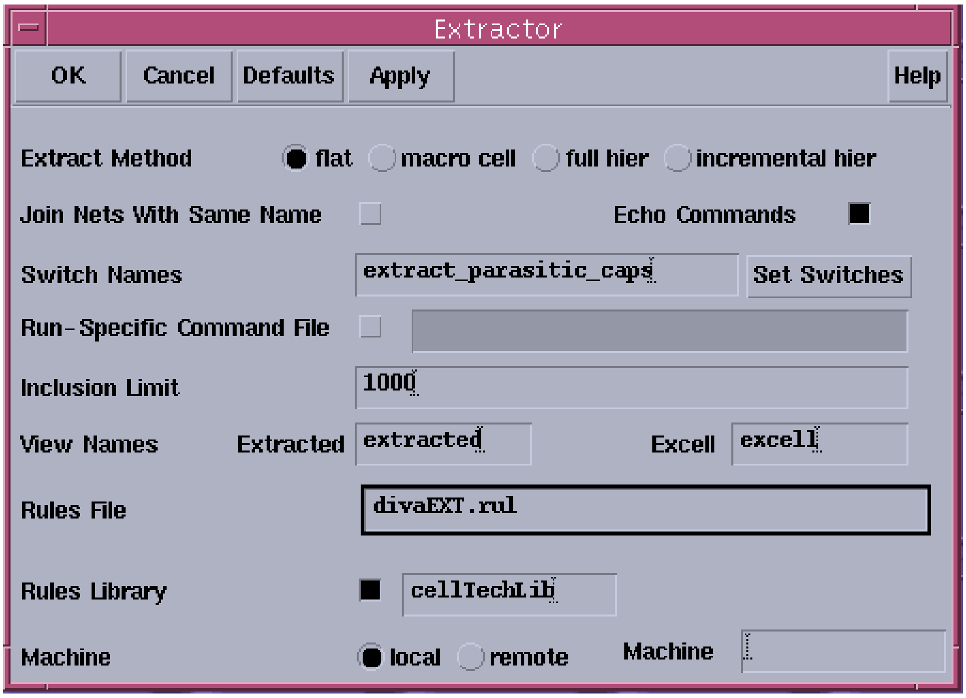
```
executing: drc("cellBoundary" "pdiff" sep < 0.1)
           drc("cellBoundary" "pdiff" enc < 0.1)
executing: drc("cellBoundary" "metal2" sep < 0.1)
           drc("cellBoundary" "metal2" enc < 0.1)
executing: drc("cellBoundary" "metal1" sep < 0.1)
           drc("cellBoundary" "metal1" enc < 0.1)
executing: drc("nimplant" "ndiff" enc < 0.5)
executing: drc("ndiff" "cont" sep < 1)
           drc("ndiff" "cont" enc < 0.5)
executing: drc("ndiff" "via" sep < 0.1)
executing: drc("ndiff" "pwell" sep < 0.1)
           drc("pwell" "ndiff" enc < 1)
executing: drc("ndiff" "poly1" sep < 0.5)
           drc("ndiff" "poly1" enc < 0.5)
executing: drc("ndiff" "pdiff" sep < 1)
executing: drc("cont" "via" sep < 1)
executing: drc("cont" "poly1" sep < 1)
           drc("poly1" "cont" enc < 0.5)
executing: drc("cont" "pdiff" sep < 1)
           drc("pdiff" "cont" enc < 0.5)
executing: drc("metal1" "cont" enc < 0.5)
executing: drc("via" "poly1" sep < 0.1)
executing: drc("via" "pdiff" sep < 0.1)
executing: drc("metal2" "via" enc < 0.5)
executing: drc("pwell" "pdiff" sep < 0.1)
           drc("pwell" "pdiff" enc < 0.1)
executing: drc("poly1" "pdiff" sep < 0.5)
           drc("pdiff" "poly1" enc < 0.5)
DRC started.......Fri Feb  2 14:43:42 2007
    completed ....Fri Feb  2 14:43:44 2007
    CPU TIME = 00:00:01  TOTAL TIME = 00:00:02
*********   Summary of rule violations for cell "inv layout"   ********
   Total errors found: 0
```

图中红线区域表示 DRC 检查的设计，黄线区域表示 DRC 检查完成，并且显示该版图中没有设计规则错误。

4. EXTRACT(参数提取) & LVS（版图与电路图的对比）

DRC 完成后，表示该版图没有设计规则错误，但是并不能保证所绘制的版图和原电路图一致，因此需要进行 LVS。操作如下

（1）首先进行参数提取，单击菜单 verify -> extract ,弹出如图对话框，提取方法选择默认的 flat ,为了加快提取参数的速度，echo commands 选择， switch names 通过单击 set switches 设置为 extract_parasitic-caps ，inclusion limit ,view name 均采用默认值,规则文件选择 divaEXT.rul ,规则库选择 celltechlib,machine 选择 local,设置完成后，单击 OK ,即可进行参数提取。



Extract Method ● flat ○ macro cell ○ full hier ○ incremental hier

Join Nets With Same Name □ Echo Commands ■

Switch Names: extract_parasitic_caps

Run-Specific Command File □

Inclusion Limit: 1000

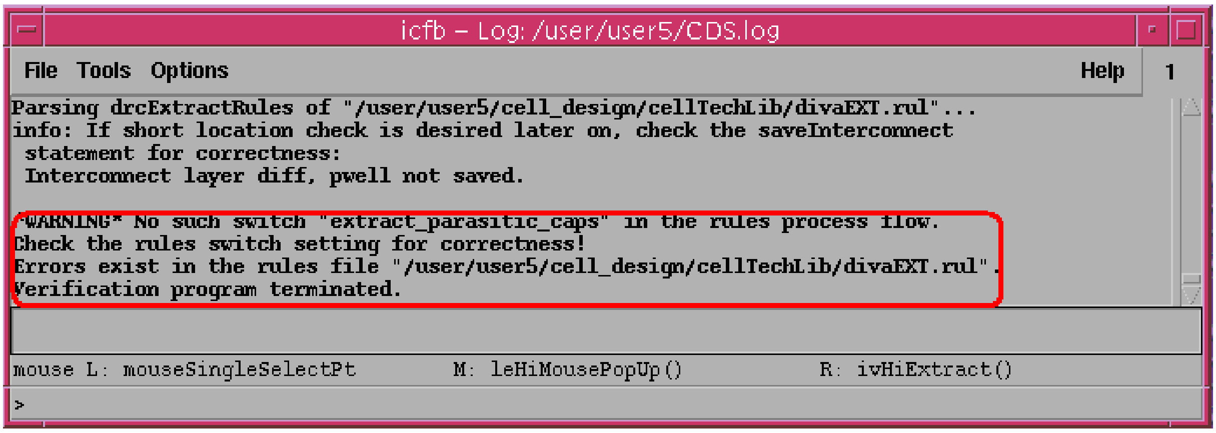
View Names Extracted: extracted Excell: excell

Rules File: divaEXT.rul

Rules Library ■ cellTechLib

Machine ● local ○ remote Machine:

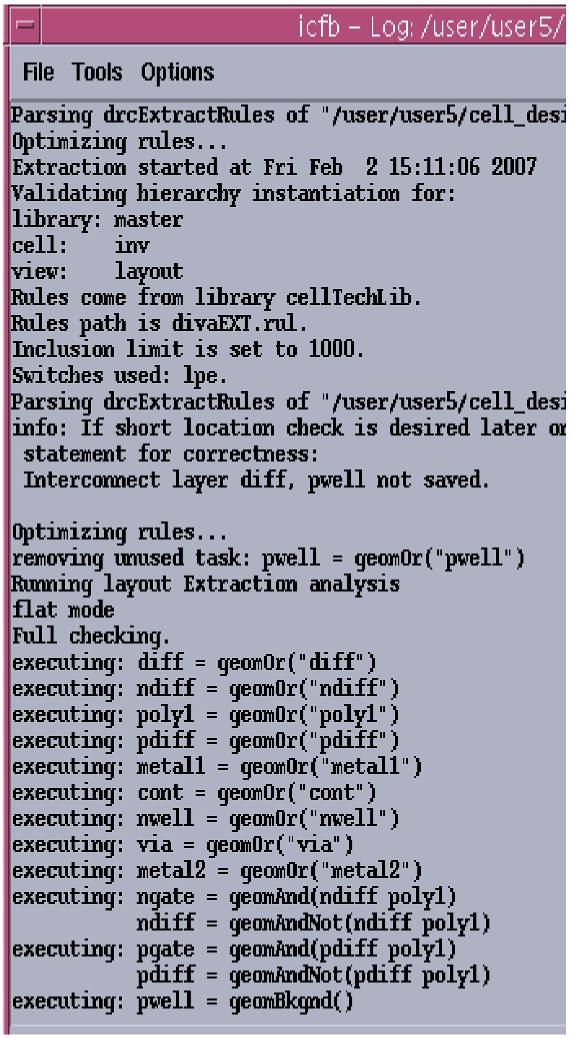
（2）参数提取运行后提示如下，



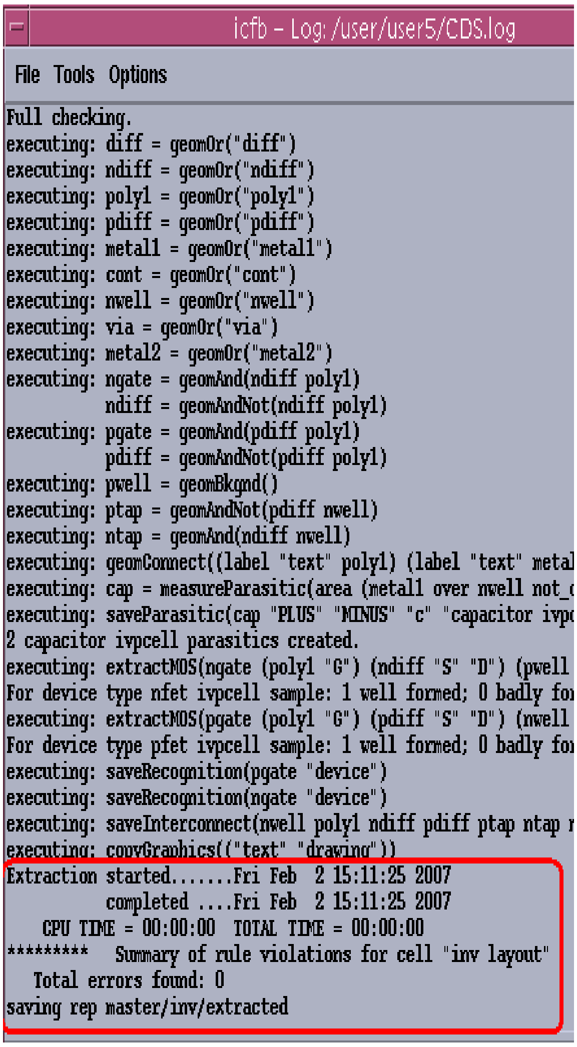
```
Parsing drcExtractRules of "/user/user5/cell_design/cellTechLib/divaEXT.rul"...
info: If short location check is desired later on, check the saveInterconnect
 statement for correctness:
 Interconnect layer diff, pwell not saved.

*WARNING* No such switch "extract_parasitic_caps" in the rules process flow.
Check the rules switch setting for correctness!
Errors exist in the rules file "/user/user5/cell_design/cellTechLib/divaEXT.rul".
Verification program terminated.
```

```
mouse L: mouseSingleSelectPt        M: leHiMousePopUp()         R: ivHiExtract()
>
```

红线区域提示提取过程被中断，出错原因是设置了错误的 switch，因为默认的规则文件中没有定义寄生电容提取的相关消息，因此，需要修正，重新单击菜单 verify -> extract ，在弹出的 EXTRACTOR 对话框中，更改 set switch ，规则文件显示有 lpe pre 两个，选择 lpe，单击 OK，运行情况如图



```
Parsing drcExtractRules of "/user/user5/cell_desi
Optimizing rules...
Extraction started at Fri Feb  2 15:11:06 2007
Validating hierarchy instantiation for:
library: master
cell:    inv
view:    layout
Rules come from library cellTechLib.
Rules path is divaEXT.rul.
Inclusion limit is set to 1000.
Switches used: lpe.
Parsing drcExtractRules of "/user/user5/cell_desi
info: If short location check is desired later or
 statement for correctness:
 Interconnect layer diff, pwell not saved.

Optimizing rules...
removing unused task: pwell = geomOr("pwell")
Running layout Extraction analysis
flat mode
Full checking.
executing: diff = geomOr("diff")
executing: ndiff = geomOr("ndiff")
executing: poly1 = geomOr("poly1")
executing: pdiff = geomOr("pdiff")
executing: metal1 = geomOr("metal1")
executing: cont = geomOr("cont")
executing: nwell = geomOr("nwell")
executing: via = geomOr("via")
executing: metal2 = geomOr("metal2")
executing: ngate = geomAnd(ndiff poly1)
           ndiff = geomAndNot(ndiff poly1)
executing: pgate = geomAnd(pdiff poly1)
           pdiff = geomAndNot(pdiff poly1)
executing: pwell = geomBkgnd()
```



```
Full checking.
executing: diff = geomOr("diff")
executing: ndiff = geomOr("ndiff")
executing: poly1 = geomOr("poly1")
executing: pdiff = geomOr("pdiff")
executing: metal1 = geomOr("metal1")
executing: cont = geomOr("cont")
executing: nwell = geomOr("nwell")
executing: via = geomOr("via")
executing: metal2 = geomOr("metal2")
executing: ngate = geomAnd(ndiff poly1)
           ndiff = geomAndNot(ndiff poly1)
executing: pgate = geomAnd(pdiff poly1)
           pdiff = geomAndNot(pdiff poly1)
executing: pwell = geomBkgnd()
executing: ptap = geomAndNot(pdiff nwell)
executing: ntap = geomAnd(ndiff nwell)
executing: geomConnect((label "text" poly1) (label "text" metal
executing: cap = measureParasitic(area (metal1 over nwell not_c
executing: saveParasitic(cap "PLUS" "MINUS" "c" "capacitor ivpc
2 capacitor ivpcell parasitics created.
executing: extractMOS(ngate (poly1 "G") (ndiff "S" "D") (pwell
For device type nfet ivpcell sample: 1 well formed; 0 badly for
executing: extractMOS(pgate (poly1 "G") (pdiff "S" "D") (nwell
For device type pfet ivpcell sample: 1 well formed; 0 badly for
executing: saveRecognition(pgate "device")
executing: saveRecognition(ngate "device")
executing: saveInterconnect(nwell poly1 ndiff pdiff ptap ntap r
executing: copyGraphics(("text" "drawing"))
Extraction started.......Fri Feb  2 15:11:25 2007
          completed ....Fri Feb  2 15:11:25 2007
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "inv layout"
   Total errors found: 0
saving rep master/inv/extracted
```

左图表示参数提取过程开始，右图红线区域表示参数提取过程完成，没有出现错误。

（3）接下来可以进行 LVS，单击菜单 verify -> LVS,弹出类似参数提取的 LVS 对话框，采用默认值即可进行 LVS。过程运行情况类似参数提取。

（4）至此，版图绘制后的相关 DRC、ERC、 LVS、 EXTRACT 操作完成。

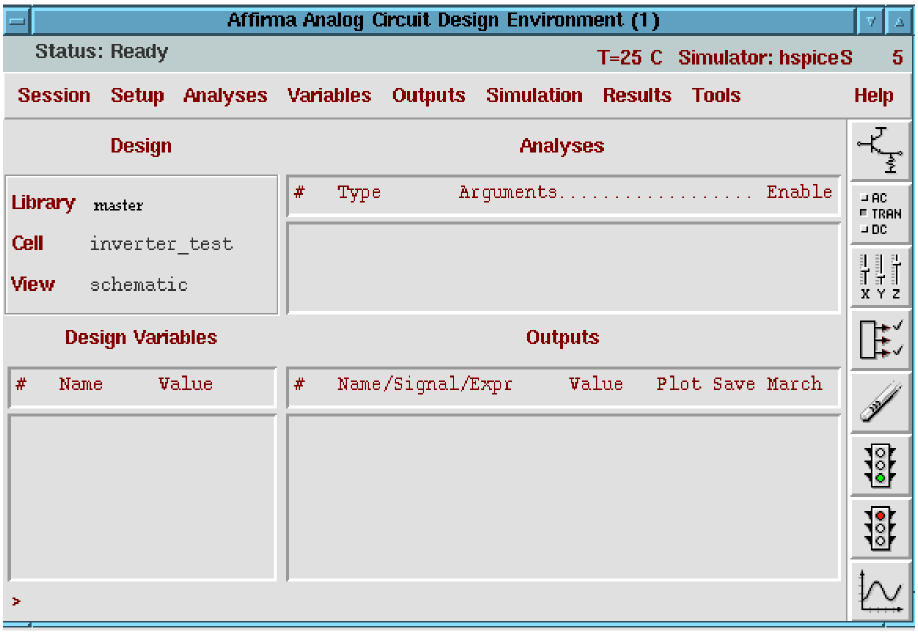
5. post layout simulation(后仿真)

作为设计的流程，之后还有一步 post layout simulation，即把提取的寄生参数，包含进原电路中，再次进行电路性能的模拟。

（1）在做 post layout simulation 之前，需要先对原电路创建一个 symbol，以建立原电路的 test view，为 master library 下的 inv 建立一个名字为 inverter_test 的 cellview 。具体操作过程完全类似 schematic 中，创建一个 schematic cellview ，此

处略去。

（2）使得 inverter_test cellview 处于可编辑状态，打开，单击菜单 tools-> analog environment



Affirma Analog Circuit Design Environment (1)
Session
Setup
Analyses
Variables
Outputs
Simulation
Results
Tools
Help
Design
Analyses
# Type Arguments.................. Enable
AC
TRAN
DC
X Y Z
Design Variables
# Name Value
Outputs
# Name/Signal/Expr Value Plot Save March
>

Status: Ready

T=25 C Simulator: hspiceS 5

Library master

Cell inverter_test

View schematic

(3) 以下的模拟过程完全类似之前实验中进行的性能模拟，只是在单击上图菜单 setup -> environment ，出现 environment options 对话框中，要把 extracted 添加进来。

（4）仿照之前的性能模拟，把寄生参数也包含进来，即可完成 post layout simulation.

6. 独立完成沟道长度均为 1um 的五管基本差分运算放大器版图的上述操作。（提示：相关文件可以采用机器上现有的文档，或者进行相应的修改后采用）

三. 思考题

1. 参数提取完成后，此时应该有几个 cellview ？

2. 在参数提取时，switch 由谁来确定，如何设置？

3. 浏览 divaDRC.rul ，divaERC.rul， divaLVS.rul ， divaEXT.rul 文档。

第四部分. 附件

(一)

Cadence Tutorial

The following Cadence CAD tools will be used in this tutorial:

- **Virtuoso Schematic** for schematic capture.
- **Analog Artist (Spectre)** for simulation.

Computer Account Setup

Please revisit Unix Tutorial before doing this new tutorial.

If you use Exceed from a PC you need to take care of this extra issue. The Cadence software has an annoying screen/refresh problem when run on a PC via Exceed. You need to do the following in order to solve the problem:
Under Xconfig -> Performance.

1. Enable Save Unders
2. Enable Change Maximum Backing Store to Always
3. Alter Default Backing Store to When Mapped
4. Alter Minimum Backing Store to When Mapped

You have to exit Exceed for the changes to take effect.

SETTING YOUR ENVIRONMENT UP FOR CADENCE AND ADDITIONAL TOOLS

In order to setup your environment to run Cadence applications you need to open an xterm window and type (EVERY TIME you login and in each window you want to run a Cadence tool)

```
. cdscdk2003
```

this script modifies your environment (sets PATH and exports variables). To see your current environment type the following at the prompt:

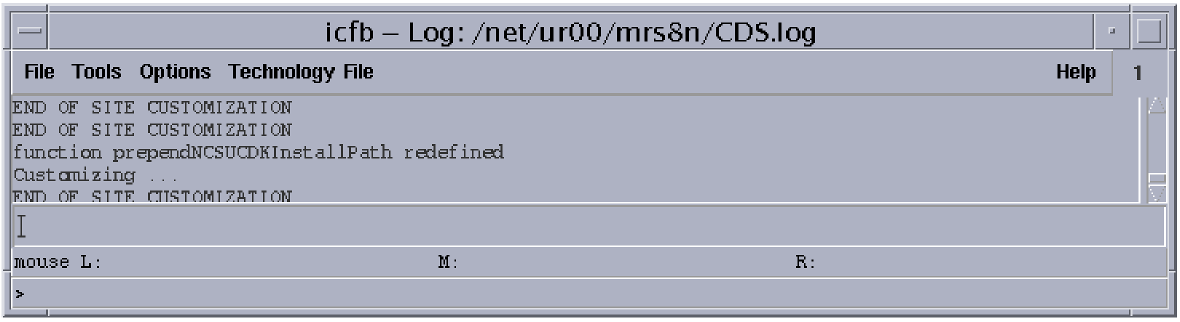
```
set
```

Running the Cadence tools

Now you should be able to run the Cadence tools. Never run Cadence from your root directory, it creates many extra files that will clutter your root. Instead please create a directory (e.g. cadence) and start Cadence there by typing:

```
mkdir cadence
cd cadence
icfb &
```

The command icfb & starts Cadence in the background and, after a couple of "update" messages that you can ignore for now (just click Continue) you should get a window with the **icfb Command Interpreter Window (CIW)** as below:

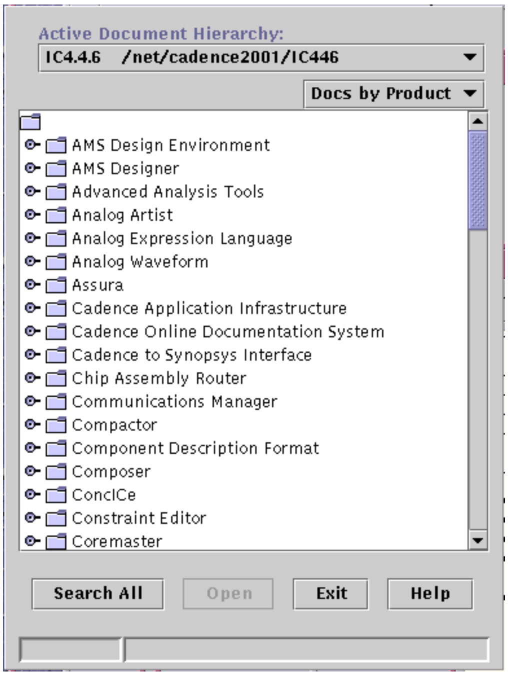


```
END OF SITE CUSTOMIZATION
END OF SITE CUSTOMIZATION
function prependNCSUCDKInstallPath redefined
Customizing ...
END OF SITE CUSTOMIZATION
```

```
mouse L:                    M:                    R:
>
```

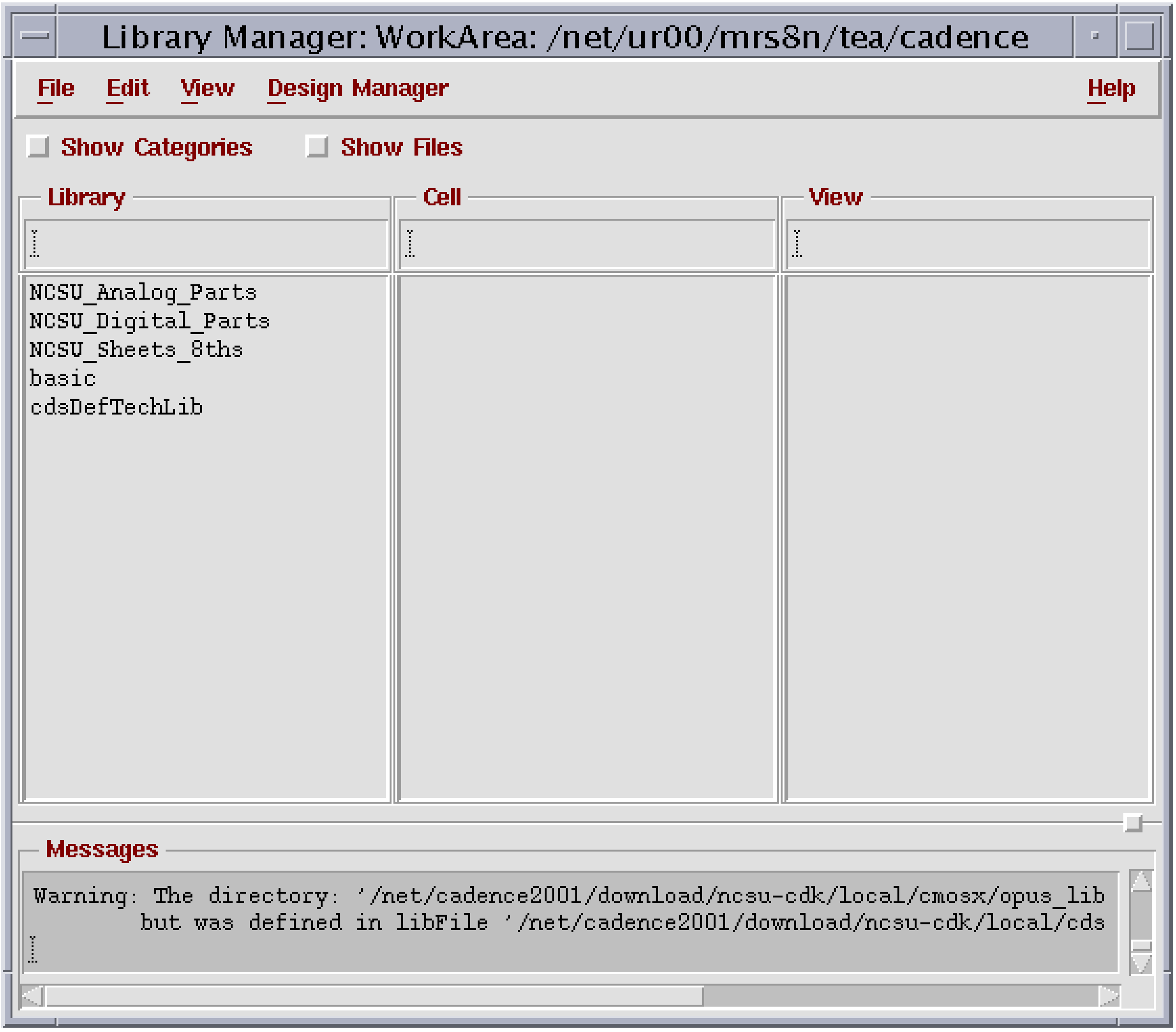
You will also get a "Cadence Update" window which you can read and then close or minimize. With the **CIW** you can launch other applications and you can also manage your files and libraries. **NEVER** use Unix commands (cp, mv) for moving Cadence design files as you may run into trouble later. For more information on the various Cadence tools I encourage you to read the corresponding user manuals. You can get to the manuals by pressing **Help -> Cadence Documentation** on any Cadence window (e.g. CIW). You can also open the on-line manuals by typing:

```
cdsdoc &
```



Spend some time browsing the manuals to understand what is available (a lot!). During the semester you will have to look for information in the on-line manuals to complement the (limited) info given by these tutorials.

You should also have the **Library Manager** window open:

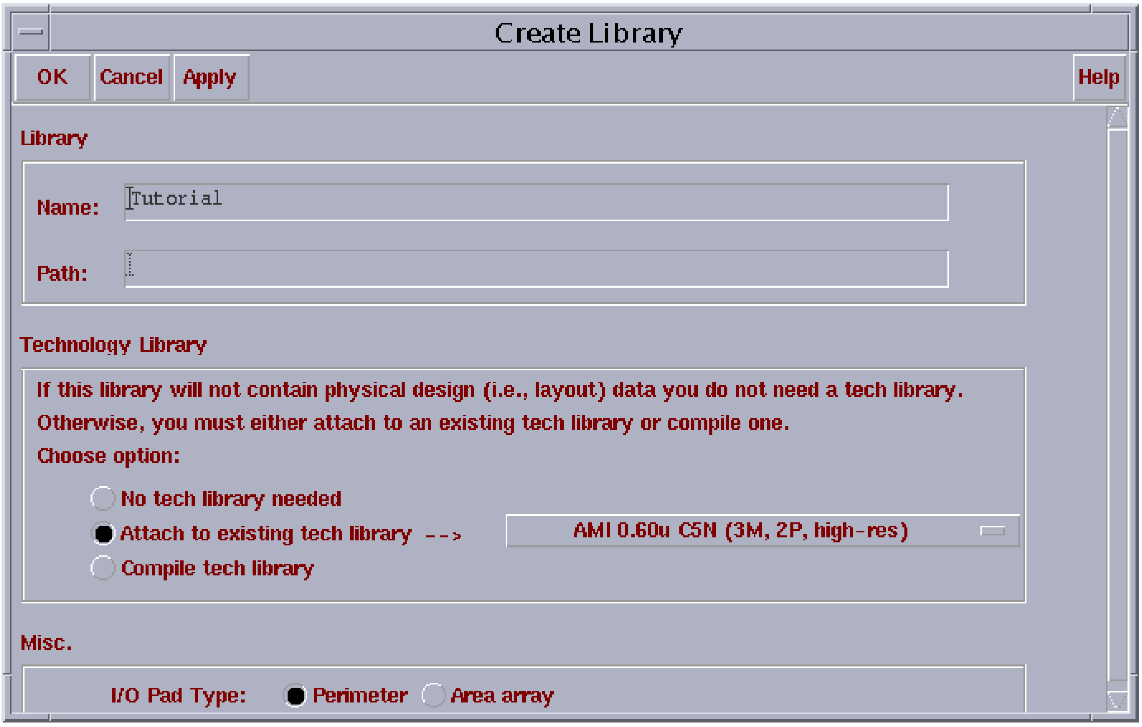


```
NCSU_Analog_Parts
NCSU_Digital_Parts
NCSU_Sheets_8ths
basic
cdsDefTechLib
```

```
Warning: The directory: '/net/cadence2001/download/ncsu-cdk/local/cmosx/opus_lib
         but was defined in libFile '/net/cadence2001/download/ncsu-cdk/local/cds
```

In case it's not open you can always go to Tools -> Library Manager on the Tools menu of the CIW.

Now we need to create a new library (to contain your circuits) so go to File -> New -> Library from the File menu of the Library Manager. Then fill in the name of the new library (e.g. Tutorial) in the dialog window, and leave the Path empty (this will create the library in the directory where you started icfb, you could also choose to set a path if you wanted another directory). Click on Attach to existing tech library and choose AMI 060u C5N (#M, 2P, high-res) from all the options. Leave I/O Pad Type as Perimeter then click OK.



Library

Name: Tutorial

Path:

Technology Library

If this library will not contain physical design (i.e., layout) data you do not need a tech library. Otherwise, you must either attach to an existing tech library or compile one.

Choose option:

○ No tech library needed
● Attach to existing tech library --> AMI 0.60u C5N (3M, 2P, high-res)
○ Compile tech library

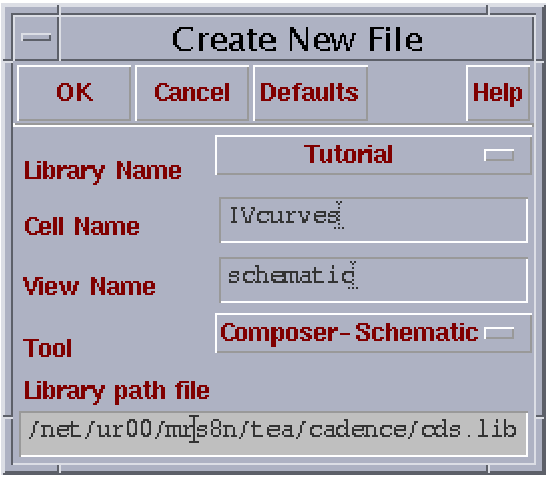
Misc.

I/O Pad Type: ● Perimeter ○ Area array

Now the Tutorial library should appear in the Library Manager window. Let's start our first schematic now!

SCHEMATIC CAPTURE

Start by clicking on the Tutorial library in the Library Manager window once, then go to **File -> New -> Cell View** and fill in with IVcurves as the cell name, schematic as the view name, and Composer - Schematic as the tool, then press OK.



Library Name: Tutorial

Cell Name: IVcurves

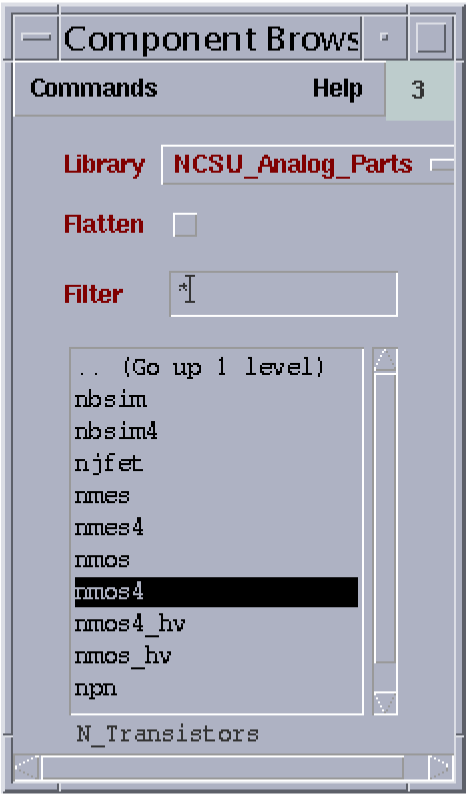
View Name: schematic

Tool: Composer-Schematic

Library path file: /net/ur00/mrs8n/tea/cadence/cds.lib

You should get the Virtuoso Schematic Editing window. Spend some time analyzing the window. On the left side you have various shortcuts to common used commands such as: placing component instances (looks like an IC), drawing wires, placing ports, stretching, copying, zooming in and out, saving, etc. If you pass the mouse pointer on top of the buttons you get short pop-up help messages. You also have access to these commands (and others) from the menu. It is not possible here to describe all the functionality of Virtuoso Schematic so you are strongly encouraged to read the on-line user manuals in cdsdoc.

Let's start our first schematic which will be used to plot I-V curves. Click on the Instance button (which looks somewhat like an IC, or go to Add -> Instance), this will pop-up two small windows, one being a Component Browser window. In this window choose NCSU_Analog_Parts as the library, click on N_Transistors, then on nmos4 (an NMOS transistor with all 4 terminals, G, S, D, B):



Component Brows

Commands Help 3

Library NCSU_Analog_Parts

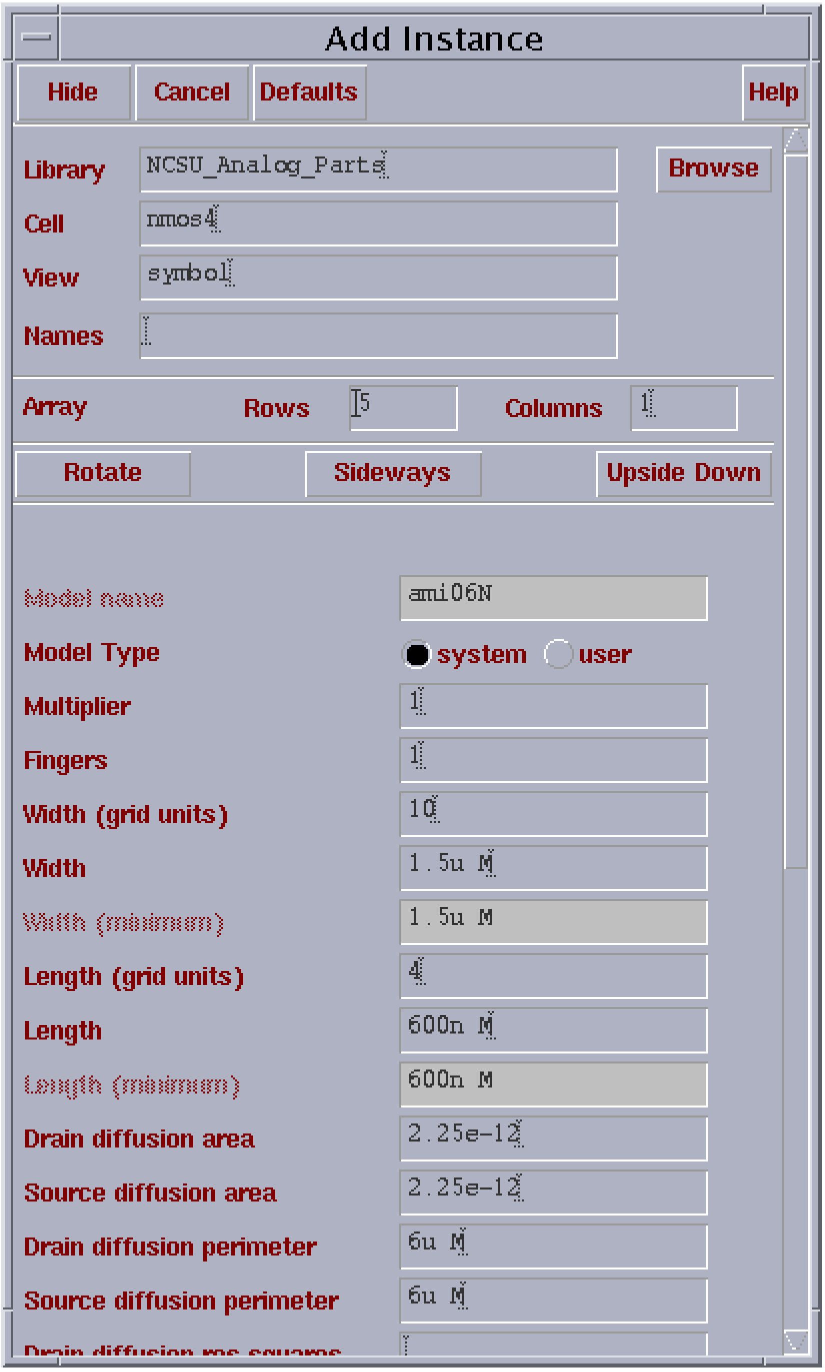
Flatten □

Filter *

.. (Go up 1 level)
nbsim
nbsim4
njfet
nmes
nmes4
nmos
nmos4
nmos4_hv
nmos_hv
npn

N_Transistors

These choices will automatically fill the other pop-up window, called the Add Instance window (you could also have filled this window directly). If you move the mouse now on top of the Virtuoso Schematic window you will see an "outline" (or ghost) of the transistor. You can move, rotate, flip this outline until you get what you want, then by clicking the left-mouse button you can place it in the schematic. You could place the transistors one by one but it's easier if you place multiple ones at a time if you know how many you need. For this part we need 5 transistors so please fill 5 for number of rows and let 1 as number of columns.

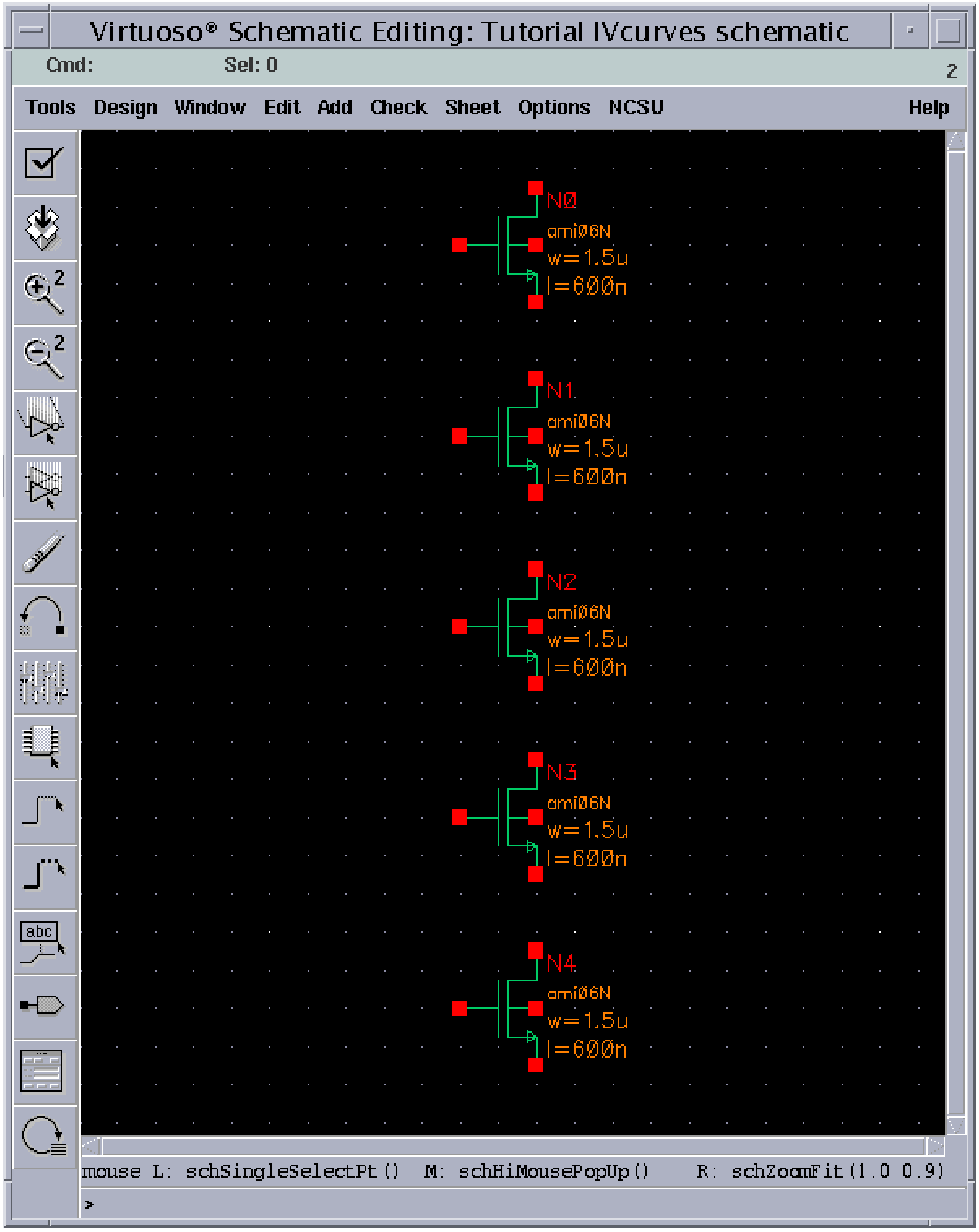


Library	NCSU_Analog_Parts
Cell	nmos4
View	symbol
Names	

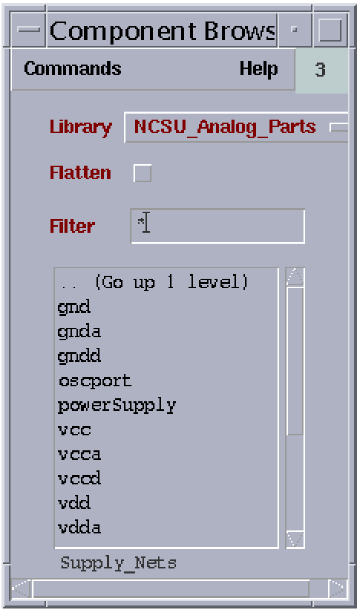
Array	Rows	5	Columns	1

Model name	ami06N
Model Type	● system ○ user
Multiplier	1
Fingers	1
Width (grid units)	10
Width	1.5u M
Width (minimum)	1.5u M
Length (grid units)	4
Length	600n M
Length (minimum)	600n M
Drain diffusion area	2.25e-12
Source diffusion area	2.25e-12
Drain diffusion perimeter	6u M
Source diffusion perimeter	6u M
Drain diffusion res squares	

Now you can place the 5 transistors by clicking on the left mouse button for the first transistor and then moving the mouse down and clicking again. Do that right now. If you make mistakes you can always go to Edit -> Undo and try again. You can press the ESC key on the keyboard to get out of the place instance mode or you can keep placing other parts.



You can also move, delete parts, please explore the different editing functions, you will only learn by making mistakes and then correcting them. Now we also need to add ports, wires and power supply. First let's add ground by clicking on Instance again and then choosing Supply-Nets and then gnd in the component browser window, then place one gnd below the 5 transistors.



Library NCSU_Analog_Parts

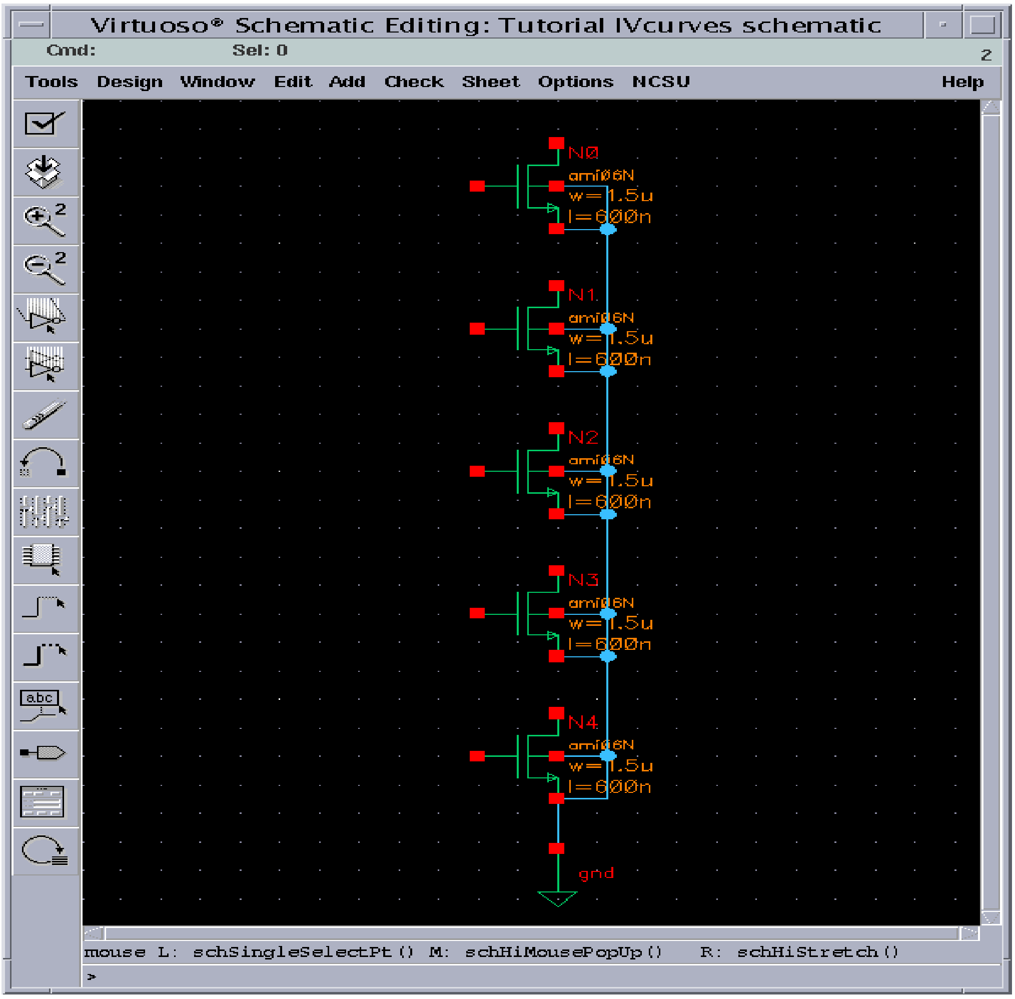
Flatten □

Filter *

```
.. (Go up 1 level)
gnd
gnda
gndd
oscport
powerSupply
vcc
vcca
vccd
vdd
vdda
```

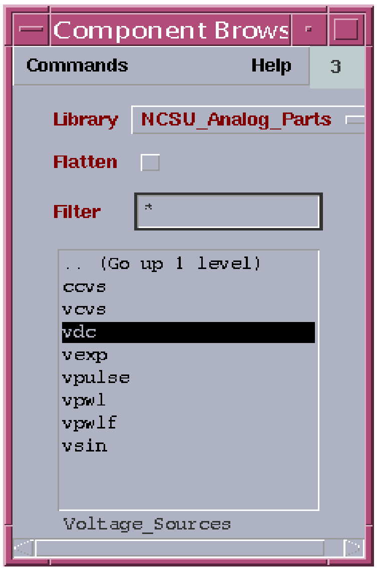
Supply_Nets

Then add wires (narrow) to connect all transistor sources and bodies to the ground.



```
mouse L: schSingleSelectPt() M: schHiMousePopUp()    R: schHiStretch()
>
```

Now add 6 DC voltage sources, one for VDS and one for each VGS and then connect them with wires to the transistors. Unfortunately we also need to add 5 more ″dummy″ voltage sources (with a value of 0 V) so that we can plot the currents in the transistors (it seems there is a bug with the transistor models right now and the transistor currents cannot be plotted directly). The DC voltage sources that we are going to use are in the Voltage_Sources directory with the name vdc. It's a good idea to save your design from time to time in case the system crashes :)



Library NCSU_Analog_Parts

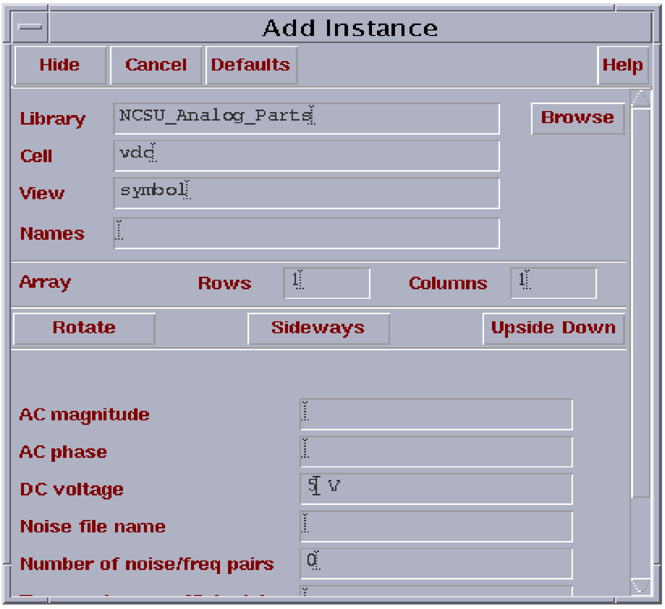
Flatten □

Filter *

```
.. (Go up 1 level)
ccvs
vcvs
vdc
vexp
vpulse
vpwl
vpwlf
vsin
```

Voltage_Sources

As you place each vdc source (you can place them one after the other, no need to click on Instance in-between) change the VGS power supplies to be 0.5, 0.75, 1, 1.25, 1.5 values to 5 V, 4 V, 3 V, 2 V, 1 V, respectively by filling the DC voltage property to the appropriate value:



Library NCSU_Analog_Parts

Cell vdc

View symbol

Names

Array Rows 1 Columns 1

AC magnitude

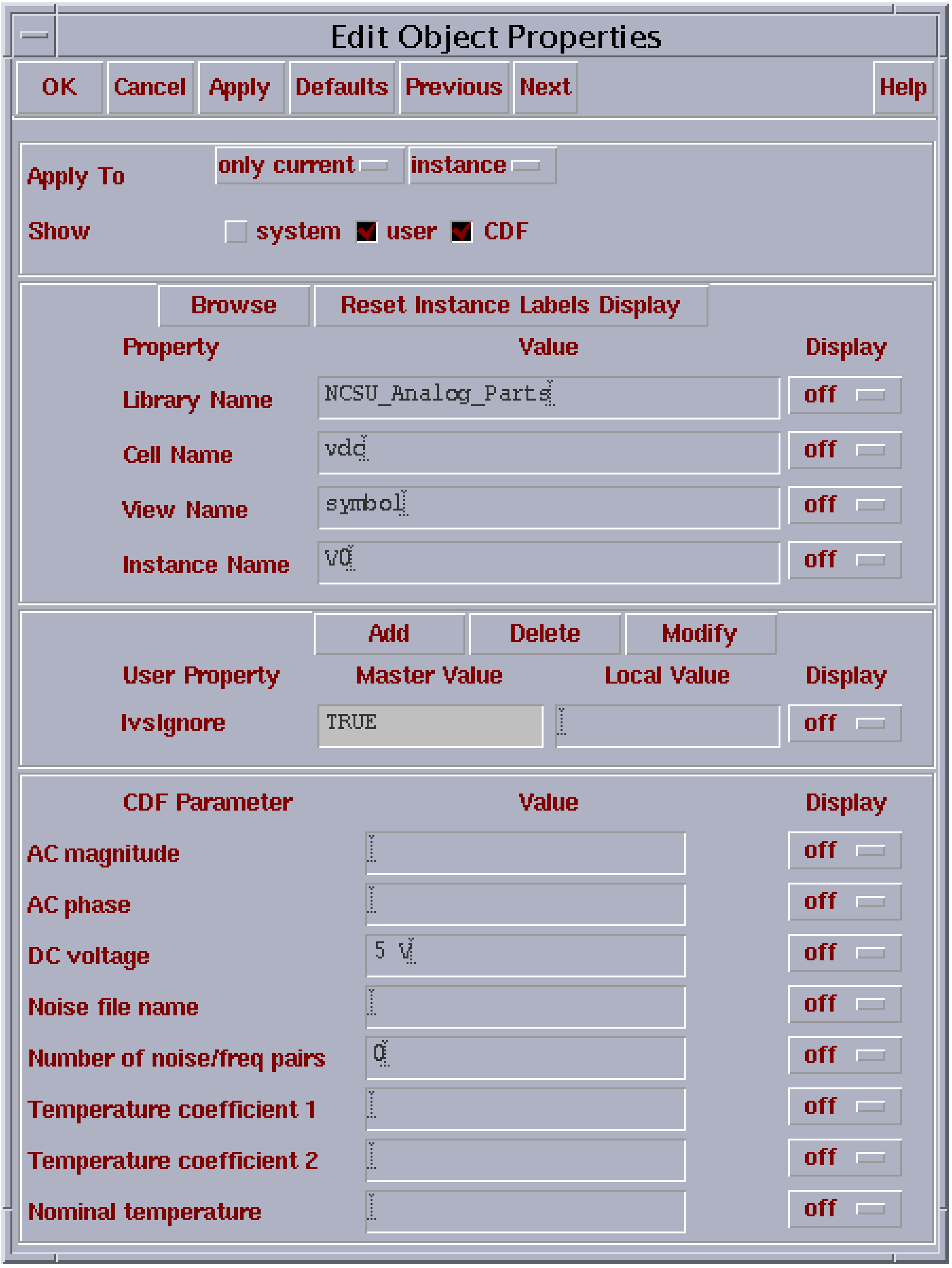
AC phase

DC voltage 5 V

Noise file name

Number of noise/freq pairs 0

Finally add the 5 dummy 0 V sources in series with the drains, and a voltage source vdc of 5 V for VDS. Press ESC to get out of the add instance mode. In case you made a mistake you can always go to Edit -> Undo, or you can correct your mistake by some form of edit. For example, if you filled in the wrong value for the DC voltage for vdc you can always change that later by first selecting the instance (click on it in the schematic) and then go to Edit -> Properties -> Objects, then a pop-up window will appear where you can change what you want:



Apply To: only current instance

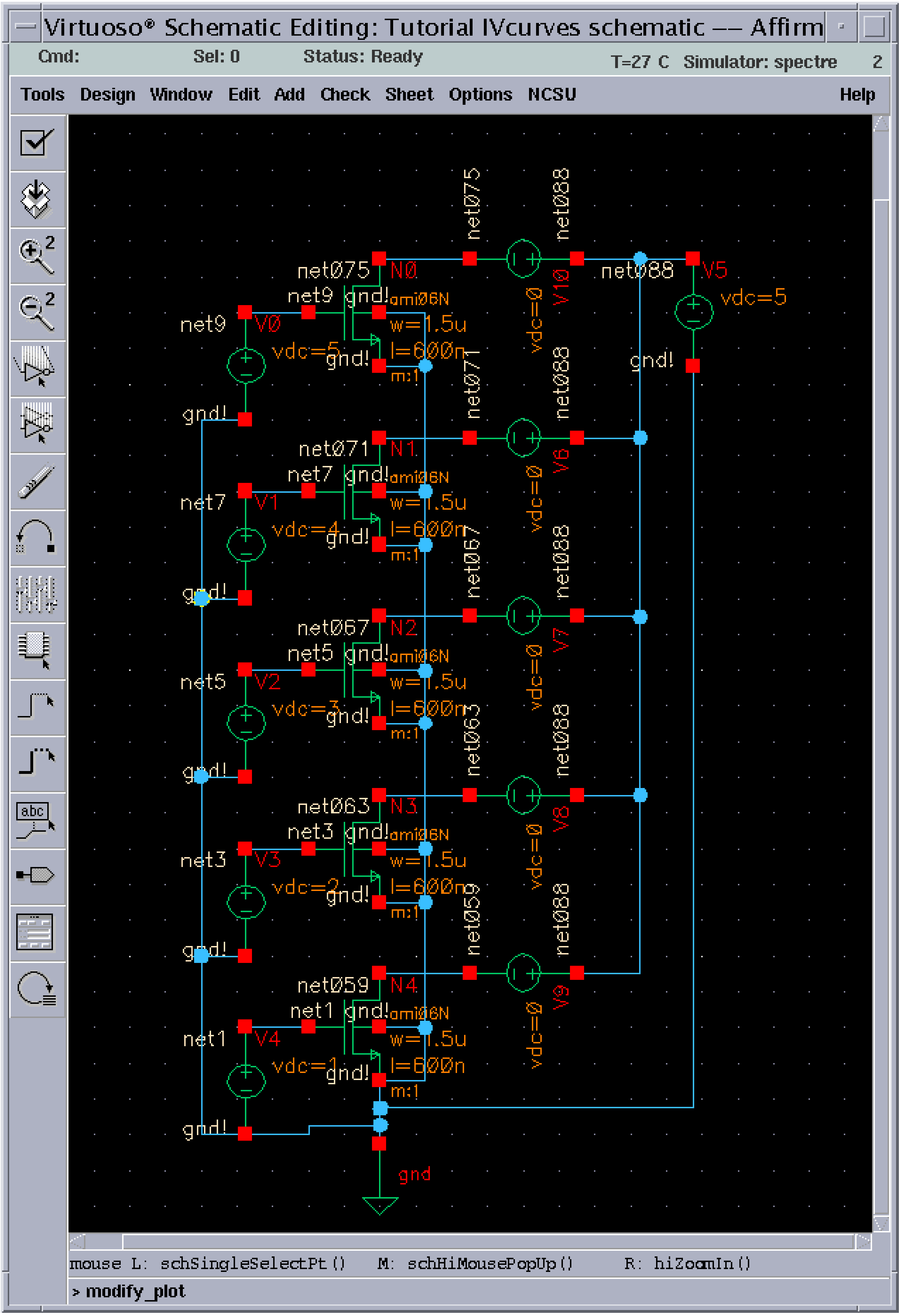
Show: □ system ☒ user ☒ CDF

Property	Value	Display
Library Name	NCSU_Analog_Parts	off
Cell Name	vdc	off
View Name	symbol	off
Instance Name	V0	off

User Property	Master Value	Local Value	Display
lvsIgnore	TRUE		off

CDF Parameter	Value	Display
AC magnitude		off
AC phase		off
DC voltage	5 V	off
Noise file name		off
Number of noise/freq pairs	0	off
Temperature coefficient 1		off
Temperature coefficient 2		off
Nominal temperature		off

The final schematic should look somewhat like this:



Virtuoso® Schematic Editing: Tutorial IVcurves schematic —— Affirm

Cmd: Sel: 0 Status: Ready T=27 C Simulator: spectre 2

mouse L: schSingleSelectPt() M: schHiMousePopUp() R: hiZoomIn()

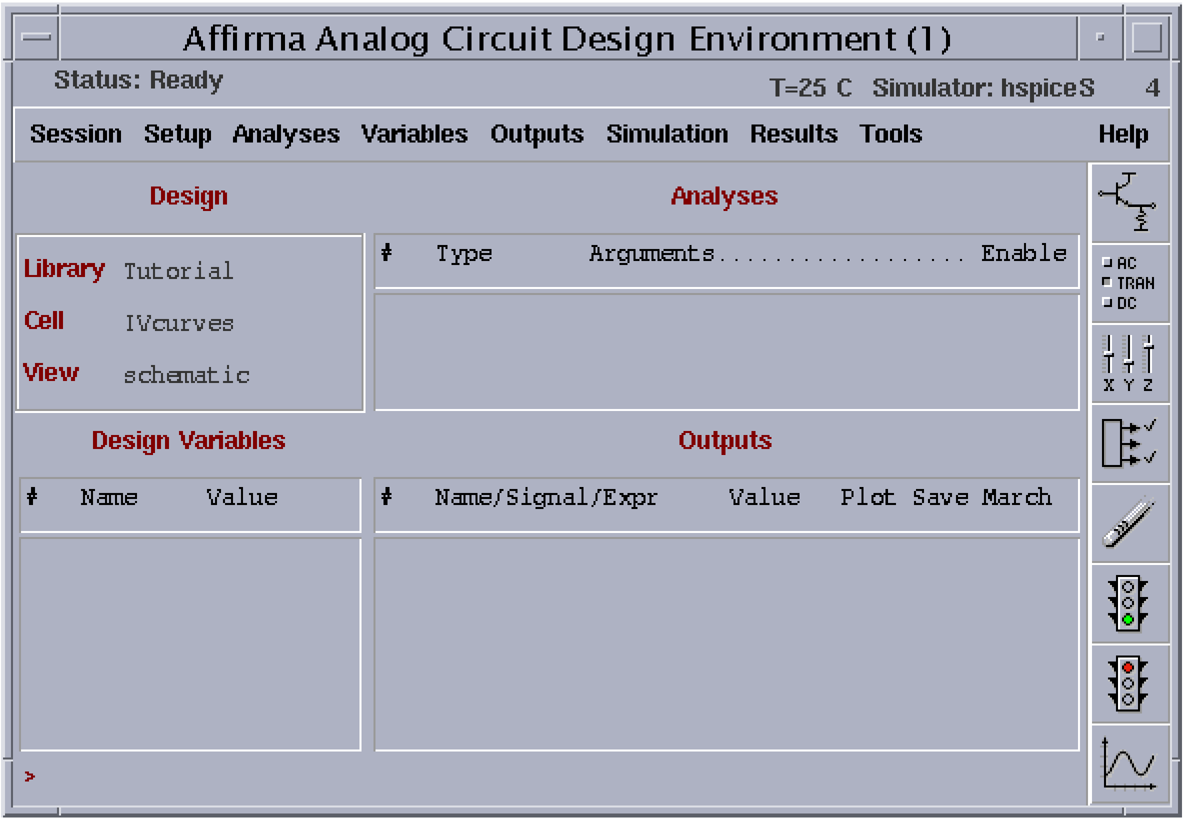
> modify_plot

Now you need to Check and Save your design (either the top left button or Design -> Check and Save). Make sure you look at the CIW window and there are no errors or warnings, if there are any you have to go back and fix them!

Assuming there are no errors we are now ready to start simulation!

SIMULATION

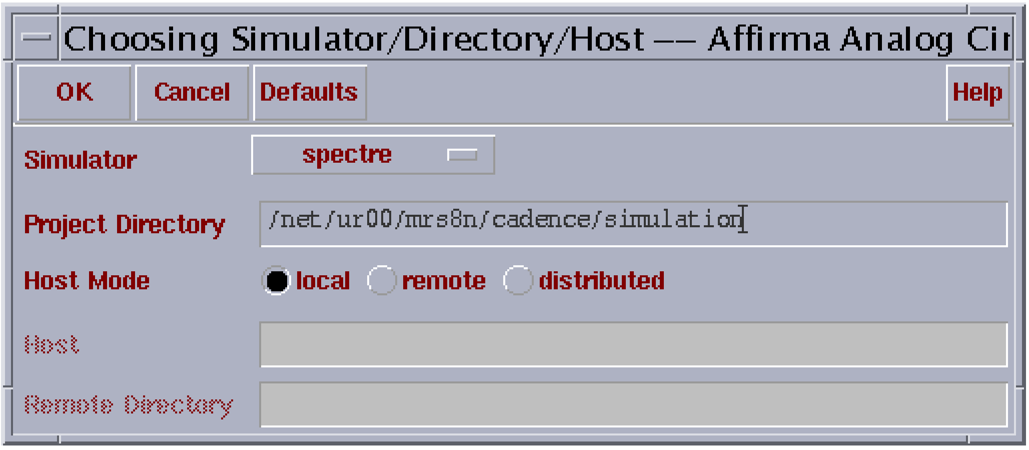
In the Virtuoso Schematic window go to Tools -> Analog Environment. There is going to the another "What's New" pop-up window that you can read and close or minimize. The design should be set to the right Library, Cell and View.



Affirma Analog Circuit Design Environment (1)
Status: Ready
T=25 C Simulator: hspiceS 4
Session Setup Analyses Variables Outputs Simulation Results Tools Help
Design
Analyses
# Type Arguments.................. Enable
AC
TRAN
DC
X Y Z
Design Variables
# Name Value
Outputs
# Name/Signal/Expr Value Plot Save March
>

Library Tutorial
Cell IVcurves
View schematic

First we need to choose the simulator, we will choose Spectre. Go to Setup -> Simulator/Directory/Host, and choose Spectre in the pop-up window, then click OK:



Choosing Simulator/Directory/Host –– Affirma Analog Cir

Simulator: spectre

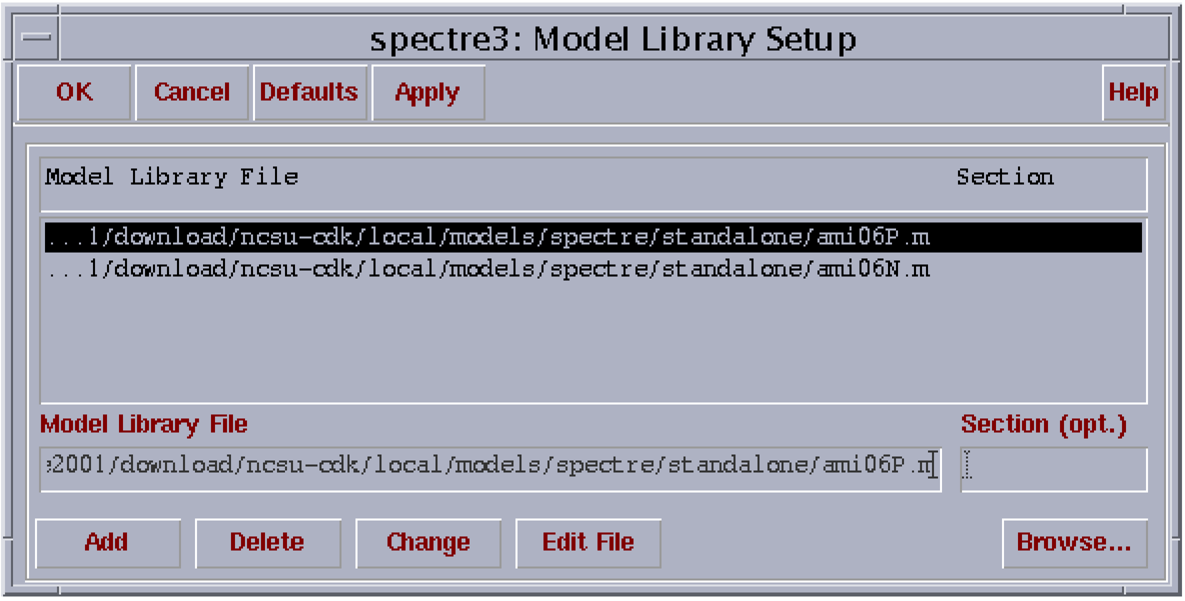
Project Directory: /net/ur00/mrs8n/cadence/simulation

Host Mode: ● local ○ remote ○ distributed

Host

Remote Directory

Go to Setup -> Model Libraries and choose (you can type directly or use Browse) /net/cadence2001/download/ncsu-cdk/local/models/spectre/standalone/ami06N.m then click Add (this is important, don't forget to do it), which adds the model for the NMOS, then /net/cadence2001/download/ncsu-cdk/local/models/spectre/standalone/ami06P.m and click Add again, which adds the model for the PMOS, then OK.



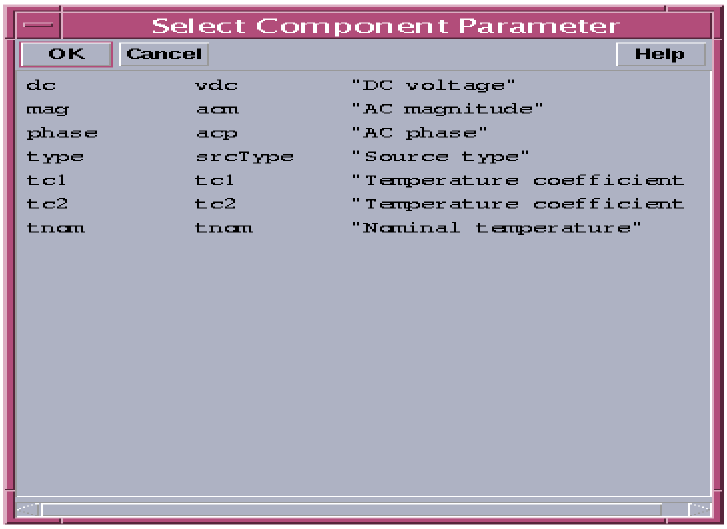
spectre3: Model Library Setup

Model Library File	Section
...1/download/ncsu-cdk/local/models/spectre/standalone/ami06P.m	
...1/download/ncsu-cdk/local/models/spectre/standalone/ami06N.m	

Model Library File: :2001/download/ncsu-cdk/local/models/spectre/standalone/ami06P.m

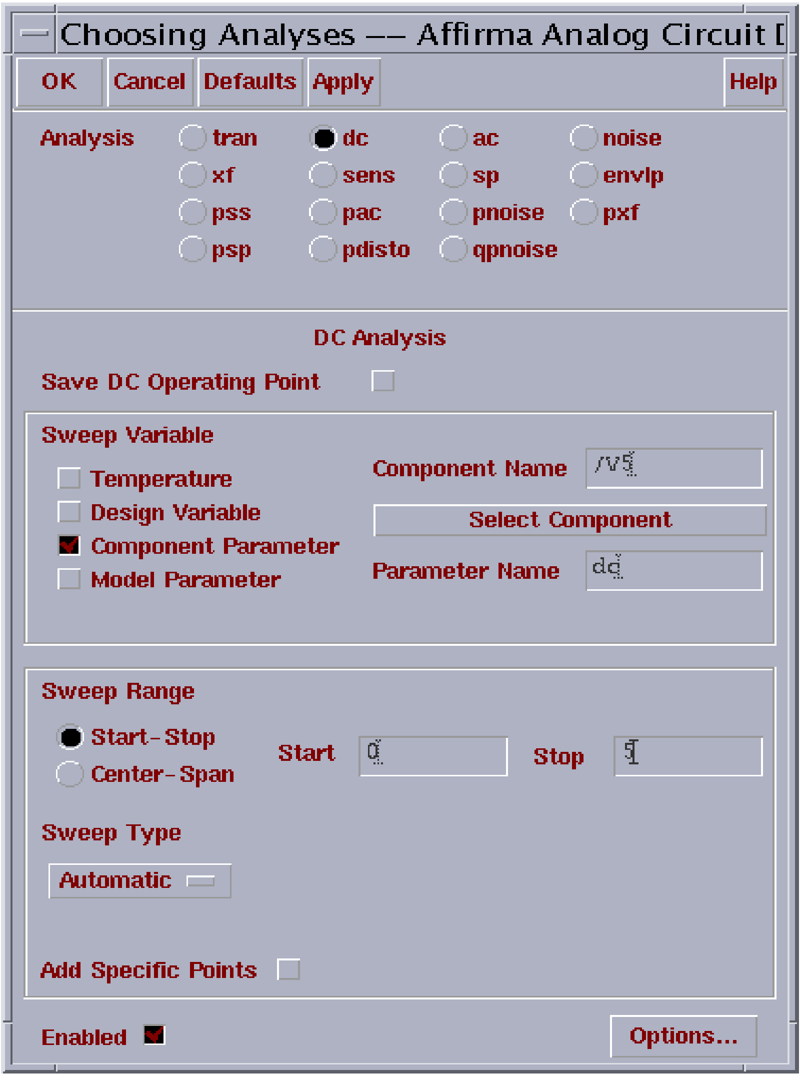
Section (opt.):

Now you need to choose the type of simulation, go to Analyses -> Choose... In this case we will choose a dc-sweep so click on the dc radio button, then on Component Parameter, then on Select Component (all of these in the Choosing Analyses dialog window) then on the VDS component in the schematic window and choose dc in the Select Component Parameter pop-up window and click OK.



```
dc          vdc        "DC voltage"
mag         acm        "AC magnitude"
phase       acp        "AC phase"
type        srcType    "Source type"
tc1         tc1        "Temperature coefficient
tc2         tc2        "Temperature coefficient
tnom        tnom       "Nominal temperature"
```

After this choose Start-Stop and 0 as the start value and 5 as the stop value, Automatic as a Sweep Type (this will do a dc sweep of VDS from 0V to 5 V). Then press OK.



Analysis ○ tran ● dc ○ ac ○ noise
○ xf ○ sens ○ sp ○ envlp
○ pss ○ pac ○ pnoise ○ pxf
○ psp ○ pdisto ○ qpnoise

DC Analysis

Save DC Operating Point □

Sweep Variable

□ Temperature
□ Design Variable
☑ Component Parameter
□ Model Parameter

Component Name /V5

Parameter Name dc

Sweep Range

● Start-Stop
○ Center-Span

Start 0 Stop 5

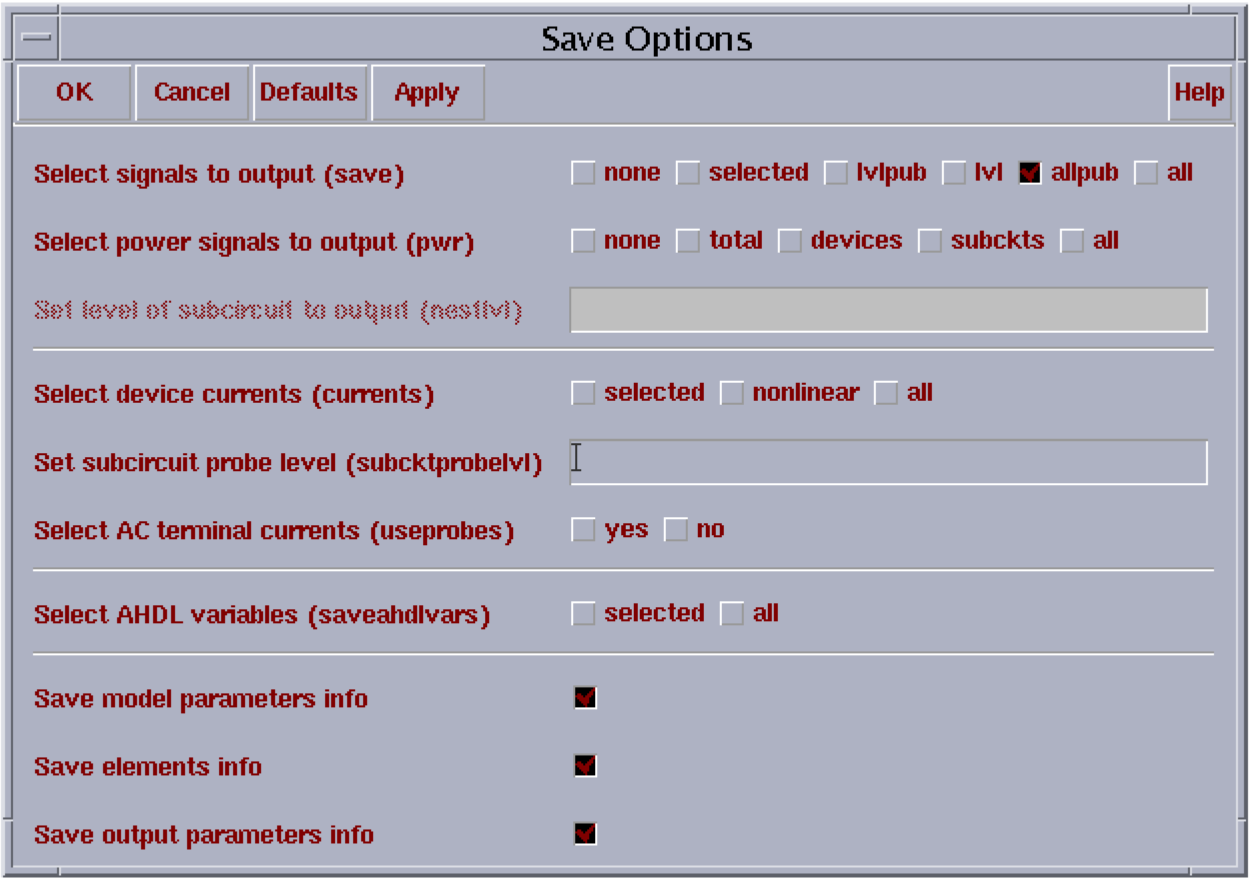
Sweep Type

Automatic

Add Specific Points □

Enabled ☑

Now go to Outputs -> Save All and click on allpub for signals to save (default). In general, for large schematics, you want to save only a subset of signals so that you save computing resources, but this schematic is small enough that it is OK to just save all. Click OK.



Select signals to output (save) □ none □ selected □ lvlpub □ lvl ☑ allpub □ all

Select power signals to output (pwr) □ none □ total □ devices □ subckts □ all

Set level of subcircuit to output (nestlvl)

Select device currents (currents) □ selected □ nonlinear □ all

Set subcircuit probe level (subcktprobelvl)

Select AC terminal currents (useprobes) □ yes □ no

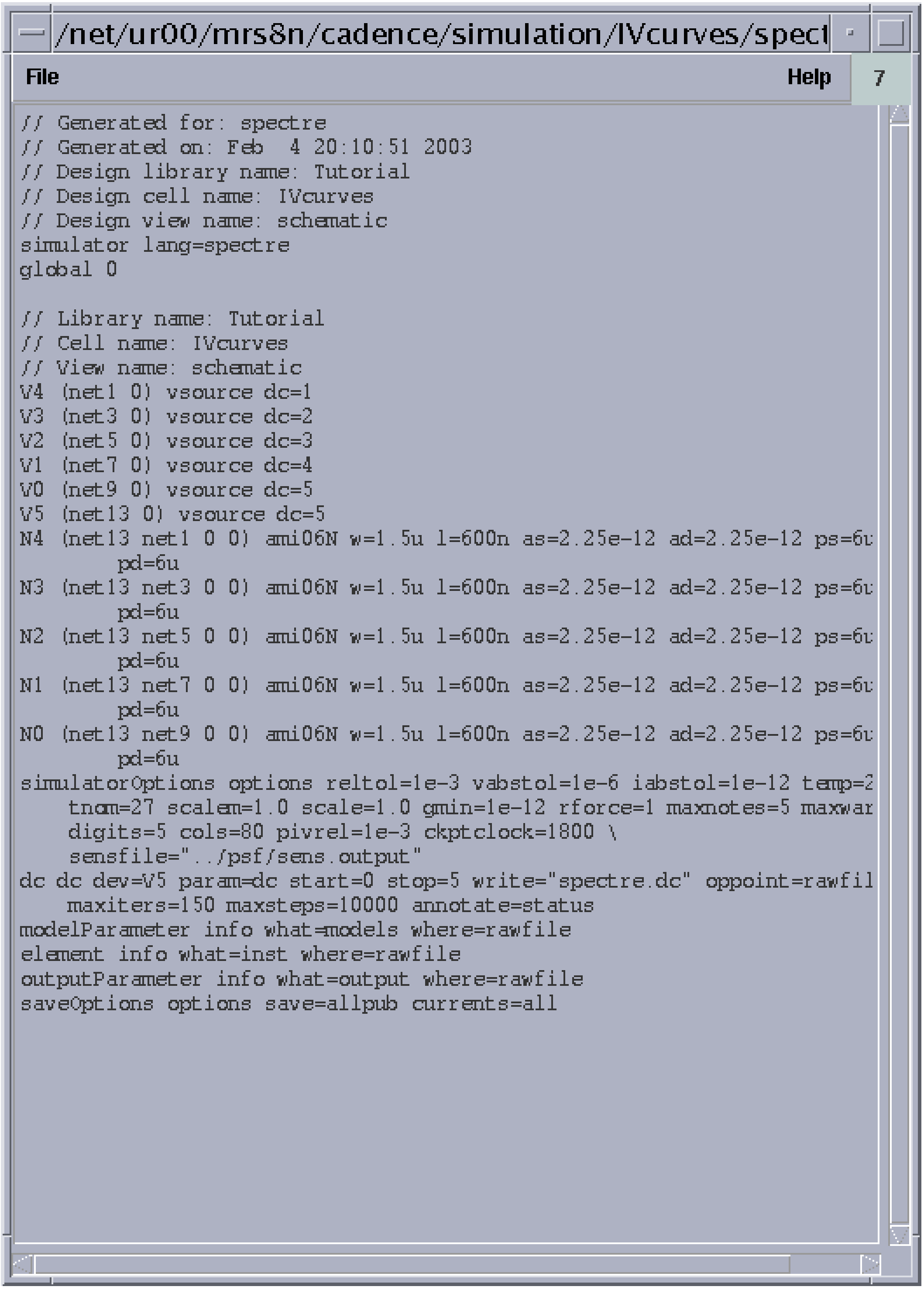
Select AHDL variables (saveahdlvars) □ selected □ all

Save model parameters info ☑

Save elements info ☑

Save output parameters info ☑

Now we can finally simulate! Click on the Netlist and Run button (looks like a green light) on the right or go to Simulation -> Netlist and Run. Click OK on the Welcome to Spectre window which should start the simulation (click OK to the pop-up window that says Welcome to Spectre). In case there are no errors you should get something like this:

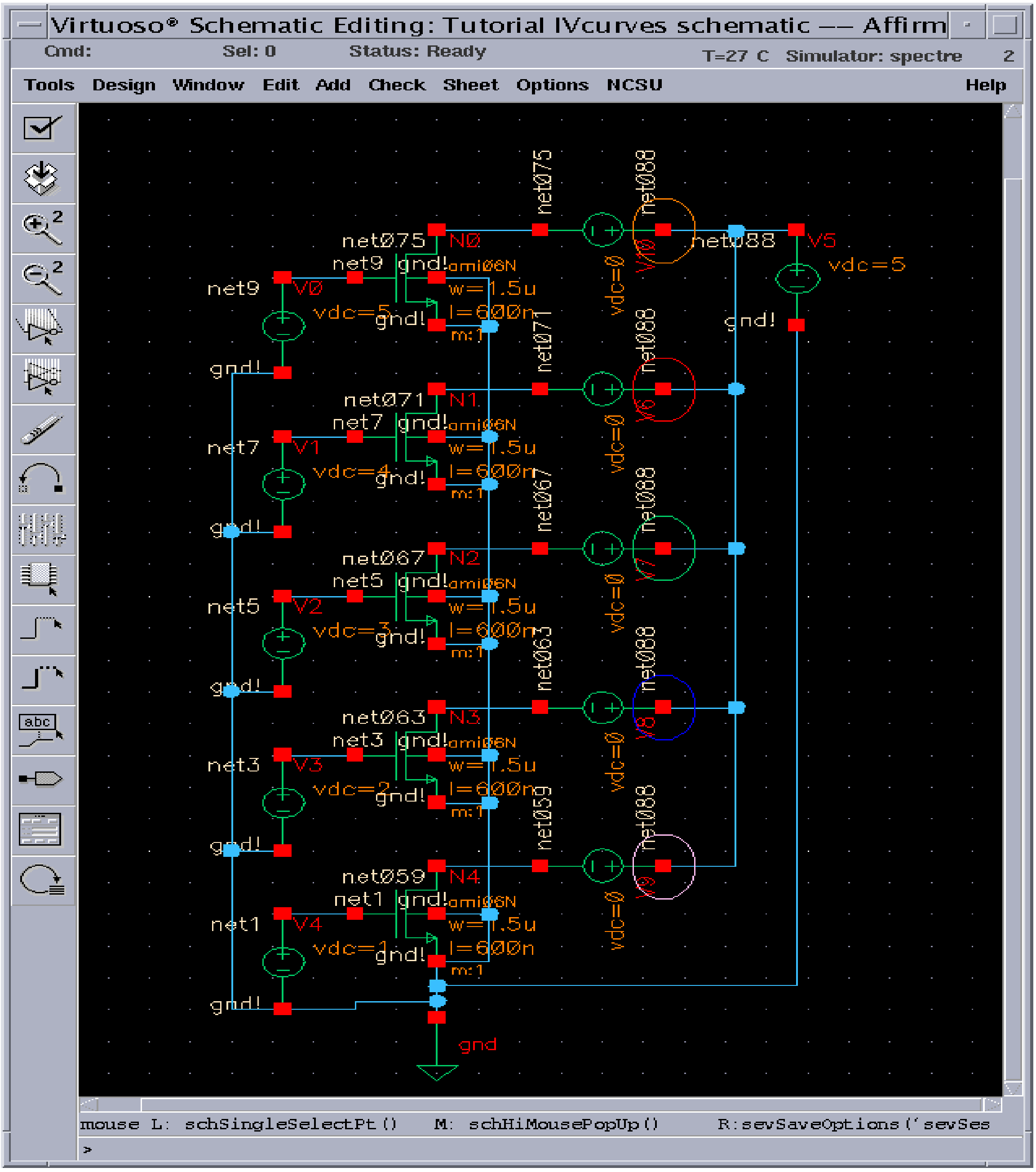


```
// Generated for: spectre
// Generated on: Feb  4 20:10:51 2003
// Design library name: Tutorial
// Design cell name: IVcurves
// Design view name: schematic
simulator lang=spectre
global 0

// Library name: Tutorial
// Cell name: IVcurves
// View name: schematic
V4 (net1 0) vsource dc=1
V3 (net3 0) vsource dc=2
V2 (net5 0) vsource dc=3
V1 (net7 0) vsource dc=4
V0 (net9 0) vsource dc=5
V5 (net13 0) vsource dc=5
N4 (net13 net1 0 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u
        pd=6u
N3 (net13 net3 0 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u
        pd=6u
N2 (net13 net5 0 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u
        pd=6u
N1 (net13 net7 0 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u
        pd=6u
N0 (net13 net9 0 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u
        pd=6u
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=2
    tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwar
    digits=5 cols=80 pivrel=1e-3 ckptclock=1800 \
    sensfile="../psf/sens.output"
dc dc dev=V5 param=dc start=0 stop=5 write="spectre.dc" oppoint=rawfil
    maxiters=150 maxsteps=10000 annotate=status
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
saveOptions options save=allpub currents=all
```

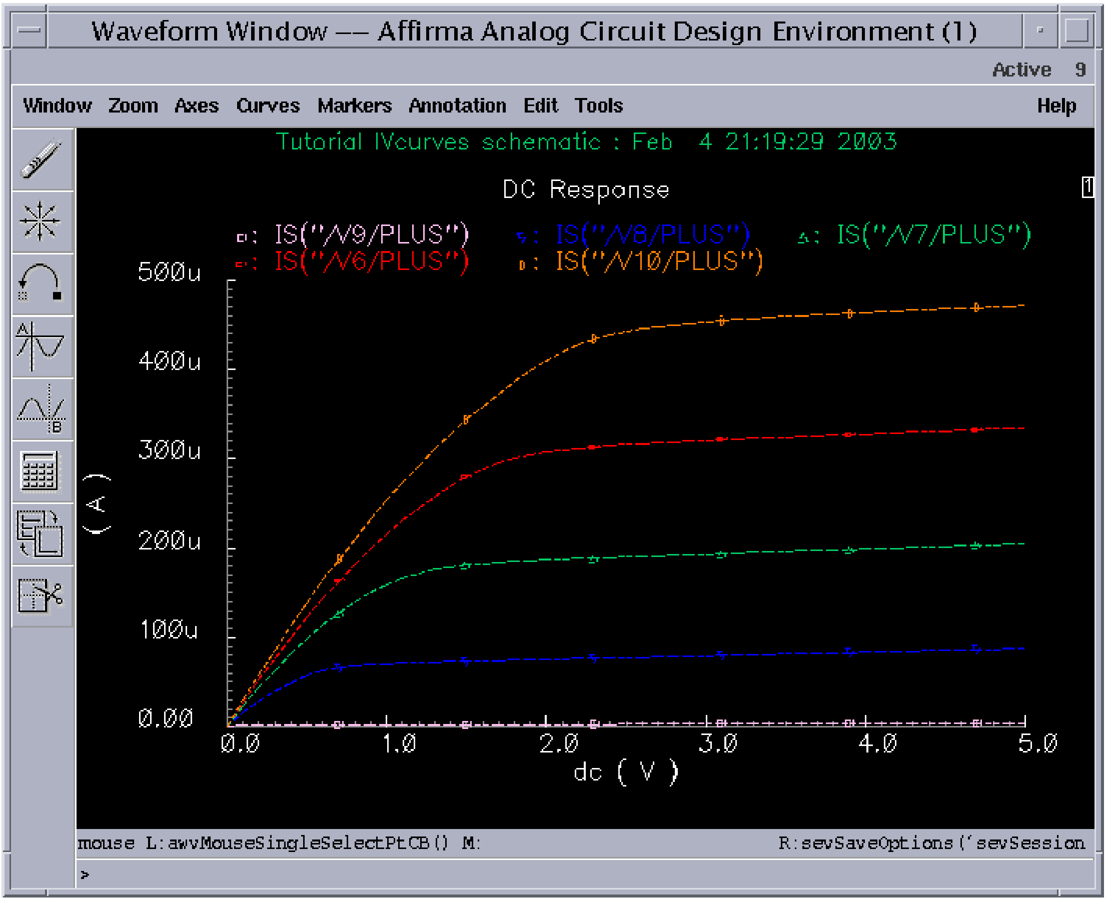
In case you have errors you will need to go back and correct them. This can be tricky! You may need to do Simulation -> Netlist -> Recreate if you change the schematic.

CAUTION Each time you change the schematic you have to do Check and Save!.

Assuming there are no errors you can now admire the simulation results. Go to Results -> Direct Plot -> DC which will pop-up your schematic window. Now you have to click on the signals you want to see. Since this is a dc-sweep we want to see the drain currents into the 5 transistors. In order to do this you have to click on the small red square at + terminal of each of the dummy power supplies in series with each drain. Make sure you click on the red square (the pin) which means current, versus any other part which means net, or voltage. Click on all 5 power supplies. If you are pressing right on the pins a circle should appear around each chosen pin.

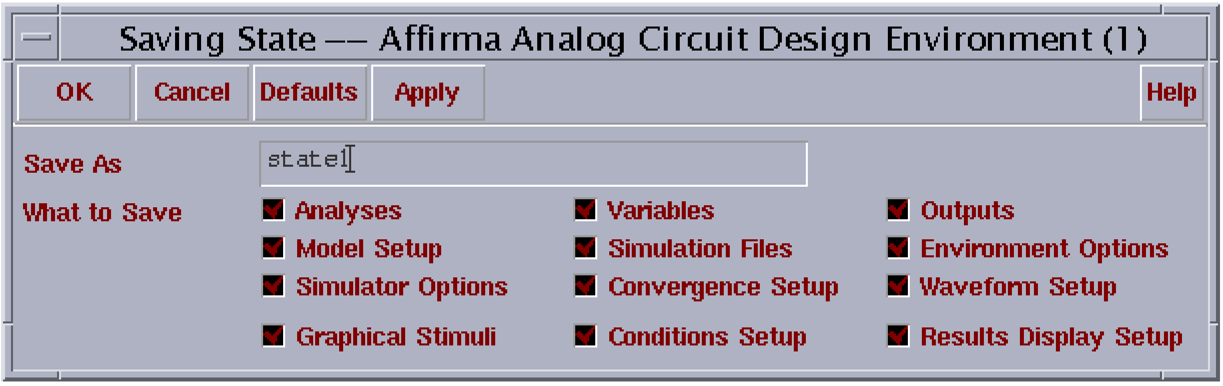


Now press on the ESC key (to finish choosing the signals) and you should finally get the desired simulation results, 5 glorious IV curves as in the textbook!


Waveform Window –– Affirma Analog Circuit Design Environment (1)
Active 9
Window Zoom Axes Curves Markers Annotation Edit Tools Help
Tutorial IVcurves schematic : Feb 4 21:19:29 2003
DC Response
IS("/V9/PLUS")
IS("/V8/PLUS")
IS("/V7/PLUS")
IS("/V6/PLUS")
IS("/V10/PLUS")
500u
400u
300u
200u
100u
0.00
(A)
0.0
1.0
2.0
3.0
4.0
5.0
dc (V)

```
mouse L:awvMouseSingleSelectPtCB() M:                R:sevSaveOptions('sevSession
>
```

It's a good idea to save the state of your simulation before you exit the simulation window. You can do that by going to Session -> Save State. This will be helpful if you want to redo any of the simualations without having to re-enter everything from scratch.


Saving State –– Affirma Analog Circuit Design Environment (1)
OK
Cancel
Defaults
Apply
Help

Save As: state1

What to Save:

☑ Analyses ☑ Variables ☑ Outputs
☑ Model Setup ☑ Simulation Files ☑ Environment Options
☑ Simulator Options ☑ Convergence Setup ☑ Waveform Setup
☑ Graphical Stimuli ☑ Conditions Setup ☑ Results Display Setup

PRINTING AND PLOTTING

To print the schematic in Virtuoso Schematic from the menu bar along the top, go to Design -> Plot -> Submit. On this menu there are a lot of options, so you can print a lot of ways. Click on help for more details. What I usually do is to write the schematic to a postscript file, then print, in this way you can have access to the file in the future without having to start Cadence:

1. uncheck Plot With header (if checked)
2. click on plot options - another form pops up
3. check Center Plot
4. click on Fit To Page
5. check Send Plot Only to File, enter a file path, e.g., ./schem.ps
6. uncheck Mail Log To (if checked)
7. click OK on the second window, click OK on the first window

You can look at you postscript before printing by:

1. at the command prompt: ghostview filepath/filename &, e.g., ghostview ./schem.ps

Now you can use the ps file in any soft document you create, or you can print a hardcopy:

1. at the command prompt: lpr -Pprintername filename, e.g., lpr -Pthn_l1 ./schem.ps

If your plot doesn't come out as you want it, click help on both windows for a more detailed explanation.

To print a Waveform, on the waveform viewer menu do Window->Hardcopy. Same as above, create a postscript, then print it.

1. uncheck header
2. change Paper Size to 8x8 inches
3. check Send Plot Only to File, enter a file path, e.g., ./sim.ps
4. uncheck Mail Log To
5. click OK on the window

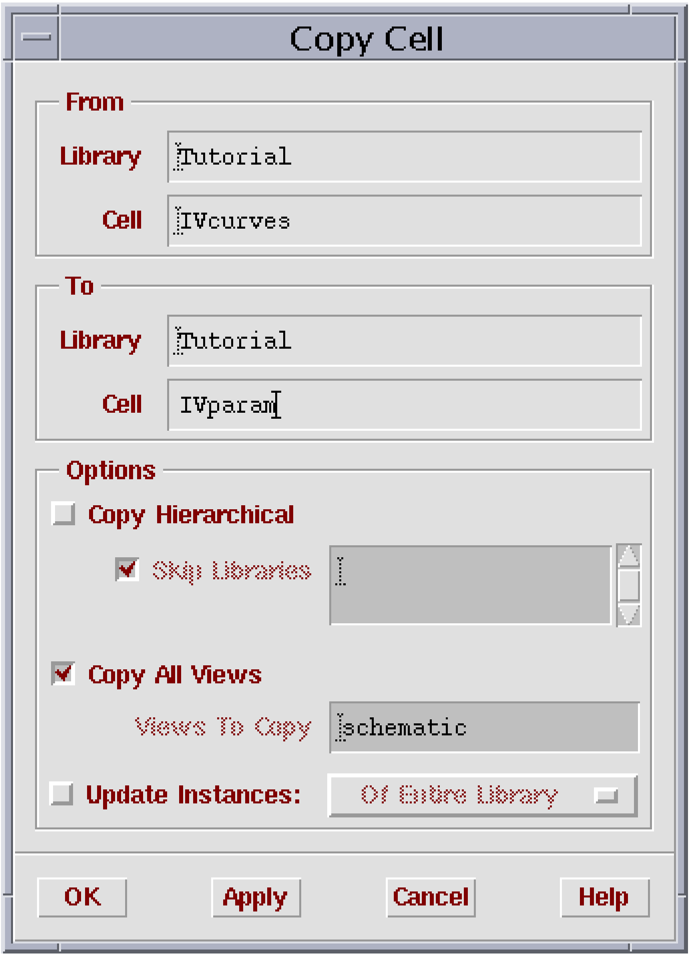
then do the same as you did for the schematic to print the hardcopy.

PARAMETRIC SIMULATION

After this long and tedious way to do things you will learn a faster way to do the same type of simulation as before. The idea is to understand that as an engineer you have many choices about how to achieve a desired result, and having more knowledge in general helps with finding a faster solution!

Until now we used multiple devices (5) in order to obtain the family of IV curves. We can achieve the same results by using a single transistor for which we change the voltage VGS. Close the Analog Environment and the IVcurves schematic and let's start another schematic, IVparam.

Instead of starting from scratch we will start from the IVcurves old schematic. In the Library Manager window right mouse click on the IVcurves cell and choose Copy... Fill in IVparam as the name of the destination cell in the Copy Cell pop-up window.



Copy Cell

From

Library: Tutorial

Cell: IVcurves

To

Library: Tutorial

Cell: IVparam

Options

□ Copy Hierarchical

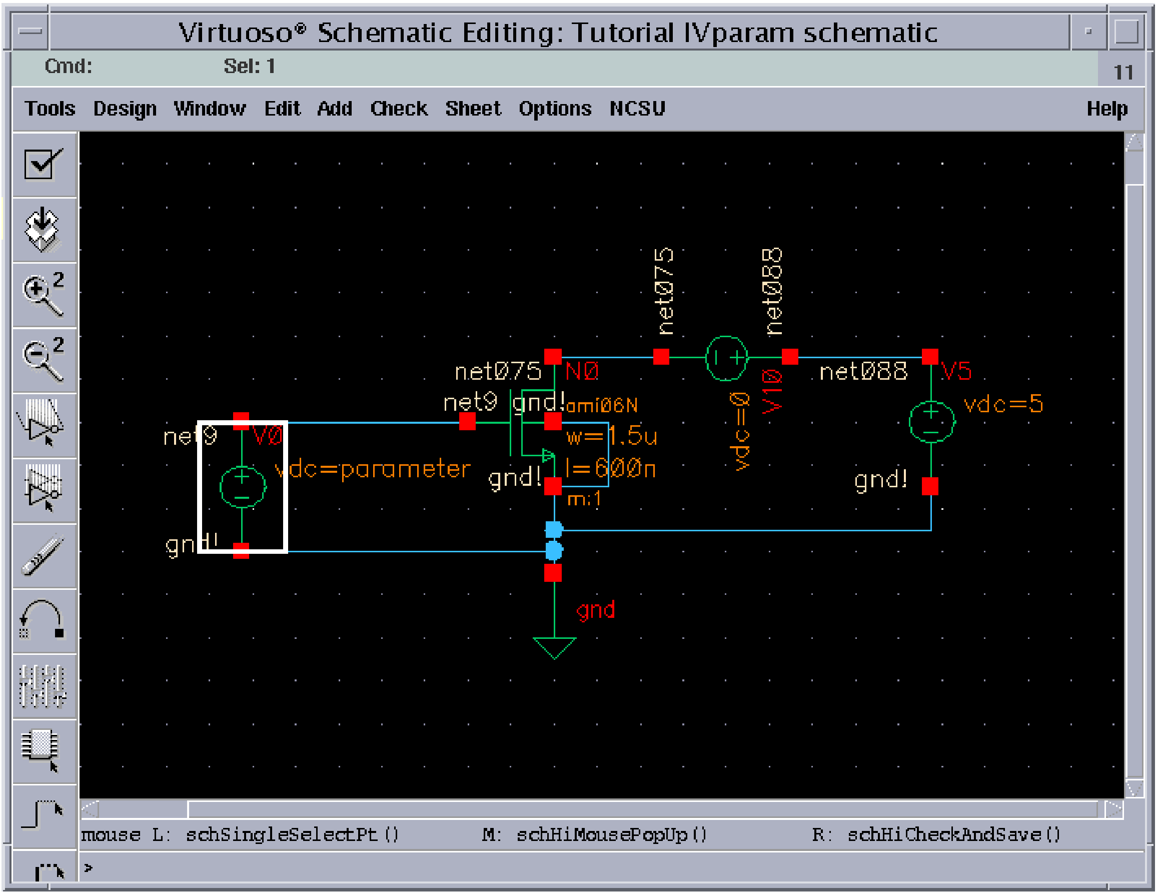
☑ Skip Libraries

☑ Copy All Views

Views To Copy: schematic

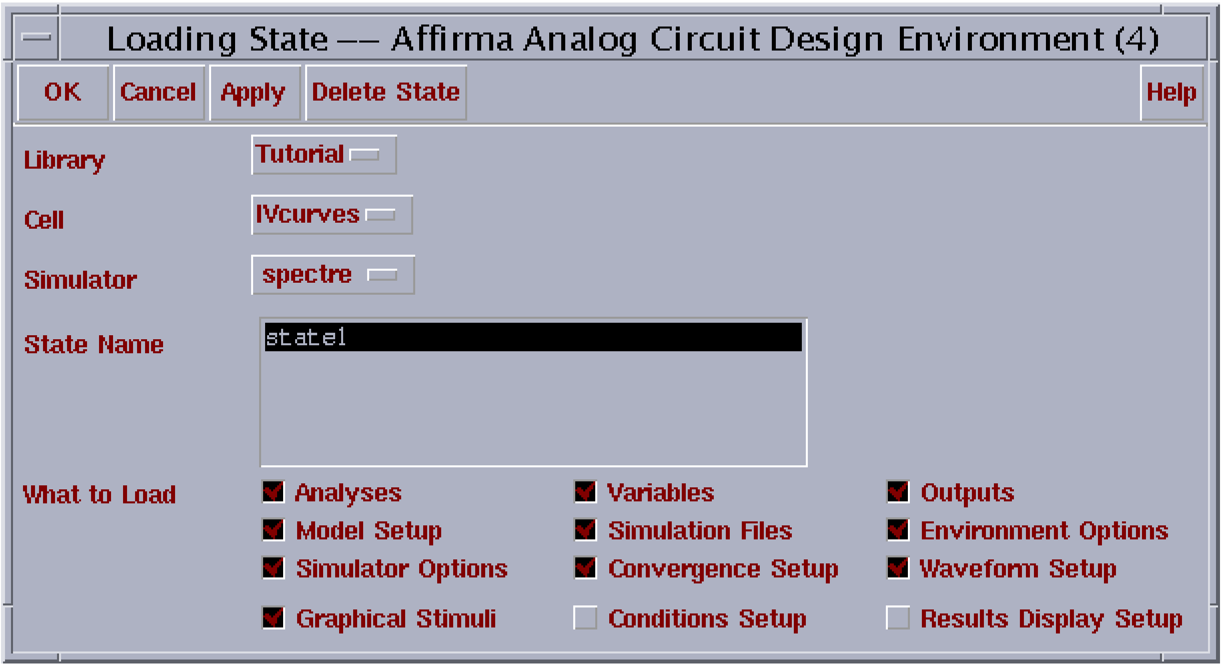
□ Update Instances: Of Entire Library

Click on the IVparam Cell and then double click on the schematic view of the IVparam cell, a schematic should pop-up which is identical to the IVcurves schematic. Let's delete the bottom 4 transistors and their connections, as well as the bottom 4 VGS and dummy power supplies (Go to Edit -> Delete or click on the "pencil" shaped button, then on the item that you want to delete, you can also delete entire areas by clicking and keeping down the mouse button while you draw a rectangle). Also change the value of the VGS power supply to "parameter" (this will be just a variable that we will have to define later). Finally move the gnd higher and reconnect it, the final schematic should look like this:



Check and Save your schematic, making sure there are no errors!

Now start the Analog Environment and choose Spectre as the simulator by going to Setup -> Simulator/Directory/Host and choosing Spectre. Now you can load the state that you previously saved Session -> Load State (how convenient!). You will have to change the name of the cell to "IVcurves" since the previous state was saved for that cell.



Loading State –– Affirma Analog Circuit Design Environment (4)

Library: Tutorial

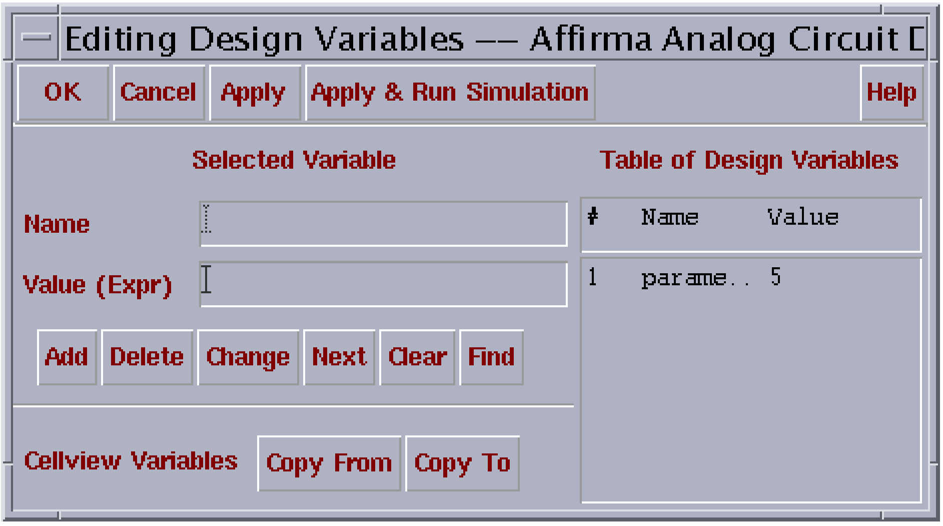
Cell: IVcurves

Simulator: spectre

State Name: state1

What to Load:
☑ Analyses ☑ Variables ☑ Outputs
☑ Model Setup ☑ Simulation Files ☑ Environment Options
☑ Simulator Options ☑ Convergence Setup ☑ Waveform Setup
☑ Graphical Stimuli ☐ Conditions Setup ☐ Results Display Setup

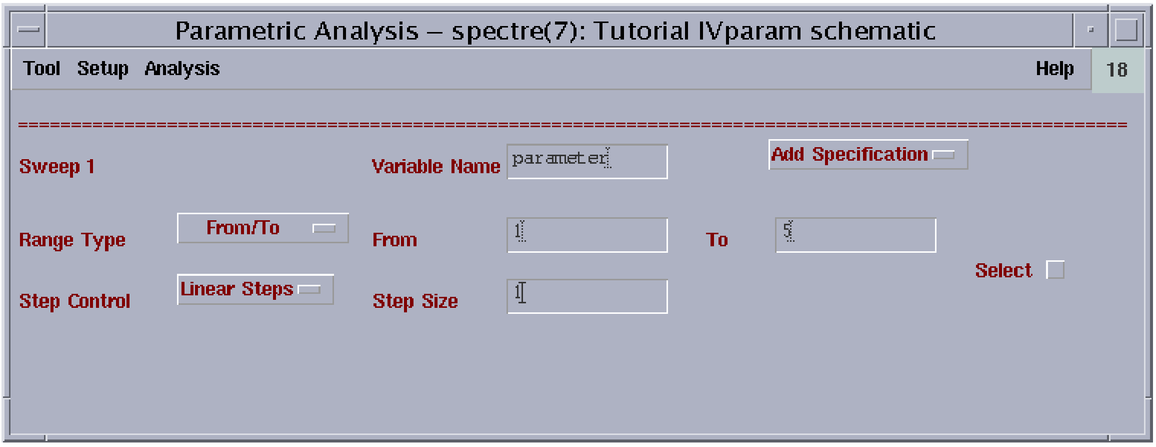
Go to Variables -> Edit.. and add the variable parameter with a value of 5. Click on Add and then on OK.



Editing Design Variables –– Affirma Analog Circuit D

#	Name	Value
1	parame..	5

You can try now to simulate (Simulation -> Netlist and Run) to make sure there are no problems. After this, instead of the usual simulation we are going to do a parametric simulation (practically this means multiple simulations with a variable as the parameter, our parameter will be the one called parameter). Go to Tools -> Parametric Analysis in the Analog Environment. Fill in parameter as the variable name, 1 as the From value, 5 as the To value, Linear Steps as Step Control with a Step Size of 1.


Parametric Analysis – spectre(7): Tutorial IVparam schematic
Tool Setup Analysis
Help 18
Add Specification

Sweep 1

Variable Name: parameter

Range Type: From/To

From: 1

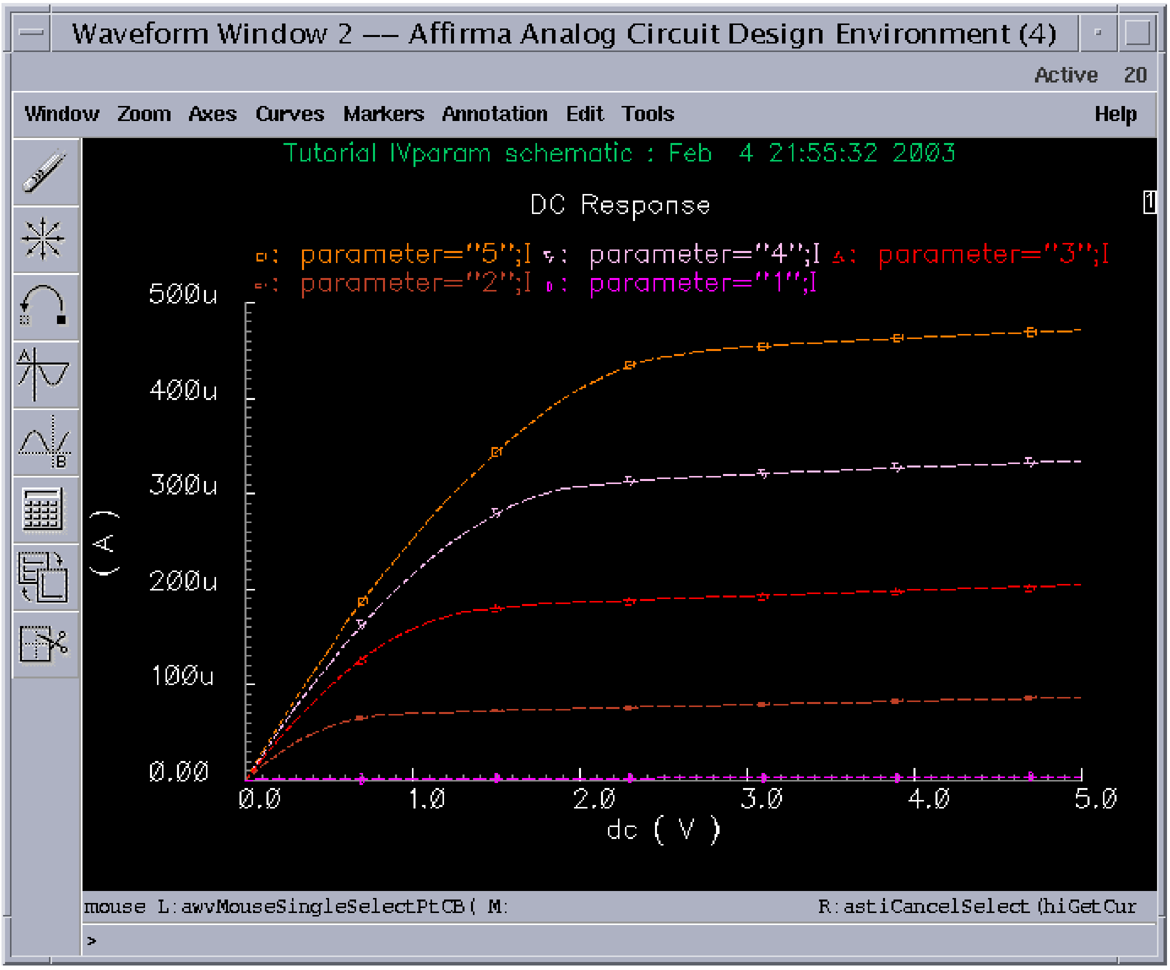
To: 5

Select □

Step Control: Linear Steps

Step Size: 1

Go to Analysis -> Start in the Parametric Analysis window. When the simulation is complete go to Results -> Direct Plot -> DC and then click on the terminal of the dummy supply in the drain of the transistor, then hit ESC. Now you should again get a nice family of IV curves.



```
mouse L:awvMouseSingleSelectPtCB( M:                R:astiCancelSelect (hiGetCur
>
```

Congratulations, this is the end of Tutorial.

第四部分.附件

（二）

Cadence virtuoso Layout editor tutorial

There are 2 ways to doing a layout: manual and automated. Manual layout usually enables the designer to pack his devices in a smaller area compared to the automated process but it is more tedious. The automated process, on the other hand, is done using standard cells and usually takes more real estate space but it is much faster. In this tutorial, you will learn how to perform MANUEL LAYOUTS ONLY and a simple inverter layout will be shown. You should know that for the purposes of this course, you are required to know how to design manual layouts, even though Cadence can accommodate either manual or automated layouts.

Before we get into the layout, first you need to understand the design rules for layout. The design rules that we will be using are the MOSIS Scalable CMOS Rules. Design rules gives guidelines for generating layouts. They dictate the spacings between wells, sizes of contacts, minimum spacing between a poly and a metal layer and many other similar rules. Design rules are essential to any successful layout design, since they account for the various allowances that need to be given during actual fabrication and to account for the sizes and the steps involved in generating masks for the final layout. The design rules that we will be using can be obtained from the following link on MOSIS Layout Design Rules. Note that the layout is very much process-dependent, since every process has a certain fixed number of available masks for layout and fabrication. For the case of this tutorial, we are using an AMI 1.6u CMOS process, which is a nwell process and supports two poly and three metal layers.

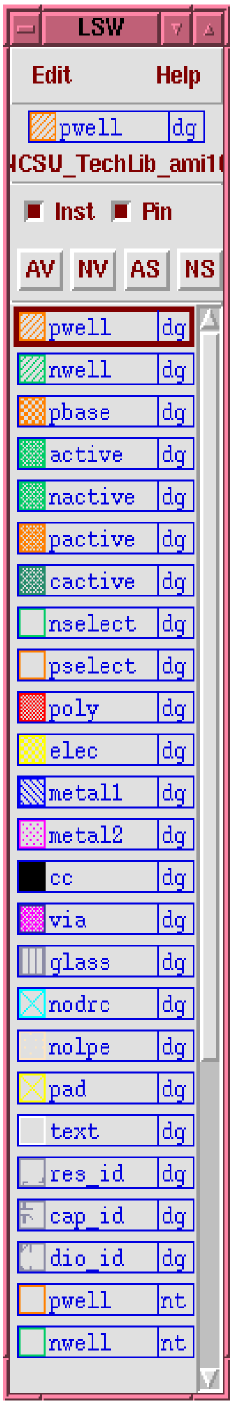
Before we proceed any further, please make sure that your present library is associated with a techfile. If you had followed this tutorial for your design of an inverter, then you might have already associated a techfile when you created a library ee560 in the first place. Otherwise, you can still do it, by clicking on the middle button by placing the mouse on the library name in the library manager window. There is an option for "Attach Tech Library". Once you choose that option, click on AMI 1.6u ABN(2P,NPN) as your process.

1. Create a layout cellview of the cell. Here we will create a layout for the inverter cell.

In the library manager window, click on the File -> New -> CellView. Choose CellName as inverter and View Name as layout. Then click on the OK button. An empty layout editor window will pop-up along with a LSW window. The LSW window will show all the layers such as nwell, pwell, active, etc. for the given process. An alternate way to open the layout editor window is to type "layout" into the View box of the inverter cell in the Library Manager window. A "Create New File" window will pop-up. Change the Tool item from "Composer-Schematic" to "Virtuoso" and make sure the View Name is "layout". If not, manually change this by typing this in.

If the LSW window is blank, then there is an error (Follow this link to solve the problem).

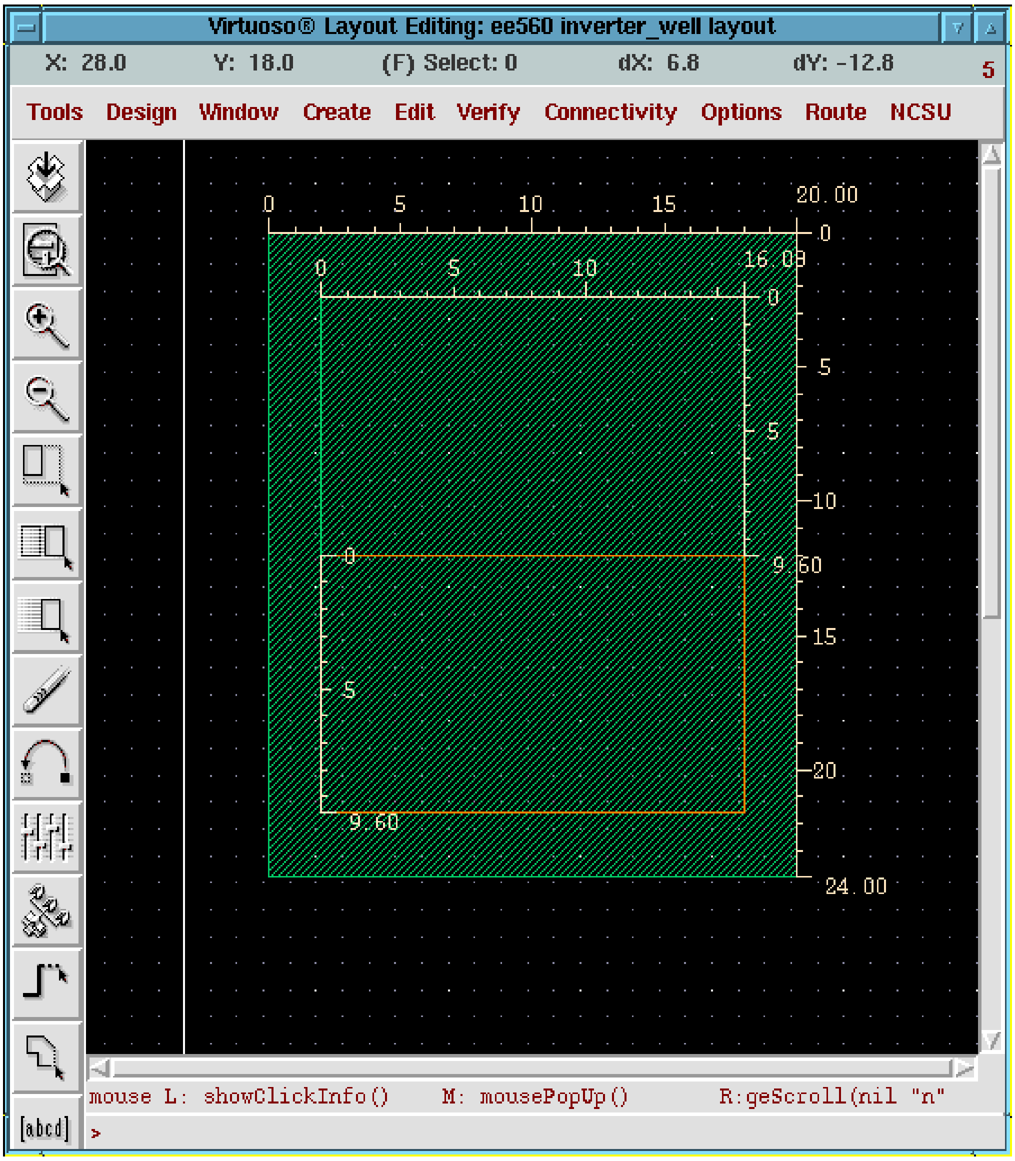
The LSW window should look something like this:



If you don't see the above (not necessary to be in the above order) you will need to set the mask layers manually. To do this, go to Edit -> Set Valid Layers and select/deselect the masks. Make sure that you at least have the following masks in your LSW window.

nwell, nselect, pselect, nactive, pactive, poly, elec, metal1, metal2, metal3 (all dg's) & metal1, metal2, metal3 (pn's).

3. Since we are using the AMI 1.6u technology, we only have an nwell process to use. Thus, the substrate will be a p-type substrate. We can always assume that the background is a p-subtrate. Now we will create a pmos transistor first. To do that, we need an nwell layer in which the pmos transistor will be formed.



mouse L: showClickInfo() M: mousePopUp() R:geScroll(nil "n"

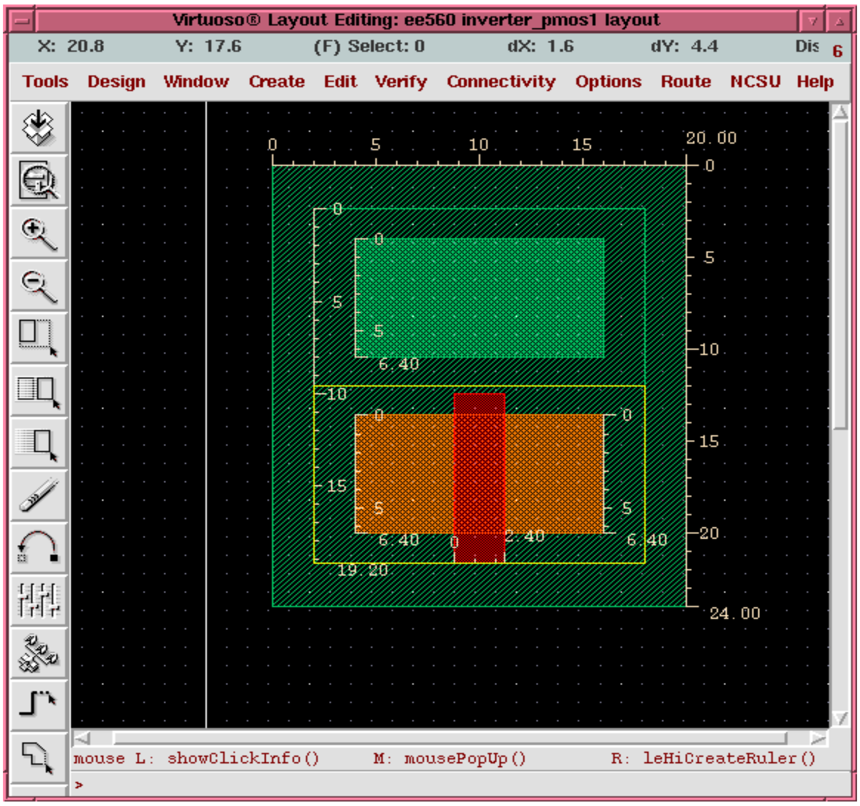
>

The green-shaded rectangle is the nwell layer, the green perimeter is nselect and the orange perimeter is pselect. The numbers represent the length in um (micrometers). Therefore, for the AMI 1.6u technology, lambda = 0.8u and 2*lambda = 1.6u. The editor options have been defaulted such that every cursor advancement corresponds to 0.4u or 1/4th the 2*lambda feature size. The ruler shown above can be invoked by typing k. It can be removed by typing capital K (shift+k). They show the length in micrometers. Note that you do not have to necessarily follow the dimensions shown above. In fact, it is probably a good idea to play around with the lengths and widths in order to see how small a mask layer you can create without violating any of the design rules.

The LSW window will be used to draw the masks in the layout editor window. To draw a mask, say an nwell layer, first choose the corresponding layer in the LSW window by clicking on the layer. Then, move your cursor into the layout window where you want to draw the nwell layer and type r (rectangle) and move your mouse. A yellow box will appear indicating the boundary of the nwell mask. Just click on the left mouse button to draw the nwell rectangle; we'll worry about the actual dimension later. To change the dimension of the rectangle, move your cursor to the side where you want to extend or shorten such that the side is highlighted and then type s (stretch). The side will move with your cursor.

4. Likewise, draw the nselect and pselect layers as shown in the figure above.

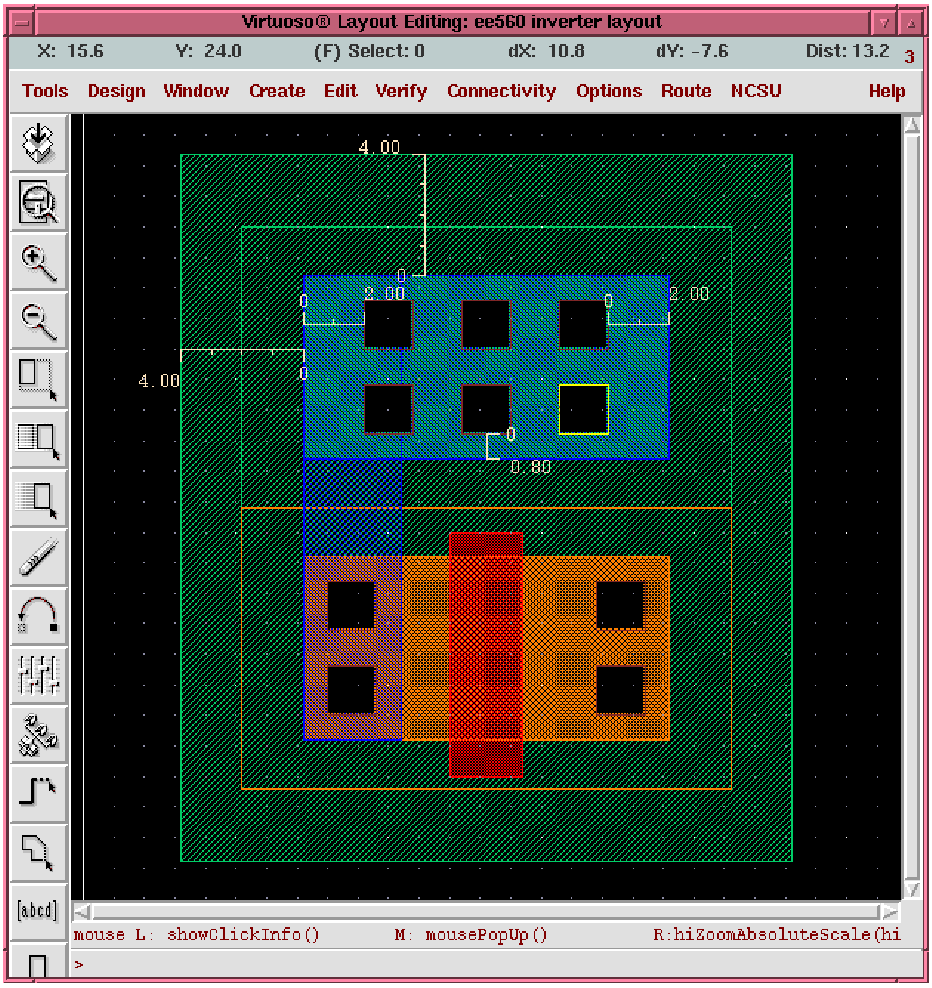
5. The pselect is where you are creating the pmos transistor since this is where the p+ diffusion is going to be formed. Draw the pactive layer on your layout as shown in the figure below. The orange shaded rectangle is the p+ active regions. The green shaded rectangle is the n+ active region. Next, draw the poly layer to form the gate of the transistor. The size of the pmos transistor shown below has W=6.4um and L=2.4um using the 1.6um CMOS technology (since 1 lambda is 0.8um).



mouse L: showClickInfo() M: mousePopUp() R: leHiCreateRuler()

6. Next we need to connect the active regions to metal lines so that they can be routed. The figure below shows the metal1 layer (blue line-shaded polygons) is connected to the active region by an active contact (cc.dg, which is solid black). Remember that the design rule usually restricts the size of the contact to be 2lambda * 2lambda, which is 1.6u * 1.6u. The nselect creates an n+ diffusion in the nwell. This is the body pin of the pmos transistor, which should be connected to power (vdd!). We'll touch on how to connect to the power supply later.

Also, a point of thought usually is how much distance there should be between all these strange looking polygons. That is governed by the design rules, the link for which is given at the website MOSIS Layout Design Rules. You should at least be familiar with some of these rules (e.g. contact size should always be 2 lambda * 2 lambda, distance between poly and active region, etc.). Once you get into the habit of designing manual layouts, you will start to remember the more common design rules. For now, you will have to perform a Design Rule Check (DRC) every now and then on your layout in order to make sure that you have satisfied the rules. More on this can be found on the next page of this online Cadence tutorial.



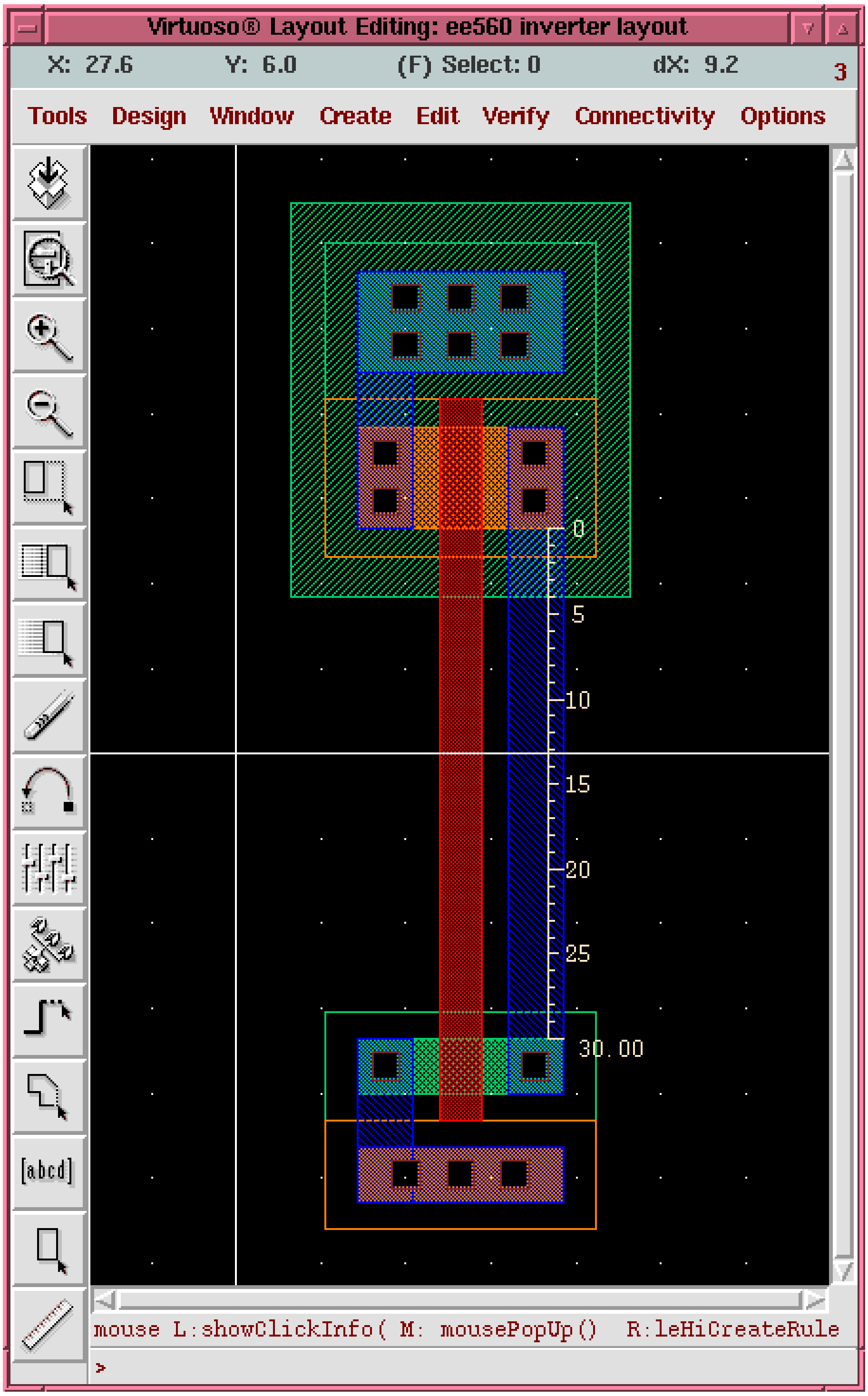
Virtuoso® Layout Editing: ee560 inverter layout

X: 15.6 Y: 24.0 (F) Select: 0 dX: 10.8 dY: -7.6 Dist: 13.2 3

mouse L: showClickInfo() M: mousePopUp() R:hiZoomAbsoluteScale(hi

>

7. Next, you can proceed to create the nmos transistor but this time your nmos needs to be created in the nselect layer while the p+ diffusion of the NMOS is in the pselect. The size of the nmos chosen in this design has the same length as the pmos (2.4um) but the width of the nmos is chosen as 3.2um instead. Note that since we are using an nwell technology, we don't need an explicit well for the nmos transistor (the pwell) since the background is p-substrate. The figure below shows the inverter.



```
mouse L:showClickInfo( M: mousePopUp()  R:leHiCreateRule
>
```

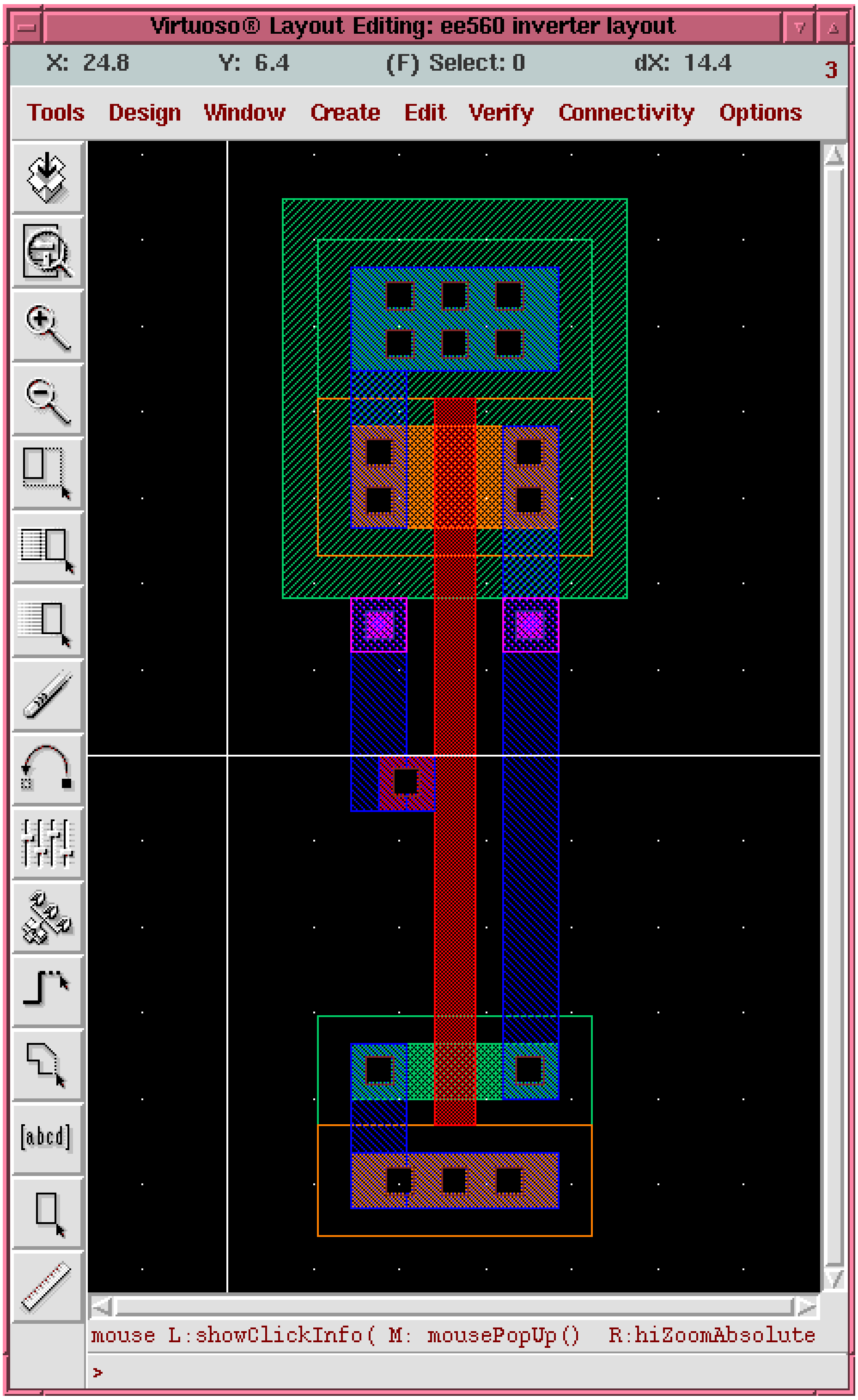
We have chosen to space the nmos and the pmos by the distance of 30um active-to-active distance for a 1.6um process. This region between the two transistors would be used for pin definitions and for routing signals from one layout cell to another. The more the distance between the nmos and the pmos transistor, the more connections can be routed and less problems to worry about in the future when designing big cells. However, a large distance may be inefficient and result in a very big layout. But for the sake of learning, we would rather choose to go with a large distance of around 30um. Note that you can stretch the distance between the active layers to make the cell shorter. One way would be to use the s command on the poly and metal1 vertical strip layers to stretch the layers upwards. You can then move the rest of the nmos transistor up by highlighting the bottom portion of the layout with your mouse (all of the edges will be highlighted in white) and using the m (move) command. Once you are in the move mode, just click once on the highlighted portion of the layout and move it upwards. Click again to release the selected layers. A good way to know if you are in the move mode is to look at the lower left-hand corner of the inverter layout view and read the messages there. You should see the following: Select the figure to be moved:

8. The gate of the transistors needs to be connected to the metal1 lines for it to be accessed. To do that you will be using a contact "cc.dg" to make a contact between an already overlapping metal1 and poly layer. Similarly, we desire to then connect the metal1 to metal2 (though it is not necessary) for pin connections. For this purpose, we will make a contact between a metal1 and a metal2 using a "via". There are two ways of doing this.

<u>Method 1</u>: Bring metal1 and metal2 to overlap each other and then draw a "via.dg" rectangle of 2lambda * 2lambda (which is 1.6u*1.6u for AMI 1.6u process). Similarly, bring poly and metal1 together and then draw a "cc.dg" rectangle of 2lambda * 2 lambda.

<u>Method 2</u>: There are some ready-to-use macros available for making contacts. To access a macro cell which has a poly-metal1 combo with a single contact, instantiate the cell " M1_P" (note capital letters) from the library "NCSU_TechLib_ami16". Similarly, to access a metal1-metal2 combo with a via, instantiate the cell "M1_M2" from the NCSU_TechLib_ami16 library. These cells will appear as a black box. To see through the cell, type "Shift -f". This will make the cell visible. Remember that you cannot update this cell, since it is a standard library cell.

The figure below shows the connection. The red-shaded polygon with a black square at the center and blue borderline is the M1_P contact. The blue-shaded polygon with a pink square at the center and pink borderline is the M1_M2 contact.



mouse L:showClickInfo(M: mousePopUp() R:hiZoomAbsolute

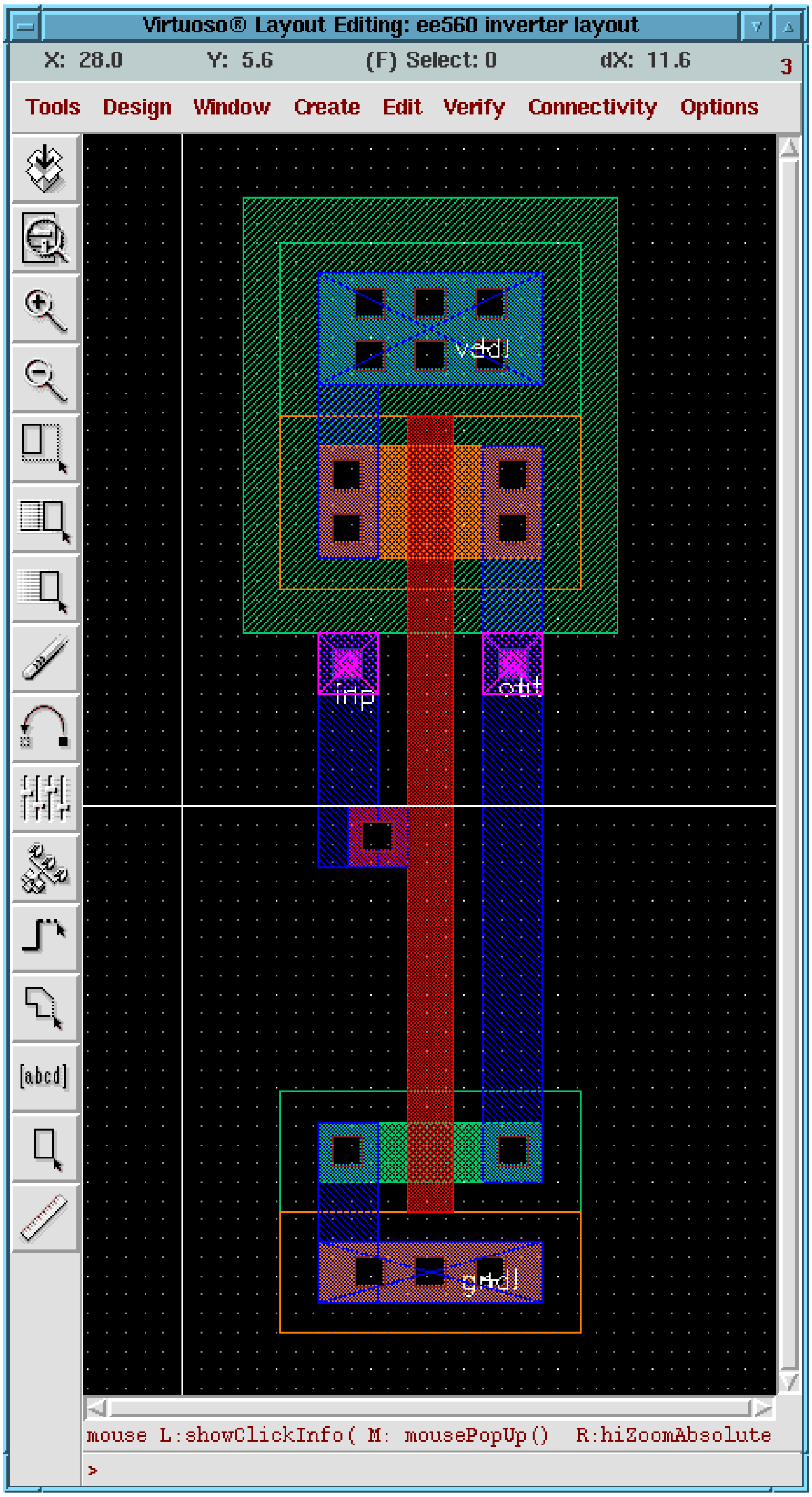
>

9. For simulation purposes and standard cell design rules, it is necessary to add the pin (pn) layer. They are identical in purpose to the input/output and vdd!/gnd! pins in the schematic view. Power and ground rail pins should be declared as jumpers. Input/output pins should be in metal2 while power/ground rail pins should be in metal1. It would not be a bad idea to label your pins with the text layer, but make sure to name the labels the same as the pins in

your schematic and put them on top of the labeled wires. Click on metal2.pn in the LSW window. Then press Ctrl-p in the layout editor window. A window will pop up. Enter the name 'inp' for labeling input. Choose "Display pin name " option and define the pin as input. Then click on the left mouse button with the cursor placed at the top left corner of the metal2 square to be labeled. Then drag the mouse to the right bottom corner of the same metal2 square to be labeled. Click one more time inside the metal2 square to place the text. Do the same steps for placing an "out" pin except for the fact that you declare the pin as "output".

10. Next we want to label the vdd! and gnd! pins. To do this, select the metal1 pn pattern, which is just a blue rectangle outline with an X across. To draw the labels, type Ctrl-P. A pop up menu will appear. Type vdd! for the Terminal Names field and select the I/O type as jumper. Then move your cursor to the starting point of the label and click on the left mouse button. Move your cursor to size the label and click on the left mouse button again. Likewise, label the gnd! pin. The figure below shows the pin labels for vdd! and gnd!

Note that at any time, you can view the properties of any layout element you placed in your layout view by highlighting the particular element with the mouse and using the p (properties) command. This is especially helpful when you want to identify a particular via or pin that you have just created.



There are many other useful layout commands and features available through Cadence and most of these options have their own hotkeys. A very good idea would be to take a little bit of time to go through the many layout functions in the menus located at the top of the layout view (eg. Window, Create, Edit, Connectivity, Options) and maybe even try some of them out on your initial layout design. You can always undo your last performed function by clicking on Edit -> Undo or by pressing the u button.

Here are some hotkeys that I have found to be very useful when designing layouts:

Move about the layout view screen - keyboard arrows (up, down, left, right)

Fit entire layout onto screen - f

Zoom in/out - Ctrl/Shift z

Save design - F2

Cancel previous command - Esc

Reveal all mask layers within each layout cell - Shift f (Use Ctrl f to hide these layers)

Properties - q

Create path - p (Convenient for making interconnections between I/O pins of layout cell; need to select mask layer first from LSW window)

Create rectangle of mask layer - r (Select .dg mask layer first from LSW)

Create pin - Ctrl p (Select .pn mask layer first from LSW)

Instantiate layout cell - i

Select more than one mask layer simultaneously - Hold down Shift and click on each layer (Use Ctrl to deselect a particular layer)

Undo - u

Copy - c

Delete - d

Move - m

Stretch - s (Point to edge of mask layer first using mouse cursor)

Ruler - k (Erase ruler - Shift k)

第四部分. 附件

（四）

SMIC 0.18um lib

实验中使用的是SMIC 0.18um V1P6工艺的mixde signal spice model,具体的模型文件见文件 Ms018v1p6.mdl 。以下为使用该模型文件时注意事项的补充说明。

一. Ms018v1p6.mdl 内容形式如下：

```
*
* No part of this file can be released without the consent of SMIC.
*
******************************************************************************************
* SMIC 0.18um Mixed Signal 1P6M 1.8V/3.3V SPICE model (for HSPICE only)                 *
******************************************************************************************
*
* Release version       : 1.6
*
* Release date          : 7/13/2005
*
* Simulation tool       : Synopsys Star-HSPICE version 2002.2
*
* Model type            :
*     MOSFET            : HSPICE Level 49(BSIM3V3.2)
*     1/f MOSFET noise : HSPICE NLEV   3
*     Junction Diode    : HSPICE Level 3
*
* Model name            :
*     MOSFET            :
*
```

```
*          |      MOSFET type      |   1.8V   |   3.3V   |
*          |=====================================|
*          |           NMOS          |    n18   |    n33   |
*          *-------------------------------------*
*          |           PMOS          |    p18   |    p33   |
*          *-------------------------------------*
*          |     Native NMOS       |   nnt18 | nnt33   |
*          *-------------------------------------*
*          |    Medium NMOS        | nmvt18 | nmvt33 |
*          *-------------------------------------*
*          |    Medium PMOS        | pmvt18 |   ----   |
*          *-------------------------------------*
**    Junction Diode    :
*          *-------------------------------------------*
*          |   Junctio Diode type      |   1.8V   |   3.3V   |
*          |===========================================|
*          |         N+/PWELL                | ndio18 | ndio33 |
*          |-------------------------------------------|
*          |         P+/NWELL                | pdio18 | pdio33 |
*          |-------------------------------------------|
*          |         NWELL/PSUB            |         nwdio          |
*          |-------------------------------------------|
*          |       Native N+/PWELL        | nndio18| nndio33|
*          |-------------------------------------------|
*          | Buried PWELL/Deep NWELL |        diobpw          |
*          *-------------------------------------------*
**      Valid temperature range is from -40C to 125C
*****************************************************************************************
*                                        1.8V CORE NMOS MODEL                                        *
****************************************************************************************
.model n18 nmos
```

```
+LEVEL      = 49
*
* GENERAL PARAMETERS
*
+CALCACM    = 1
+LMIN       = 1.5E-7                  LMAX       = 1.0E-5                 WMIN       = 1.9E-7
+WMAX       = 1.0E-4                  TNOM       = 25.0                   VERSION    = 3.2
+TOX        = '3.87E-09+DTOX_N18' TOXM       = 3.87E-09               XJ         = 1.6000000E-07
+NCH        = 3.8694000E+17           LLN        = 1.1205959              LWN        = 0.9200000
+WLN        = 1.0599999               WWN        = 0.8768474              LINT       = 1.5757085E-08
+LL         = 2.6352781E-16           LW         = -2.2625584E-16         LWL        = -2.0576711E-22
+WINT       = -1.4450482E-09          WL         = -2.3664573E-16         WW         = -3.6409690E-14
+WWL        = -4.0000000E-21          MOBMOD     = 1                      BINUNIT    = 2
+XL         = '1.0E-8+DXL_N18'        XW         = '0.00+DXW_N18'         DWG        = -5.9600000E-09
+DWB        = 4.5000000E-09
* DIODE PARAMETERS
+ACM        = 12                      LDIF       = 7.00E-08               HDIF       = 2.00E-07
+RSH        = 7.08                    RD         = 0                      RS         = 0
+RSC        = 1.7                     RDC        = 1.7
…………………………..
```

二．使用注意事项

1．该模型只适用与 HSpice 系列性能模拟器；

2．该模型中，类似 TOX = '3.87E-09+DTOX_N18' 中的 DTOX_N18 为由所采用的 MOS 管类型决定的参数，类型包括“TT、FF、SS”三种，采用不同的类型时，对类似的这些参数需要采用不同的数据，具体请参考文档 TD-MM18-SP-2001v7R.pdf 。本实验部分内容二中，采用 HSpiceD 作为模拟器进行性能模拟时，采用的默认类型为“TT”。

3．模型中没有包括进 corner 的参数；

4．双极晶体管和电阻元件的模型没有包括在内，其模型文件分别参考文档 ms018_v1p6_bjt.mdl 和 ms018_v1p6_res.mdl 。