CITY UNIVERSITY

Final Lab Report

Digital System Design

Course code : CSE 412

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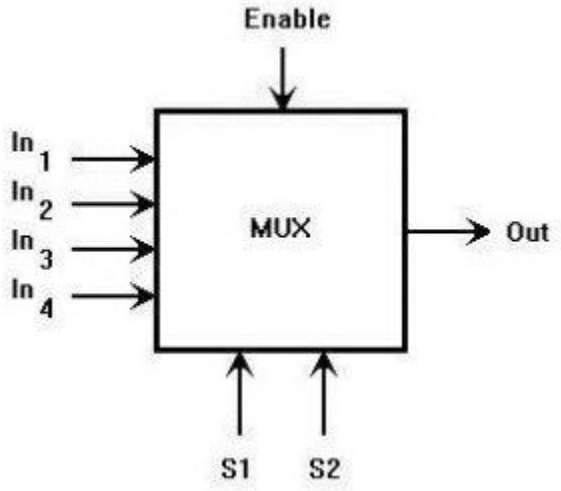
Name of the experiment:Digital multiplexer

AIM:
To realize digital multiplexer using basic gates

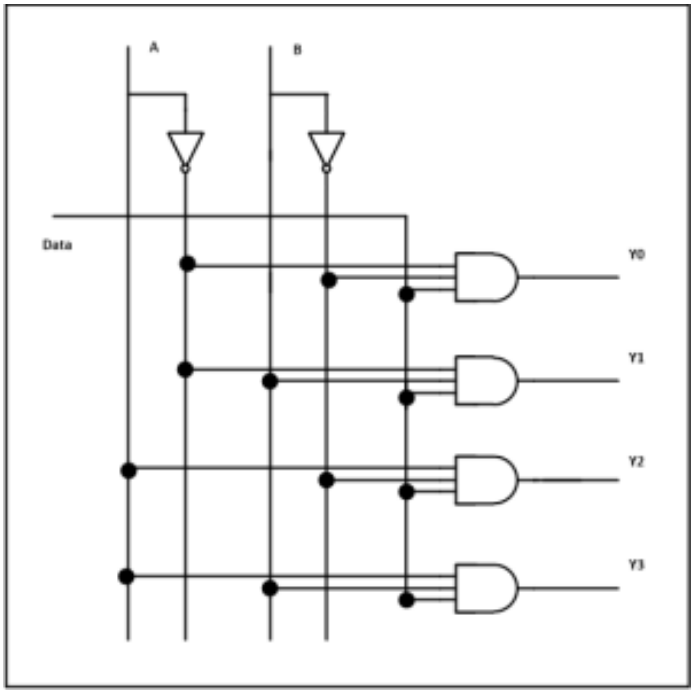
Theory:
The multiplexer is one of the basic building blocks of any digital design system.A digital multiplexer or data selector is a logic circuit that accepts several inputs and selects one of them at any given time to pass on the output. A 4yto one multiplexer that accepts 4inputs and produce one output. Selects input provides which will pass to output. The 74LS153 is a very high speed duel 4-input multiplexer with common select input and individual enable input for each slection.it can select two bits of data from the source.

Equipment and apparatus:
1. AND gate ,OR gate
2. Breadeboard
3. Connecting wire

Pin diagram:

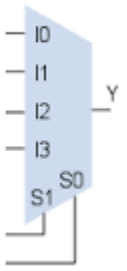


Circuit diagram:



S1	S0	Y
0	0	I0
0	1	I1
1	0	I2
1	1	I3

S1 \ S0	0	1
0	I0	I1
1	I2	I3



Procedure:

1. Multiplexing is the process in which multiple data streams, coming from different sources are combined and transmitted over a single Data cannel or data Stream
2. Give biasing to the input and do not need connection
3. Give various combination of input
4. Connect the ground and Vcc of for all IC's used in the circuit through the logical trainer kit.
5. Verify the functionality of the circuit by trying all input combinations and write down the observed outputs in the truth table.

Name of the experiment:Light Detector Circuit Using a NAND Gate

AIM:

To realizeLight Detector Circuit Using a NAND Gate

Theory:

In this project, we will build a light detector circuit using a NAND gate chip.A light detector circuit is a circuit that can detect light.When a bright light shines on the circuit, such as from a flashlight, we will make it so that a buzzer turns on.

The circuit is very basic. The component that will allow us to detect light is a photoresistor. We will use a photoresistor's light-sensing ability to detect whether the circuit is exposed to darkness or bright light. How this works is that a photoresistor's resistance changes in proportion to the amount of light it is exposed to. In darkness, it has very high resistance. In bright light, its resistance drops dramatically. If placed in a voltage divider circuit with a fixed resistor, we can exploit this resistance-altering behavior so that when connected to a NAND gate, we can produce a logic HIGH output when the photoresistor is exposed to bright light and a logic LOW output when the photoresistor is exposed to darkness.

Apparatus:

- NAND gate IC 74-00.
- LDR.
- LED.
- Resistors 330ohm, 6.8kohm.
- Connecting wires.
- Bread board.
- Regulator.

Circuit:

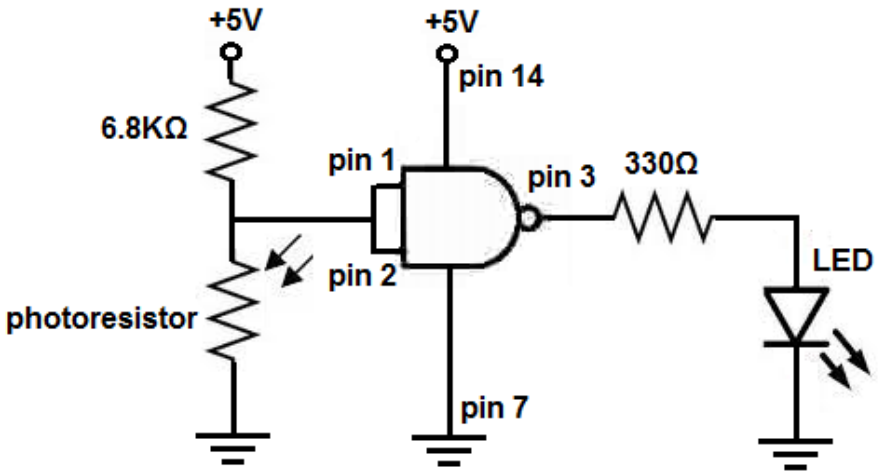


Table:

NAND Gate Logic		
Inputs		Outputs
0	0	1
0	1	1
1	0	1
1	1	0

Procedure:

1.we must give power to the NAND gate IC

2. will feed it 5V of power, so we give +5V to pin 14 and we connect pin 7 to GND
3. The component that allows us to detect light is a photo resistor (LDR).
4 We set up a voltage divider circuit composed of a photo resistor and a 6.8KΩ fixed resistor.
5.Connect the ground and Vcc of for all IC's used in the circuit through the logical trainer kit.
6. Verify the functionality of the circuit by trying all input combinations and write down the observed outputs in the truth table.

Name of the experiment :Design, implementation and study of a ladder type D/A converter

AIM:

To realizea ladder type D/A converter

Theory:

Digital-to-analog converter (DAC)

Digital-to-analog converter (DAC), which converts digital output from the computer, is it to a proportional analog voltage or current. For example, the computer might produce a digital output ranging from 00000000 to 11111111, which the DAC converts to a voltage ranging from 0 to 10 V.

R/2R Ladder

The DC circuits we have looked at thus far use binary-weighted resistors to produce the proper weighting of each bit. Whereas this method works in theory, it has some practical limitations. The biggest problem in the large difference in register values between the LSB and the MSB, especially in high-resolution DACs. For example, if the MSB register is 1kilo ohm in a 12-bit DAC, the LSB register will be over 2 Mega ohms. With the current IC fabrication technology, it is very difficult to produce resistance values over a wide resistance range that maintain an accurate ratio, especially with variations in temperature. For this reason, it is preferable to have a circuit that uses resistances that are fairly close in value .One of the most widely used a DAC circuit that satisfies this requirement is the R/2R ladder network, where the resistance values span a range of only 2 to 1.

Note how the resistors are arranged, especially note that only two different values are used, R and 2R. The current *I*OUT depends on the positions of the four switches, and the binary inputs B3 B2 B1 B0 control the states of the switches. This current is allowed to flow through an op-amp current-to-voltage converter to develop *V*OUT. We will not perform a detailed analysis of this circuit here, but it can be shown that the value of *V*OUT is given by the expression.

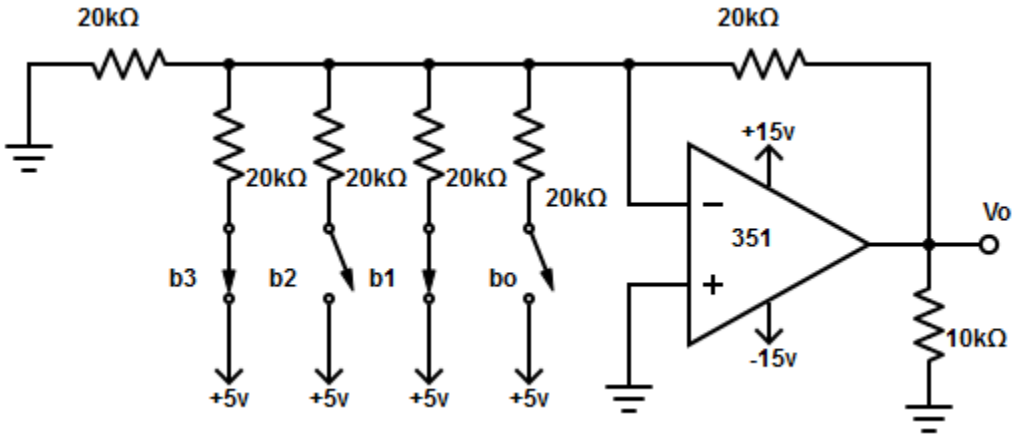
$$\text{Vout} = \frac{-Vref}{16} \times B$$

Where B is the value of the binary input, which can range from 0000 (0) to 1111(15).

Required Apparatus:

Digital IC Trainer Kit	01
Discrete Components: Op-Amp LM741	02
Resistor 1 kilo ohm	04
Resistor 2 kilo ohms	05
Digital AVO Meter	01
Connecting Wires	As necessary.

Circuit Diagram:



Data Table:

B3	B2	B1	B0	Theoretical Values (V0Its)	Practical Values (V0Its)	%Error
0	**0**	**0**	**0**	**0.000**	**0.000**	**0%**
0	**0**	**0**	**1**	**-0.625**	**-0.605**	**3.2%**
0	**0**	**1**	**0**	**-1.250**	**-1.240**	**0.8%**

0	**0**	**1**	**1**	**-1.875**	**-1.855**	**1%**
0	**1**	**0**	**0**	**-2.500**	**-2.490**	**0.4%**
0	**1**	**0**	**1**	**-3.125**	**-3.105**	**0.64%**
0	**1**	**1**	**0**	**-3.750**	**-3.740**	**0.26%**
0	**1**	**1**	**1**	**-4.375**	**-4.370**	**0.1%**
1	**0**	**0**	**0**	**-5.000**	**-4.900**	**2%**
1	**0**	**0**	**1**	**-5.525**	**-5.520**	**0.09%**
1	**0**	**1**	**0**	**-6.250**	**-6.241**	**0.14%**
1	**0**	**1**	**1**	**-6.875**	**-6.870**	**0.07%**
1	**1**	**0**	**0**	**-7.500**	**-7.490**	**0.13%**
1	**1**	**0**	**1**	**-8.125**	**-8.124**	**0.01%**
1	**1**	**1**	**0**	**-8.750**	**-8.749**	**0.01%**
1	**1**	**1**	**1**	**-9.375**	**-9.370**	**0.5%**

Calculation:

Assume that *V*REF=10 V for the R/2R DAC. What are the resolution and full-scale output of this converter?

Solution:

The resolution is equal to the weight of the LSB, which we can determine by setting B = 0001 = 1.

$$\text{Resolution} = \frac{-10V \times 1}{16}$$

$$= -0.625 \text{ V}$$

The full-scale output occurs for B = 1111 = 15_{10}

$$\text{Full-scale} = \frac{-10V \times 15}{-9.375}$$

$$= -9.375 \text{ V}$$

Error:

Theoretical Values – Practical Values

$$\% \text{ Error} = \frac{\text{Theoretical Values}}{\text{Theoretical Values}} \times 100$$

Result: 0.58% Average

Discussion:

As only one resistor is used per it in the resistor network, thus it is economical D/A converter.

It is very difficult to match the temperature coefficients of all the resisters. This factor is especially important in D/A converters operation over a wide temperature range. It is very difficult to ensure the absolute accuracy and stability of all the resistors.

Name of the experiment: Digital Demultiplexer

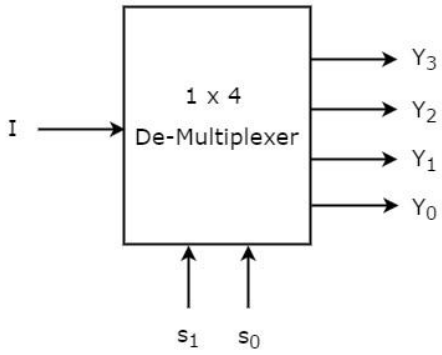
AIM:

To realize digital demultiplexer using basic gates .

Understand the definition of Demultiplexer.

Theory:

The Demultiplexer is combinational logic circuit that performs the reverse operation of Multiplexer. It has only one input, n selectors and 2n outputs. Depending on the combination of the select lines, one of the outputs will be selected to take the state of the input. The following figure shows the block diagram and the truth table for 1x4 Demultiplexer.



"Block diagram"

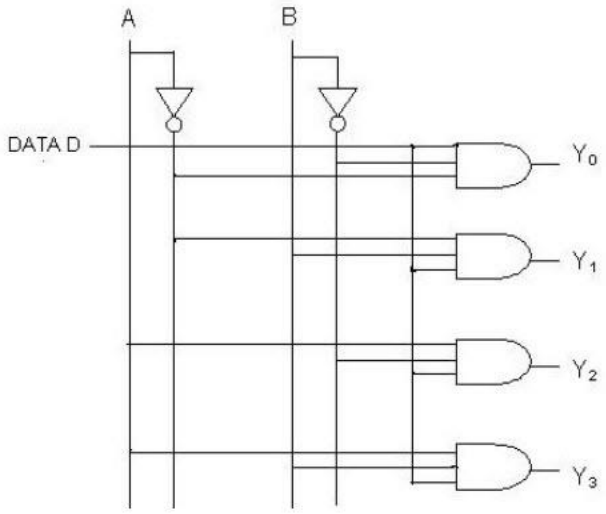
Data Input	Select Inputs		Outputs			
D	S_1	S_0	Y_3	Y_2	Y_1	Y_0
D	0	0	0	0	0	D
D	0	1	0	0	D	0
D	1	0	0	D	0	0
D	1	1	D	0	0	0

"Truth table"

Equipment and apparatus:

1. power supply capable of 5V DC output
2. AND gate
3. Breadeboard
4. Connecting wire
5. Connecting wire

Circuit diagram:



$Y0 = \overline{S1}\ \overline{S0}\ D$

$Y1 = \overline{S1}\ S0\ D$

$Y2 = S1\ \overline{S0}\ D$

$Y3 = S1\ S0\ D$

Procedure:

1. Develop the truth table and get the Boolean expression for MUX and DEMUX.
2. Draw the circuit diagram for a DEMUX.
3. Give biasing to the input and do not need connection.
4. Give various combination of input.
5. Connect the ground and Vcc of for all IC's used in the circuit through the logical trainer kit.
6. Verify the functionality of the circuit by trying all input combinations and write down the observed outputs in the truth table.

Name of the experiment: Design and implementation a 3 input circuit which output will be high when maximum input will be high.

AIM:

To realize 3 input circuit which output will be high when maximum input will be high. using basic gates

Theory:

This increase in the number of possible input states obviously allows for more complex gate behavior. Now, instead of merely inverting or amplifying (buffering) a single "high" or "low" logic level, the output of the gate will be determined by whatever *combination* of 1's and 0's is present at the input terminals.

Since so many combinations are possible with just a few input terminals, there are many different types of multiple-input gates, unlike single-input gates which can only be inverters or buffers. Each basic gate type will be presented in this section, showing its standard symbol, truth table, and practical operation. The actual TTL circuitry of these different gates will be explored in subsequent sections.

Equipment and apparatus:

1.AND gate ,OR gate
2.Breadboard
3.Connecting wire

Circuit:

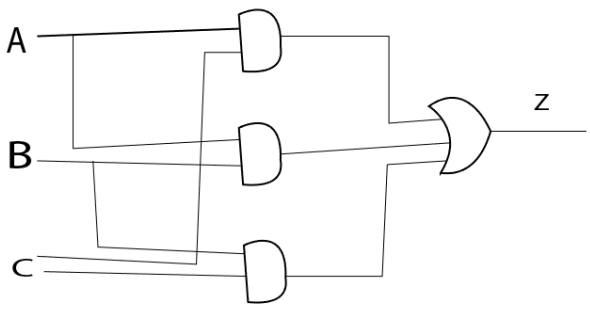


Table 1

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Y = A*B*C + A*B*C + A*B*C + A*B*C

Procedure:

1.we must give power to the AND gate and OR gate IC.
2.Give various combination of input
3.Connect the ground and Vcc of for all IC's used in the circuit through the logical trainer kit.
4. Verify the functionality of the circuit by trying all input combinations and write down the observed outputs in the truth table.