Project : Create testbench in SystemVerilog for AHB-lite Slave

Objectives:

- After this project, you should be able to read a specification document and create a verification plan. This is a must-have skill for every verification engineer.
- After this project, you should develop good familiarity with different components of a testbench. This will help you relate concepts when you later work with layered testbenches.

Document and Files Provided:

- AHB-lite spec document (https://www.eecs.umich.edu/courses/eecs373/readings/ARM_IHI0033A_AMBA_AHB-Lite_SPEC.pdf)
- Verification TestPlan Template
- Verification Review Presentation Template
- Design files:
    - design.sv(DUT)
    - mem.sv(DUT)
    - testbench.sv(Modify as needed)
    - ahb3lite_pkg.sv(contain defines)
    - Makefile(Modify as needed)
    - covfile.ccf
        - necessary flags for tool to enable coverage
        - see Makefile to know how to configure this
    - restore.tcl
        - contains necessary setup to enable waves by default
        - Use `*-input restore.tcl*` in your xrun command to use this

Tasks:

The task is to connect the DUT to a simple testbench and drive different signals to its input and observe the output. It is recommended that before writing the testbench, you should go through the specification briefly and record all features to be tested, the stimulus required and the expected result. Verification engineers typically record this in a separate document, a sample “Verification Plan Template” is provided to help you organize this information.

Deliverables:

- Complete testplan document (sheet 2 of VerificationTestplanTemplate.xlsx).
- Your testbench file including coverpoints
- Assertions file
- Screenshots showing final coverage both code and functional coverage
    - Also attach exclusion file
    - If you have written multiple tests then use `*-covworkdir <path of directory>*` while running tests for coverage
    - Make a file `*cov_paths.list*` which should contain the paths till `*test*` folder of each directory made in above command (default path is `*cov_work/scope/test*`)

    - When all tests have been completed and you want to extract coverage for all tests then use following:
        - *imc -execcmd "merge -runfile cov_paths.list -out cov_merged_data -overwrite"*
        - *imc -gui -load cov_work/scope/cov_merged_data &*
- Extra Credit: Provided you have completed the above tasks, and are willing to spend some extra time on the project, consider bringing up the design in JasperGold using lab instructions as your guide. Try to prove a few basic assert and cover properties. If you see any failures, debug them and add assumptions if needed. Then, time permitting, move on to other properties from the simulation environment. Present your results in the final project presentation.

Note: Pay attention to the cleanliness of your code, use proper indentations and add comments wherever necessary.

Deadline:

- Final deadline to submit the above listed *Deliverables* is **April 30, 2025 @3PM**
- Verification Review Presentations will be held on **May 1, 2025**.(TBD)