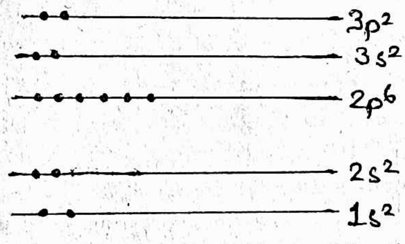
Energy bands in solids

Ques. Explain the formation of energy bands in solids. What are valence band, conduction band and forbidden energy gap?

Ans.- The electrons is an isolated atom revolve around the atomic nucleus in various fixed orbits have only certain discrete energies. Therefore, the electron in an isolated atom have well defined energy levels.

In a crystal, there are very large number of closely. packed atoms ($\simeq 10^{23}/cm^3$). Thus each atom in a crystal is surrounded by a large number of atoms. Hence a very large number of energy levels are created because of splitting of energy levels due to the interaction between various atoms.This set of closely spaced energy levels is called energy band.

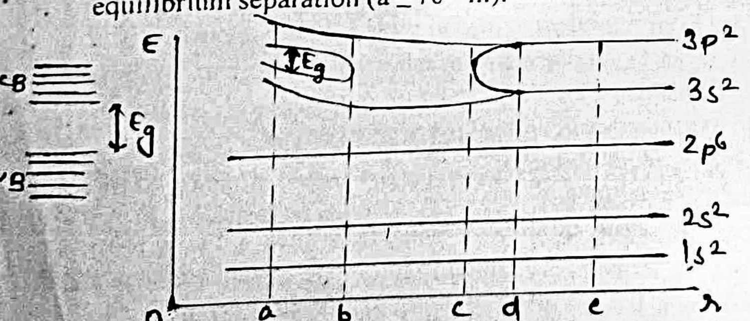
However, the splitting, is not appreciable in the case of the energy levels of the electrons in the inner shells.



In order to understand the modification of the energy levels, consider a single silicon crystal having N atoms. A silicon atom has 14 electrons whose electronic configuration is $1s^2, 2s^2, 2p^6, 3s^2, 3p^2$. The energy levels of electrons in an isolated silicon atom are shown in fig. (a). In each silicon atom, there 2 energy levels in subshell 1s, 2 energy levels in subshell 2s, 6 energy levels in subshell 2p. 2 energy levels in 3s subshell and 6 energy levels in 3p subshell out of which 2 energy levels are filled and 4 energy levels are empty.

In silicon crystal, there 2N energy levels in subshell 1s, 2N energy levels in subshell 2s, 6N energy levels in subshell 2p, 2N energy levels in 3s subshell and 6N energy levels in 3p subshell out of which 2N energy levels are filled and 4N energy levels are empty.

Let the atoms forming the silicon crystal initially be far apart so that there is no interaction between them. The distance between them is gradually reduced till it becomes equal to the inter-atomic separation between them i.e. the equilibrium separation ($a \simeq 10^{-10}$m).



(i) When r = d >>> a i.e. when the interatomic separation is very large- There is no interaction between the atoms in this situation. Hence, they behave like free atoms having identical discrete energy levels.

(ii) When r = c >> a- In this situation, the interaction between the valence electrons of the atoms becomes appreciable.The single 3s and 3p energy levels split into large numbers of closely spaced energy levels (i.e. 2N s-energy levels and 6N p-energy levels). This results in the formation of small energy bands corresponding to 3s and 3p energy levels. Hence the energy gap between 3s and 3p levels decreases.

(iii) When r = b > a - When the interatomic separation is further reduced from c to b. The energy gap between 3s and 3p disappears and the two bands starts overlapping.

In this situation, all the 8N energy levels (2N s-energy levels and 6N p-energy levels) get continuously distributed and form a single energy band. At this stage, it is not possible to distinguish between 3s and 3p energy levels. One can only say that 4N levels are filled and remaining 4N levels are empty.

(iv) When r = a i.e. interatomic separation becomes equal to the equilibrium separation- When interatomic separation is reduced from b to a. The filled and the unfilled bands get separated from each other by an energy gap called the forbidden energy gap which is generally denoted by E_g.

The lower energy band of 4 N filled energy levels is called the valence band (VB) and upper energy band of 4 N empty energy levels is called the conduction band (CB).

Difference between conductors (metals), insulators and semiconductors

Ques.-Distinguish between conductors. insulators and semiconductors.

Ans.- The difference between the electrical conductivity of different solids can be easily understood with the help of their energy band diagrams.

(A) Conductors (metals)- There are two types of energy band structures is conductors-

(i) There is energy gap between the completely filled valence band and the partially filled conduction band. Sodium and other alkali metals belong to this category

(ii) The conduction and valence bands partly overlaps. Beryllium, magnesium and zinc belong to this category.

When electric is applied across conductors then the motion of electrons takes place in conduction band in the opposite direction of electric feild even at 0K.Thus. the flow of electric current takes place in conductors even at 0K.

(B)Insulators- In insulators, the valence band is completely filled with electrons and the conduction band is empty. A large fobidden energy gap of about 6 eV separates the valence and the conduction band. Hence the electrons from the valence band cannot move to the conduction band even at high temperature.Thus, the flow of electric current does not take place in insulators when electric feild is applied across them.

(C)Semiconductors- In semiconductors, the valence band is completely filled and the conduction band is empty. But there is a small forbidden energy gap of the order of 1eV(In case of Ge and Si, the forbidden gap is of 0.74 eV and 1.12eV respectively).

At 0K semiconductors behave like perfect insulators but at room temperature. Some electrons from the valence band acquire sufficient thermal energy and move to conduction band. This causes electric current to flow in them

* For semiconductor, $E_g < 3eV$ * For insulator, $E_g > 3eV$

when electric feild is applied across them. The resistivity of such material lies between the insulators and the conductors therefore they are called semiconductors.

Note-1. The highest energy level occupied by an electron at zero kelvin is called fermi level and the corresponding energy is called fermi energy.

Note-2. The fraction of electrons excited to the conduction band at any temperature T is given by $p \propto e^{-E_g/KT}$.

where E_g is the forbidden energy gap and K is Boltzmann's constant.

Intrinsic semiconductors

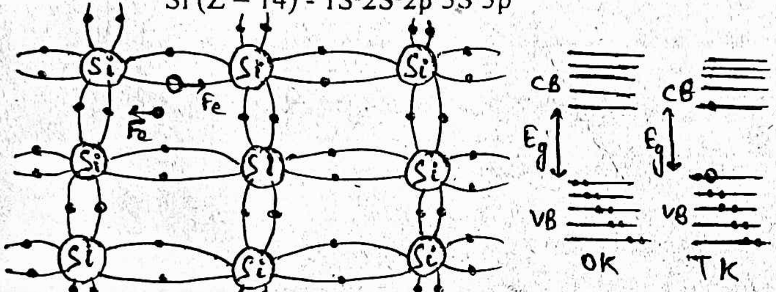
Ques.-What are intrinsic semiconductors? On the basis of valence bond model, explain the mechanism of conduction in intrinsic semiconductors.

Ans.- A semiconductor in pure form (having no impurity atoms) is called an intrinsic semiconductors. Pure Ge and Si crystals are the important examples of intrinsic semiconductors. Both Ge and Si are tetravalent and their electronic configurations are as under.

E →

Ge (Z = 32) - $1S^2 2S^2 2p^6 3S^2 3p^6 3d^{10} 4S^2 4p^2$

Si (Z = 14) - $1S^2 2S^2 2p^6 3S^2 3p^2$



TK

Each atom in both crystals has four valence electrons which forms four covalent bands by sharing these electrons with four neighbouring atoms.

At zero kelvin, there is no free electron for conduction of current. At room temperature, some electrons break away from the bonds and become free. At the same time equal number of holes are created in the bonds. Hence conduction in an intrinsic semiconductor is due to the motion of the electrons in the conduction band and holes in the valence band.

The electron and holes reponsible for electrical conduction in an intrinsic semiconductor are called the intrinsic current carriers and

$$n_e = n_h = n_i$$

where n_e and n_h are respectively the number density (number per unit volume) of the electron in the conduction band and holes in the valence band and n_i is the intrinsic carrier concentration.

When an electric field is applied across an intrinsic semiconductor, the electrons drift in the direction opposite to that of the electric field and constitute the electronic current. At the same time, the holes in the valence band drift along the direction of the electric field and constitute the hole current. Since the conventional current is opposite is opposite to the flow of electrons, the electronic current and the hole current add up to give the total current in the direction of the electric field.

$$\therefore \quad I = I_e + I_h$$

Because of small value of n_e and n_h, the current in the intrinsic semiconductor is very small.

Note-Mobility of charge carriers- The mobility of a charge carrier, i.e. electron or a hole is defined as the drift velocity acquired by the charge carrier per unit electric field applied. It is represented by the symbol μ.

$$\therefore \quad \mu = \frac{v}{E}$$

As the movement of holes in the valence band is due to the movement of the electrons (bounded) in the valence band therefore the electrons (free) in the conduction band drift more freely than the holes in the valence band.

Hence the mobility of electrons (μ_e) is greater than the mobility of holes (μ_h).

Doping

Ques.-(a) What is the limitation of intrinsic semiconductors?

(b) What is doping? What are the requirements of doping?.

Ans.-(a) The electrical conductivity of an intrinsic semiconductor at room temperatures is very small and is inadequate for any useful application. The conductivity of intrinsic semiconductor can be improved remarkable by adding small amount of suitable impurity to it.

(b) The process of addition of impurities in an intrinsic semi-conductor is called doping. The impurity atoms so added are called the dopants and the semi-conductor with impurity atoms i.e. a doped semiconductor is called extrinsic semiconductor.

For a tetravalent intrinsic semiconductor (such as Ge or Si), the dopants are trivalent or pentavalent. The dopant should be such that.

(i) It substitutes the semiconductor atom in the crystal lattice.

(ii) Its. size is almost the same as that of the semiconductor atom.

Note- 1.- A semiconductor is doped by bombarding the semiconductor with the ions of the dopant atoms

Note-2.- Doping is effective only when dopant atoms are such that they do not distort the crystal lattice.

Extrinsic semiconductors

Ques.-What are extrinsic semiconductors? On the basis of valence bond model, explain how can an intrinsic semiconductor can be converted into n-type and p-type semiconductor.

Ans.- A semiconductor doped with suitable impurity atoms so as to increase the number of charge carriers is called an extrinsic semiconductor

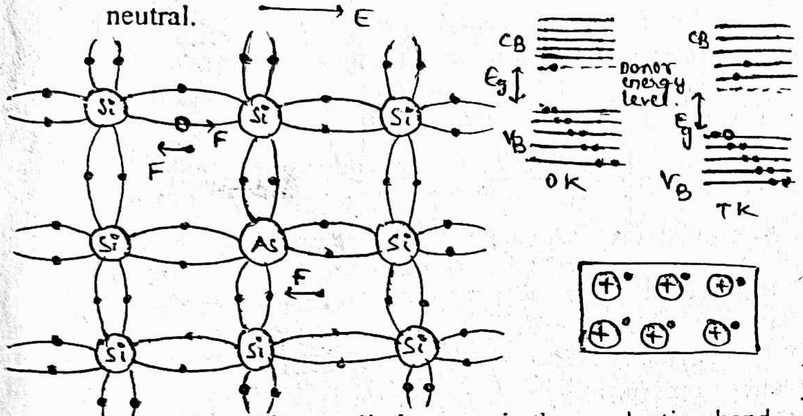
The extrinsic semiconductor are of two types-

(i) n-type semiconductor

(ii) p-type semiconductor

(i) n-type semiconductor- When pentavalent impurity atoms (As, Sb or P) are added to the intrinsic semiconductors, the extrinsic semiconductor so obtained is called n-type semiconductor

Consider a pure Si crystal when it is doped with pentavalent atoms say As, which has 5 valence electrons, then each As atom replaces Si atom and forms four covalent bonds by sharing its four electrons with the surrounding Si atoms. The fifth electron of the As atom remains weakly attached to it with a small binding energy which is 0.05 eV. In energy band diagram, the energy level of fifth electron lies in the forbidden energy gap about 0.05 eV below the conduction band which is called the donor energy level. Even at room temperature, almost all donor electrons acquire sufficient energy (> 0.05 eV) and move from the donor energy level to the conduction band due to which the electrical conductivity of the semiconductor is remarkably increased. Since, each impurity atom donates one electron to crystal therefore pentavalent impurity atoms are called donor atoms. As the donor atoms lose their fifth electron therefore they become positive ions but the material as a whole remains electrically neutral.



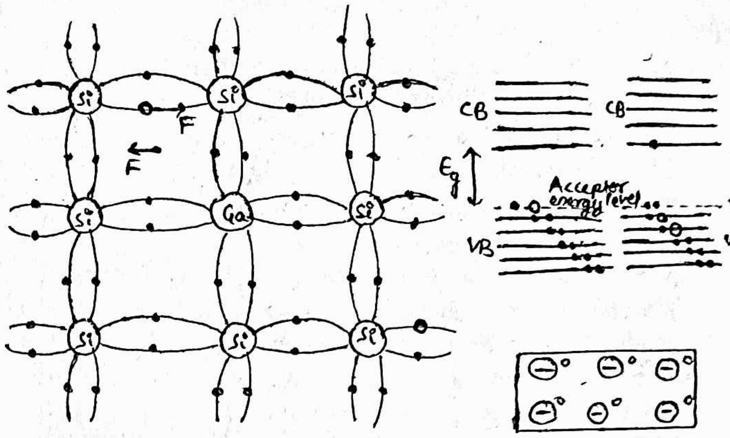
Since, almost all electrons in the conduction band come from the donor level and only a very few from the valence band due to temperature and an equal number of holes are created in valence band therefore the conductivity of n-type semiconductor is mainly due to the donor electrons and not due to the holes. Since, the electrons and holes are respectively the majority and minority current carriers therefore the resultant semiconductor so obtained is called n-type semiconductor..

Here $n_e' >> n_h'$

and $n_e' \cdot n_h' = n_i^2$

(ii) p-type semiconductor- When trivalent impurity atoms (In, Ga, Al or B) are added to the intrinsic semiconductors, the extrinsic semiconductor so obtained is called p-type semiconductor.

Consider ~~a~~ pure Si crystal when it is doped with trivalent atoms ~~say~~ Ga, which has 3 valence electrons, then each Ga atom replaces and Si atom and forms three covalent bonds by sharing its three valence electrons with surrounding Si atoms. The fourth bond will be incomplete due to deficiency of one electron, this deficiency acts as a hole. In energy band diagram, the energy level of this hole lies in the energy gap about 0.05 eV above the valence band which is called the acceptor energy level. Even at room temperature, the electrons acquire sufficient energy and move from the valence band to the acceptor energy level and hence large number of holes are created in the valence band due to which the conductivity of the semiconductor is remarkably increased. Since, each impurity atom acceptes one electron from the crystal therefore trivalent impurity atoms are called acceptor atoms. As the acceptor atoms gain electrons therefore they become nega~~posi~~tive ions but the material as a whole remains electrically neutral.



Since, almost all holes in the valence band come from the acceptor level and only a very few holes are created in valence band due to temperature and an equal number of electrons are created in conduction band therefore the conductivity of p-type semiconductor is mainly due to the holes and not due to electrons. Since, the holes and electrons are respectively the majority and minority current carriers therefore the resultant semiconductor so obtained is called p-type semiconductor..

Here $n_h' >> n_e'$

and $n_h' \cdot n_e' = n_i^2$

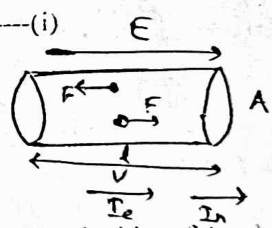
Electrical conductivity of semiconductors

Ques.- Using the concept of electron and hole current, derive expression for the conductivity of a semiconductor.

Ans.- Consider a block of semiconductor of length ℓ and area of cross section A. Let n_e and n_h be the number of density of the electrons (in CB) and the holes (in VB) respectively. Let V be the potential difference applied across the ends of the block.

∴ Electric field established in the block

$$E = \frac{V}{\ell} \quad \text{----(i)}$$



Let v_e and v_h be the drift velocities of the electrons and the holes under the influence of the electric field E. Since both the electrons and holes contribute the current I_e and I_h in the direction of E, the total current I will be

$$I = I_e + I_h$$

or $$I = n_e A e v_e + n_h A e v_h \qquad (\because I = nAev_d)$$

or $$I = Ae(n_e v_e + n_h v_h) \quad \text{----(ii)}$$

From Ohm's law, $I = \frac{V}{R}$ Also $R = \frac{\rho\ell}{A}$

and from eq. (i) $V = E\ell$

$$\therefore \quad I = \frac{V}{R} = \frac{E\ell A}{\rho\ell} = \frac{EA}{\rho} \quad \text{----(iii)}$$

Comparing eq (ii) and (iii), we get

$$\frac{EA}{\rho} = Ae(n_e v_e + n_h v_h)$$

or $$\frac{1}{\rho} = e\left(n_e \frac{v_e}{E} + n_h \frac{v_h}{E}\right) \quad \text{---(iv)}$$

But $\frac{v}{E} = \mu$ i.e. drift velocity per unit electric field is called the mobility of charge carriers and is denoted by u.

$\therefore$ Mobility of elelctrons $\mu_e = \frac{v_e}{E}$ and holes $\mu_h = \frac{v_h}{E}$

From eq. (iv) $\quad \frac{1}{\rho} = e\,(n_e\mu_e + n_h\mu_h)$

But the reciprocal of resistivity (ρ) is the electrical conductivity (σ) of the semiconductor.

$$\therefore \quad \sigma = e\,(n_e\mu_e + n_h\mu_h) \quad \text{----(v)}$$

The above relation shows that the conductivity of a semiconductor depends on the number densities as well as the mobility of the electrons and the holes.

Effect of rise in temperature the electrical conductivity of semiconductor

Ques.- Explain the variation of conductivity of a semiconductor with temperature.

Ans.- As the temperature increases, the number density of the elelctron and holes i.e. n_e and n_h increases due to the breaking up of more covalent bonds. But their mobility (μ_e and μ_h) decreases as the charge carriers suffer more frequent collisions. Since the increase in n_e and n_h is much larger than the decrease in μ_e and μ_h, the result is that conductivity of the semiconductor increases with the increase in the temperature.

Difference between the intrinsic and extrinsic semiconductor-

Intrinsic semiconductor	Extrinsic semiconductor
(i) It is a pure crystal of IV group elements such as Ge and Si.	(i) It is formed when an intrinsic semiconductor is doped with pentavalent or trivalent impurities.
(ii) The number of electrons in the conduction band is always equal to the number or holes in the valence band.	(ii) The number of free electrons is never equal to the number of holes.
(iii) Their electrical conductivity is low.	(iii) Their conductivity is high.
(iv) Their conductivity only depends on the temperature.	(iv) Their conductivity depends on the temperature as well as on the quantity of impurity doped in the crystal.

Difference between the n-type and p-type semiconductor-

n-type semiconductor	p-type semiconductor
(i) It is formed when an intrinsic semiconductor is doped with pentavalent impurity.	(i) It is formed when an intrinsic semiconductor is doped with trivalent impurity.
(ii) The electrons are majority charge carriers and the holes are minority charge carriers.	(ii) The holes are majority charge carriers and the electrons are minority charge carriers.
(iii) Each impurity atom doped provide an extra electron to the crystal and is called donor.	(iii) Each impurity atom doped creates a hole (or accepts an electron) and is called acceptor.

p-n junction

Ques.- What is a p-n junction? Explain with the help of diagram, how is a depletion layer formed near its junction. How is a potential barrier set up in it?

Ans. When a p-type semiconductor is placed is close contact with a n-type semiconductor the arrangement so formed is called p-n junction.

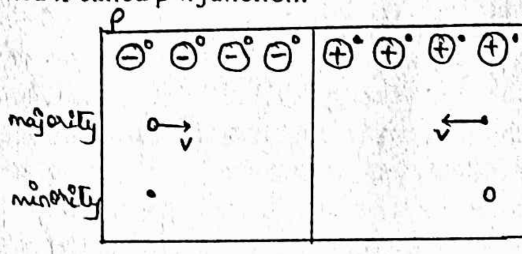
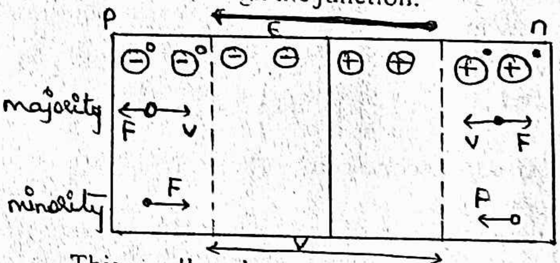


Figure shows a p-n junction diode whose left half is p-type and the right half is n-type. In a junction diode, in the p-region holes as the majority charge carriers whereas in the n-region the electrons are the majority charge carriers. Because of the difference in the concentration of the charge carriers in the two regions, the electrons from the n-region duffuse through the junction into the p-region. At the same time the holes from the p-region diffuse through the junction into the n-region due to which neutralization of electrons and holes takes at the junction. As a result of which a small region near the junction on the n-side becomes devoid of free electrons and that on the p-side becomes devoid of the holes. The region is left with ionized donor atoms (positively charge) on the n-side of the junction and the with the ionised acceptor atoms (negativity charge) on the p-side of the junction. These charges being immobile act as barrier for further migration of the electrons and holes through the junction.

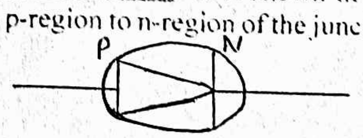


This small region near the junction on both sides which is devoid of free charge carriers (electrons and holes) and has only immobile ions is called the depletion layer of depletion retion. The width of the depletion layer is of the order of 10^{-6} m. $\boxed{V = E\gamma}$

$\gamma = 10^{-6}$

The accumulation of equal positive and negative charges in the two regions across the junction establishes an electric field (E). This field (E) is directed from n-region to the p-region and hence prevents further diffusion of electrons and holes through the junction. The electric field in the depletion layer created a potential difference across the depletion layer. This is called the potential barrier. The magnitude of the potential barrier is about 0.3 V for Ge and 0.7 V for Si.

Circuit symbol of a diode- It is shown in fig. the arrow points from p-region to n-region of the junction diode.

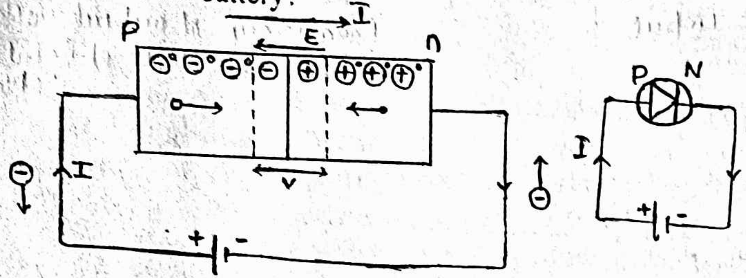


Working of a p-n junction

Ques.- Explain the working of a junction diode when it is (i) forward biased and (ii) reverse biased

Ans.- The arrangement of applying an external potential difference (or an electric field) across a p-n junction is called biasing. A junction diode can be biased in the following two ways-

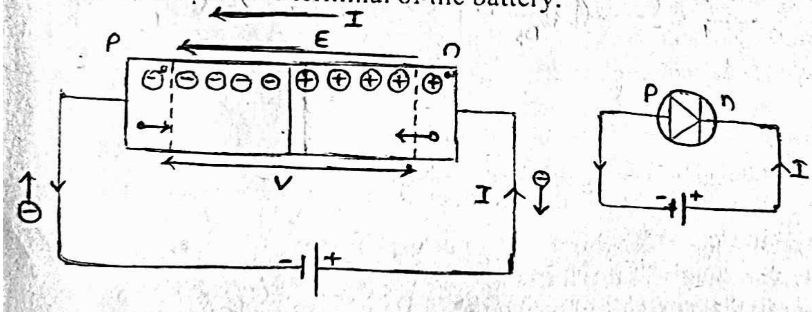
(1) Forward baising- A junction diode is said be forward biased when its p-region is connected to the positive terminal and the n-region is connected to the negative terminal of the battery.



In this biasing the applied potential difference (also called the forward bias voltage) opposes the barrier potential across the junction. As a result, the width of depletion layer decreases and the barrier potential is also reduced. If the applied voltage is greater than the barrier potential, the free electrons from the n-region move easily to the p-region through the junction and the holes move from the p-region to the n-region.

The flow of charges across the junction constitutes the forward current which is of the order of 10^{-3}A. However, the current in external circuit is due to the flow of electrons. Thus, a diode offers a low resistance in forward biasing circuit.

(2) Reverse biasing- A junction diode is said to be reverse biased when its p-region is connected to the negative terminal of the external battery and the n-region is connected to the positive terminal of the battery.



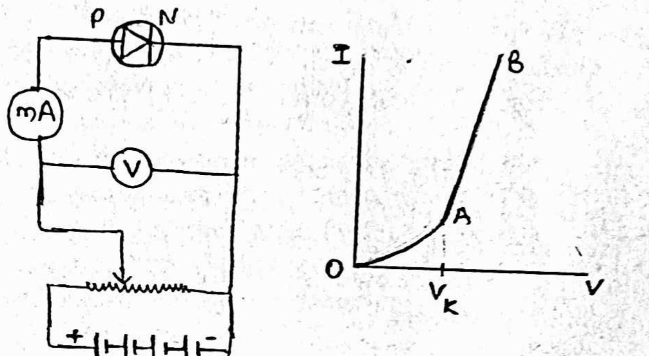
In this biasing, the applied voltage (called the reverse bias voltage) supports the potential barrier across the junction. As a result of which the width of the depletion layer as well as the potential barrier increases. Hence the majority charge carriers from the two regions can not cross the junction. However, the minority charge carriers i.e. electrons in p-region and the holes in the n-region are able to cross the junction under high reverse bias voltage. This result in a very small current in the direction opposite to that in the forward biasing. This current is called the reverse current which of the order of 10^{-6}A. However, the current in external circuit is due to the flow of electrons. Thus, a diode offers a high resistance in reverse biasing circuit.

Characteristics of a p-n junction diode

Ques.- With the help of suitable circuit diagrams, explain how will you sketch the characteristics curves of a junction diode. Explain these curves.

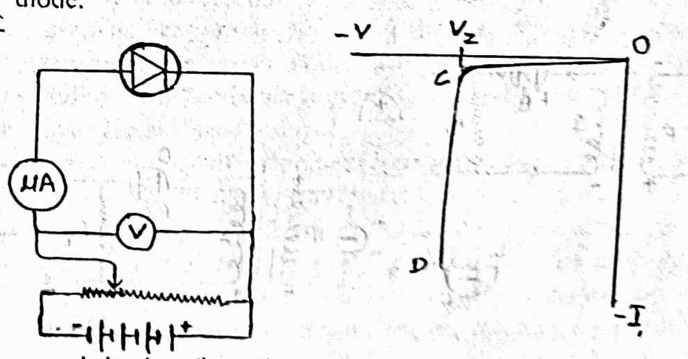
Ans.- The graphical variation of the current through a p-n junction with voltage applied across the junction is called the characterstic of the p-n junction. Depending upon the biasing, the p-n junction diode characteristic are of two types-

(i) Forward bias characteristics- Fig. (a) shows a junction diode in forward biasing through a voltmeter and an milliammeter. The applied voltage is increased gradually and the corresponding value of the forward current is recorded. A graph plotted between the forward bias voltage (V) and forward current (I) is shown in fig. (b). The V-I curve OAB is the forward bias characteristics of junction diode.



It is clear from the graph that when forward bias voltage (V) is less then the barrier potential, the current is small. As V is increased till it overcomes barrier potential, the current increases sharply. Beyond V_K (called the knee voltage), the current increases linearly with V.

(ii) Reverse bias characteristics- Fig.(a) shows a junction diode in reverse biasing through a voltmeter and a microammeter. The applied voltage is increased gradually and the corresponding value of the reverse current is recorded. A graph plotted between the reverse bias voltage (V) and reverse current (I) is shown in fig. (b). The V-I curve OCD is the reverse bias characteristics of junction diode.



It is clear from the curve that there is a very small reverse current over a long range of the reverse bias voltage. If reverse voltage is made very large, the reverse current increases sharply to become very large. This value of reverse bias voltage is known as zener voltage (V_Z) and the phenomenon is known as the zener voltage breakdown. The value of the zener voltage vary from 1 to 2V to several hundred volts.

Note- The current in forward biased junction diode is given by $I = I_0(e^{eV/kT} - 1)$

where I_0 is the reverse saturation current, T is the absolute temperature and V is the applied voltage.

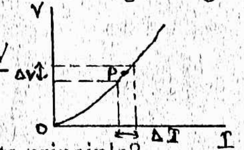
Dynamic resistance of junction diode

Ques.- Define dynamic resistance of a junction diode.

Ans.- Junction diode characteristics indicate that the current is not proportional to the potential difference applied across the junction. Hence, the circuit containing junction diode is a non-ohmic circuit.

The dynamic resistance of a junction diode is defined as the ratio of the small change in the applied voltage to the corresponding change in the current flowing through the junction.

$\therefore$ Dynamic resistance $R_d = \dfrac{\Delta V}{\Delta I}$



Junction diode as a rectifier

Ques.- What is a rectifier? What is its principle?

Ans. - The process of converting A.C. into D.C. is called rectification. A device which converts an alternating current (voltage) into direct current (voltage) is called rectifier.

Principle of rectifier- A junction diode conducts when forward biased and does not conduct when reverse biased. This unidirectional feature makes it suitable for rectification. A diode can be used as a rectifier in two ways-

(i) As a half rectifier.

(ii) As a full rectifier

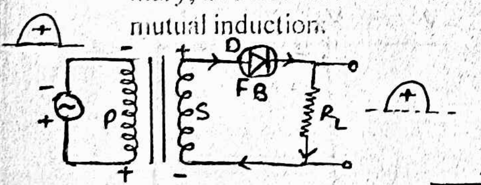
Diode as a half wave rectifier

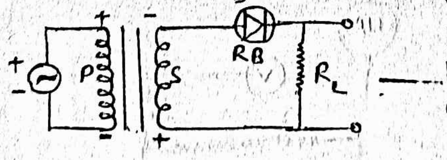
Ques.- With the help of a circuit diagram, explain the use of a junction diode as a half wave rectifier. Draw the input and output waveforms.

Ans. - The rectifier which rectifies only the positive half of the input a.c. supply is called the half wave rectifier.

Circuit arrangement- A half rectifier consists of a junction diode D, a transformer and a load resistance R_L. The a.c. to be rectified is connected to the primary coil of the transformer and the secondary coil is connected to the diode D through a load resistance R_L [Fig.(a)].

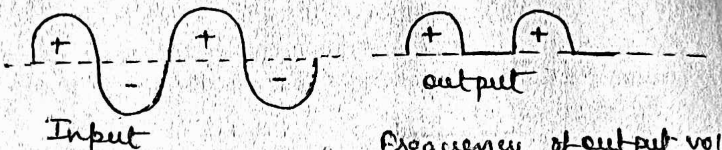
Working- When an A.C. voltage is applied across the primary, an A.C. emf is induced in the secondary coil due to mutual induction.





During the positive half cycle of the input A.C. voltage, end S_1 becomes positive w.r.t. end S_2. The junction diode becomes forward biased and hence the forward current flows through R_L. Due to which an output voltage is obtained acros the load resistance R_L during the positive half cycle which has the same shape as the positive half of the input.

During the negative half cycle of the input A.C. voltage end S_1 becomes negative withe respect to end S_2. The junction diode becomes reverse biased and no current flows in the circuit. Due to which an output voltage is not obtained across the load resistance R_L during the negative half cycle. The process repeats in the next cycles and a discontinuous and pulsating d.c. voltage output across the load resistance [Fig.(b)].



Frequency of output voltage is same as that of input voltage

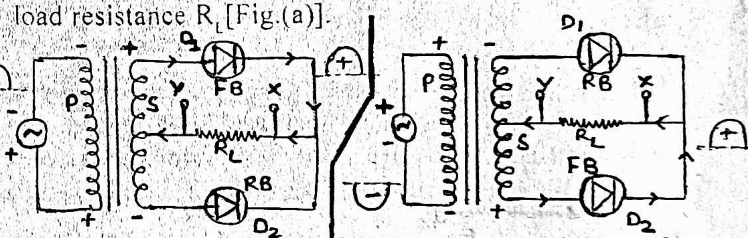
Note-Half wave rectification in not preferred because the output is not continuous. Hence there is lot of wastage of energy which results in low efficiency.

Diode as full wave rectifier

Ques.- With the help of a circuit diagram, explain the use of a junction diode as a full wave rectifier. Draw the input and output waveforms.

Ans. - The rectifier which rectifies both the halves of the input a.c. supply is called the full wave rectifier.

Circuit arrangement- It consists of two junction diodes D_1 and D_2, a transfomer and a load resistance (R_L). The A.C. to be rectified is connected to the primary coil of the transfomer. The ends S_1 and S_2 of the secondary coil are respectively connected to the p-region of the diodes D_1 and D_2. The load resistance (R_L) is connected across the n-region of the two diodes and the central tapping of the secondary coil. The output voltage is obtained across the load resistance R_L [Fig.(a)].



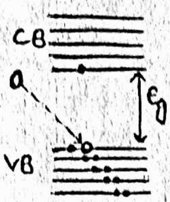
Working- During the positive half cycle of the input A.C. voltage, end S_1 becomes positive w.r.t. end S_2. The diode D_1 becomes forward biased and D_2 becomes reverse biased. Hence D_1 conducts and D_2 does not conduct. The current due to D_1 flows through R_L in the direction as shown in fig. (a).

During the negative half cycle of the A.C. input voltage, end S_1 becomes negative w.r.t. end S_2. The diode D_1 becomes reverse biased and D_2 becomes forward biased. Hence D_2 conducts and D_1 does not conduct. The current due to D_2 flows through R_L in the direction as shown in fig. (b).

Thus the current flows through R_L in the same direction during both half cycles of the input voltage. The process keeps repeating in the next cycles and a continuous and pulsating output voltage is obtained across the load resistance.

Note 1.- The frequency D.C.output voltage of a full wave rectifier is twice that of a half wave rectifier.

~~**Note 2.**-Bridge rectifier- During the positive half of the a.c. input voltage D_1 and D_2 conduct and D_3 and D_4 do not conduct. During the negative half, D_3 and D_4 conduct but D_1 and D_2 do not conduct. Thus output is obtained across R_L during both halves of the input A.C. voltage.~~

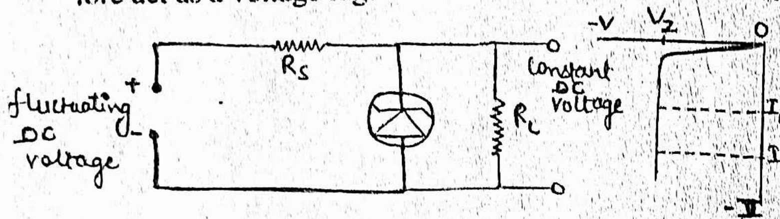


Zener diode

Ques.- What is zener diode? Give its symbol. Explain its use as a voltage regulator.

Ans. - It is a junction diode designed to work in breakdown region of reverse biasing. An ordinary junction diode can not work after zener breakdown. It gets damaged.

In a zener diode, the voltage drop is practically independent of the current that flows though it. It can therefore act as a voltage regulator.



Zener diode as a voltage regulator- The Zener diode is connected to the fluctuating D.C. in reverse biasing through a resistance R of suitable value. The output is obtained across a load resistance R_l, which is connected in parallel with zener diode. When the input fluctuating D.C. increases beyond a certain limiting value i.e. break down voltage, the current through zener diode increases sharply. As a result the voltage drop across resistance R_S increases. Hence, voltage drop across the load resisatnce R_l falls back to the normal value. Thus, zener diode helps to regulate the output voltage to a constant value.

★★ Optoelectronic junction devices

Ques.- What are Optoelectronic junction devices? How they are classified?

Ans. - The current through the semiconductor diodes changes either due to electron excitation by photons or due to electron excitation by biased voltage. These semiconductor devices are called optoelectronic junction devices.

∴ Optoelectronic junction devices are classified as follows-

(i) Photo-detectors used for detecting light signals e.g. photodiodes.

(ii) Photovoltaic devices which convert light energy into electricity e.g. solar cells

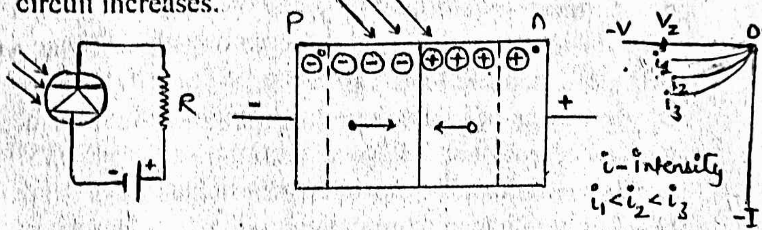
(iii) Light emitting diodes (LED) which convert ~~light~~ electrical energy into ~~electricity~~ light.

Photodiode

Ques.- What is a photodiode? Explain its working principle.

Ans. - It is a junction diode made from photo sensitive semiconductor material whose conductivity can be controlled by the light incident on it.

Figure shows a photo diode in reverse biasing but the reverse bias voltage is less than the breakdown voltage. Thus a very small reverse current (I) will flow in the circuit when light of suitable frequency is made to fall on the photo diode. Eelctrons starts moving from the valence band to the conduction band. As a result, the current in the circuit increases.



If the intensity of the light is ~~gradually~~ increased, the circuit current also increases. ~~till it attains the maximum saturation value.~~

Uses-(i) In detection of optical signals.

(ii) In light operated switches.

(iii) In electronic counters.

$ **Ques.**- Why a photodiode is operated in reverse bias?

Ans.- Consider an n-type semiconductor. Its majority electron density is much larger than the minority hole density i.e. n>>p. When illuminated with light, both types of carriers increase equally in number.

$$n' = n + \Delta n$$

and $p' = p + \Delta p$

Now $n >> p$ and $\Delta n = \Delta p$

$$\therefore \quad \frac{\Delta n}{n} << \frac{\Delta p}{p}$$

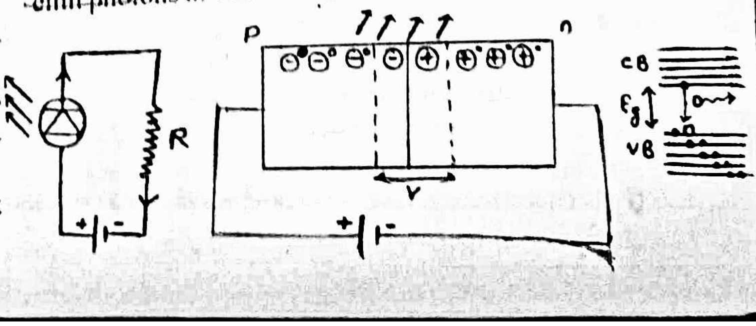
That is the fractional increase in majority carriers is much less than the fractional increase in minority carriers. As a result of which due to photo-effects the fractional change in the minorty carrier dominated reverse bias current is more easily measurable than the fractional change in the majority carrier dominated forward bias current. Hence photodiodes are used in reverse bias condition.

Light emitting diode (LED)

Ques.- What is a light emitting diode? Draw a circuit diagram and explain its action. How do we choose the semiconductor, to be used in light emitting diode, if the emitted radiation is in visible region? Give advantages of LEDs over incandescent lamps.

Ans. - A specially designed junction diode, which emits visible light when forward biased, is called light emitting diode. It therefore converts electrical energy into light energy. When a junction diode is forward biased, both the electrons from n-region and the holes from p-region move across the junction and combine together. In each electrons hole recombination, energy is released at the junction.

~~In Ge and Si diodes, the wavelength of the emitted photon falls in infra-red region. But the junction diodes made from the compounds like gallium arsenide or Indium phosphide emit photons in visible range.~~



$ **Choice of semiconductor used in LED**- The wavelength of visible light ranges from 0.4 μm to 0.7 μm (energy from 3eV to 1.8eV). For a semiconductor to emit visible light, the minimum band gap must be 1.8eV. The compound semiconductor Gallium-Arsenide-Phosphide ($GaAs_{1-x}P_x$) is used for making LEDs of different colours. $GaAs_{0.6}P_{0.4}$ is used for red LED and GaAs is used for infrared LED.

$ **Advantages of LEDs over incandescent lamps**-
(i) Low operational voltage and less power consumption.
(ii) Fast action and no warm up time required.
(iii) It is nearly monochromatic.
(iv) Long life and ruggedness.
(v) Fast on-off switching capability.

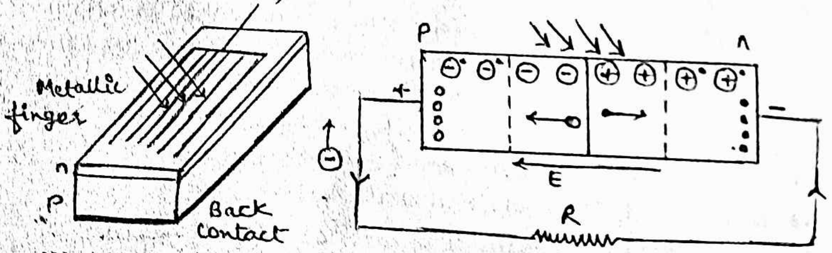
Uses- LEDs are used in remote controls, burglar alarm, optical communication etc.

Solar cell

Ques.- What is a solar cell? Explain its construction and working. Name the materials commonly used to prepare solar cells.

Ans. - A solar cell is a junction diode which converts solar energy into electrical energy. It works on the photovoltaic effect. When light is incident on a p-n junction, an emf is generated across its terminal.

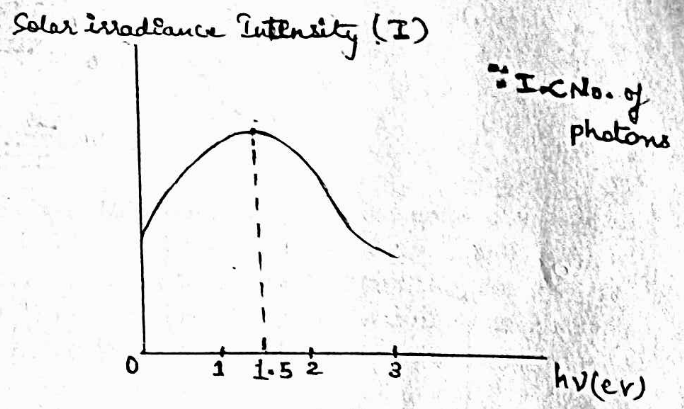
It consists of a p-n junction made from Si in which a thin layer n-type is taken on a p-type semiconductor. On the top of n-layer there is metal finger electrode (front contact) and on the other side of p-layer is coated with metal (back contact).

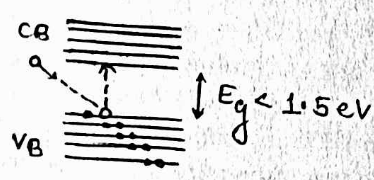


Working- When light is incident on p-n junction, each photon absorbed creates an electron and a hole. It is because the electron acquires sufficient energy and moves from the valance band to the conduction band. As a result, the number of free electrons and holes increases. The internal barrier electric field pushes these electrons towards the n-region and the holes towards the p-region. As a result of this, the two regions of the junction become oppositely charged and hence an emf is developed across the diode terminals. This is the photovoltaic emf which drives a current in the external circuit.

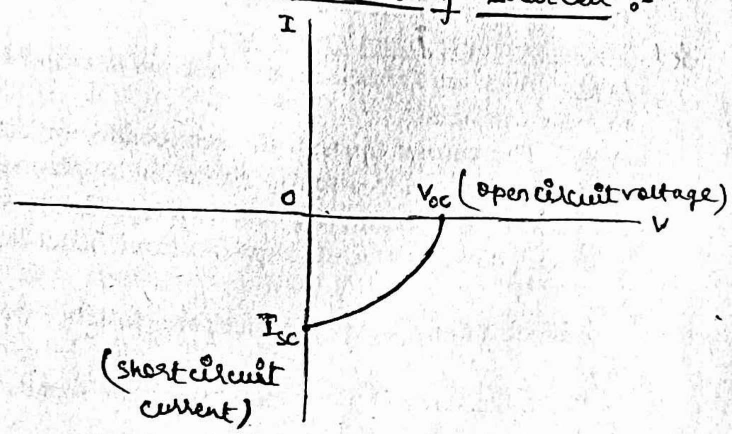
$ **Materials used to prepare solar cells**- Semiconductors with band gap close to 1.5eV are ideal materials for solar cells fabrication. Solar cells are made with semiconductors like Si (E_g = 1.1eV), GaAs (E_g = 1.43eV), CdTe (E_g = 1.45eV) etc. The important criteria for the selection of material for solar cell fabrication are-
(i) Band gap (1eV to 1.8eV)
(ii) High optical absorption (10^4 cm^{-1})
(iii) Electrical conductivity
(iv) Availability of raw material
(v) Cost

Uses- (i) Solar cells are used to produce power in artificial satellites and space crafts.
(ii) They are used for charging storage batteries during day time which can supply power during night.
(iii) They are used in wrist-watches and calculators.





⊛ I-V characteristics of solar cell :-



Transistor (Transfer of Resistor)

Ques.- What is a transistor? Mention its two types. Give their symbolic representations. Describe the construction of a transistor state the function of each of its part.

Ans. - A transistor is a semiconductor device having two p-n junctions and three terminals. It is obtained by sandwitching a thin layer of an extrinsic (p or n-type) semiconductor between two thick similar layers of the opposite extrinsic semiconductor (n or p-type).

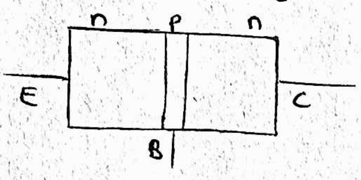
Transistor was invented in 1947 by Bardeen and Brattain.

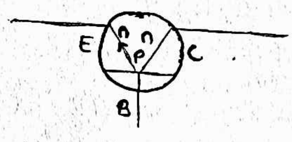
Transistors are of two types-

(i) n-p-n transistors

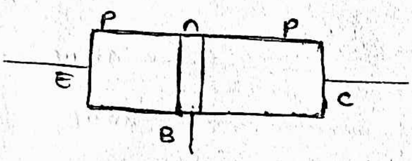
(ii) p-n-p transistor

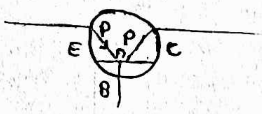
An n-p-n transistor is obtained when a thin layer of p type semiconductor is sandwitched between two thick layers of n-type semiconductor. The symbol of n-p-n transistor is shown in fig.





A p-n-p transistor is obtained when a thin layer of n type semiconductor is sandwitched between two thick layers of p-type semiconductor.The symbol of p-n transistor is shown in fig.





A transistor has three sections namely emitter, base and collector.

(a) Emitter- It is a heavily doped thick region. It supplies the majority charge carriers into the sandwiched region. i.e. the base.

(b) Base- It is a very lightly doped thin region. Hence most of the charge carriers coming from the emitter pass through it.

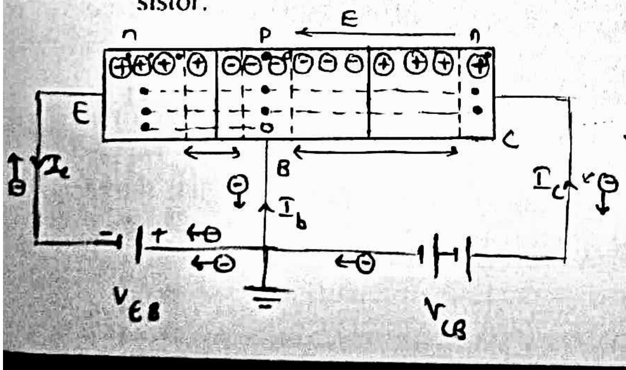
(c) Collector- It collects the charge carriers from the base. Its thickness is larger than that of the emitter.

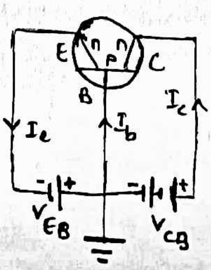
Action or working of a transistor

Ques.- Explain the action of a transistor witha proper circuit diagram showing the biasing of transistor.

Ans. - A transistor works when its emitter base junction is forward baised and the collector base junction is reverse biased.

(i) Working of n-p-n transistor- Fig. shows the circuit arrangement for analysing the working of an n-p-n transistor.





The emitter base junction is forward biased and the collector base junction is reverse biased. As a result the width of depletion layer (hence the resistance) decreases at EB junction but increases at the CB junction. The majority charge carriers i.e. electrons in the emitter are repelled towards base due to the forward biasing. These electrons diffusing from the emitter into the base consitute the emitter current (I_e).

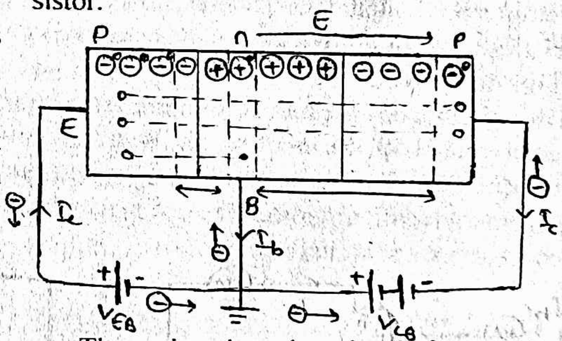
Since the base region is vary thin and lightly doped most of the electrons entering the base cross over into the collector region. A few (less than 5%) of these electrons recombine with the majority holes in the base region.

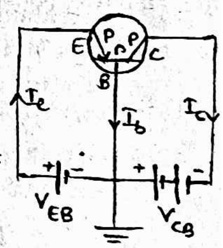
Since. the CB junction in reverse biased the electrons entering the collector region are attracted by the positive terminal of the battery V_{CB}. These electrons going from the collector to the battery V_{CB} constitute the collector current (I_c). For each electron combining with a hole in the base region. a covalent bond breaks in the base region and creates an electron and a hole. This electron through terminal B reaches the positive terminal of battery V_{BE} and constitute the base current (I_b). The hole created compensates for the hole lost in recombination in the base region. The electrons coming out at terminal C and B flow through the external circuit and reach the positive terminal of battery V_{BE}. Thus the flow of electrons from the emitter to the collector through the base continues. It is clear that

$$I_e = I_b + I_c$$

The value of I_b depends upon the thickness of the base and the doping level of emitter. base and the collector regions.

(ii) Working of p-n-p transistor- Fig shows the circuit arrangement for analysing the working of an p-n-p transistor.





The emitter base junction is forward biased and the collector base junction is reverse biased. As a result. the width of depletion layer (hence the resistance) decreases at EB junction but increases at the CB junction. The majority charge carriers i.e.holes in the emitter are repelled towards base due to the forward biasing. These holes diffusing from the emitter into the base consitute the emitter current (I_e).

Since the base region is vary thin and lightly doped most of the holes entering the base cross over into the collector region. A few (less than 5%) of these holes recombine with the majority electrons in the base region.

Each hole coming from the emitter to the collector region moves out through terminal C and gets neutralised by an electrons supplied by the negative terminal of the battery V_{CB}.These electrons going from the battery V_{CB}

to the collector constitute the collector current (I_c). At the same time, a covalent band breaks in the emitter region and an electron hole pair is created. The hole compensates for the loss (due to diffusion into the base) and the electrons moves out though terminal E to reach the positive terminal of the battery V_{EB}. A few of these electrons move from the negative terminal of the battery V_{EB} and enter into base these electrons compensates for the electrons lost in recombination in the base region and constitute the base current (I_b) nd the remaining electrons enter into the positive terminal of the battery V_{CB}. Thus the flow of the holes from the emitter to the collector through the base continues. It is clear that

$$I_e = I_b + I_c$$

Circuit configurations (or modes) of a transistor

Ques.- Which are the three circuit configurations of a transistor.

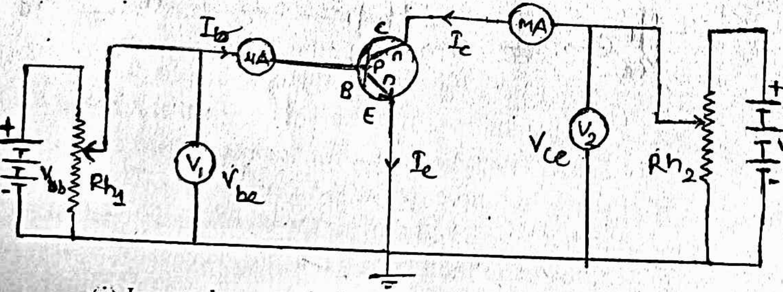
Ans. - When a transistor is used in a circuit, two terminals are required for the input and two terminals for the output. Hence, we require four terminals, But a transistor has only three terminals. The problem can be solved by making one terminal common to both the input and the output circuit. The common terminal generally connected to the ground and is used as a reference point for the entire circuit. Accordingly, there can be three ways in which a transistor can be used in a circuit. These are known as three circuit configuration (or modes) of a transistor. These are-

(i) Common base configuration
(ii) Common emitter configuration
(iii) Common collector configuration

Common emitter characteristics of a transistor

Ques.- Draw a circuit diagram for an n-p-n transistor in common emitter configuration to study its input and output characteristics. Draw approximate of these curves and give their important features.

Ans. - In this circuit configuration, the emitter of the transistor is common to both the input and the output circuits and is grounded. The characteristics of an n-p-n transistor in common emitter configuration can be understood by the circuit arrangement shown in fig.

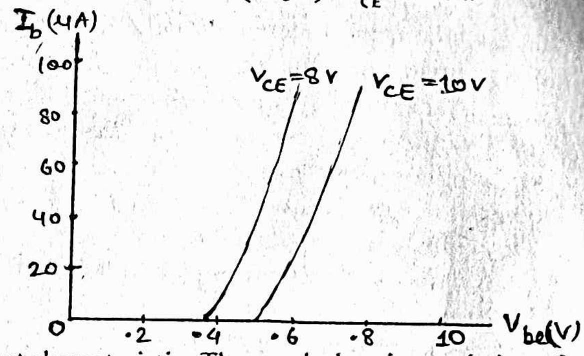


(i) Input characteristics- The graph showing variation of the base current (I_b) with the base emitter voltage (V_{BE}) at different constant values of the collector emitter voltage (V_{CE}) are called the input characteristics of the transistor. Following conclusions can be drawn from these characteristics-

(a) These are similar to the V-I characteristics of a junction diode in forward biasing.

(b) At a given value of V_{CE}, the base current (I_b) increases **rapidly with the increase** in base emitter voltage (V_{BE}).

(c) The input resistance $r_i = \left(\dfrac{\Delta V_{BE}}{\Delta I_b}\right)_{V_{CE}=\text{constt.}}$ is small



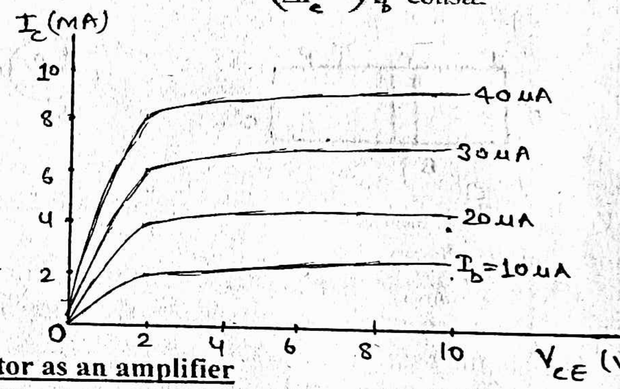
(ii) Output characteristic- The graph showing variation of the collector current (I_c) with the collector emitter voltage (V_{CE}) at different constant values of the base current are called the output characteristics. Following conclusions can be drawn from these characteristics-

(a) At a given value of the base current (I_b), the collector current (I_c) increases rapidly with the increase in collector emitter voltage (V_{CE}) but soon becomes almost constant.

(b) For a given value of V_{CE}, the collector (I_c) increases with the increase in the base current (I_b).

(c) A small collector current exists even when the base current (I_b) is zero.

(d) The output resistance, $r_o = \left(\dfrac{\Delta V_{CE}}{\Delta I_c}\right)_{I_b=\text{constt.}}$ is large.



Transistor as an amplifier

Ques.- What is an amplifier?

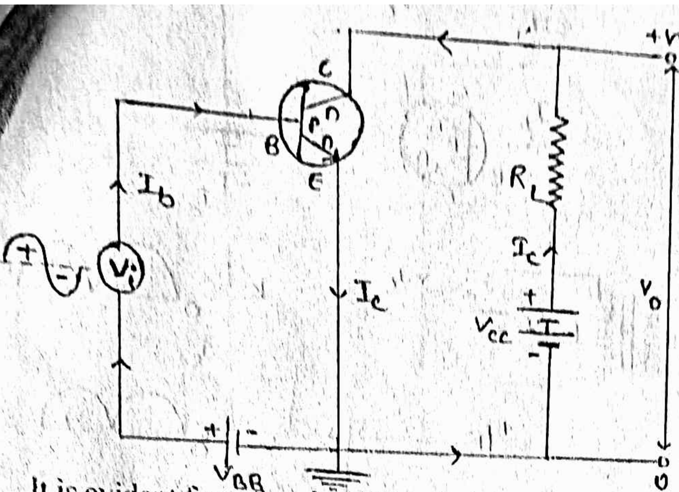
Ans. - An amplifier is a device which increases the amplitude of alternating voltage or power. It therefore produes an enlarged version of a weak input signal.

Transistor as common emitter amplifier using n-p-n transistor

Ques.- With the help of a labelled circuit diagram, explain the use of n-p-n transistor as a common emitter amplifier. Discuss phase relationships between input and output voltages.

Ans. - In this type of amplifier, the emitter is common to the input and the output circuits. The emitter base junction is forward biased by a battery (V_{BB}). The collector base junction is reverse biased by another battery (V_{CC}). Hence the resistance of the input circuit (R_i) becomes low and that of the output circuit (R_o) becomes high.

The input signal (V_i) is connected between the emitter and the base and the amplified output (V_o) is obtained across the collector and the ground. Figure shows the common emitter amplifier circuit using n-p-n transistor.



It is evident from the circuit that

$$I_e = I_b + I_c$$

In the output circuit

$$V_0 = V_{ce} - I_c R_L \qquad ----(i)$$

where $V_0 = V_{CE}$ is the output or the collector voltage.

When the input a.c. signal is fed to the input (emitter base) circuit. It changes the emitter base voltage. As a result, the emitter current and hence the collector current (I_c) changes. This is turn results in the variation of the output voltage (V_0) in accordance to equation (i) which appears as an amplified output voltage.

(a) <u>During the positive half cycle of the input signal</u>- The input signal supports the forward biasing (V_{BE}) across the EB junction. This increases the emitter current (I_e) and hence the collector current (I_c). The increase of the collector current increases the potential drop across the load resistance (i.e. $I_c R_L$). As a result, the output voltage (V_0) decreases. This means that the collector becomes less positive. Hence negative half cycle of the amplified output signal is obtained.

(b) <u>During the negative half cycle of the input signal</u>- The input signal opposes the forward biasing of the EB junction. This decreases the emitter current (I_e) and hence the collector current (I_c). The decrease of collector current decreases the potential drop across the load resistance (i.e. $I_c R_L$). As a result the output voltage (V_0) increases. This means that collector becomes more positive. Hence, the positive half cycle of the amplified output signal is obtained.

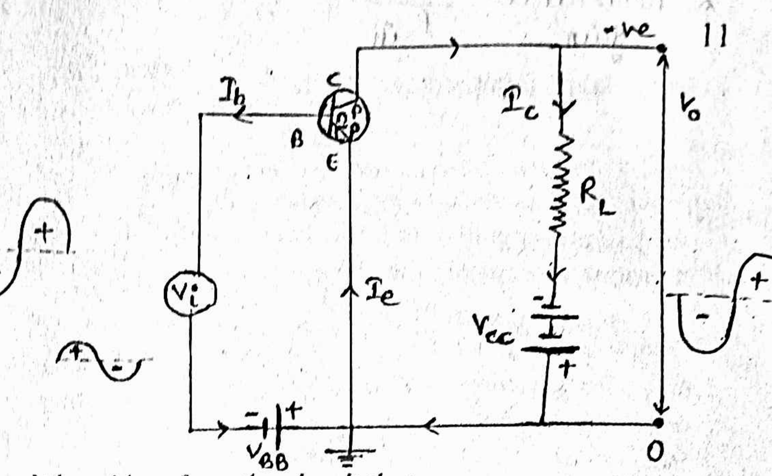
Thus, it can be concluded that in a common emitter emplifier, the input and the output signals are in the opposite phase.

<u>Common emitter amplifier circuit using p-n-p transistor</u>

<u>Ques.</u>- With the help of a labelled circuit diagram, explain the use of n-p-n transistor as a common emitter amplifier. Discuss phase relationships between input and output voltages.

<u>Ans.</u> - In this type of amplifier, the emitter is common to the input and the output circuits. The emitter base junction is forward biased by a battery (V_{BB}). The collector base junction is reverse biased by another battery (V_{CC}). Hence the resistance of the input circuit (R_i) becomes low and that of the output circuit (R_0) becomes high.

The input signal (V_i) is connected between the emitter and the base and the amplified output (V_0) is obtained across the collector and the ground. Figure shows the common emitter amplifier circuit using p-n-p transistor.



It is evident from the circuit that

$$I_e = I_b + I_c$$

In the output circuit

$$V_0 = V_{CC} - I_c R_L \qquad ----(i)$$

where $V_0 = V_{CE}$ is the output or the collector voltage.

When the input a.c. signal is fed to the input (emitter base) circuit. It changes the emitter base voltage. As a result, the emitter current and hence the collector current (I_c) changes. This is turn results in the variation of the output voltage (V_0) in accordance to equation (i) which appears as an amplified output voltage.

(a) <u>During the positive half cycle of the input signal</u>- The input signal opposes the forward biasing of the EB junction. This decreases the emitter current (I_e) and hence the collector current (I_c). The decrease of collector current decreases the potential drop across the load resistance (i.e. $I_c R_L$). As a result the output voltage (V_0) increases. This means that collector becomes more negative. Hence negative half cycle of the amplified output signal is obtained.

(b) <u>During the negative half cycle of the input signal</u>- The input signal supports the forward biasing of the EB junction. This increases the emitter current (I_e) and hence the collector current (I_c). The increase of collector current increases the potential drop across the load resistance (i.e. $I_c R_L$). As a result the output voltage (V_0) decreases. This means that collector becomes less negative. Hence, the positive half cycle of the amplified output signal is obtained.

Thus, it can be concluded that in a common emitter emplifier, the input and the output signals are in the opposite phase.

<u>Various gains in common emitter amplifier</u>

<u>Ques.</u>- Write the expressions of various gains of a common emitter amplifier.

<u>Ans.</u> - (i)<u>Current gain or amplification (β)</u>

(a) <u>D.C. current gain (β)</u>- It is defined as the ratio of the collector current (I_c) to the base current (I_b) at constant collector emitter voltage.

$$\beta = \left(\frac{I_c}{I_b}\right) V_{CE} = \text{constt.}$$

The value of β is large (> 15)

(b) <u>A.C. current gain (β_{ac})</u>-It is defined as the ratio of the change in the collector current (ΔI_c) to the change in the base current (ΔI_b) at constant collector emitter voltage.

$$\therefore \quad \beta_{ac} = \left(\frac{\Delta I_c}{\Delta I_b}\right) V_{CE} = \text{constt.}$$

(ii)<u>A.C. voltage gain (A_v)</u>- It is defined as the ratio of small change in the output voltage (ΔV_0) to the small

Resistance gain $= \frac{R_{out}}{R_{in}}$

change in the input voltage (ΔV_i).

$$\therefore \quad A_v = \frac{\Delta V_0}{\Delta V_i} = \frac{\Delta I_c \times R_0}{\Delta I_b \times R_i}$$

$$= \beta_{ac} \times \text{Resistance gain}$$

(iii) A.C. power gain- It is defined as the ratio of the change in the output power to the change in the input power.

$$\therefore \quad \text{Power gain} = \frac{\Delta P_0}{\Delta P_i} = \frac{\Delta V_0}{\Delta V_i} \times \frac{\Delta I_c}{\Delta I_b}$$

or Power gain = Voltage gain × Current gain

or Power gain $= A_v \times \beta_{ac}$

But $A_v = \beta_{ac} \times$ Resistance gain

$\therefore$ Power gain $= \beta^2_{ac} \times$ Resistance gain

Note- Transconductance- It is defined as the ratio of the change in collector current to the change in the emitter-base voltage. It is denoted by g_m.

$$\therefore \text{Trasconductance } g_m = \frac{\Delta I_c}{\Delta V_{BE}}$$

★ **Transistor as an oscillator** (Not in CBSE)

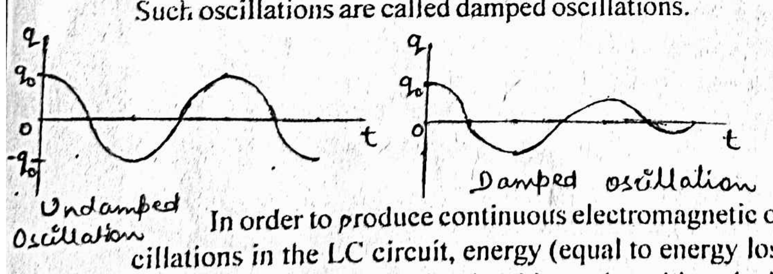
Ques.- What is an oscillator? Give its working principle. With the help of labelled of diagram, explain how a transistor can be used to obtain oscillations of constant amplitude.

Ans. - An oscillator is an electronic device which produces undamped electromagnetic oscillations.

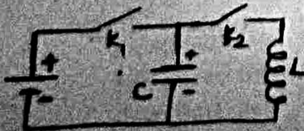
When a charged capacitor (C) is allowed to discharge through an inductor (L), the energy in the circuit shuttles back and forth between the electric field energy (inside the capacitor) and the magnetic field energy (inside the inductor). Consequently, electromagnet oscillations are produced in the circuit. The frequency of such oscillations is given by.

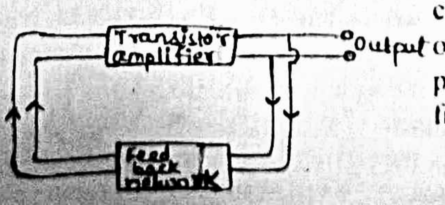
$$\nu = \frac{1}{2\pi\sqrt{LC}}$$

Since the circuit has some resistance, the energy is gradually lost in the form of heat. Hence the amplitude of the oscillations gradually decreases with time they die away. Such oscillations are called damped oscillations.



In order to produce continuous electromagnetic oscillations in the LC circuit, energy (equal to energy lost) must be supplied to the circuit. This can be achieved with the help of a transistor. The damped oscillations occuring in LC circuit are applied to the input of the transistor amplifier. The transistor produces an amplified output of these oscillations. A part of the amplified output voltage of the transistor is fed back in the LC circuit (input) in proper phase to make up for the energy losses in LC circuit. Hence continuous undamped oscillations (of constant amplitide) are produced.





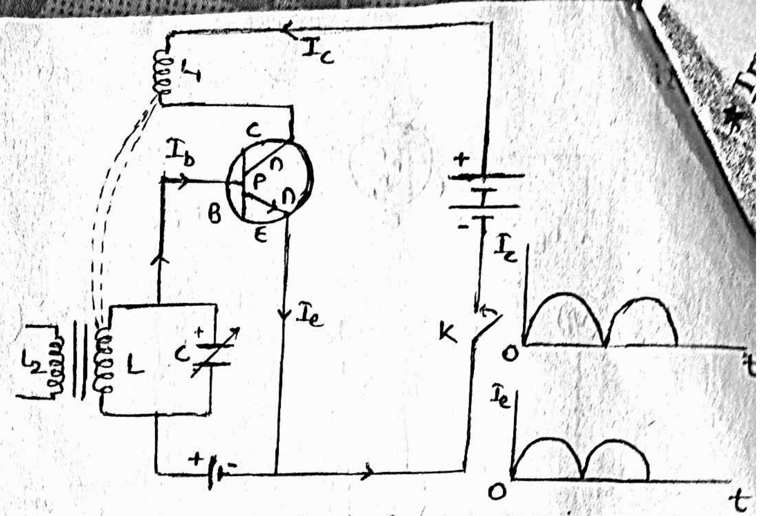


Figure shows the circuit of an n-p-n transistor as an oscillator in common emitter configuration. A tank circuit consisting of an inductor L and a variable capacitor C, connected between the emitter and the base along with suitable forward biasing provided by battery (B_1). Another inductor (L_1) called the feed back coil is connected between the emitter and the collector along with the necessary reverse biasing provided by battery (B_2). The coil L_1 is coupled with the coil L through mutual inductance in such a manner that an increasing magnetic flux through coil L supports the forward biasing and a decreasing magnetic flux opposes the forward biasing.

Working- When key K is closed, the collector current starts increasing through L_1. Due to this, the magnetic flux linked with coil L also increases. This in turn induces an emf in coil L. This is called the feed back voltage. The induced emf charges the capacitor such that its upper plate starts acquiring positive charge. This supports the forward biasing of the emitter base junction and hence the emitter current increases. Consequently, the collector current increases. Increase in the collector current also increases the magnetic flux through L_1 and hence through L. Thus the emf induced in L further increases. This subsequently increases I_e and I_c. The process continues till the collector current (I_c) attains the saturation (maximum) value.

As the current through coil L_1 stops changing the mutual induction stops playing its role and the capacitor starts discharging through coil L. Consequently the emitter current and hence the collector current decreases. The decreasing collector current through L_1 causes the magnitic flux linked with coil L to decrease. This causes the induction of an emf in L which opposes the forward biasing resulting a decrease in the emitter current and hence in the collector current. The process continues till the collector current becomes zero. The induced emf at this stage becomes zero. The capacitor gets discharged through the coil L. The emitter current and hence the collector again starts increasing. The process repeats and the collector current oscillates between a maximum (saturated) value and zero.

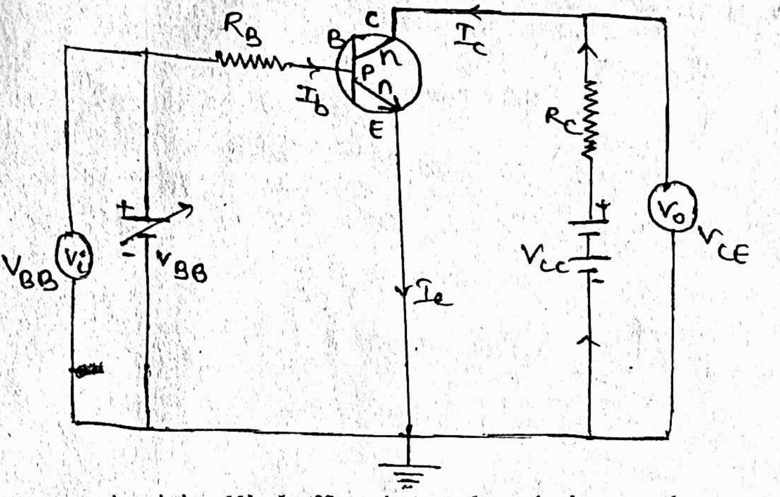
The output signal in the common emitter configuration of a transistor is 180° out of phase with input. The coupling between L_1 and L further produces a phase change of 180°. Thus the energy fed to the tank circuit is in proper phase and maintains oscillations of constant amplitude and frequency (ν) given by.

$$\nu = \frac{1}{2\pi\sqrt{LC}}$$

Transistor as a switch (Not in CBSE)

Ques.- How transistor is used as a switch? Explain.

Ans. - The operation of transistor as a switch can be understood by analysing the behaviour of transistor in CE configuration as shown in fig.



Applying Kirchoff's voltage rule to the input and output sides of this circuit, we get

$$V_{BB} = I_b R_B + V_{BE}$$

and $V_{CE} = V_{CC} - I_C R_C$

The V_{BB} is treated as the dc input voltage V_i and V_{CE} is treated as the dc output voltage V_o. So, we have

$$V_i = I_B R_B + V_{BE}$$

and $\quad V_o = V_{CC} - I_C R_C$

In the case of Si transistor, as long as input V_i is less than 0.6 V, the transistor will be in cut off state and current I_C will be zero. Hence $V_o = V_{CC}$

When V_i becomes greater than 0.6 V the transistor is in active state with some current in output path and the output V_o decrease as the term $I_C R_C$ increases. With increase of V_i, I_C increases almost linearly and so V_o decreases linearly till its value becomes less than about 1.0 V. Beyond this, the change becomes non linear and transistor goes into saturation state. With further increase in V_i the output voltage is found to decrease further towards zero though it may never become zero.

As long as V_i is low and unable to forward bias the transistor, V_o is high (V_{CC}). If V_i is high enough to drive the transistor into saturation, then V_o is low (very close to zero). When the transistor is not conducting it is said to be switched off and when it is driven into saturation it is said to be switched on. We can say that a low input to the transistor gives a high output and a high input gives a low output. The switching circuits are designed in such a way that the transistor does not remain in active state.

Advantages and disadvantages of semiconductor devices

Ques.- Give some advantages and disadvantages of semiconductor devices over vacuum tubes.

Ans. -Advantages- (i) Semiconductor devices are cheaper and more economical than the vacuum tube devices.

(ii) They are very small in size and weight as compared to the vacuum tubes.

(iii) They have no filaments. Hence no heating is required for emission of electrons. This saves a lot of electric power.

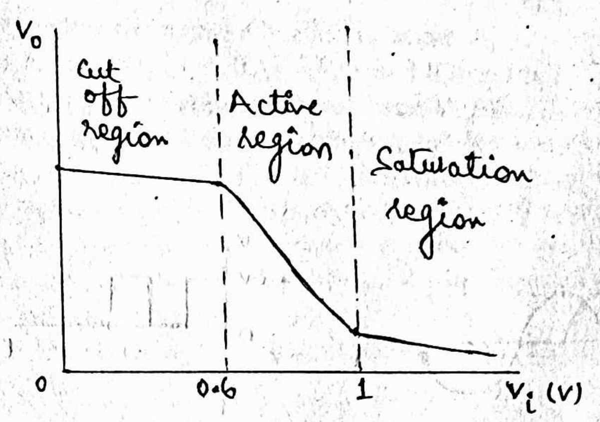
(v) They have small resistance and hence require very small power.

(vii) They do not produce any humming sound during their use.

Disadvantages- (i) Semiconductor devices are very sensitive to the temperature changes and hence get damaged due to overheating.

(ii) They cannot handle as much power as the vacuum tube devices can.

(iii) They are not suitable for high frequency inputs because of their poor response.

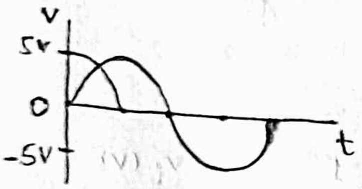


Analogue and digital signals

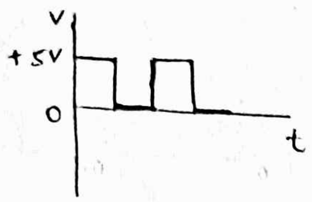
There are basically two types of electronic circuits- Analogue circuits and digital circuits. Analogue circuit deals with continuously varying voltage signals of sinusoidal nature. Such a continuously varying voltage signal is called an analogue signal.

In such circuits, the output changes continuously in accordance with the variations of the input. Hence, the output can have infinite number of values. Figure (a) shows a voltage analogue signal varying sinusoidally between +5 and -5 V.

A digital circuits, the output will either be (low or ligh) or (OFF or ON) or (0 or 1). The circuit is named digital as it expresses the value in digits 0's or 1's figure (b) shows a digital signal in which the voltage at any time is either 5 V or zero.



Analogue signal



Digital signal

Decimal number system

A decimal number system uses ten digits. 0, 1, 2, 3, 4, 5, 6, 7, 8, 9 to represent a number. Each digit in the number has place value. For example a number 3742 can be written as

$$3742 = 3 \times 10^3 + 7 \times 10^2 + 4 \times 10^1 + 2 \times 10^0$$

Thus, we find that the digit 3 is in thousand's place, 7 is in hundred's place, 4 is in ten's place and 2 is in unit's place. It is clear that the base of the decimal number system is 10.

Binary number system-

A binary number system uses only two digits 0 and 1 to represent any number. Each binary digit is called a 'bit'. The base of number system is 2 instead of the base 10 used in decimal system.

For example- Binary number 1 stands for $1 \times 2^0 = 1$

Binary number 11 stands for $1 \times 2^1 + 1 \times 2^0 = 3$

Binary number 101 stands for $1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 = 5$

Binary number 1101 stands for $1 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0$

$= 8 + 4 + 0 + 1 = 13$

Converting a decimal number to binary number

Divide the given decimal number by 2 and the successive quotients by 2 till the quotient becomes zero. The sequence of the remainders, taken in reverse order forms the binary number.

The last remainder obtained during the division is called the most significant digit or bit (MSD or MSB) of the binary number and the first remainder is called the least significant digit or bit (LSD or LSB) of the binary number.

Examples- (i) Binary equivalence of decimal number 2 decimal number

$2 \div 2 = 1$ and remainder 0

$1 \div 2 = 0$ and remainder 1

Hence binary equivalent of decimal number 2 is 10.

or $(2)_{10} = (10)_2$

In binary number 10, 1 is MSB and 0 is LSB.

(ii) Binary equivalent of decimal number 9

$9 \div 2 = 4$ and remainder 1 ← LSB

$4 \div 2 = 2$ and remainder 0

$2 \div 2 = 1$ and remainder 0

$1 \div 2 = 0$ and remainder 1 ← MSB

$\therefore (9)_{10} = (1001)_2$

(iii) Binary equivalent of 13

$13 \div 2 = 6$ and remainder 1 ← LSB

$6 \div 2 = 3$ and remainder 0

$3 \div 2 = 1$ and remainder 1

$1 \div 2 = 0$ and remainder 1 ← MSB

$\therefore (13)_{10} = (1101)_2$

Conversion of binary number to decimal number

In binary number system if one goes from LSB to MSB the multipliers of the bits are $2^0, 2^1, 2^2$........ Using these multipliers, we can find the decimal equivalent of a binary number.

Examples- (i) Decimal equivalent of binary number 1001

$1001 = 1 \times 2^3 + 0 \times 2^2 + 0 \times 2^1 + 1 \times 2^0$

↑ ↑

MSB LSB $= 8 + 0 + 0 + 1 = 9$

$\therefore (1001)_2 = (9)_{10}$

Hence decimal number equivalent to binary number 1001 is 9.

(ii) Decimal equivalent of 1110

$1110 = 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 0 \times 2^0$

↑ ↑

MSB LSB $= 8 + 4 + 2 + 0 = 14$

$\therefore (1110)_2 = (14)_{10}$

Logic gates

A digital circuit which works on a certain logical relationship between input and the output is called logic gate. A logic gate has one or more inputs but only one output. It either allows a signal to pass through or stops it.

The logic gates are the building blocks of a digital circuits.

The basic logic gates are of three types-

(i) OR gate

(ii) AND gate

and (iii) NOT gate

Each gate is represented by a symbol and its operation (i.e. function) is decribed either by a boolean expression or by a truth table.

Truth table

A table which lists all possible input combination and the corresponding output combination for a ligic gate is called its truth table.

@ SBoolean expression

The logical relation that a logic gate follows is called its boolean expresson..

Boolean algebra was invented by George Boole, an english mathematician. It deals with logical statements which have only two values namely true or false, ON or OFF, high or low etc. represented by binary numbers 1 and 0 respectively.

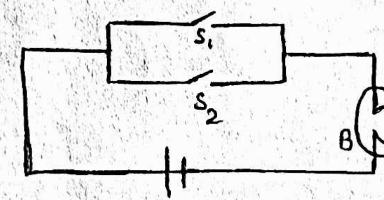
In Boolean algebra, three operations carried out on Boolean variables are-

(i) The OR operation
(ii) The AND operation
(iii) The NOT operation

(i) The OR operation- It is represented by addition (+) sign and the Boolean expression for this operation is given by

$$A + B = Y$$

It reads A or B equals Y. It means that the output Y is high if any A or B or both the inputs are high. Thus the output will be low (0) if both inputs are low (0).



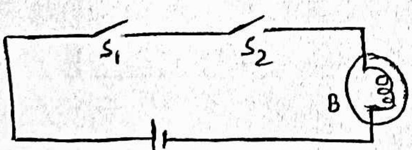
The electric circuit with two switches S_1 and S_2 connected in paralled with a battery and an electric bulb B demonstrates the OR operation. It is evident from the circuit that the bulb will glow if either switch S_1 or S_2 or both switches are closed. The bulb will not glow when both the switches are open. The action of the circuit is summerised in the following table-

Switch (S_1)	Switch (S_2)	Bulb (B)
OFF (0)	OFF (0)	OFF (0)
OFF (0)	ON (0)	ON (1)
ON (1)	OFF (0)	ON (1)
ON (1)	ON (1)	ON (1)

(ii) The AND operation- It is represented by dot (.) sign and the Boolean expression for this operation is given by

$$A . B = Y$$

It reads A and B equals Y. It means that the output Y is high when both the inputs A and B are high. Thus the output will be low (0) if any or both inputs are low (0).



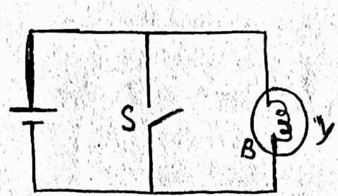
The electric circuit with two switches S_1 and S_2 connected in series with an electric bulb B and a battery demonstrates the AND operation. It is clear from the circuit that the bulb B will glow only when both switches S_1 and S_2 are closed The bulb will not glow when either of the two switches or both switches are open. The action of the circuit is summerised in the following table-

Switch (S_1)	Switch (S_2)	Bulb (B)
OFF (0)	OFF (0)	OFF (0)
OFF (0)	ON (1)	OFF (0)
ON (1)	OFF (0)	OFF (0)
ON (1)	ON (1)	ON (1)

(iii) The NOT operation- It is represented by a bar over the Boolean variable and the Boolean expression for this operation is given by

$$\overline{A} = Y$$

It reads NOT A equals Y. It means that the output Y is low when the input A is high and vice versa.
Thus, if A = 1 then Y = 0 and A = 0 then Y = 1.



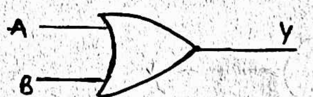
The electric circuit with switch S and an electric bulb B connected in paralled with a battery demonstrates the NOT operation. It is clear from the circuit that the bulb B glows when switch S is kept open. It however, will not glow when switch S is closed. It is because nearly whole current will then flow through the low resistance path containing switch S.

The action of the circuit is summerised in the following table-

Switch (S)	Bulb (B)
OFF (0)	ON (1)
ON (1)	OFF (0)

The OR gate

It is a device which has two (or more) inputs and one output. It gives output (1) if input A or input B or both inputs A and B are high (1), otherwise the output is zero.



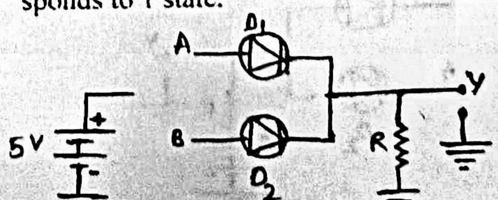
The logic symbol of OR gate is shown in fig. The boolean expression of OR gate is

$$A + B = Y$$

It reads as A or B equals Y. The truth table or OR gate is shown in the following table-

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Realization of OR gate- An OR gate can be realized by means of two p-n junctions diodes D_1 and D_2 connected in an electric circuit as shown in fig. The negative terminal of the battery is earthed (zero potential) and hence corresponds to 0 state. The positive terminal is at 5V and corresponds to 1 state.



Depending upon how the input terminals A and B are connected to 0 and 1 state, there may or may not be potential drop across the resistor R i.e. output Y. The work

-ing of OR gate can be understood by considering the following four possible cases-

(i) When A = 0 and B = 0 i.e when both input terminals A and B are connec ·d to earth. In this case, both the diodes do not conduct and hence there is no potential drop across the resistor R. Hence the output is zero i.e. Y=0.

(ii) When A = 0 and B = 1 i.e. input terminal A is connected to earth and terminal B is connected to positive terminal of the battery. In this case, diode D_2 being forward biased conducts but diode D_1 does not conduct. This current causes a potential drop of 5 V across the resistor R. Hence the output is 5V i.e. Y=1.

(iii) When A = 1 and B = 0 i.e. terminal A is connected to the positive terminal of the battery and terminal B is connected to earth. In this case, diode D_1 being forward biased conducts current but D_2 does not conduct. This current causes a potential drop of 5 V across the resistor R. Hence the output is 5V i.e. Y=1.

(iv) When A = 1 and B = 1 i.e. both A and B are connected to the posi·ive terminal of the battery. In this case, both diodes D_1 and D_2 get forward biased and conducts current. This current causes a potential drop of 5 V across the resistor R. Hence the output is 5V i.e. Y=1.

Thus, the possible combinations of the inputs A and B and the corresponding outputs Y as shown in the truth table of OR gate are satisfied.

The AND gate

It is device which has two (or more) inputs and one output. It gives output (1) if both inputs A and B are high (1), otherwise the output is zero.

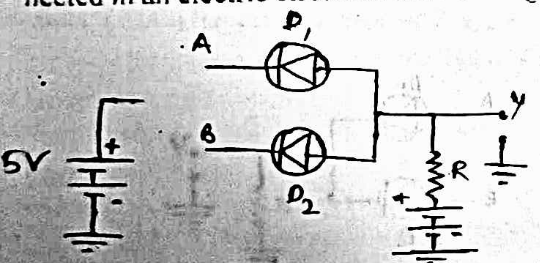
The logic symbol of AND gate is shown in fig. The Boolean express·on of AND gate is

$$A . B = Y$$

It reads as A and B equals Y. The truth table of AND gate in shown in fig.

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

S@Realization of AND gate- An AND gate can be realized by using two p-n junctions diodes D_1 and D_2 connected in an electric circuit as shown in fig.



The resistor R is permanently connected to the positive terminal of a 5V battery (B_2). The negative terminal of the battery B_1 is earthed (zero potential) and hence corresponds to 0 state. The positive terminal is at 5V and corresponds to 1 state.

Depending upon how the input terminals A and B are connected to 0 and 1 state, there may or may not be potential drop across the resistor R i.e. output Y. The working of AND gate can be understood by considering the following four possible cases-

(i) When A = 0 and B = 0 i.e when both input terminals A and B are connected to earth. In this case, both diodes D_1 and D_2 get forward biased and conducts current. This current causes a potential drop of 5 V across the resistor R. Hence the output is zero i.e. Y=0.

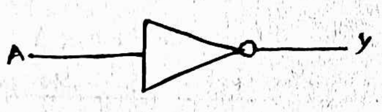
(ii) When A = 0 and B = 1 i.e. input terminal A is connected to earth and terminal B is connected to positive terminal of the battery. In this case, diode D_1 being forward biased conducts but diode D_2 does not conduct. This current causes a potential drop of 5 V across the resistor R. Hence the output is zero i.e. Y=0.

(iii) When A = 1 and B = 0 i.e. terminal A is connected to the positive terminal of the battery and terminal B is connected to earth. In this case, diode D_2 being forward biased conducts current but D_1 does not conduct. This current causes a potential drop of 5 V across the resistor R. Hence the output is zero i.e. Y=0.

(iv) When A = 1 and B = 1 i.e. both A and B are connected to the positive terminal of the battery. In this case, both the diodes do not conduct and hence there is no potential drop across the resistor R. Hence the output is 5V i.e. Y=1.

The NOT gate

It is a device which has only on input and one output. Its output is high (1) if the input is low (0) and vice versa. It is therefore also called the inverter.



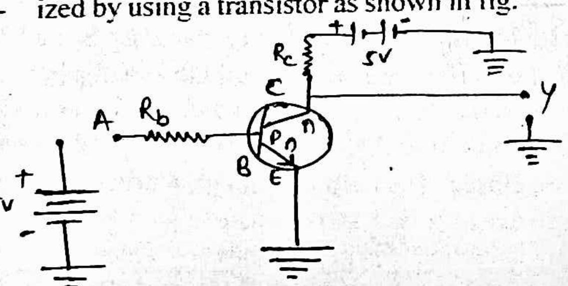
The logic symbol of NOT gate is shown in fig. The Boolean expression of AND gate is

$$A = Y$$

It reads as NOT A equals Y. The truth table of NOT gate is shown in fig.

A	Y
0	1
1	0

S@Realization of NOT gate- A NOT gate can be realized by using a transistor as shown in fig.



The base B of the transistor is connected to the input through resistance R_B. The collector is connected to earth through resistor R_C and a 5V battery and the emitter is connected to earth. The output is the voltage at C w.r.t. to earth.

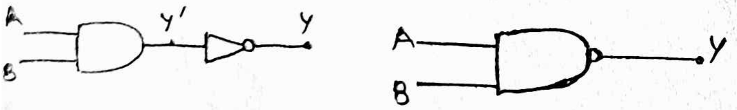
The two possible cases that explain the working of NOT gate are.

(i) When A = 0 i.e. terminal A is connected to earth. In this case the base emitter junction remains unbiased but the base collector junction gets reverse biased. Hence there will be no collector current. It means there will be no potential drop across the resistor R_C. Hence, the output Y will be 5V i.e. Y = 1

(ii) When A = 1 i.e. terminal A is connected to the positive terminal of the battery. In this case, the emitter base junction gets forward biased and the base collector junction is reverse biased. As a result, large collector current flows through R_C, and a potential drop equal to 5V is developed across R_C. Hence, the output Y will be zero i.e. Y = 0.

Combination of gates- Various combinations of the three basic gates i.e. OR, AND and NOT produce complicated digital circuits. Such combinations are also called gates. These gates are represented by using the symbols of the basic gates. The two most commonly used combinations of gates- NAND gate and NOR gate are described below.

(i) **The NAND gate**- The word NAND is an abbreviation of NOT-AND. The NAND gate is a combination of AND and NOT gates. In other words, if the output of an AND gate is connected to the input of a NOT gate (fig. a) the gate so formed is called NAND gate. Fig. (b) shows the logic symbol of a NAND gate.



The Boolean expression for NAND gate is

$$\overline{A.B} = Y$$

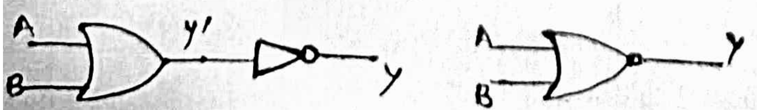
It reads as A and B negated equals Y.

The truth table of the NAND gate can be obtained by combing the truth tables of AND and NOT gates.

A	B	Y' (=A.B)	Y(= $\overline{A.B}$)
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

(ii) **The NOR gate**- The word NOR is the abbreviation of NOT-OR. The NOR gate is combination of OR and NOT gates. In other works, if the output of OR gate is connected to the input of a NOT gate [fig. 9.61(a)]. The gate so formed is called NOR gate. Figure 9.61 shows the logic symbol of a NOR gate.



The Boolean expression fo NOR gate is

$$\overline{A+B} = Y$$

It reads as A or B negated equals Y.

The truth table of NOR gate can be obtained by combing the truth tables of OR and NOT gates.

A	B	Y' (=A+B)	Y(= $\overline{A+B}$)
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

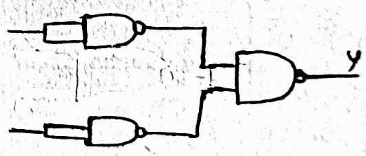
NAND (or NOR) gate as a digital building block

The three basic gates i.e. OR, AND and NOT gate alone can not form different gates by repeated use. But the repeated use of NAND (for NOR) gate can form all other gates including the three basic gates OR, AND, and NOT. It is for this reason that the NAND (or NOR) gate serve as building block in digital circuits and are called universal gates.

Forming NOT gate from NAND gate- If the two inputs A and B of the NAND gate are joined together to make one input, then the NAND gate works as a NOT gate. The logic symbol of the NOT gate obtained from the NAND gate is shown in fig. Its turth table is obtained by taking A = B in the truth table of the NAND gate.

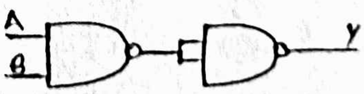
A	B(= A)	Y
0	0	1
1	1	0

Forming OR gate from NAND gate- If the outputs of two NOT gates (obtained from the NAND gates) is fed to a third NAND gate. Then this combined gate works as an OR gate. The truth table of this gate is shown in fig.



A	B	$\overline{A}$	$\overline{B}$	Y
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

Forming AND gate from NAND gate- If the output of the NAND gate is fed to the NOT gate (obtained from the NAND gate) then the combined gate works as the AND gate. The truth table of this gate is shown in fig.

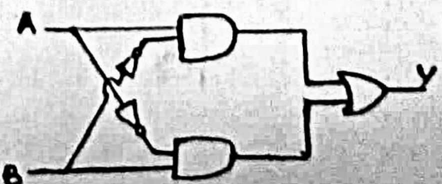


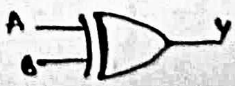
A	B	Y'	Y
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

The XOR gate

The XOR gate is the abbreviation of exclusive OR gate. It is obtained by combining two NOT gates, two AND and an OR gate as shown in fig(a). Its logic symbol is shown in (b). The Boolean experssion for the XOR gate is

$$Y = A \cdot \overline{B} + \overline{A} \cdot B$$

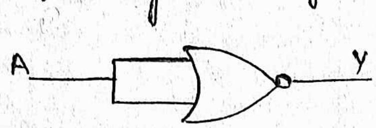




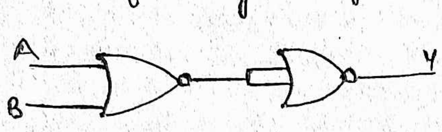
Input		Output
A	B	Y
0	0	0
1	0	1
0	1	1

* NOR gate as digital building block :-

1) forming NOT gate from NOR gate



2) forming OR gate from NOR gate



3) forming AND gate from NOR gate