Project 2- ECE 506

Dragon and Firefly Cache Coherence Protocol Implementations

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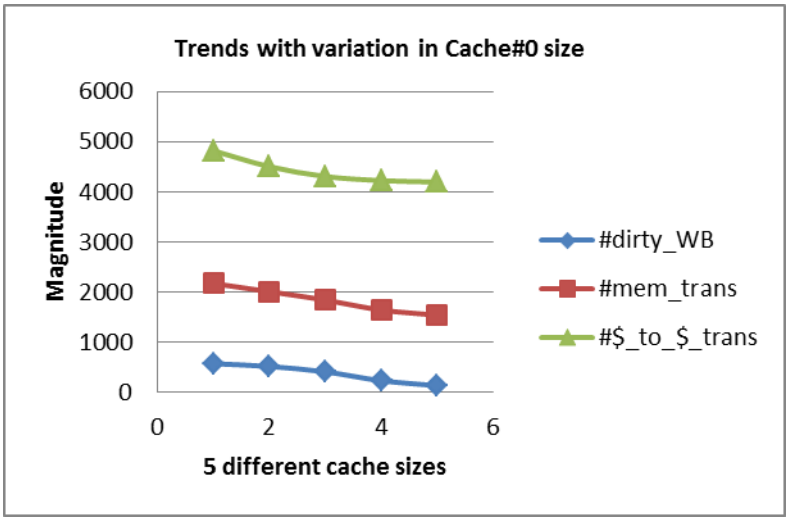
Experiment 1 on the Dragon protocol

Varying the cache size keeping the associativity(8) & block size(64B) constant

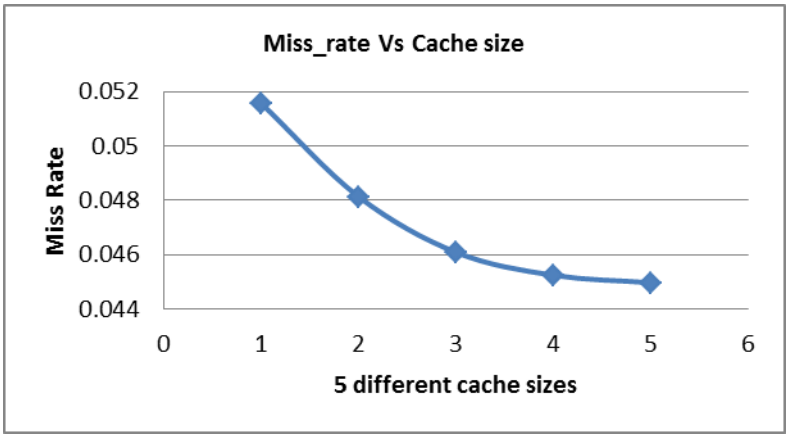
RESULTS

Cache#0					
Cache size	**32KB**	**64KB**	**128KB**	**256KB**	**512KB**
#reads	112661	112661	112661	112661	112661
#read_misses	6423	5995	5470	5635	5601
#writes	11942	11942	11942	11942	11942
#write_misses	3	3	3	3	3
Miss_rate	0.051572	0.048137	0.04609	0.045248	0.044975
#dirty_WB	567	512	404	226	128
#mem_trans	2169	2006	1839	1639	1536
#$_to_$_trans	4824	4504	4308	4225	4196



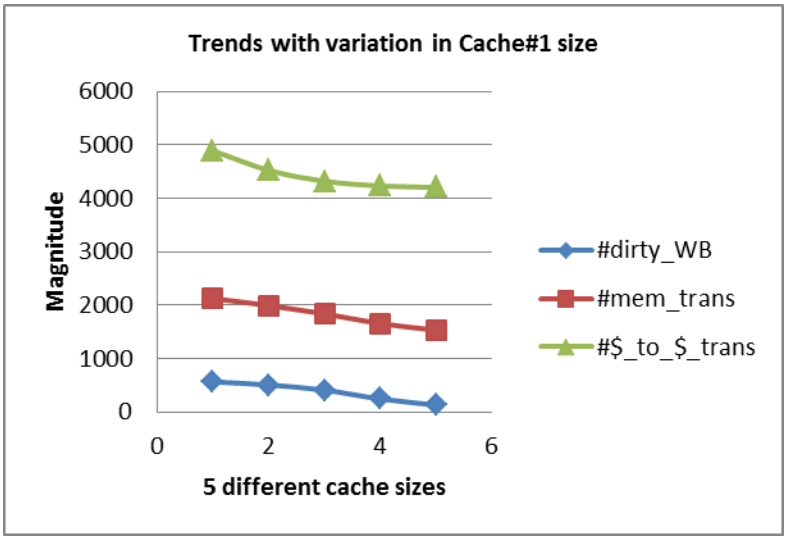
Discussion: We see that as the cache size increases, all the 3 parameters i.e. the number dirty Write_Backs, number of memory transactions and cache to cache transfers decrease.

This is because larger caches can hold more data and thus,as the number of sets increase,the number of misses that are incurred will also decreases as seen in the table for Cache#0

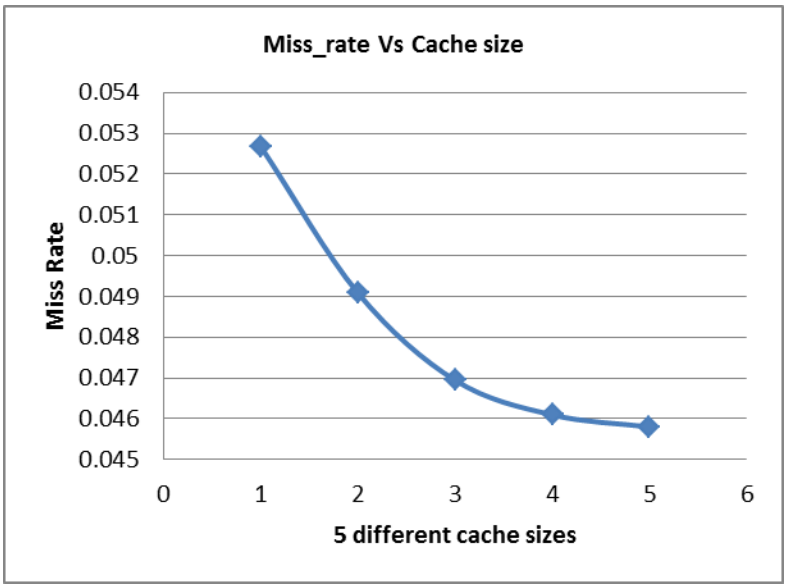


Discussion:As the number of read misses decrease,it also brings about a reduction in the miss rate exponentially as seen in the graph alongside

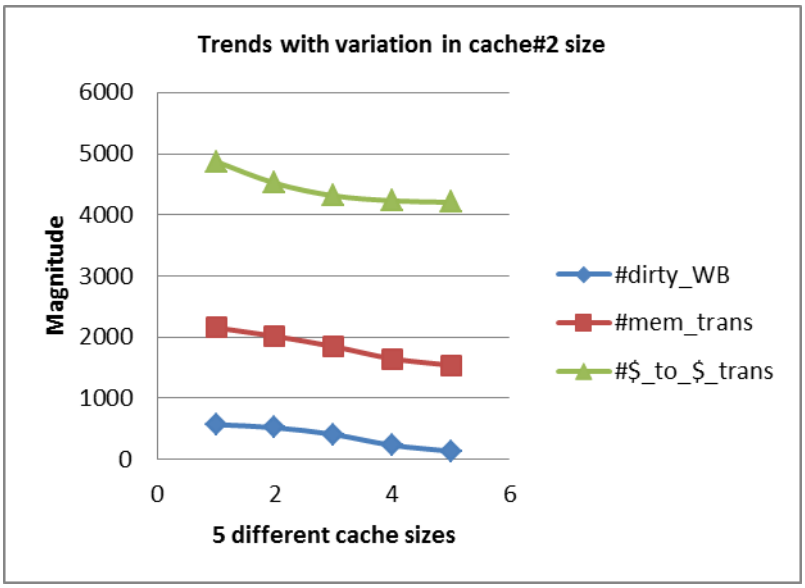
Cache#1					
Cache size	**32KB**	**64KB**	**128KB**	**256KB**	**512KB**
#reads	110830	110830	110830	110830	110830
#read_misses	6452	6012	5750	5646	5610
#writes	11710	11710	11710	11710	11710
#write_misses	2	2	2	2	2
Miss_rate	0.052669	0.049078	0.04694	0.046091	0.045797
#dirty_WB	562	506	408	243	127
#mem_trans	2124	1993	1838	1656	1532
#$_to_$_trans	4892	4527	4322	4235	4207

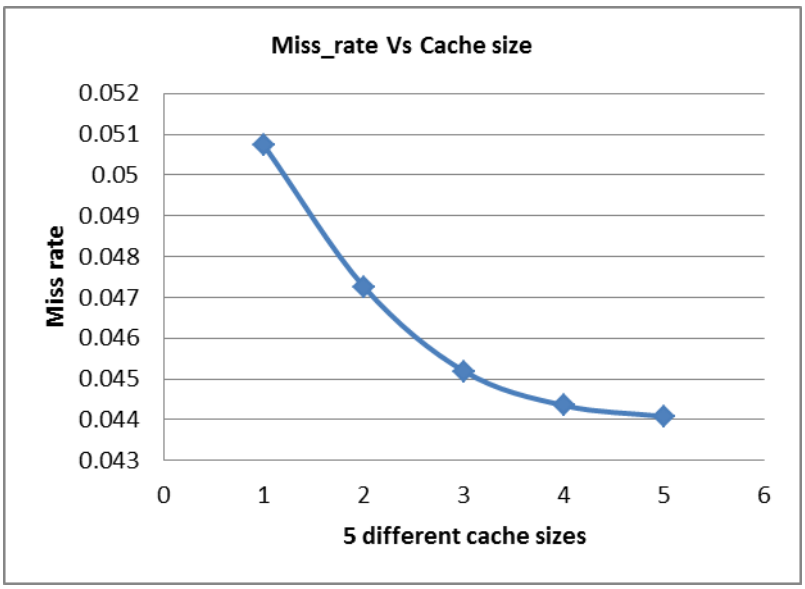


Discussion: As seen previously in the trend for cache#0,cache#1 also shows the same trend of reduction in the number of dirty writebacks, number of memory transactions and the number of cache to cache transfers.The miss rate is also seen to decrease with the reduction in the number of read misses



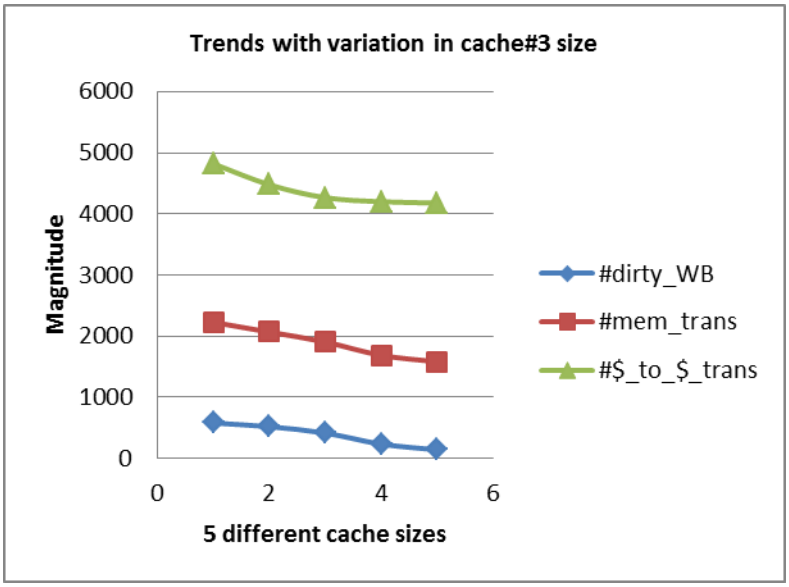
Cache#2					
Cache size	**32KB**	**64KB**	**128KB**	**256KB**	**512KB**
#reads	114938	114938	114938	114938	114938
#read_misses	6456	6014	5751	5644	5610
#writes	12383	12383	12383	12383	12383
#write_misses	2	2	2	2	2
Miss_rate	0.050722	0.047251	0.045185	0.044345	0.044078
#dirty_WB	569	519	409	232	135
#mem_trans	2154	2015	1848	1647	1541
#$_to_$_trans	4873	4520	4314	4231	4206

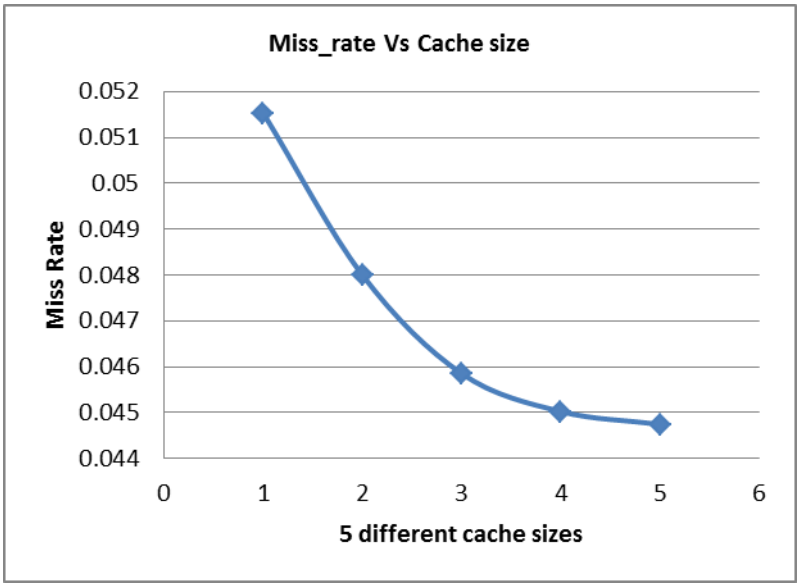




Cache#3

Cache size	32KB	64KB	128KB	256KB	512KB
#reads	113428	113428	113428	113428	113428
#read_misses	6468	6025	5756	5652	5617
#writes	12108	12108	12108	12108	12108
#write_misses	1	0	0	0	0
Miss_rate	0.051531	0.047994	0.045851	0.045023	0.044744
#dirty_WB	580	519	415	234	141
#mem_trans	2227	2067	1905	1686	1581
#$_to_$_trans	4822	4477	4266	4200	4177



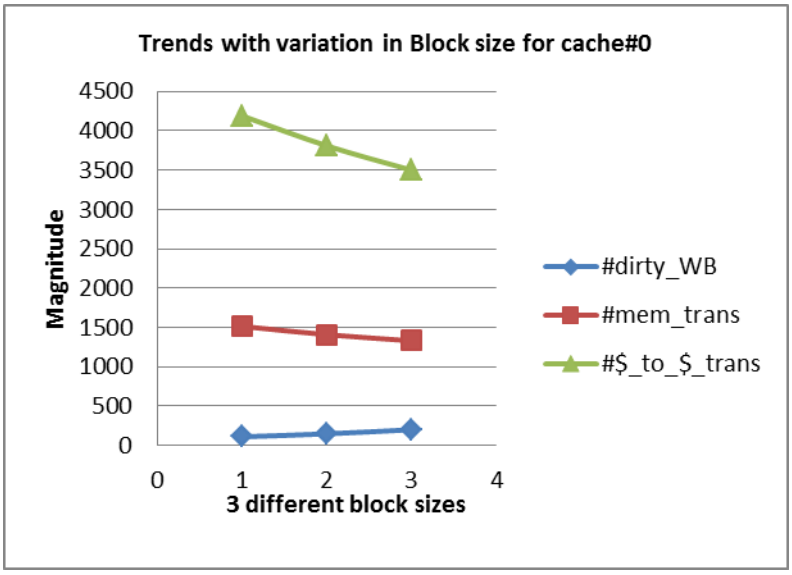


Experiment 2 on the Dragon protocol

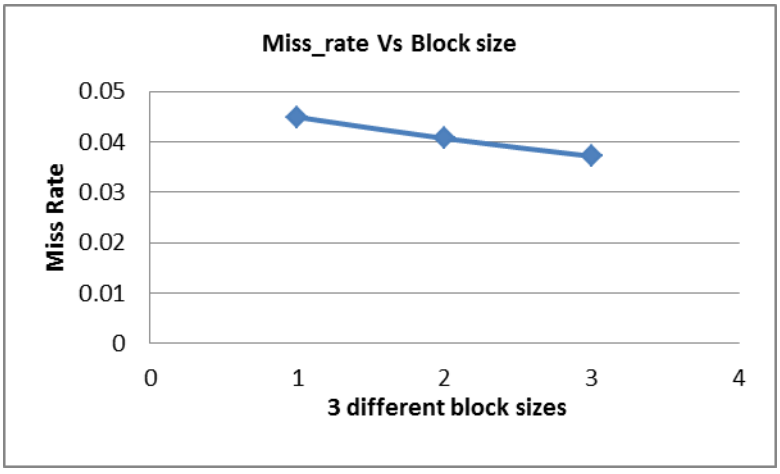
Varying the block size keeping the cache size constant(1MB) & associativity constant(8)

RESULTS

Cache#0	Size 1MB		
Block size	**64**	**128**	**256**
#reads	112661	112661	112661
#read_misses	5595	5069	4628
#writes	11942	11942	11942
#write_misses	3	3	3
Miss_rate	0.044927	0.040705	0.037166
#dirty_WB	107	145	198
#mem_trans	1513	1407	1329
#$_to_$_trans	4192	3810	3500

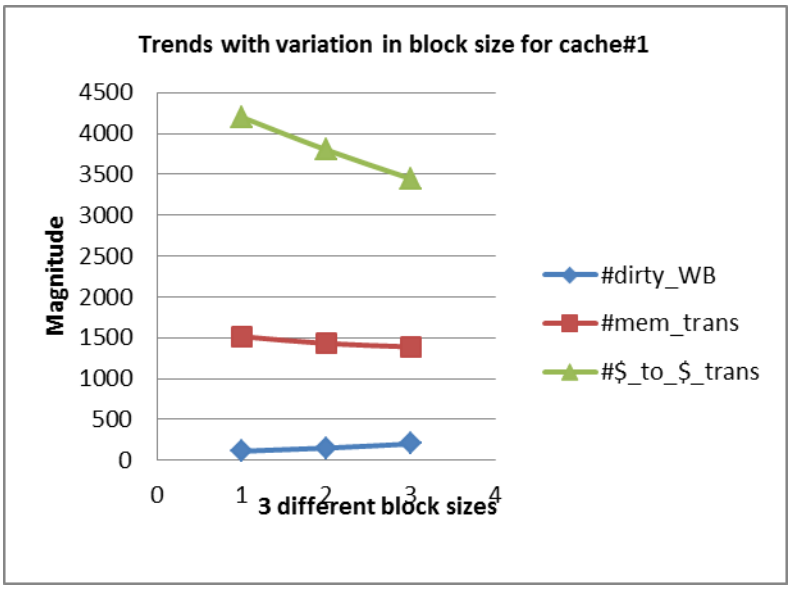


Discussion: As the block size increases, the number of blocks that the cache can hold decreases. This is the reason that the number of dirty writebacks increase. With larger blocks, as spatial locality is exploited, the number of cache to cache transfers and the number of transactions with the memory decrease. As we see, the number of read misses are less, we will require fewer times to fetch data from the memory and supports the trend of decreasing memory transactions.

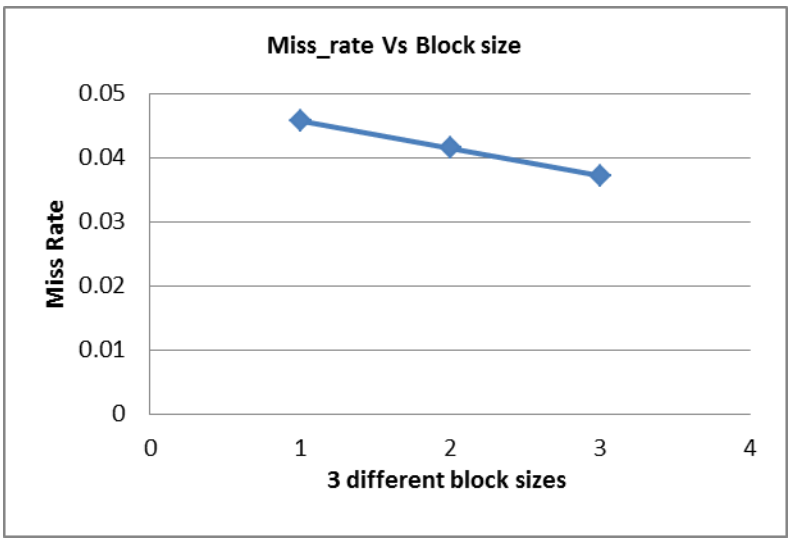


Discussion: The miss rate decreases due to the reduction in the read misses being a ratio of the number of misses(read+write) divided by the total number of reads and writes.Unlike the previous trends,this is a linear reduction with variation in the block size

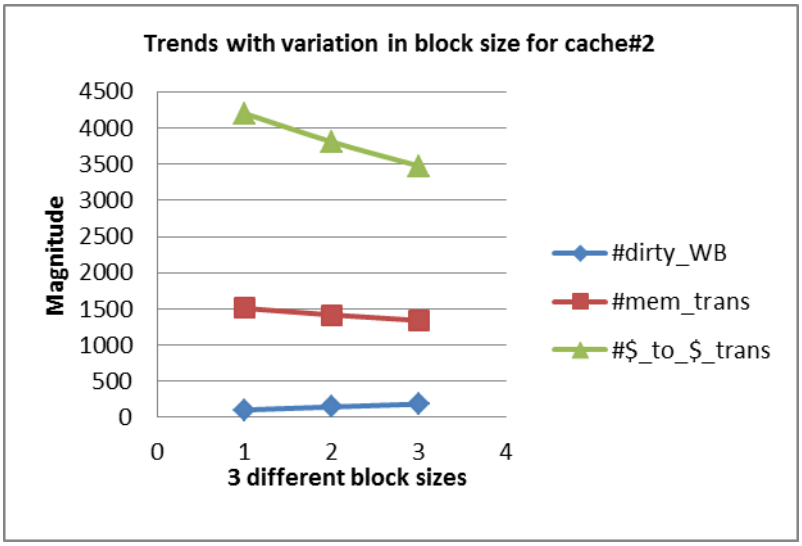
Cache#1	Size1MB		
Block size	**64**	**128**	**256**
#reads	110830	110830	110830
#read_misses	5604	5080	4633
#writes	11710	11710	11710
#write_misses	2	1	1
Miss_rate	0.045748	0.041464	0.037186
#dirty_WB	110	149	200
#mem_trans	1514	1430	1388
#$_to_$_trans	4202	3800	3446

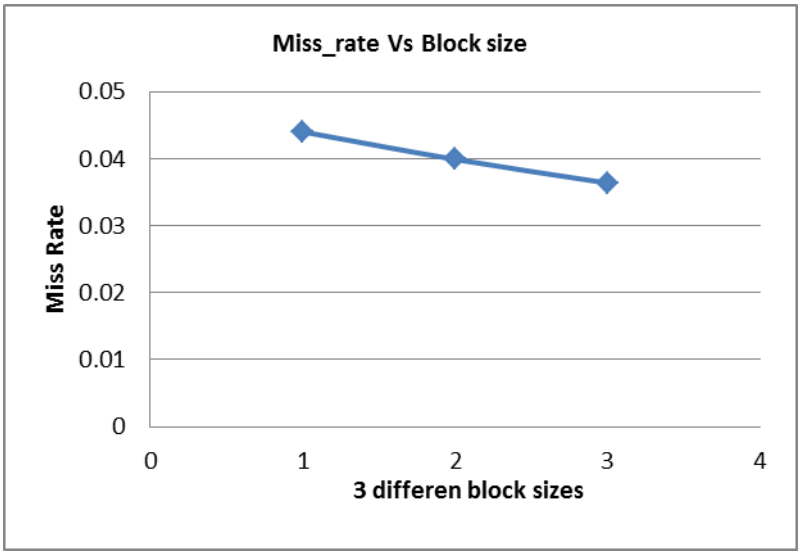


Discussion: The trends for cache#1,cache#2 and cache#3 are the same as that of cache#0.The number of cache to cache transfers and the number of memory transactions decrease with the increase in the block size.The number of writebacks increases due to the fact that blocks may need to be replaced more often to make place for new blocks coming in. The miss rate is also shown to decrease linearly

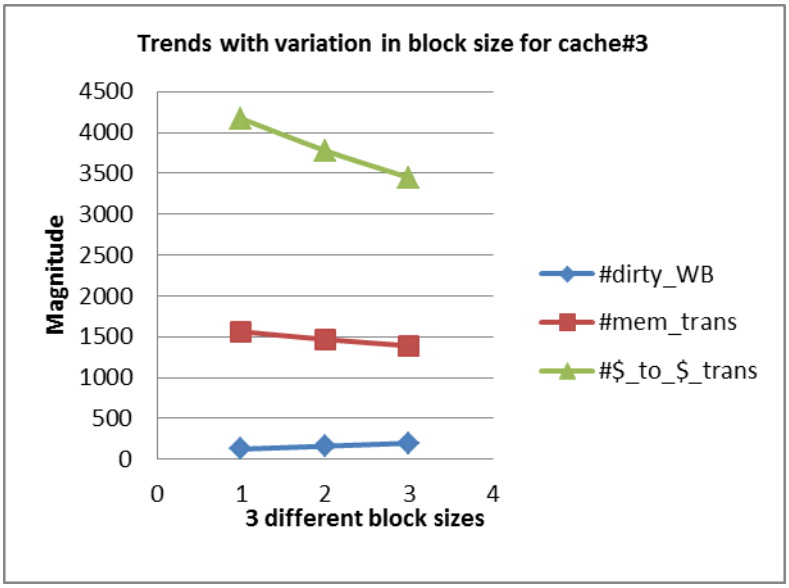


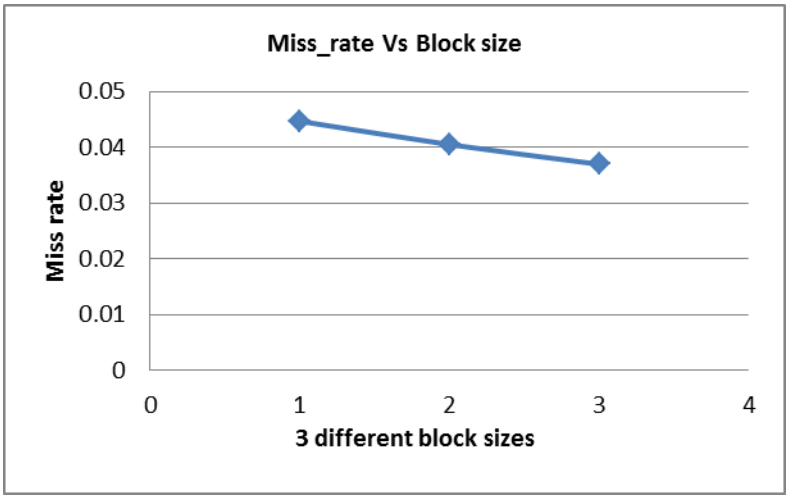
Cache#2	Size1MB		
Block size	**64**	**128**	**256**
#reads	114938	114938	114938
#read_misses	5604	5080	4630
#writes	12383	12383	12383
#write_misses	2	2	2
Miss_rate	0.04403	0.039915	0.03638
#dirty_WB	105	145	185
#mem_trans	1509	1418	1341
#$_to_$_trans	4202	3809	3476





Cache#3	Size1MB		
Block size	**64**	**128**	**256**
#reads	113428	113428	113428
#read_misses	5611	5086	4640
#writes	12108	12108	12108
#write_misses	0	0	0
Miss_rate	0.044696	0.040514	0.036963
#dirty_WB	123	160	196
#mem_trans	1562	1467	1389
#$_to_$_trans	4172	3779	3447




Miss_rate Vs Block size
0.05
0.04
0.03
0.02
0.01
0
Miss rate
0
1
2
3
4
3 different block sizes

Experiment 1 on the Firefly Protocol:

Varying the cache size keeping the associativity (8) & block size(64B) constant.

Results:

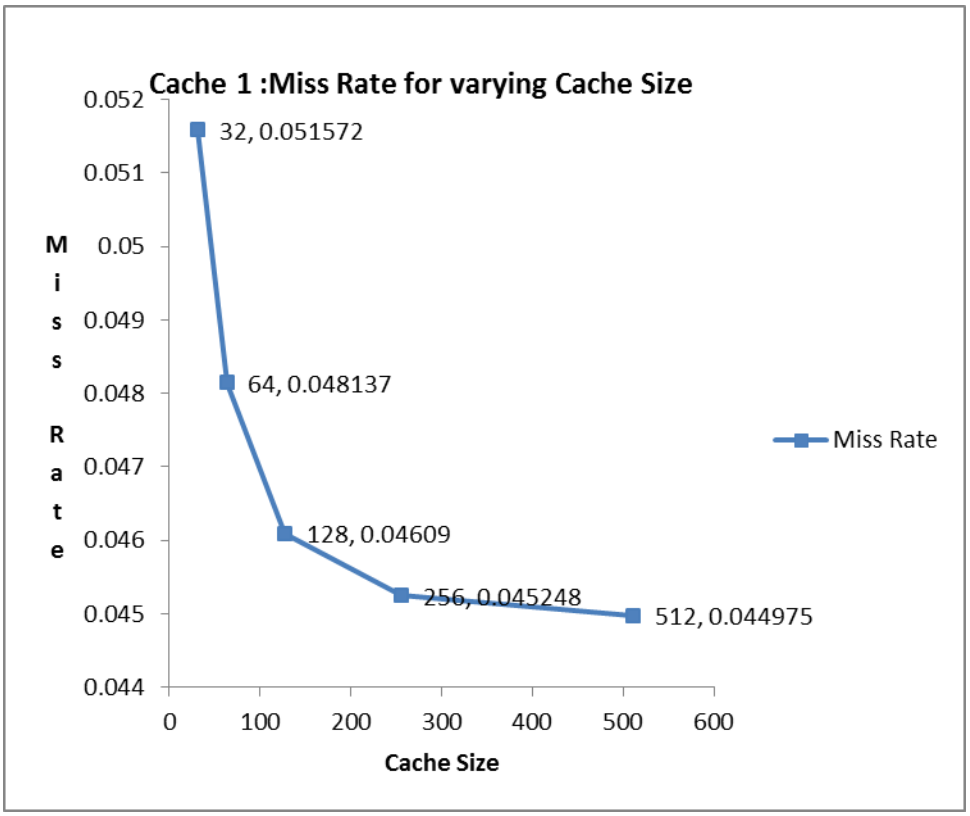
For Cache#1

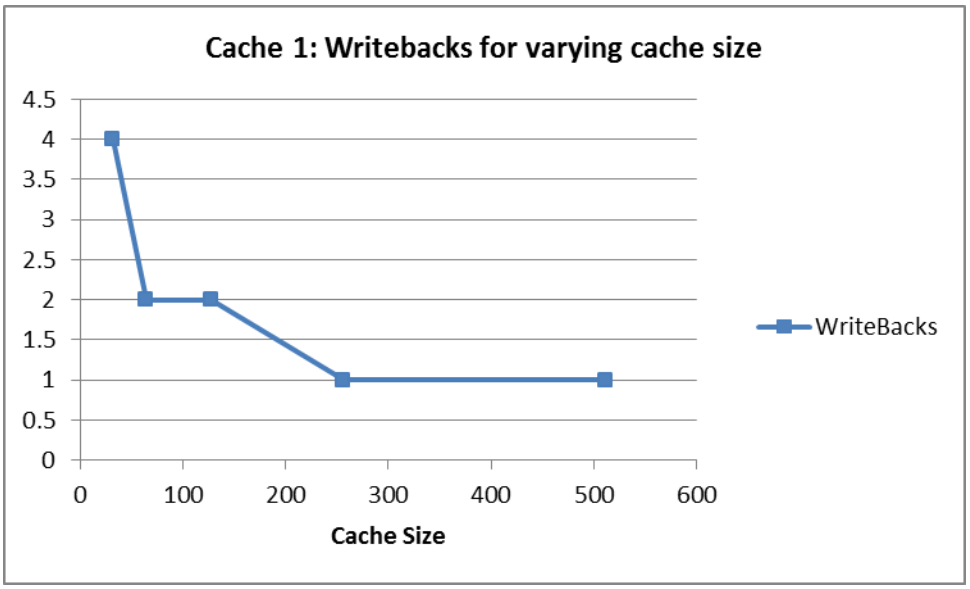
The readings recorded for the experiment are as follows:

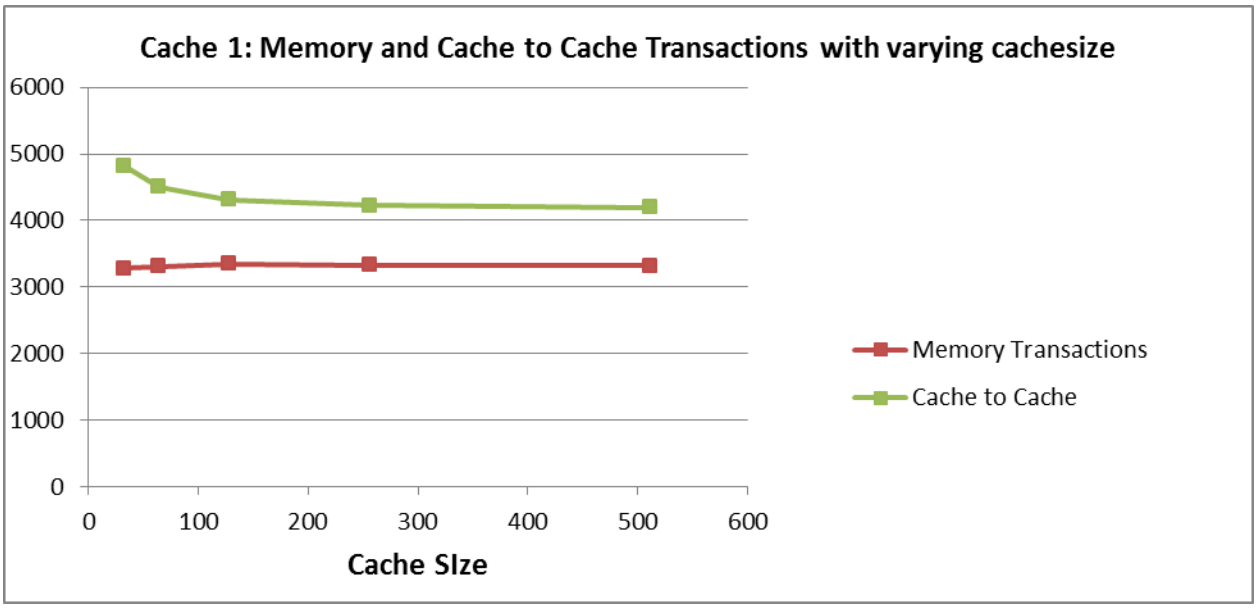
Cache size	32	64	128	256	512
#reads	112661	112661	112661	112661	112661
#read_misses	6423	5995	5740	5635	5601
#writes	11942	11942	11942	11942	11942
#write_misses	3	3	3	3	3
Miss_rate	0.051572	0.048137	0.04609	0.045248	0.044975
#dirty_WB	4	2	2	1	1
#mem_trans	3283	3313	3347	3324	3319
#cache_to_cache_trans	4824	4504	4308	4225	4196

Discussion : We observe the following from the graphs for Cache 1 on varying the cache sizes:

- The miss rate decreases with the increase in cache size. This is because the capacity misses will reduce as the size of the cache increases.
- The number of writebacks decreases as the capacity increases, less blocks have to be evicted from the cache.
- As the number of misses decreases, the cache to cache transfers will reduce as shown in the graph. This is because the number of blocks requested from other caches would reduce.
- As the cache size increases, the number of misses decreases and thus the number of write-throughs to the memory increases. Hence, increasing the number of memory transactions.


Cache 1 :Miss Rate for varying Cache Size
0.052
0.051
0.05
0.049
0.048
0.047
0.046
0.045
0.044
Miss Rate
32, 0.051572
64, 0.048137
128, 0.04609
256, 0.045248
512, 0.044975
0
100
200
300
400
500
600
Cache Size
Miss Rate


Cache 1: Writebacks for varying cache size
4.5
4
3.5
3
2.5
2
1.5
1
0.5
0
0
100
200
300
400
500
600
Cache Size
WriteBacks



For Cache #2:

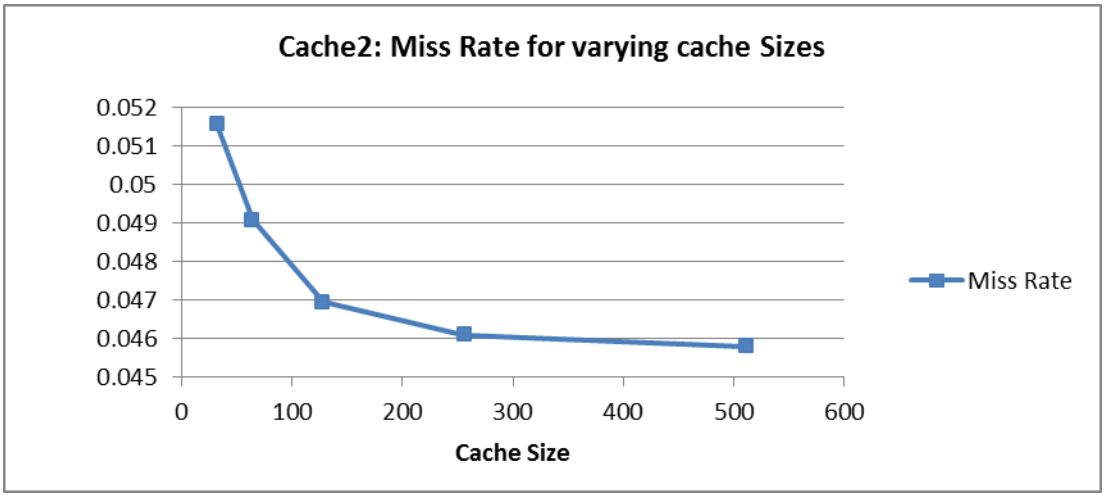
The readings recorded were as follows:

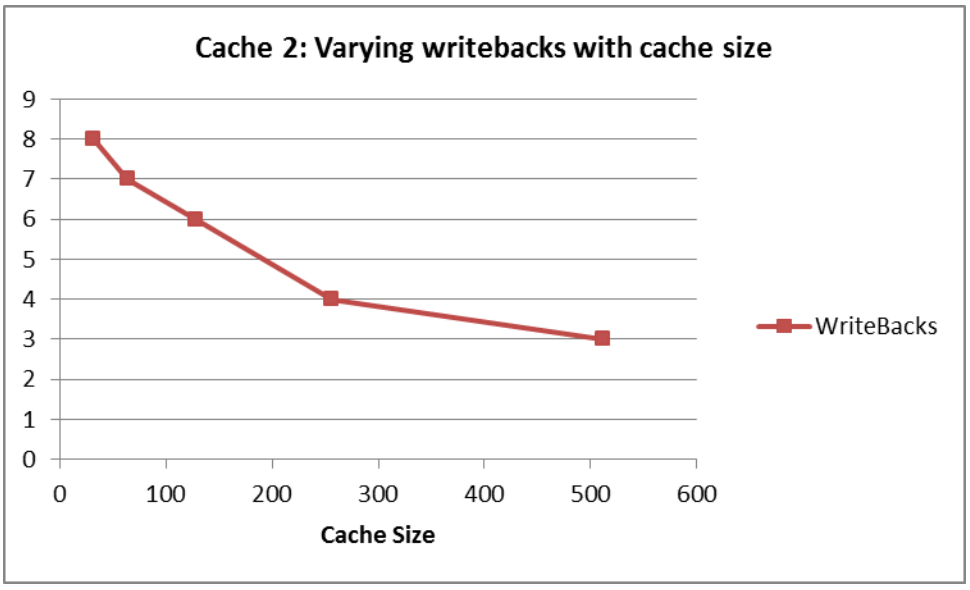
Cache size	32	64	128	256	512
#reads	110830	110830	110830	110830	110830
#read_misses	6452	6012	5750	5646	5610
#writes	11710	11710	11710	11710	11710
#write_misses	2	2	2	2	2
Miss_rate	0.051572	0.049078	0.04694	0.046091	0.045797
#dirty_WB	8	7	6	4	3
#mem_trans	3452	3475	3531	3512	3503
#cache_to_cache_trans	4892	4527	4322	4235	4207

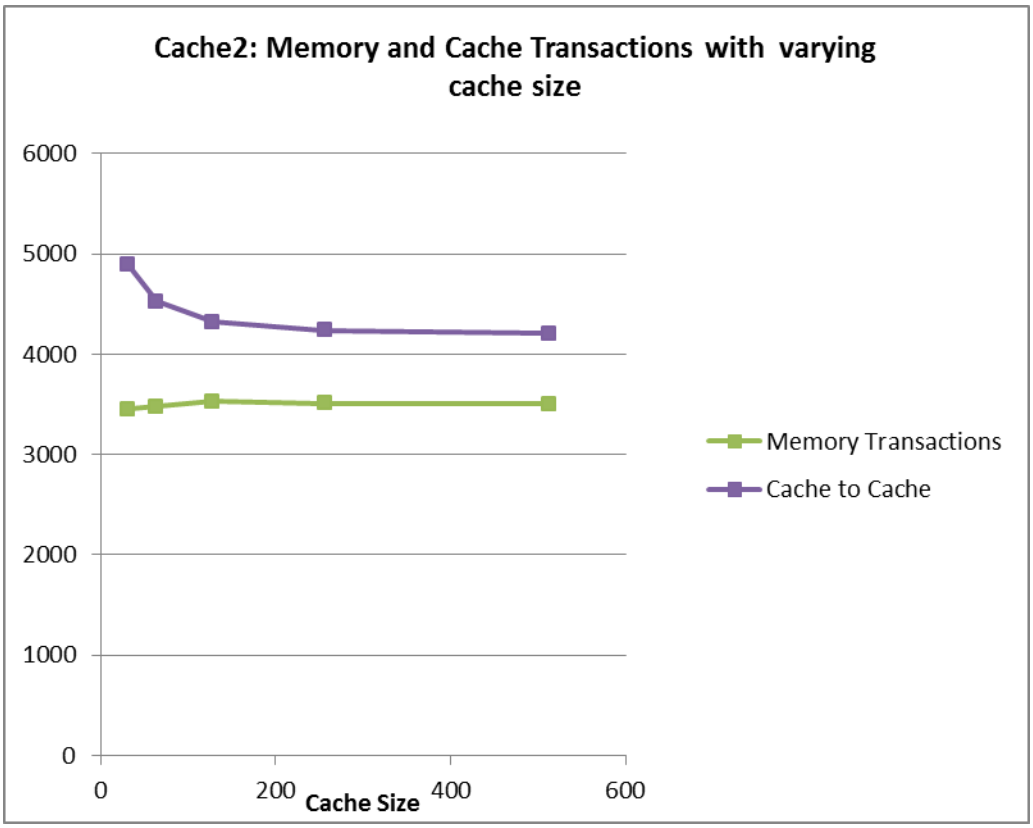
Discussion: We observe the following from the graphs for Cache 2 on varying the cache sizes:

- The miss rate decreases with the increase in cache size. This is because the capacity misses will reduce as the size of the cache increases.
- The number of writebacks decreases as the capacity increases, less blocks have to be evicted from the cache.
- As the number of misses decreases, the cache to cache transfers will reduce as shown in the graph. This is because the number of blocks requested from other caches would reduce.

- As the cache size increases, the number of misses decreases and thus the number of write-throughs to the memory increases. Hence, increasing the number of memory transactions.







For Cache #3:

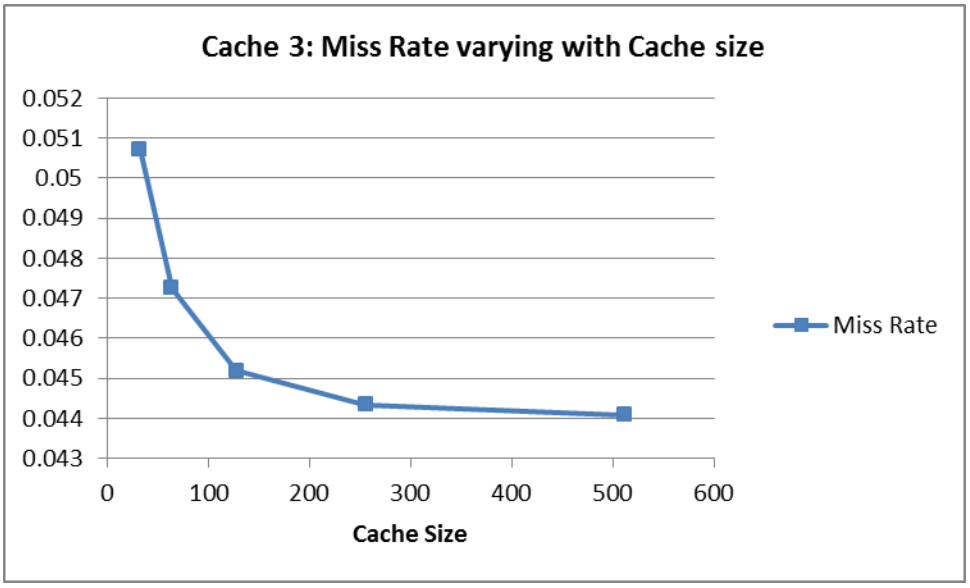
The following readings were recorded:

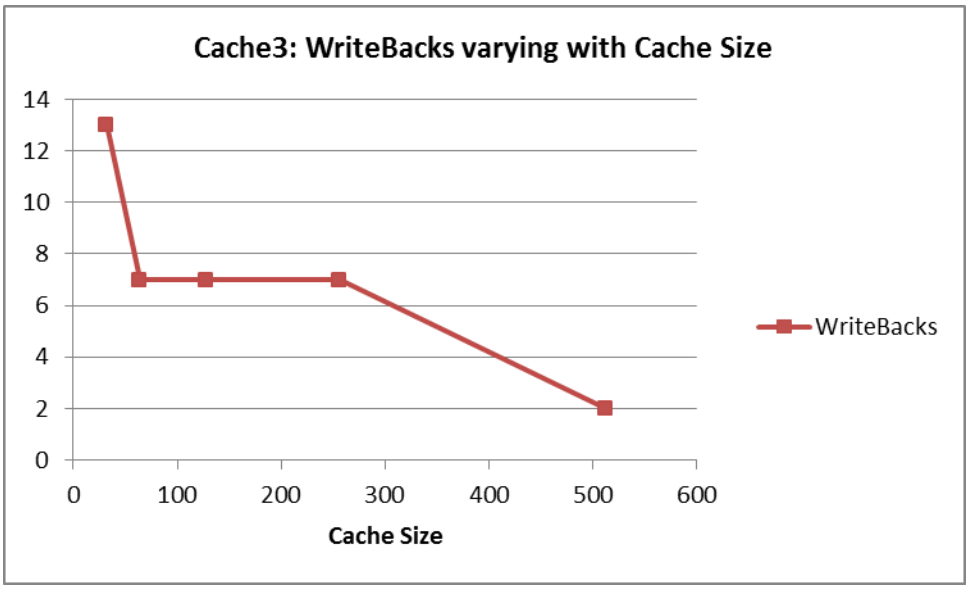
Cache size	**32**	**64**	**128**	**256**	**512**
#reads	114938	114938	114938	114938	114938
#read_misses	6456	6014	5751	5644	5610
#writes	12383	12383	12383	12383	12383
#write_misses	2	2	2	2	2
Miss_rate	0.050722	0.047251	0.045185	0.044345	0.044078
#dirty_WB	13	7	7	7	2
#mem_trans	3484	3631	3709	3685	3671
#$_to_$_trans	4873	4520	4314	4231	4206

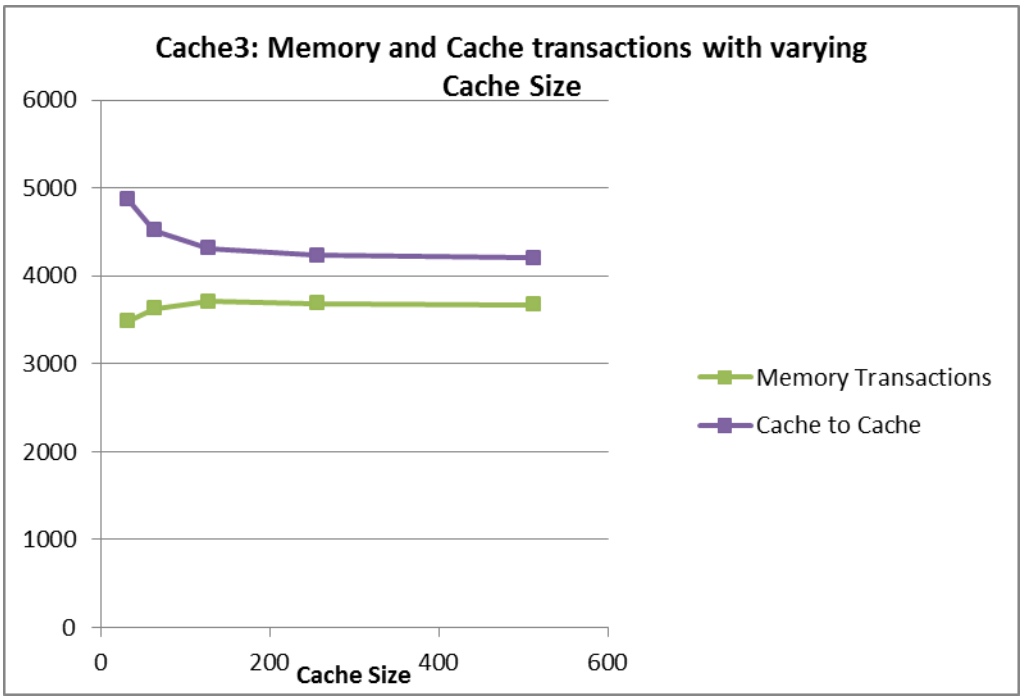
Discussion: We observe the following from the graphs for Cache 3 on varying the cache sizes:

- The miss rate decreases with the increase in cache size. This is because the capacity misses will reduce as the size of the cache increases.
- The number of writebacks decreases as the capacity increases, less blocks have to be evicted from the cache.

- As the number of misses decreases, the cache to cache transfers will reduce as shown in the graph. This is because the number of blocks requested from other caches would reduce.
- As the cache size increases, the number of misses decreases and thus the number of write-throughs to the memory increases. Hence, increasing the number of memory transactions.







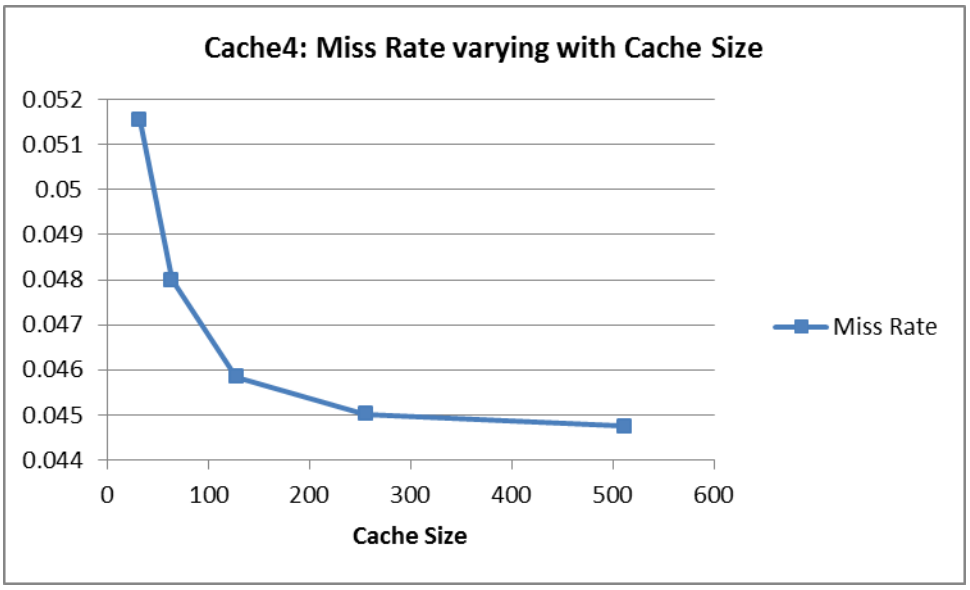
For Cache #4:

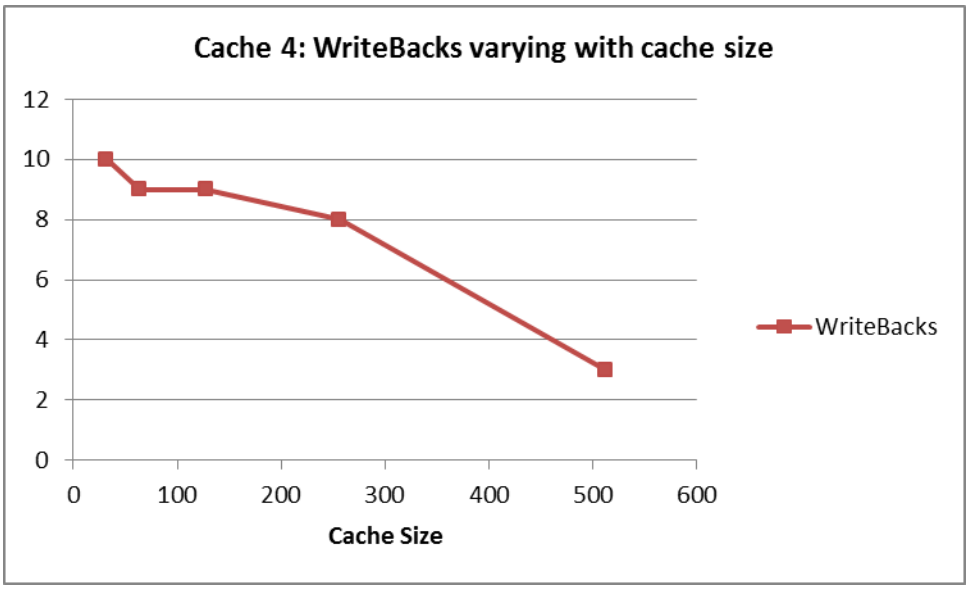
The following readings were recorded:

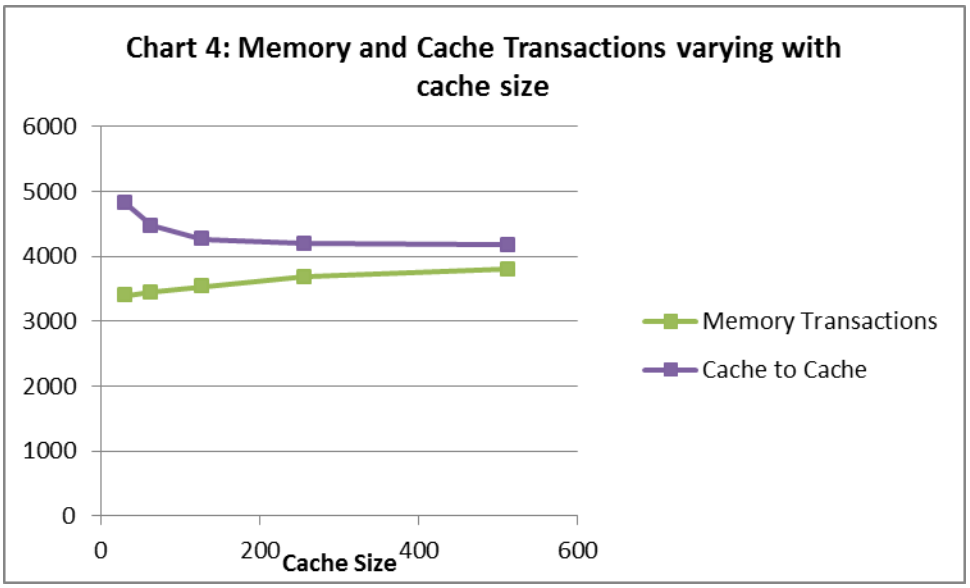
Cache size	**32**	**64**	**128**	**256**	**512**
#reads	113428	113428	113428	113428	113428
#read_misses	6468	6025	5756	5652	5617
#writes	12108	12108	12108	12108	12108
#write_misses	1	1	1	1	1
Miss_rate	0.051531	0.047994	0.045851	0.045023	0.044744
#dirty_WB	10	9	9	8	3
#mem_trans	3400	3445	3531	3681	3800
#$_to_$_trans	4822	4477	4266	4200	4177

Discussion: We observe the following from the graphs for Cache 4 on varying the cache sizes:

- The miss rate decreases with the increase in cache size. This is because the capacity misses will reduce as the size of the cache increases.
- The number of writebacks decreases as the capacity increases, less blocks have to be evicted from the cache.
- As the number of misses decreases, the cache to cache transfers will reduce as shown in the graph. This is because the number of blocks requested from other caches would reduce.
- As the cache size increases, the number of misses decreases and thus the number of write-throughs to the memory increases. Hence, increasing the number of memory transactions.


Cache4: Miss Rate varying with Cache Size
0.052
0.051
0.05
0.049
0.048
0.047
0.046
0.045
0.044
0
100
200
300
400
500
600
Cache Size
Miss Rate


Cache 4: WriteBacks varying with cache size
12
10
8
6
4
2
0
0
100
200
300
400
500
600
Cache Size
WriteBacks



Experiment #2 on Firefly protocol

Varying the block size keeping the cache size constant(1MB) & associativity constant(8)

Results:

For Cache 1:

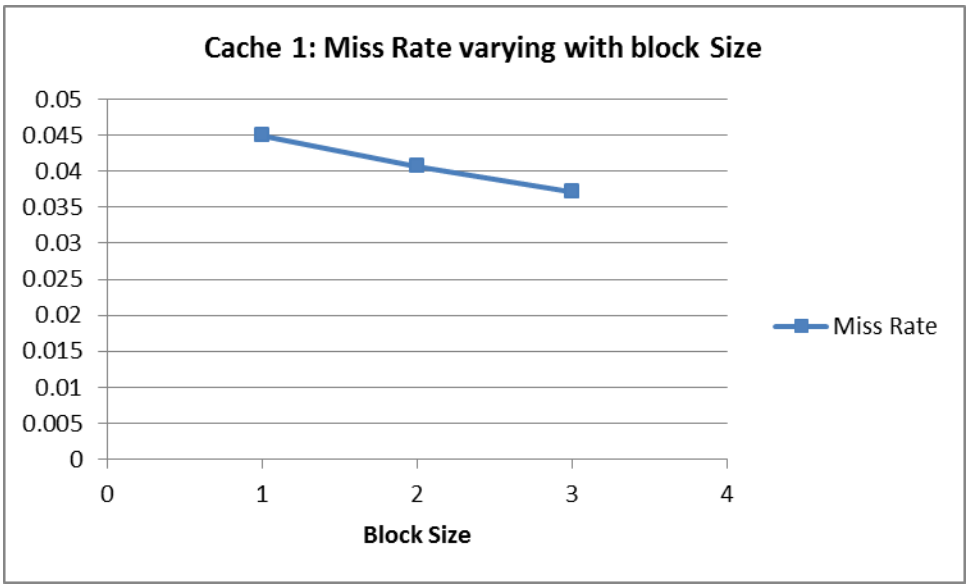
The readings are as follows:

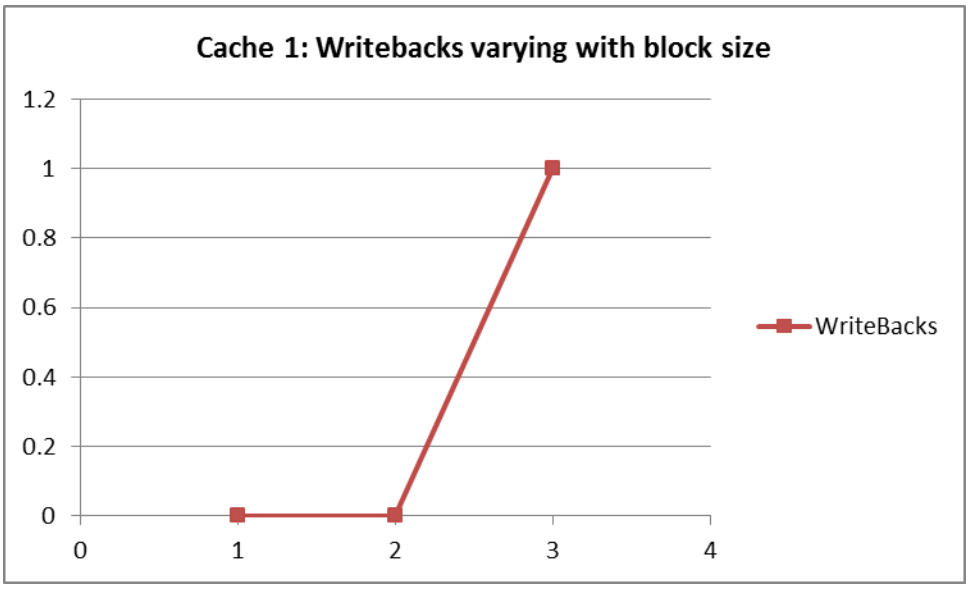
BlockSize	64	128	256
#reads	112665	112661	112661
#read_misses	5595	5069	4628
#writes	11942	11942	11942
#write_misses	3	3	3
Miss_rate	0.044927	0.040705	0.037166
#dirty_WB	0	0	1
#mem_trans	3316	5467	6085
#cache_to_cache_trans	4192	3810	3500

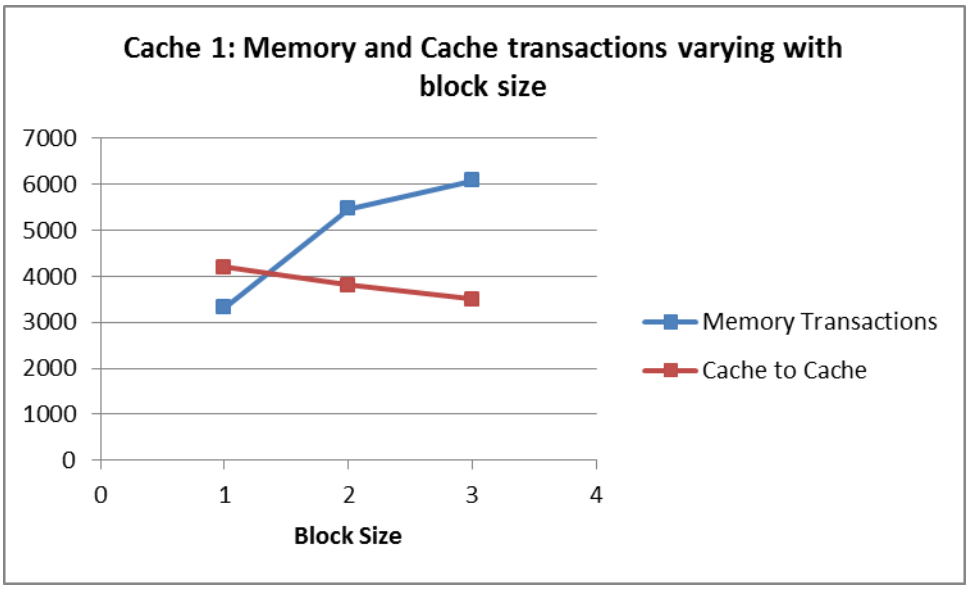
Discussion: We observe the following from the graphs for Cache 1 on varying the block sizes:

- The miss rate decreases with the increase in block size. This is because the spatial locality of the cache increases as the block size increases.

- The number of writebacks increases as the blocksize increases, as the entire block gets invalidated when one word gets invalidated. Thus the number of writebacks increases.
- As the number of misses decreases, the cache to cache transfers will reduce as shown in the graph since the data will not have to be fetched from other caches.
- As the block size increases, the number of misses decreases, but at the same time the write-throughs from the cache to the memory increases. Thus, increasing the number of memory transactions.







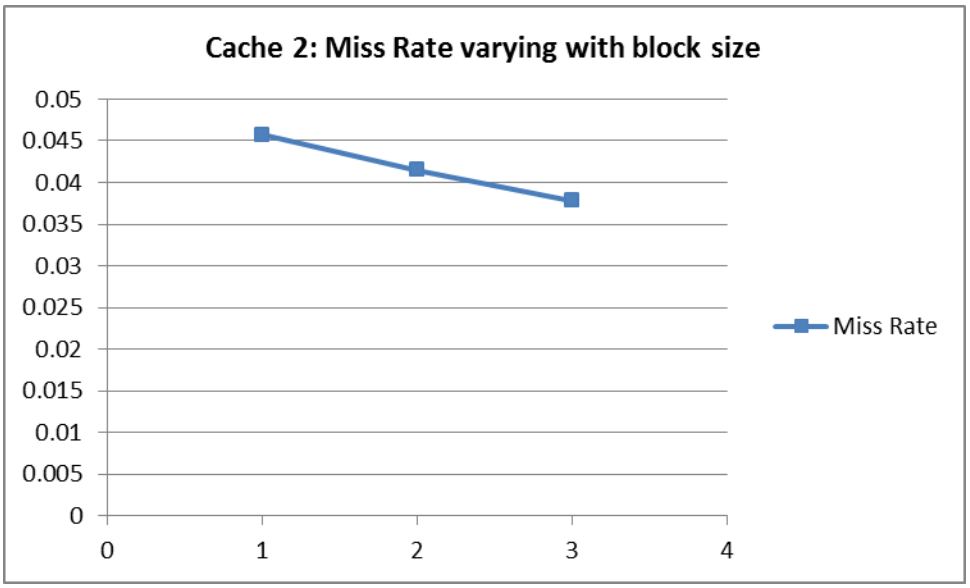
For Cache 2:

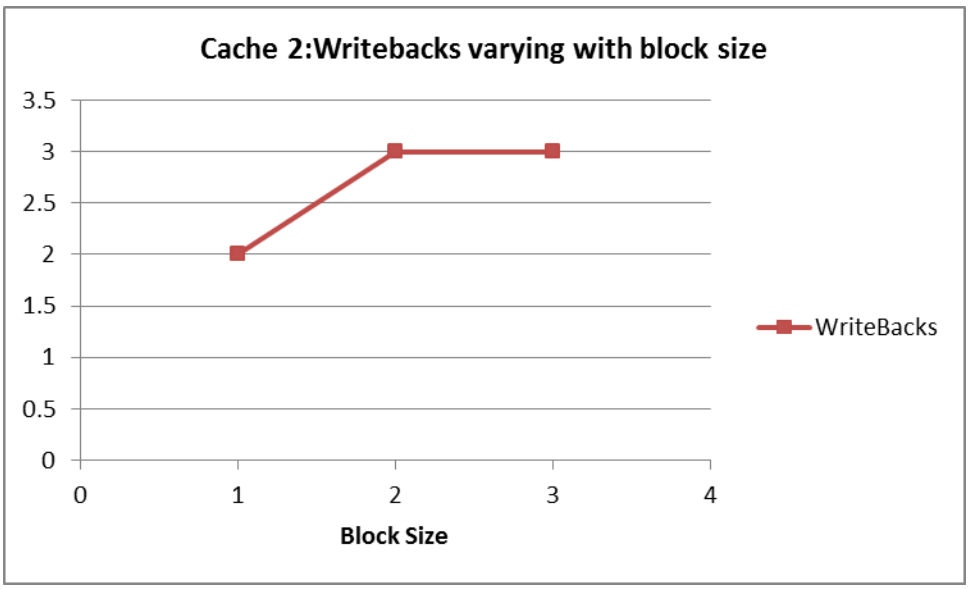
The readings are as follows:

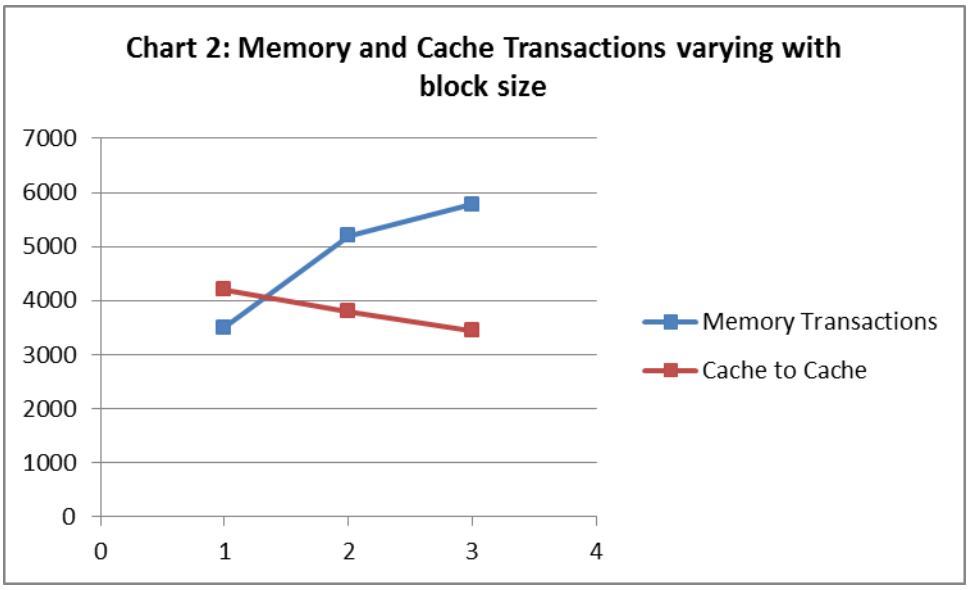
Block size	**64**	**128**	**256**
#reads	110830	110830	110830
#read_misses	5604	5080	4633
#writes	11710	11710	11710
#write_misses	2	1	1
Miss_rate	0.045748	0.041464	0.037816
#dirty_WB	2	3	3
#mem_trans	3501	5201	5777
#cache_to_cache_trans	4202	3800	3446

Discussion: We observe the following from the graphs for Cache 2 on varying the block sizes:

- The miss rate decreases with the increase in block size. This is because the spatial locality of the cache increases as the block size increases.
- The number of writebacks increases as the blocksize increases, as the entire block gets invalidated when one word gets invalidated. Thus the number of writebacks increases.
- As the number of misses decreases, the cache to cache transfers will reduce as shown in the graph since the data will not have to be fetched from other caches.
- As the block size increases, the number of misses decreases, but at the same time the write-throughs from the cache to the memory increases. Thus, increasing the number of memory transactions.


Cache 2: Miss Rate varying with block size
0.05
0.045
0.04
0.035
0.03
0.025
0.02
0.015
0.01
0.005
0
0
1
2
3
4
Miss Rate


Cache 2:Writebacks varying with block size
3.5
3
2.5
2
1.5
1
0.5
0
0
1
2
3
4
Block Size
WriteBacks



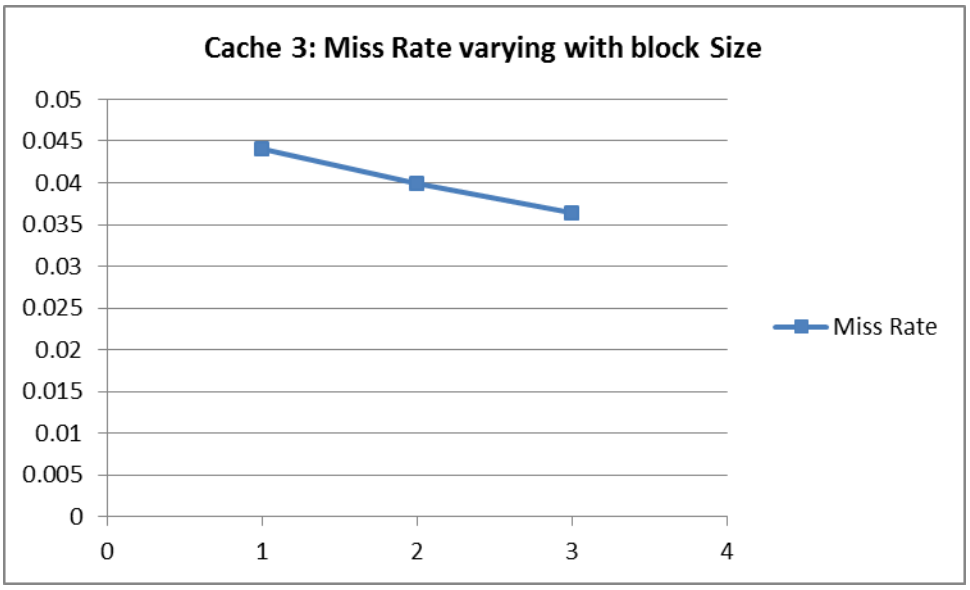
For Cache 3:

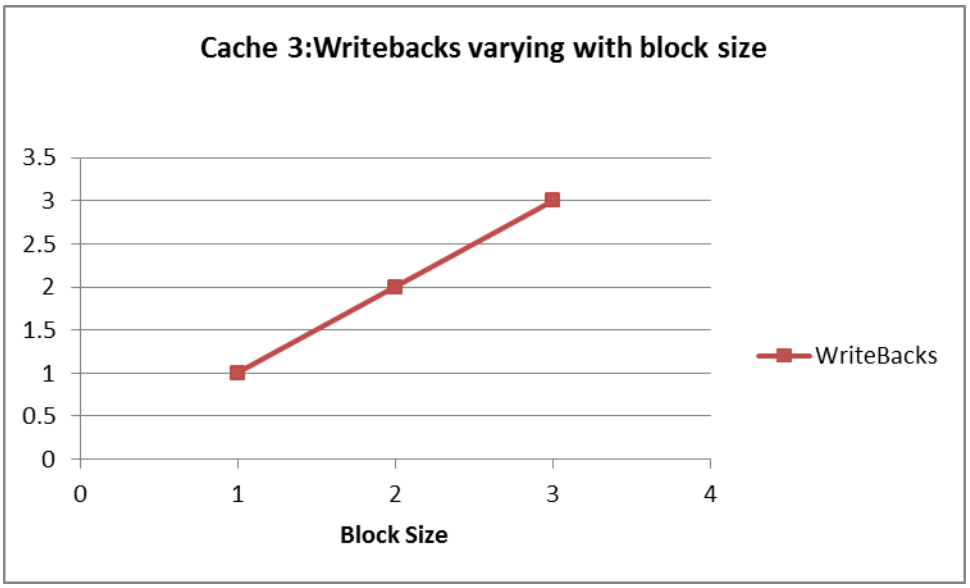
The readings are as follows:

Block size	**64**	**128**	**256**
#reads	114938	114938	114938
#read_misses	5604	5080	4630
#writes	12383	12383	12383
#write_misses	2	2	2
Miss_rate	0.04403	0.039915	0.03638
#dirty_WB	1	2	3
#mem_trans	3668	5340	6741
#$_to_$_trans	4202	3809	3476

Discussion: We observe the following from the graphs for Cache 3 on varying the block sizes:

- The miss rate decreases with the increase in block size. This is because the spatial locality of the cache increases as the block size increases.
- The number of writebacks increases as the blocksize increases, as the entire block gets invalidated when one word gets invalidated. Thus the number of writebacks increases.
- As the number of misses decreases, the cache to cache transfers will reduce as shown in the graph since the data will not have to be fetched from other caches.
- As the block size increases, the number of misses decreases, but at the same time the write-throughs from the cache to the memory increases. Thus, increasing the number of memory transactions.


Cache 3: Miss Rate varying with block Size
0.05
0.045
0.04
0.035
0.03
0.025
0.02
0.015
0.01
0.005
0
0
1
2
3
4
Miss Rate


Cache 3:Writebacks varying with block size
3.5
3
2.5
2
1.5
1
0.5
0
0
1
2
3
4
Block Size
WriteBacks

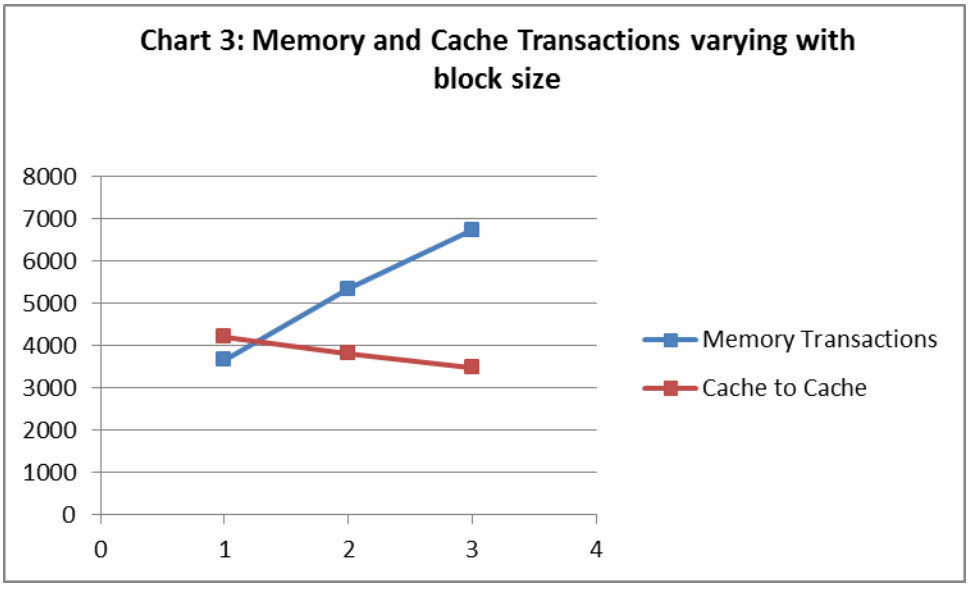


Chart 3: Memory and Cache Transactions varying with block size
8000
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
Memory Transactions
Cache to Cache

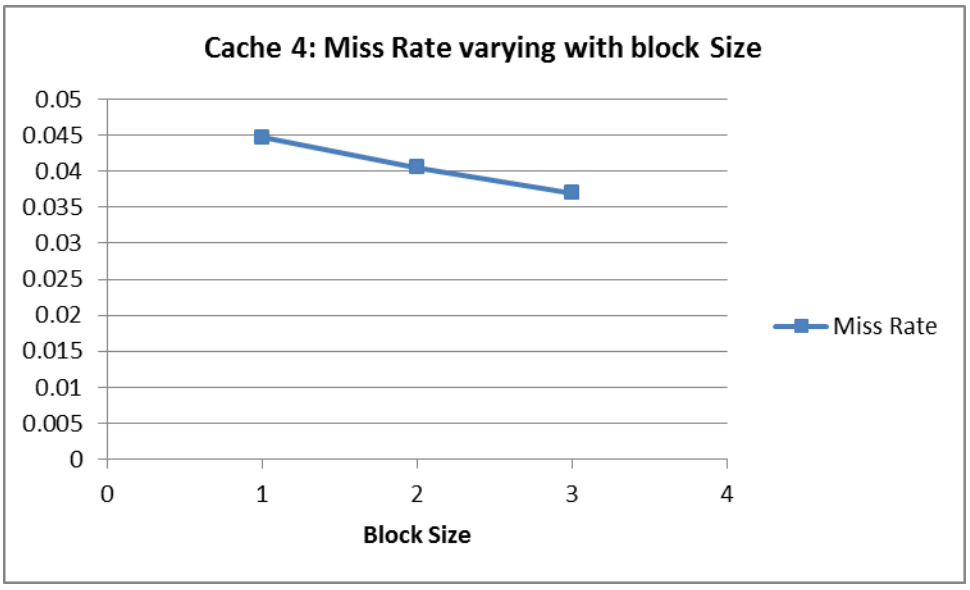
For Cache 4:

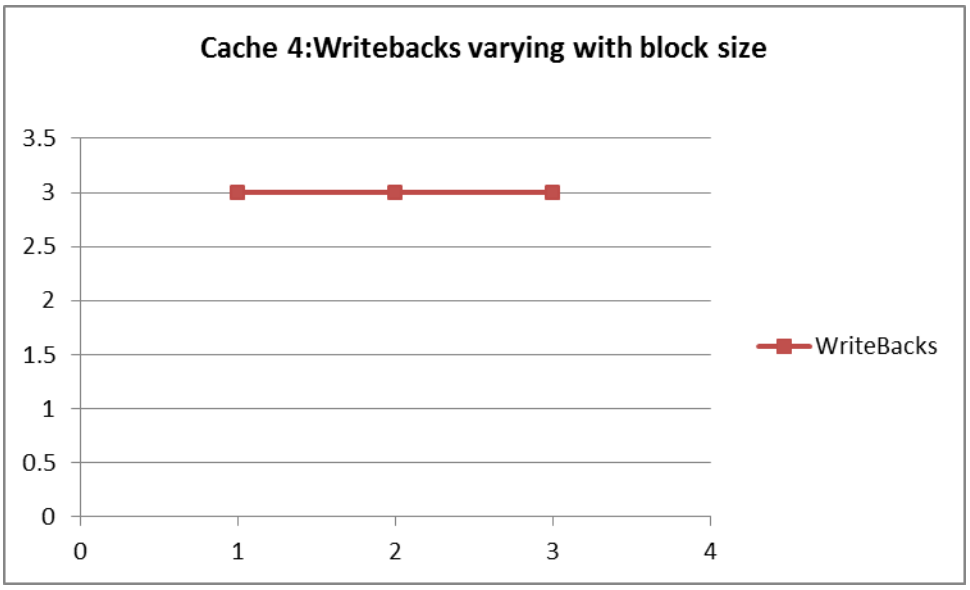
The readings are as follows:

Block size	64	128	256
#reads	113428	113428	113428
#read_misses	5611	5086	4640
#writes	12108	12108	12108
#write_misses	0	0	0
Miss_rate	0.044696	0.040514	0.036962
#dirty_WB	3	3	3
#mem_trans	3799	6631	6637
#cache_to_cache_trans	4172	3779	3447

Discussion: We observe the following from the graphs for Cache 1 on varying the block sizes:

- The miss rate decreases with the increase in block size. This is because the spatial locality of the cache increases as the block size increases.
- The number of writebacks increases as the blocksize increases, as the entire block gets invalidated when one word gets invalidated. Thus the number of writebacks increases.
- As the number of misses decreases, the cache to cache transfers will reduce as shown in the graph since the data will not have to be fetched from other caches.
- As the block size increases, the number of misses decreases, but at the same time the write-throughs from the cache to the memory increases. Thus, increasing the number of memory transactions.




Cache 4:Writebacks varying with block size
3.5
3
2.5
2
1.5
1
0.5
0
0
1
2
3
4
WriteBacks

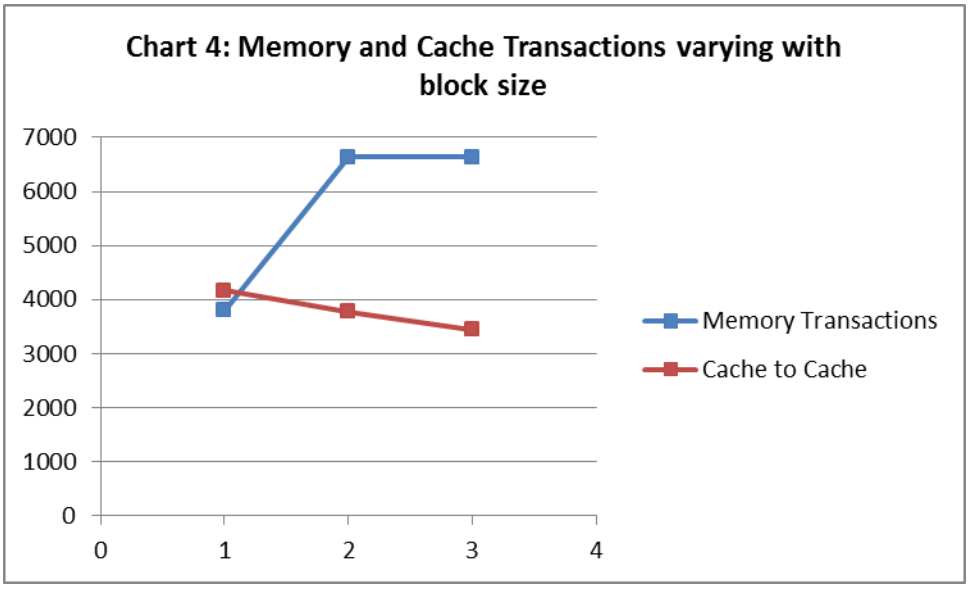


Chart 4: Memory and Cache Transactions varying with block size
7000
6000
5000
4000
3000
2000
1000
0
0
1
2
3
4
Memory Transactions
Cache to Cache

Discussion of Dragon and Firefly Coherence Protocols:

Firefly:

- Firefly is a partial write-through and write-update protocol.
- All updates are written to the memory instantly.
- The protocol never causes invalidation.
- The updates are sent to the other caches instantly.

Dragon:

- Dragon is a Write-Update and Write-Back protocol.
- Memory upgrades are done only when the blocks are being replaced.
- Writes to the shared block are not instantly sent to the memory , only to the other caches.

Due to the above characteristics of Dragon and Firefly protocol, the number of bus transactions and memory transactions in Firefly is much higher than that of Dragon. This causes the memory transactions of Firefly to increase with the cache size and blocksize as observed in the experiments.