Specification

This document specifies the specifications for the design of a 16 bit computer.

Requirement Definitions

The following requirements are imposed on the design of the computer:

Clock	Variable from 0-1000 Hz
Stack Memory	Seperate stack memory to prevent stack overflows.
Registers	8 registers including a Stack Pointer Register and a Program Counter, additionally one general purpose shift register and 5 general purpose registers. The flag register has flags for negative, zero, overflow and carry
ALU	Addition, subtraction, AND, OR, NOT, left shifting, sign extension of bytes, flag register
Instruction Register	The first 5 bits define the instruction.

Architecture

The basic architecture is a Von-Neumann architecture where the memory and the CPU are connected by one single system bus.

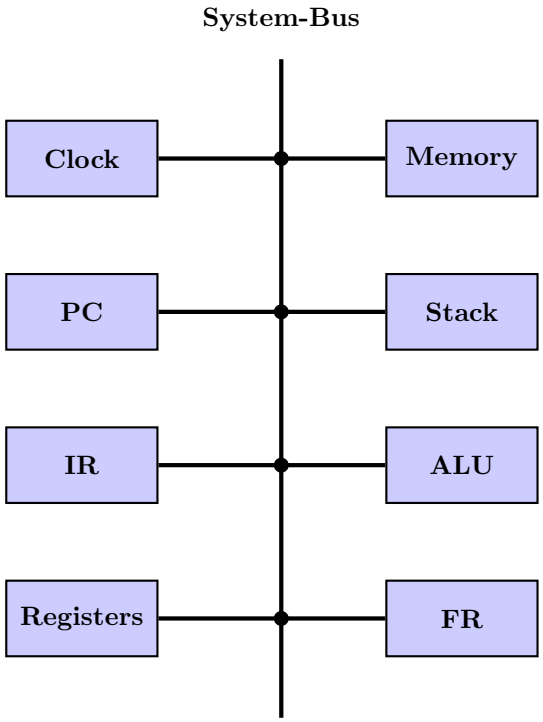


Figure 1: System architecture

Instruction Set

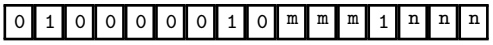
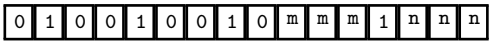
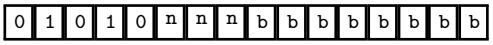
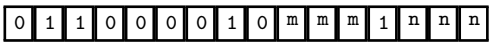
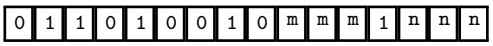
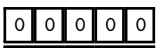
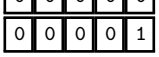
General Overview

The instruction set consists of 32 different instructions. The first 5 bit of the operation code are interpreted as the instruction. The instructions that have to implemented are the following:

Data transfer	1	LDW	Load a value of a memory address into a register
	2	LDB	Load the LSB of a memory address into a register
	3	MOVE	Move a value from one register to the next
	4	STRW	Store the value of a register in a memory adress
	5	STRB	Store the LSB of a register value in a memory address
Stack	6	PUSH	Push register value onto the stack
	7	POP	Pop value from the stack
ALU	8	ADD	Add the values of two registers
	9	SUB	Subtract the values of two registers
	10	AND	Bitwise AND of the values of two registers
	11	OR	Bitwise OR of the values of two registers
	12	NOT	Bitwise inversion of the value in one register
	13	LSHIFT	Shift the value in one register to the left by a variable amount
	14	RSHIFT	Shift the value in one register to the right by a variable amount
	15	SIXT	Sign extension of the LSB

The free adresses may be used for instructions that extend the functionality. For example, instructions that take immediate values. The operation codes have the following general layout:

Instruction Set Architecture

Operation Code	Mnemonic	Description
	LDW	Load the word that is stored at the address held by the register `Rmmm` into the register `Rnnn`.
	LDB	Load the least significant byte of the word at the address held by the register `Rmmm` into the register `Rnnn`.
	MOVE	Move the value `bbbb'bbbb` into the register `Rnnn`.
	STRW	Store the value of the register `Rmmm` at the address held by the register `Rnnn`.
	STRB	Store the least significant byte of the value in register `Rmmm` at the address held by the register `Rnnn`.
	PUSH	`TODO`
	POP	`TODO`

1 0 0 0 0 0 1 m m m n n n d d d	ADD	Add the values of the registers `Rmmm` and `Rnnn` and store the result in the register `Rddd`.
1 0 0 0 1 0 1 m m m n n n d d d	SUB	Subtract the value in the register `Rnnn` from the value in the register `Rmmm` and store the result in the register `Rddd`.
1 0 0 1 0 0 1 m m m n n n d d d	AND	Calculate a bitwise AND of the values in the registers `Rmmm` and `Rnnn`. Store the result in the register `Rddd`.
1 0 0 1 1 0 1 m m m n n n d d d	OR	Calculate a bitwise OR of the values in the registers `Rmmm` and `Rnnn`. Store the result in the register `Rddd`.
1 0 1 0 0 0 0 1 0 m m m 1 d d d	NOT	Bitwise inversion of the value in the register `Rmmm`. Store the result in the register `Rddd`.
1 0 1 0 1 0 0 1 0 m m m b b b b	LSHIFT	Shift the value in the register `Rmmm` by `bbbb` to the left.
1 0 1 1 0 0 0 1 0 m m m b b b b	RSHIFT	Shift the value in the register `Rmmm` by `bbbb` to the right.
1 0 1 1 1 0 0 0 0 0 0 0 1 n n n	SIXT	Signextend the least significant byte of the value that is stored in the register `Rnnn`.

CPU Overview

The CPU has the following subcomponents:

- Instruction Register (IR)
- Flag Register (FR)
- Carry-Look-Ahead-Adder (CLAA)
- etc.