

## Specification

This document specifies the specifications for the design of a 16 bit computer.

## Requirement Definitions

The following requirements are imposed on the design of the computer:

<b>Clock</b>	Variable from 0-1000 Hz
<b>Stack Memory</b>	Seperate stack memory to prevent stack overflows.
<b>Registers</b>	8 registers including a Stack Pointer Register and a Program Counter, additionally one general purpose shift register and 5 general purpose registers. The flag register has flags for negative, zero, overflow and carry
<b>ALU</b>	Addition, subtraction, AND, OR, NOT, left shifting, sign extension of bytes, flag register
<b>Instruction Register</b>	The first 5 bits define the instruction.

## Architecture

The basic architecture is a Von-Neumann architecture where the memory and the CPU are connected by one single system bus.

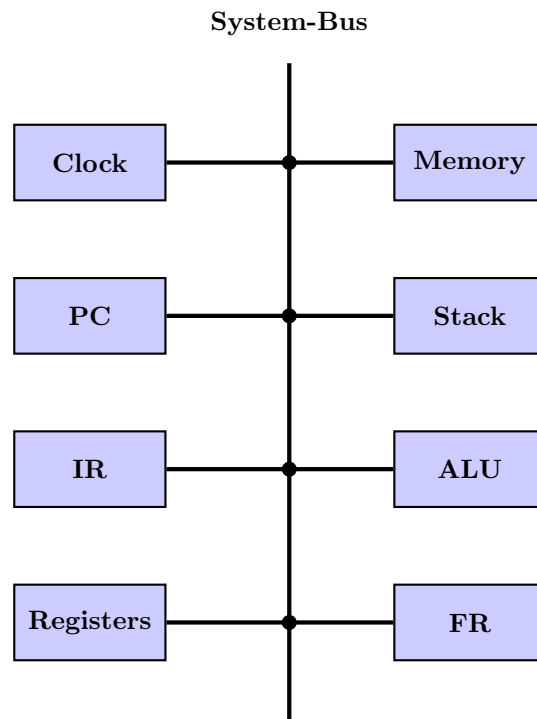


Figure 1: System architecture

## Instruction Set

### General Overview

The instruction set consists of 32 different instructions. The first 5 bit of the operation code are interpreted as the instruction. The instructions that have to implemented are the following:

<b>Data transfer</b>	1	LDW	Load a value of a memory address into a register
	2	LDB	Load the LSB of a memory address into a register
	3	MOV	Move a value from one register to another
	4	MOV	Move an immediate value in a register
	5	STW	Store the value of a register in a memory address
	6	STB	Store the LSB of a register value in a memory address
<b>Stack</b>	7	PSH	Push register values onto the stack
	8	POP	Pop values from the stack
<b>ALU</b>	9	ADD	Add the values of two registers
	10	ADD	Add an immediate value to a register
	11	SUB	Subtract the values of two registers
	12	SUB	Subtract an immediate value from a register
	13	MUL	Multiply the values of two registers
	14	AND	Bitwise AND of the values of two registers
	15	ORR	Bitwise OR of the values of two registers
	16	XOR	Bitwise XOR of the values of two registers
	17	NOT	Bitwise inversion of the value in one register
	18	LLS	Shift the value in a register left by a variable amount
	19	ALS	Shift the value in a register arithmetically left by a variable amount
	20	RLS	Rotate the value in a register left by a variable amount
	21	LRS	Shift the value in a register right by a variable amount
	22	ARS	Shift the value in a register arithmetically right by a variable amount
	23	RRS	Rotate the value in a register right by a variable amount
	24	SXT	Sign extension of the LSB
<b>Branching</b>	25	BRX	Branch to the address stored in a register
	26	BIF	Branch if a certain flag is set in the flag register

The operation codes have the following general layout:

### Instruction Set Architecture

Operation Code	Mnemonic	Description																
<table><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>m</td><td>m</td><td>m</td><td>1</td><td>n</td><td>n</td><td>n</td></tr></table>	0	1	0	0	0	0	0	1	0	m	m	m	1	n	n	n	LDW	Load the word that is stored at the address held by the register <b>Rmmm</b> into the register <b>Rnnn</b> .
0	1	0	0	0	0	0	1	0	m	m	m	1	n	n	n			
<table><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>m</td><td>m</td><td>m</td><td>1</td><td>n</td><td>n</td><td>n</td></tr></table>	0	1	0	0	1	0	0	1	0	m	m	m	1	n	n	n	LDB	Load the least significant byte of the word at the address held by the register <b>Rmmm</b> into the register <b>Rnnn</b> .
0	1	0	0	1	0	0	1	0	m	m	m	1	n	n	n			
<table><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>n</td><td>n</td><td>n</td><td>b</td><td>b</td><td>b</td><td>b</td><td>b</td><td>b</td><td>b</td><td>b</td></tr></table>	0	1	0	1	0	n	n	n	b	b	b	b	b	b	b	b	MOVE	Move the value <b>bbbb'bbbb</b> into the register <b>Rnnn</b> .
0	1	0	1	0	n	n	n	b	b	b	b	b	b	b	b			

<div>011000010mm1nnn</div>	STRW	Store the value of the register <b>Rmmm</b> at the address held by the register <b>Rnnn</b> .
<div>011010010mm1nnn</div>	STRB	Store the least significant byte of the value in register <b>Rmmm</b> at the address held by the register <b>Rnnn</b> .
<div>000000psxxxxxx</div>	PUSH	Push the declared registers <b>x</b> , the stack pointer <b>s</b> or the program counter <b>p</b> on the stack
<div>000010psxxxxxx</div>	POP	Pop values from the stack in the declared registers <b>x</b> , the stack pointer <b>s</b> or the program counter <b>p</b> .
<div>1000001mmnnddd</div>	ADD	Add the values of the registers <b>Rmmm</b> and <b>Rnnn</b> and store the result in the register <b>Rddd</b> .
<div>1000101mmnnddd</div>	SUB	Subtract the value in the register <b>Rnnn</b> from the value in the register <b>Rmmm</b> and store the result in the register <b>Rddd</b> .
<div>1001001mmnnddd</div>	AND	Calculate a bitwise AND of the values in the registers <b>Rmmm</b> and <b>Rnnn</b> . Store the result in the register <b>Rddd</b> .
<div>1001101mmnnddd</div>	OR	Calculate a bitwise OR of the values in the registers <b>Rmmm</b> and <b>Rnnn</b> . Store the result in the register <b>Rddd</b> .
<div>101000010mm1ddd</div>	NOT	Bitwise inversion of the value in the register <b>Rmmm</b> . Store the result in the register <b>Rddd</b> .
<div>101010010mmbbb</div>	LSHIFT	Shift the value in the register <b>Rmmm</b> by <b>bbbb</b> to the left.
<div>101100010mmbbb</div>	RSHIFT	Shift the value in the register <b>Rmmm</b> by <b>bbbb</b> to the right.
<div>1011100000001nnn</div>	SIXT	Signextend the least significant byte of the value that is stored in the register <b>Rnnn</b> .

## ALU

The ALU consists of the following components:

- carry lookahead adder (CLAA)
- barrel shifter
- wallace tree multiplier
- logic unit
- flag register

