

UVM Framework Users Guide

Revision 3.6c_0

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1 Introduction to the UVM Framework (UVMF)

1.1 Motivation for using UVMF

1.1.1 UVM Jumpstart

The steep learning curve of UVM often prevents product teams from realizing the productivity and quality benefits of using advanced verification methodology. The UVM Framework (UVMF) provides a jump-start for learning UVM and building UVM verification environments. It defines an architecture and reuse methodology upon UVM, enabling teams new to UVM to be productive from the beginning while coming up the UVM learning curve. The python scripts provided automate the creation of the files, infrastructure and interconnect for interface packages, environment packages and project benches. Once generated, developers can promptly focus on adding functionality specific to the design and interfaces used.

1.1.2 Reuse Methodology

The UVM Framework is a model reuse methodology that verification teams can leverage. It supports component level verification reuse across projects and environment reuse from block through chip to system level simulation. The UVM Framework is an established verification reuse methodology that is in use at many companies in multiple industries across North America and Europe.

1.1.3 Single Architecture for Simulation and Emulation

The UVM Framework provides an architecture that supports pure simulation and accelerated simulation using emulation. This enables the creation of a single unified environment that supports block, chip and system level tests, and with the choice of running on a pure simulation platform (e.g. Questa) or a hardware-assisted acceleration platform using emulation (e.g. Veloce).

1.2 Major Divisions of Functionality Within UVMF

1.2.1 UVMF Base Package

The UVMF base package, `uvmf_base_pkg`, is a library of base classes that implement core functionality of components found in all simulation benches. This includes base classes for transactions, sequences, drivers, monitors, predictors, scoreboards, environments and tests. All classes in the UVMF base package are derived from UVM classes. User extensions then provide variables, tasks and functions specific to the design under test.

The UVMF base package and the package structure used within UVMF define a UVM reuse methodology. This methodology supports horizontal reuse, i.e. reuse of components

across projects, as well as vertical reuse, i.e. environment reuse from block to chip to system.

1.2.2 Interface Packages

UVMF interface packages and their associated BFM^s provide all of the functionality required to monitor and optionally drive a design interface. Interface packages and BFM^s are reusable across projects. An interface package is composed of three pieces: a signal bundle interface, BFM interfaces and the package declaration. The signal bundle contains all signals used in the protocol. The BFMs implement the protocol signaling to drive and monitor transactions at the pin level. The package declaration includes all class definitions and type definitions used by the interface agent.

1.2.3 Environment Packages

The environment package is a key aspect that enables vertical reuse of environments within the UVMF. The environment package contains the environment class definition, its configuration class definition and any environment level sequences that could be used in higher level simulations. Block level environments contain agents, predictors, scoreboards, coverage collectors and other components. All other levels of environment include other environments. Environments are structured hierarchically similar to the way RTL is composed hierarchically.

1.2.4 Verification IP

The verification_ip folder contains all packages that are reused across projects and from block to top. This folder contains environment packages, interface packages, utility packages, etc.

1.2.5 Project Benches

The simulation bench is composed of top level elements that are not generally intended to be reusable horizontally nor vertically. It defines test level parameters, the top level modules, top level sequence and top level UVM test. It also includes derived sequences and tests used to implement additional test scenarios.

1.2.6 Example Groups

UVMF examples are divided into groups. The groups include base_examples, vip_examples and vista_examples. The base examples are the core examples and run in simulation and emulation. The vip examples contain a Questa VIP and emulatable VIP example for AXI4. A Questa VIP license and software installation is required in addition to a Questa license to run the QVIP example. A Veloce software license and software installation is required in addition to a Questa license to run the VIP example. The Vista example requires a Vista license and software installation in addition to a Questa license to run.

Each example group contains a verification_ip and project_benches folder. The verification_ip folder contains all reusable packages used and shared among benches in the project_benches folder. The benches can also use packages found in the verification_ip folder in the base_examples group.

1.3 UVMF Base Class Package Overview

1.3.1 Overview

The `uvmf_base_pkg`, located under the `verification_ip` directory, provides a library of classes that implements the methodology used by the UVMF. In order to support emulation UVMF is divided into two packages: `uvmf_base_pkg` and `uvmf_base_pkg_hdl`. The latter only contains the synthesizable typedefs and parameters required by the emulated portion of a test bench. The former includes all class definitions and other non-synthesizable typedefs. The `uvmf_base_pkg_hdl` package is imported by `uvmf_base_pkg`. Each class within `uvmf_base_pkg` is described below.

1.3.2 Stimulus Classes

1.3.2.1 `uvmf_transaction_base.svh`

This is the base class for all sequence items, i.e. transactions, within UVMF. It provides a unique transaction ID variable and associated functions useful for debug. It also provides variables used for transaction viewing and a unique key for storing the transaction in associative arrays.

1.3.2.2 `uvmf_sequence_base.svh`

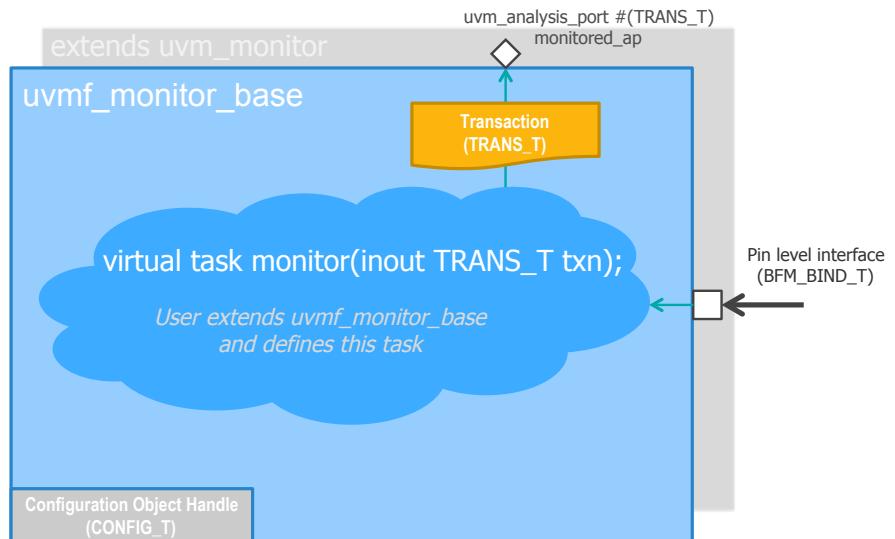
This is the base class for all sequences within UVMF. It extends `uvm_sequence` but provides no additional functionality. It provides a location where functionality common to all UVMF sequences can be added.

1.3.3 Agent Classes

1.3.3.1 `uvmf_monitor_base.svh`

This is the base class for all UVMF monitors. Only monitors extended from `uvmf_monitor_base` should be used as specialization of the `MONITOR_T` parameter of the `uvmf_parameterized_agent` base class. When extending the `uvmf_monitor_base`, only the monitor task must be defined. The monitor task either observes and captures bus activity directly or calls a task in the monitor BFM which captures bus activity. It is recommended that signal level bus monitoring be done in the monitor BFM for optimal run-time performance, especially with emulation.

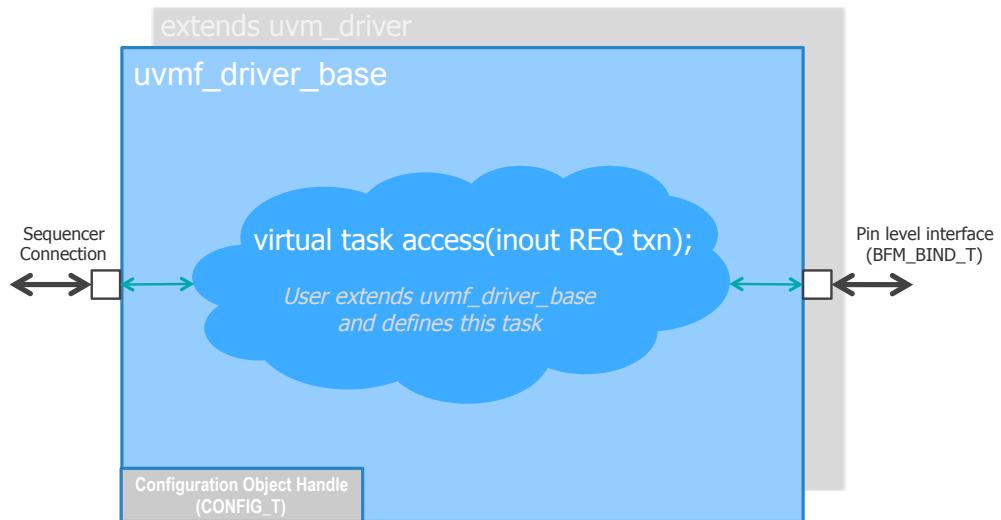
UVMF Monitor Base



1.3.3.2 *uvmf_driver_base.svh*

This is the base class for all UVMF drivers. Only drivers extended from `uvmf_driver_base` should be used as specialization of the `DRIVER_T` parameter of the `uvmf_parameterized_agent` base class. When extending `uvmf_driver_base`, only the access task must be defined. The access task either drives bus activity directly or calls a task in the driver BFM which drives activity. It is recommended that signal level bus driving be done in the driver BFM for optimal run-time performance, especially with emulation.

UVMF Driver Base



1.3.3.3 `uvmf_parameterized_agent_configuration_base.svh`

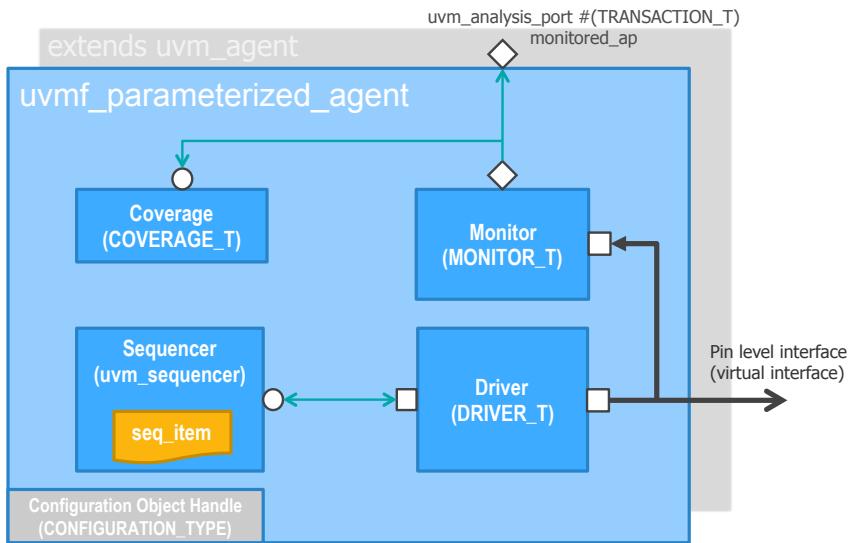
This is the base class for all interface agent configurations. Only configurations extended from `uvmf_parameterized_agent_configuration_base` should be used as specialization of the `CONFIG_T` parameter of the `uvmf_parameterized_agent` base class. Variables common to all agents and specific to the `uvmf_parameterized_agent` are in the `uvmf_parameterized_agent_configuration_base`. Add protocol specific configuration variables to an extension of `uvmf_parameterized_agent_configuration_class`.

1.3.3.4 `uvmf_parameterized_agent.svh`

This class implements an interface agent. This agent can be used with any protocol. The protocol specific features reside in the configuration, driver, monitor, coverage and transaction types used as parameters to this class. If the agent is active then it automatically places its sequencer within the `uvm_config_db` for retrieval by the top level sequence.

Prior to constructing a monitor, the parameterized agent checks the `uvm_config_db` for a monitor of the required type. If one is returned then it is used instead of constructing a local monitor. This is to support construction of a shared monitor in an upper level environment. The shared monitor is created in an upper level environment where lower level environments monitor common interfaces.

UVMF Parameterized Agent

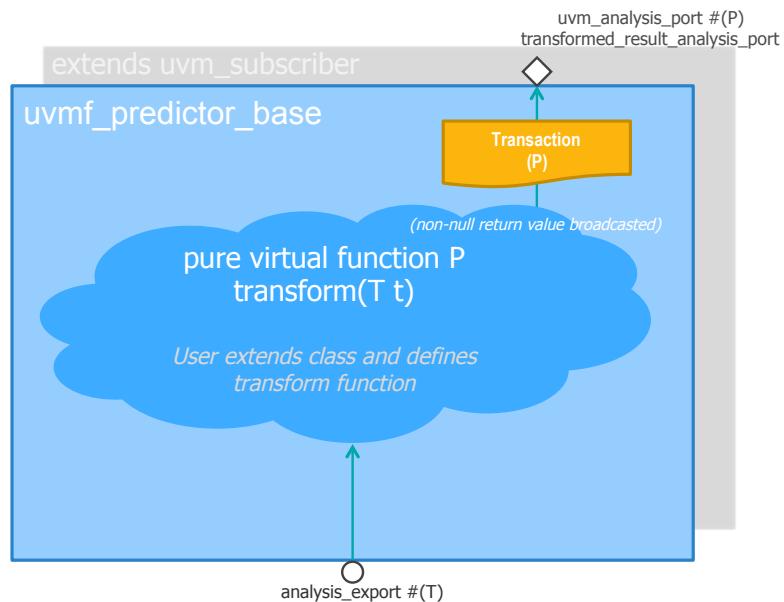


1.3.4 Predictor Classes

1.3.4.1 `uvmf_predictor_base.svh`

This is the base class for a predictor with a single input port and output port. The predictor base is a `uvm_subscriber` with a UVM analysis_port. The predictor base is a virtual class and defines a pure virtual function named `transform`. When extending the predictor base only the `transform` function needs to be provided to implement the golden model of the design. The model may be written in SystemVerilog or as an external C/C++ model accessed through DPI-C calls.

UVMF Predictor Base



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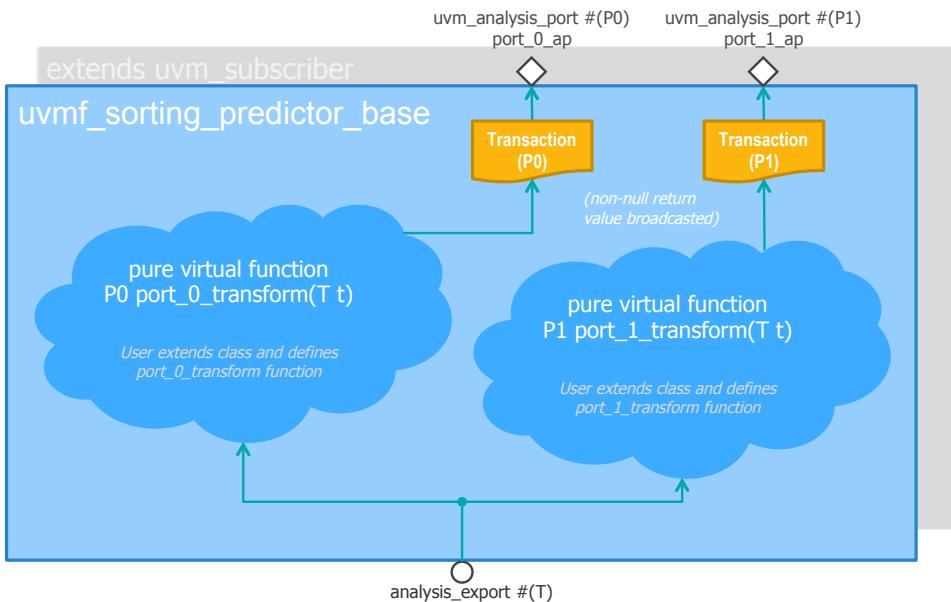
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1.3.4.2 `uvmf_sorting_predictor_base.svh`

This class operates in a manner similar to the predictor base. The sorting predictor has two UVM analysis ports and two transform functions. Each transform function is associated with one of the analysis ports. The sorting predictor base creates two output transaction streams from the single input transaction stream. The input transaction is applied to both transform functions. The output of each transform function determines if a transaction is sent to an analysis port. As a result, an incoming transaction may result in an output transaction on neither, either or both analysis ports.

UVMF Sorting Predictor Base



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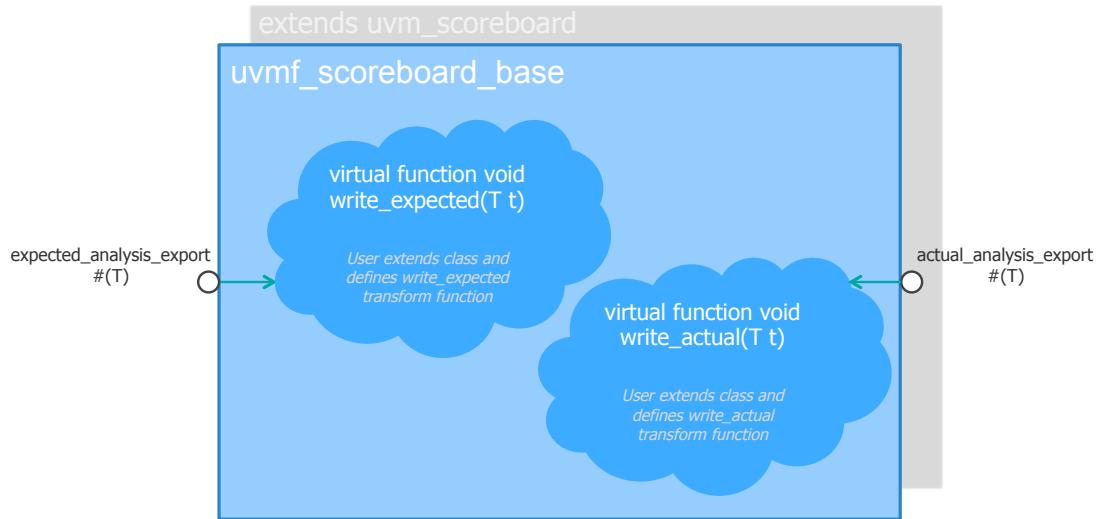


1.3.5 Scoreboard Classes

1.3.5.1 `uvmf_scoreboard_base.svh`

This is the base class for all scoreboards within the UVM Framework. It provides the two analysis exports for receiving transactions, `expected_export` and `actual_export`. It also provides basic end of test use checks and reporting.

UVMF Scoreboard Base



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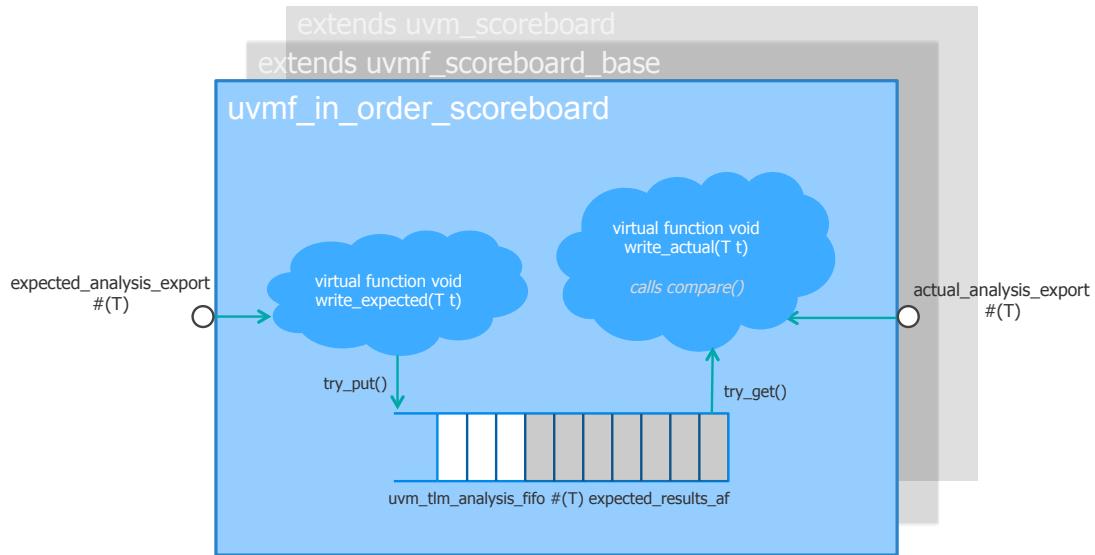


1.3.5.2 `uvmf_in_order_scoreboard.svh`

This scoreboard is used in circumstances where the data order through the DUT is preserved.

The in order scoreboard extends the scoreboard base. It adds an analysis FIFO for storing expected results. Transactions received through the `expected_export` are placed into the analysis FIFO. Transactions observed on the DUT output are sent to the actual export for comparison. The arrival of a transaction on the actual export causes the next transaction to be removed from the analysis FIFO and compared to the actual transaction. An error is generated if the FIFO is empty.

UVMF In-Order Scoreboard



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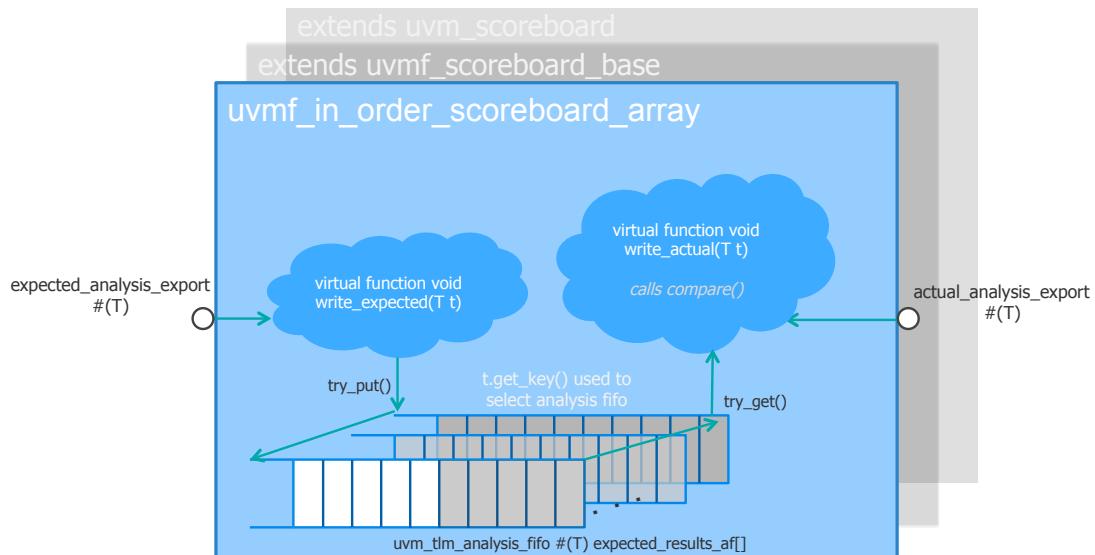


1.3.5.3 `uvmf_in_order_scoreboard_array.svh`

This scoreboard is used in circumstances where data through a physical channel is divided into multiple logical channels and data order within a logical channel is in order.

The in order scoreboard array implements an analysis FIFO for each logical channel. The behavior for each channel is identical to the in order scoreboard. The logical channel for each incoming transaction is identified using the `get_key` function of the transaction.

UVMF In-Order Scoreboard Array



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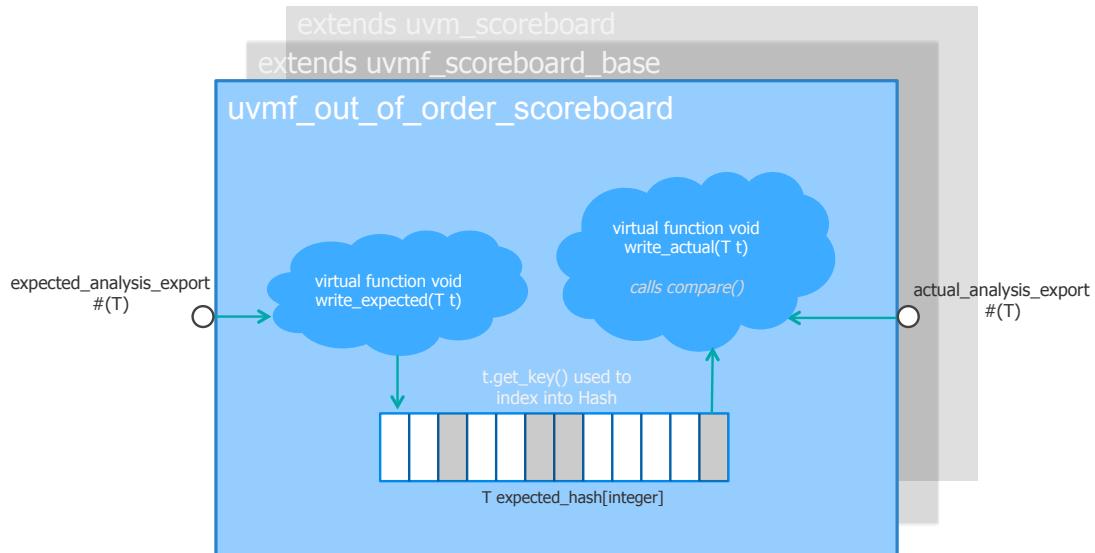
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1.3.5.4 `uvmf_out_of_order_scoreboard.svh`

The out of order scoreboard is used in circumstances where data order through the DUT is not guaranteed or not predictable.

The out of order scoreboard extends the scoreboard base. It adds a SystemVerilog associative array for storing expected results. Transactions received through the `expected_export` are placed into the associative array using the value returned from the `get_key` function as the key of the entry. Transactions observed on the DUT output are sent to the actual export for comparison. The arrival of a transaction on the actual export causes a transaction to be removed from the associative array and compared to the actual transaction. The `get_key` function of the actual transaction is used to identify a matching transaction in the associative array. An error is generated if the associative array does not have an entry that matches the key returned from the actual transactions `get_key` function.

UVMF Out-of-Order Scoreboard



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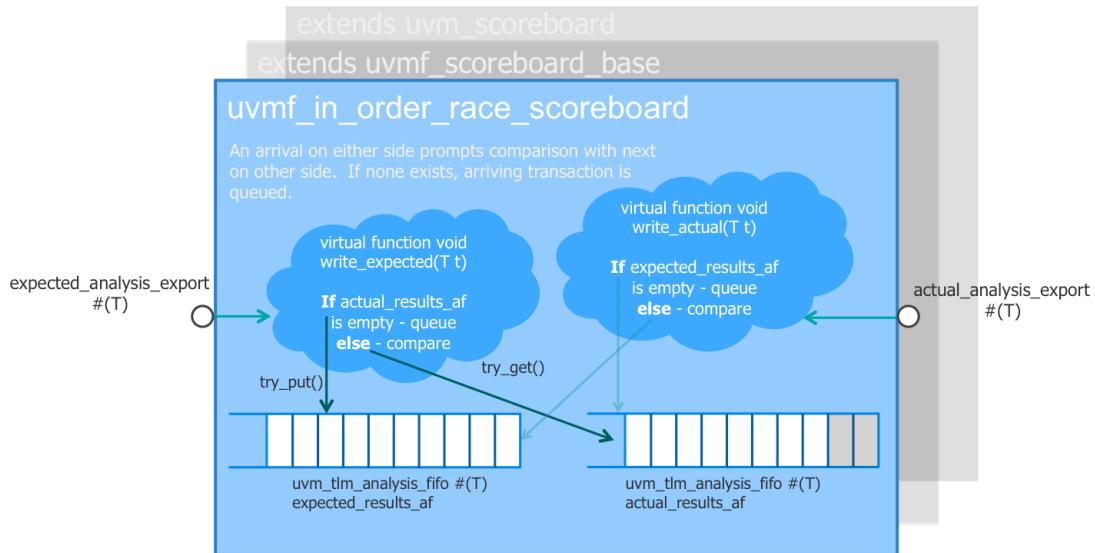


1.3.5.5 `uvmf_in_order_race_scoreboard.svh`

The in order race scoreboard is used in circumstances where data order through the DUT is preserved and the DUT can send output transactions before input transactions are received.

The in order race scoreboard extends the scoreboard base. It adds an analysis FIFO for the expected_export and actual_export. When a transaction arrives on either port the other port is checked for an entry to compare against. If an entry exists in the FIFO for the other port then the entry is pulled from the FIFO for comparison. If an entry does not exist in the FIFO for the other port then the entry is queued for later comparison.

UVMF In-Order Race Scoreboard



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1.3.6 Environment Classes

1.3.6.1 `uvmf_environment_configuration_base.svh`

This is the base class for environment (as opposed to agent) configuration classes, for environments derived from the `uvmf_environment_base` base class. It defines the prototype for the `initialize` function, used to initialize agent configurations in block level environments, as well as sub environments in environments instantiating other environments.

1.3.6.2 `uvmf_environment_base.svh`

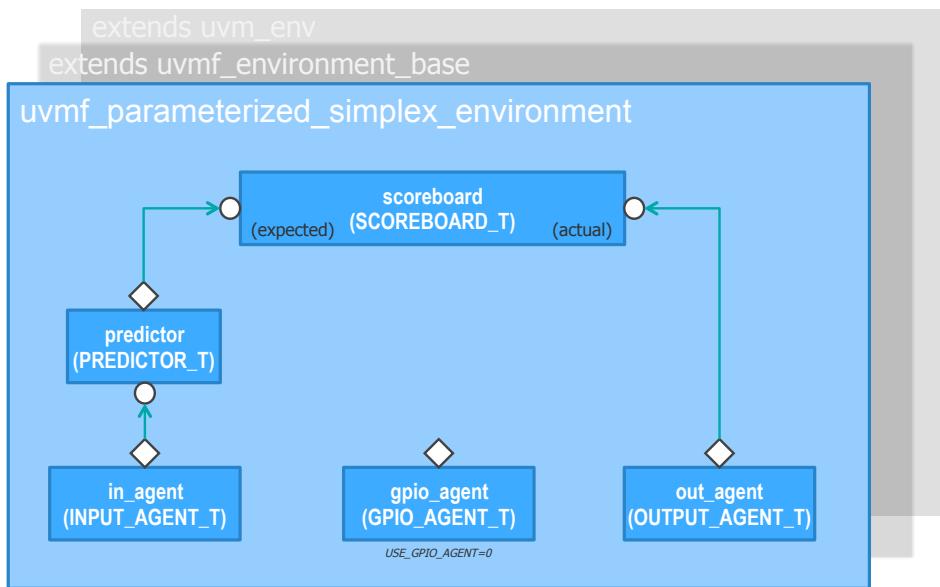
This is the base class for environment classes. It defines the prototype for the `set_config` function used to pass the configuration object handle into the environment and down through the environment hierarchy.

1.3.6.3 `uvmf_parameterized_simplex_environment.svh`

This and subsequent parameterized environment classes extend from the `uvmf_environment_base` class. The simplex environment is used for block level

environments where the design has two ports and data flows in one direction. The parameterized environment also optionally has a GPIO agent to drive pseudo-static input and output pins on the design.

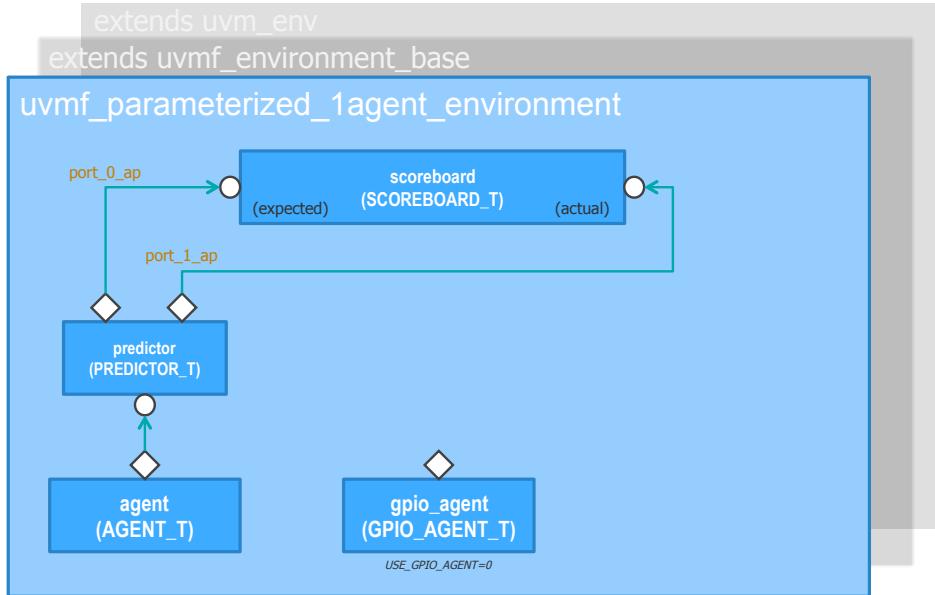
UVMF Parameterized Simplex Environment



1.3.6.4 *uvmf_parameterized_1agent_environment.svh*

The parameterized “1agent” environment is used for block level environments where the design has one port and data flows into and out of the design through the single port. The parameterized environment also optionally has a GPIO agent to drive pseudo-static input and output pins on the design.

UVMF Parameterized 1 Agent Environment



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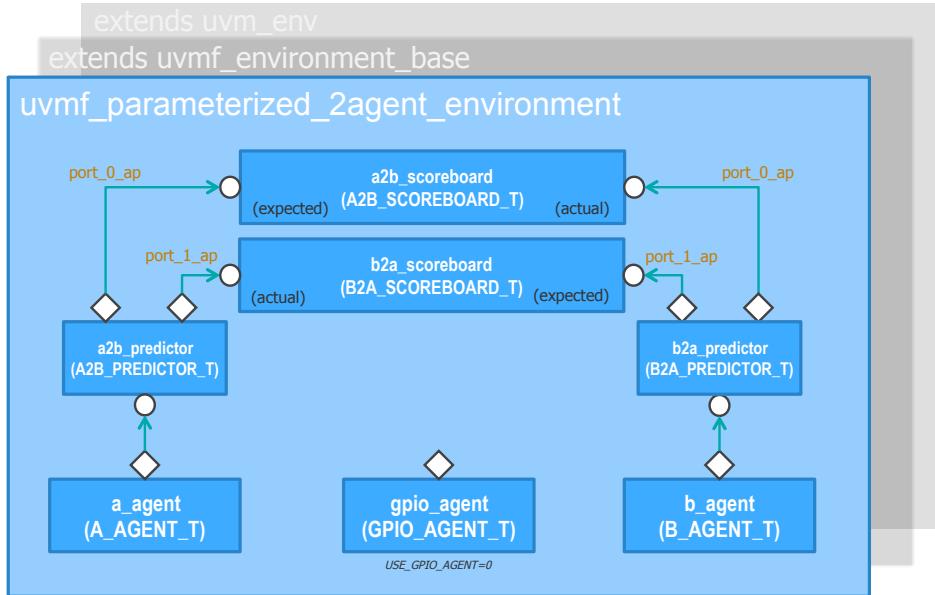
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1.3.6.5 `uvmf_parameterized_2agent_environment.svh`

The parameterized “2agent” environment is used for block level environments where the design has two ports and data flows in both directions. The parameterized environment also optionally has a GPIO agent to drive pseudo-static input and output pins on the design.

UVMF Parameterized 2 Agent Environment



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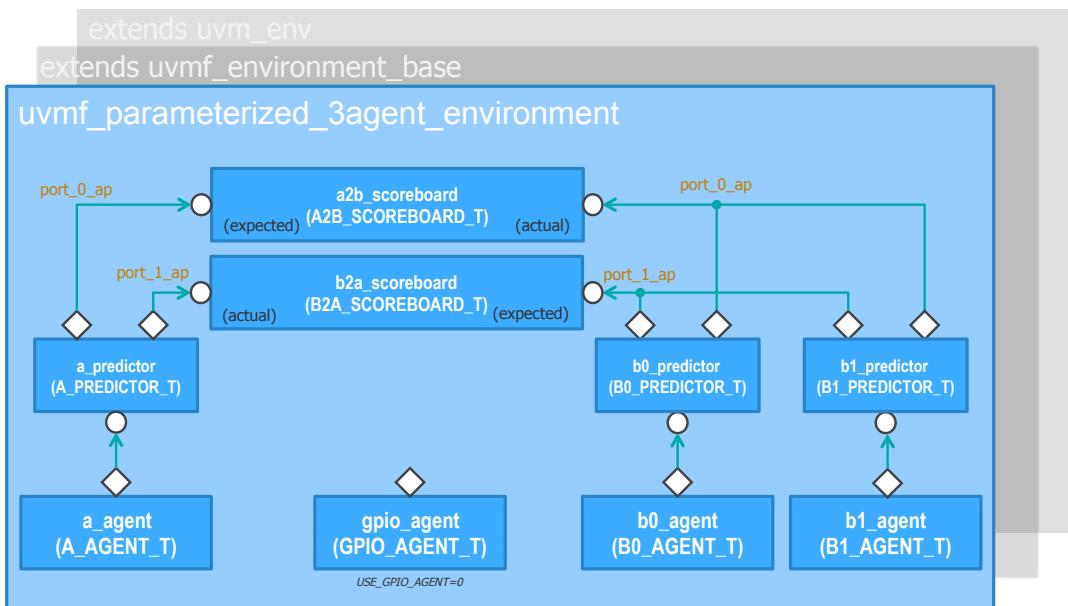
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1.3.6.6 `uvmf_parameterized_3agent_environment.svh`

The parameterized “3agent” environment is used for block level environments where the design has three ports. Data flows in both directions between the A side ports and B side ports. Data does not flow between ports B0 and B1. The parameterized environment also optionally has a GPIO agent to drive pseudo-static input and output pins on the design.

UVMF Parameterized 3 Agent Environment



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1.3.7 Test Classes

1.3.7.1 *uvmf_test_base.svh*

This is the base class for the base test for all simulation benches. The `uvmf_test_base` instantiates the top level configuration, top level environment and top level sequence. The test class directly extended from `uvmf_test_base` is named `test_top` and must define the parameters for the top level configuration, environment and sequence and calls the initialize function of the configuration class. `Test top` is then extended to create additional test cases by specifying factory overrides.

1.4 UVMF Interface Overview

Introduction

The interface used to implement a protocol is divided into three pieces: driver BFM, monitor BFM and signal bundle. Each of these pieces is a SystemVerilog interface. The driver BFM interface provides the tasks and functions needed to drive signals according to the protocol specification. The monitor BFM interface provides the tasks and functions needed to observe the interface protocol and capture relevant information from each bus.

transfer. The signal bundle interface contains all signals used by the protocol. It is also where assertions for protocol checking should reside.

The signals in the signal bundle interface are all of net type, either wire, tri, tri0 or tri1. The signals in this interface cannot be defined as types with storage, bit, reg or logic in order to enable binding the signal bundle into the design where signals are driven by RTL.

The signals are separated into an interface to support block to top reuse. The signal bundle interface is either hierarchically connected or bound into the desired level of hierarchy when the bus to be observed is driven by RTL instead of a driver_BFM. The signal bundle interface is connected to a monitor BFM and optionally a driver BFM through the BFM's port list. When the signal bundle is bound into the design the signal bundle is passed to the BFM's by hierarchical reference.

The diagrams below describe the function of and interaction between the signal bundle interface, the BFM interface and the UVM component. It is important to note that though the examples use a SystemVerilog virtual interface handle as the connection between the BFM and UVM component, the BFM_BIND_T parameter of the UVM component allows for alternative models of communication with the BFM, such as the DPI-C based function call model which requires instead the use of SystemVerilog hierarchical scopes stored as chandles to establish the connection between BFM and UVM component

1.4.1 Interface Driver BFM Flow

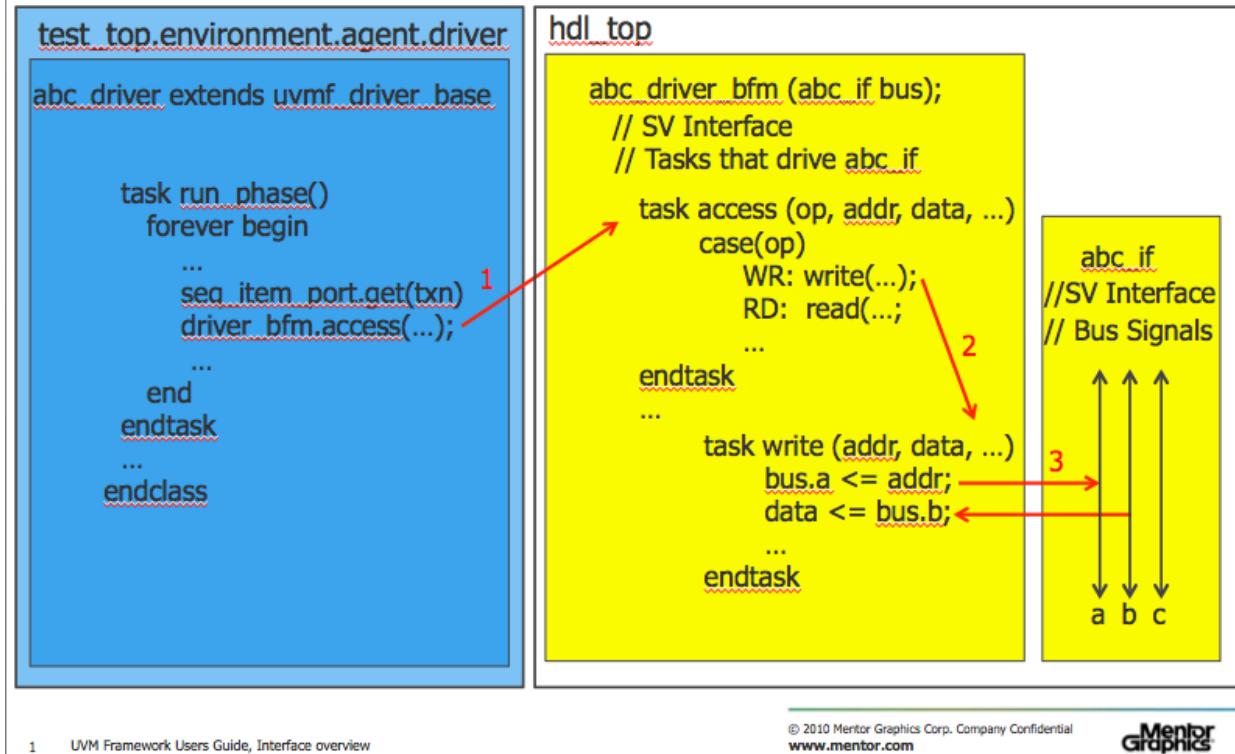
The following diagram shows the function of and interaction between the UVM driver, driver BFM and signal bundle interface.

The abc_driver is a UVM component derived from uvmf_driver_base. Its role is to request sequence items from the sequencer and send pertinent transaction information to the driver BFM. The sequence item handle can be sent directly from the abc_driver to the abc_driver_bfm. Alternatively, in support of emulation, the arguments to the access task must be synthesizable. In this case individual data attributes from the sequence item can be passed as arguments to the access task or the data attributes can be encapsulated into a packed struct that is passed to the abc_driver_bfm through the access task.

The abc_driver_bfm is a SystemVerilog interface that drives the bus signals according to the protocol specification. The content of this interface needs to be synthesizable in order to support emulation. In emulation, the BFM's as along with the DUT are synthesized and loaded into the emulator. Access to the signal bundle interface is provided to the driver BFM through its port list. The driver BFM drives the signals in the signal bundle interface.

The signal bundle interface contains all signals used in the protocol. It is used to connect the DUT to the monitor BFM and optionally the driver BFM.

UVMF Interface Driver Data Flow



1 UVM Framework Users Guide, Interface overview

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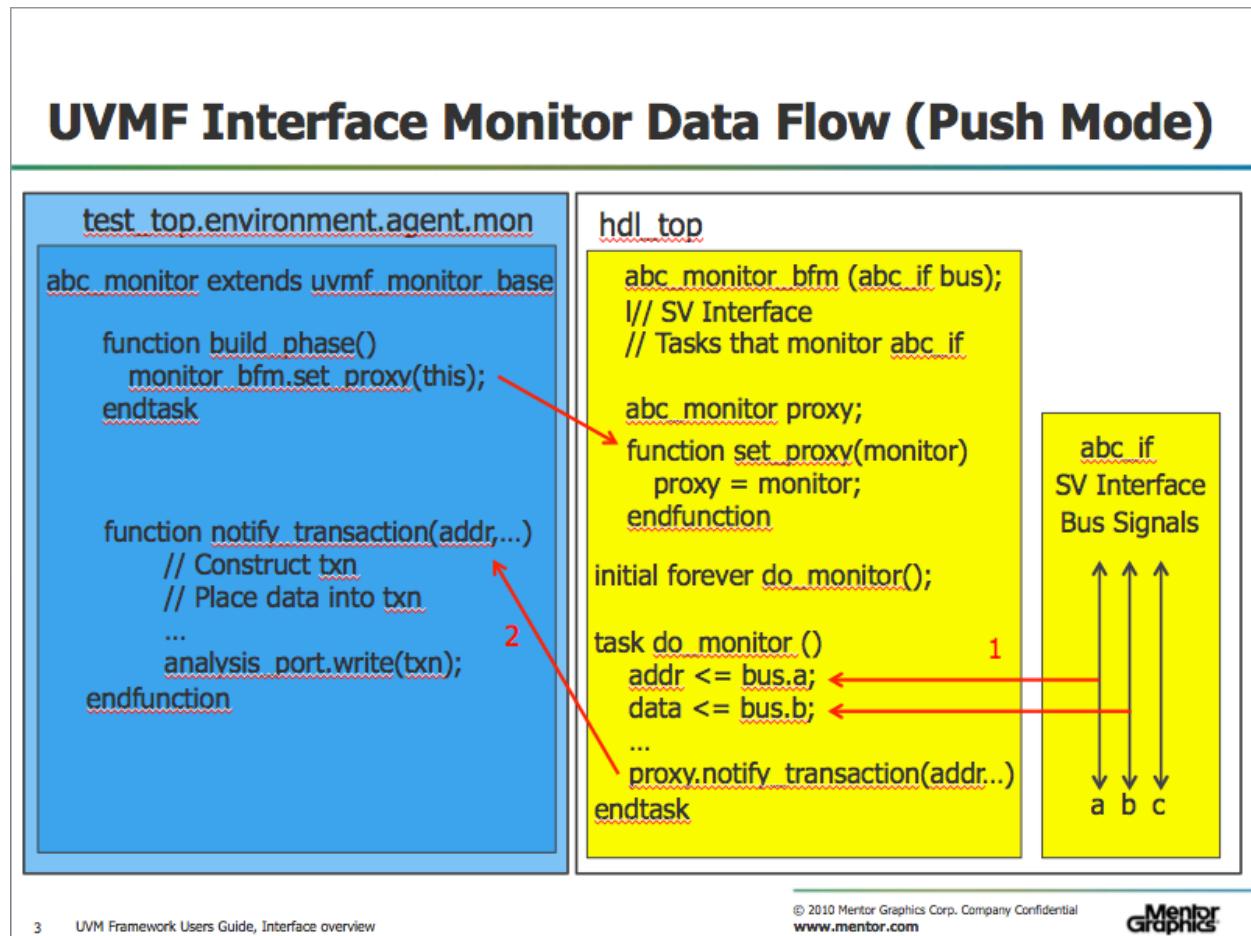
1.4.2 Interface Monitor BFM Flow

1.4.2.1 Push Mode Interface Monitor BFM Flow

The following diagram shows the function of and interaction between the UVM monitor, monitor BFM and signal bundle interface for a monitor using the s-called push mode for data transfer between the monitor BFM and UVM monitor. In the push mode the UVM BFM passes, or ‘pushes’, data unidirectionally to the UVM monitor. That is, communication only happens from the monitor BFM to the UVM monitor and this is done in zero simulation time since a function in the UVM monitor is used to receive the pushed data. The communication overhead between the `abc_monitor` and `abc_monitor_bfm` is minimized which can significantly increase in particular emulation performance.

The `abc_monitor` is a UVM component derived from `uvmf_monitor_base`. Its role is to broadcast sequence items received from the monitor BFM to other UVM components in the environment. Its handle in the monitor BFM is set using the `set_proxy` function in the monitor BFM during the UVM `build_phase`. This handle allows the monitor BFM to call functions in the UVM monitor to push data to the monitor.

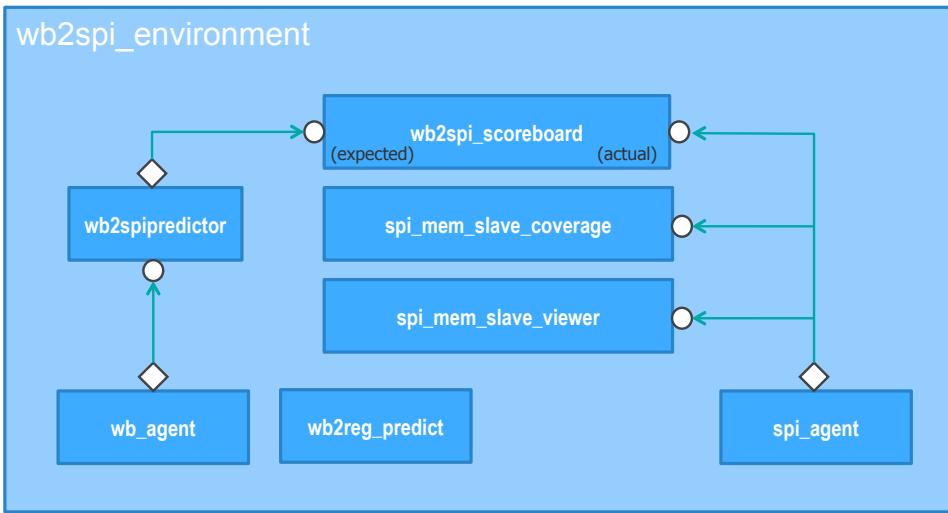
The abc_monitor_bfm is a SystemVerilog interface that observes the bus signals according to the protocol specification. The content of this interface needs to be synthesizable in order to support emulation. In emulation, the BFMAs well as the DUT are synthesized and loaded into the emulator. Access to the signal bundle interface is provided to the monitor BFM through its port list. The monitor BFM observes the signals in the signal bundle interface. Once the abc_monitor_bfm has observed a complete transfer on the bus it pushes the data observed to the abc_monitor using the notify_transaction function. The notify_transaction function in the abc_monitor copies the data to a transaction object and broadcasts the transaction to other components in the environment.



1.5 UVMF Environment Overview

The diagram below shows a block level environment. It is from the WB2SPI example. Block level environments include agents, predictors, scoreboards, coverage collectors and other components that are connected based on design data flow.

WB2SPI Example: Environment



WB2SPI Example Block Diagrams

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The diagram below shows a chip level environment. It is from the AHB2SPI example. Chip level environments include other environments. This is true for all environments other than block level environments. Environments are structured in a hierarchical manner similar to how RTL blocks are composed hierarchically. This allows for environment reuse as RTL components are reused.

AHB2SPI Example: Environment



WB2SPI Example Block Diagrams

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1.6 UVMF Simulation Bench Overview

The structure of the simulation bench is shown below. It is from the AHB2WB simulation bench.

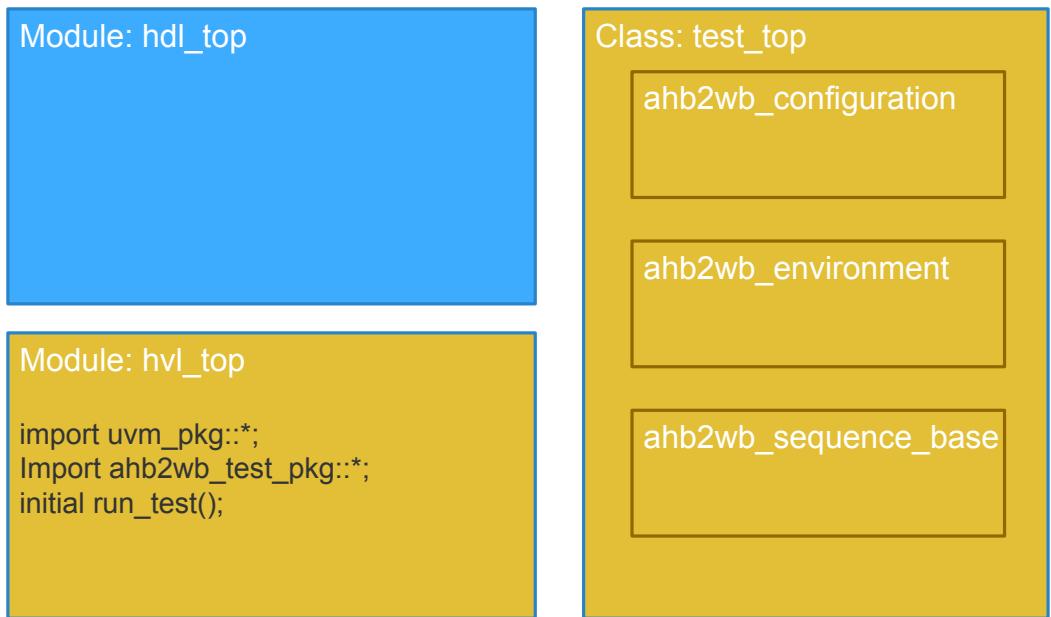
The three top level elements in every UVMF simulation bench are hdl_top, hvl_top and test_top.

Synthesizable content that may be run in emulation is placed in hdl_top. This includes the DUT, driver BFM's, monitor BFM's, signal bundle interfaces and any other logic required by the DUT.

The non-synthesizable elements that must be in a module are placed in hvl_top. This includes the test package import and the call to UVM's run_test to start the UVM phases.

The top level configuration, top level environment and top level sequence are placed in test_top. This defines the base test from which all other tests are derived.

AHB2WB Example: Test Bench



AHB2WB Example Block Diagrams

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2 UVM Framework Examples

2.1 Example Benches

2.1.1 AHB to wishbone Example

The AHB2WB example demonstrates a block level environment. It is located in the `base_examples` group. This block level environment is reused in the AHB2SPI chip level environment example. This example also demonstrates the use of a parameterized environment. The use of a parameterized environment alleviates the need to write an environment class.

This example demonstrates the following:

1. Block level environment that will be reused at the chip level
2. Use of a parameterized environment
3. Test plan import
4. Merging of test results
5. Generation of a custom coverage report

A specification for the `ahb2wb` DUT can be found in the `doc` folder of the example.

AHB2WB Example: Test Bench



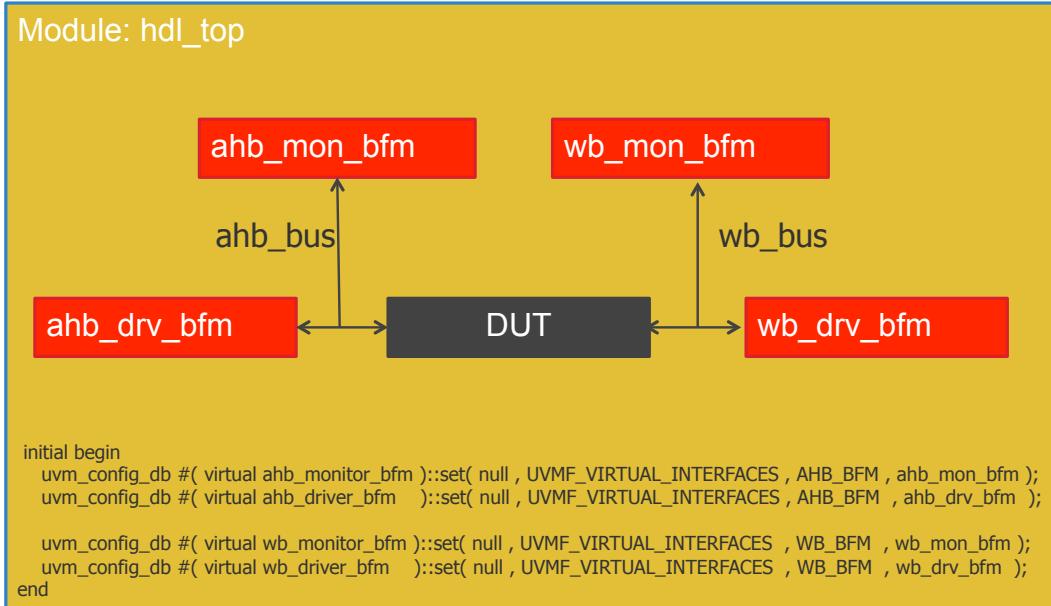
AHB2WB Example Block Diagrams

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As with all UVMF test benches, the AHB2WB test bench is composed of three top levels: `hdl_top`, `hvl_top` and `test_top`. The module named `hdl_top` contains the DUT, BFM's and signal bundle interfaces that tie them together. All content in `hdl_top` is synthesizable to support emulation. The module named `hvl_top` contains all content that must reside within a module but is not synthesizable. This includes importing the test package and calling `run_test` to start the UVM phases. The class named `test_top` is the top level UVM test class. It is selected using the `+UVM_TESTNAME` argument on the command line and constructed by the UVM factory.

AHB2WB Example: hdl_top



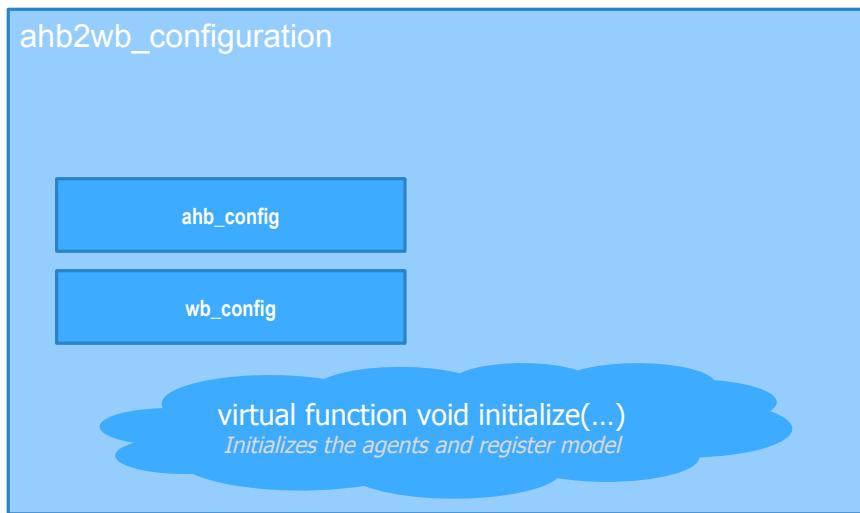
AHB2WB Example Block Diagrams

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The hdl_top module contains the DUT and BFM_s used to drive and monitor bus activity. The _drv_bfm interfaces provide signal stimulus. The _mon_bfm interfaces observe signal activity and capture transaction information for broadcasting to the environment for prediction, scoreboard_{ing} and coverage collection. An interface containing all of the signals for the bus ties the monitor BFM, driver BFM and DUT signal ports together. Protocol signals are separated into an interface to enable block to top reuse of environments and monitor BFMs. All BFMs are placed into the uvm_config_db by hdl_top for retrieval by the appropriate agent configuration. This mechanism is described in the section on resource sharing and initialization within the UVM Framework.

AHB2WB Example: Configuration



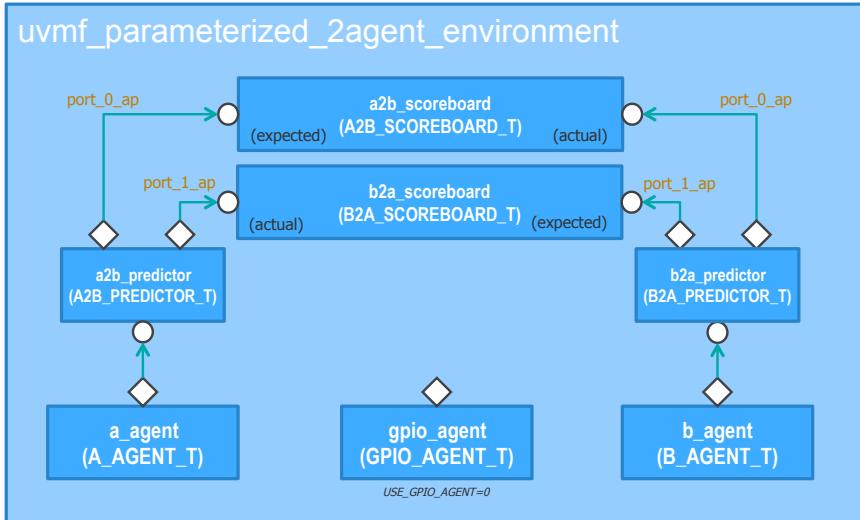
AHB2WB Example Block Diagrams

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The `ahb2wb_configuration` class contains a configuration for each agent in the environment. A function named `initialize` provides the agent configurations with the active/passive state of the agent, the path to its agent in the environment and the string name of the interface to be retrieved from the `uvm_config_db`. The `ahb2wb` configuration also contains DUT configuration specific variables that can be randomized as needed. The `ahb2wb` configuration class is constructed, randomized and initialized before the environment build phase is executed. This ensures that the environment can be built according to the configuration for the simulation.

AHB2WB Example: Environment



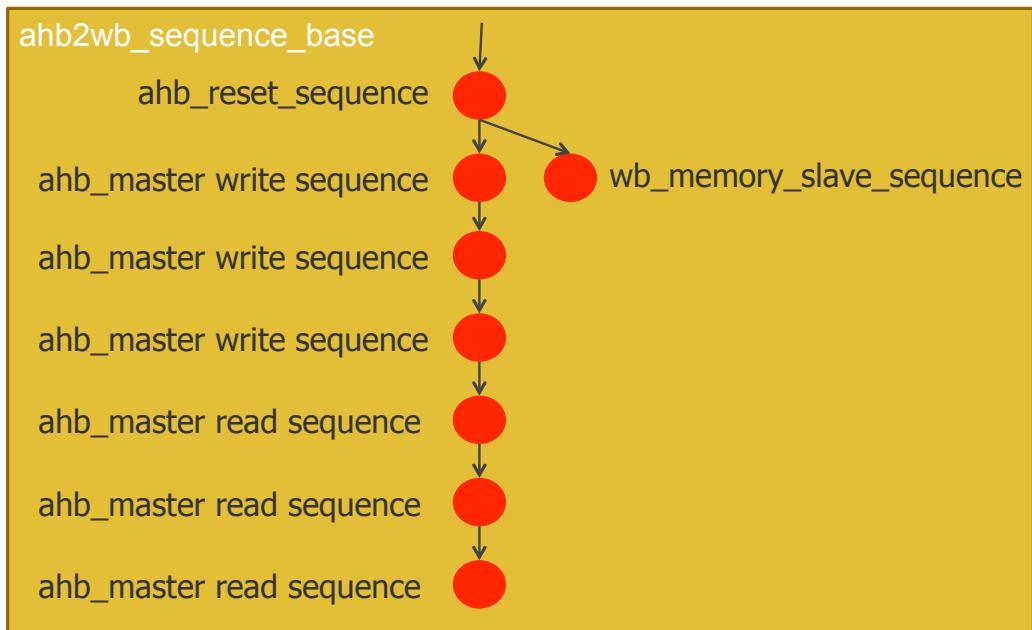
AHB2WB Example Block Diagrams

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The ahb2wb environment utilizes the uvmf_parameterized_2agent_environment. This alleviates the need to write an environment class. The ahb2wb environment is a type specialization of the parameterized environment. Creating a type specialization of the parameterized agents only requires the creation of a typedef. The typedefs used in the ahb2wb example can be found in verification_ip/environment_packages/ahb2wb_env_pkg/src/ahb2wb_environment.svh

AHB2WB Example: Top Level Sequence



AHB2WB Example Block Diagrams

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The top level sequence, named `ahb2wb_sequence_base`, orchestrates and controls all stimulus within the simulation. The stimulus flow is shown in the diagram above. The first sequence to be started is the `ahb reset sequence`. This causes the `ahb_drv_bfm` to assert and then release reset. Once the reset sequence has completed the wishbone memory slave sequence is started. This sequence is forked off because it will remain active throughout the simulation. This is because a slave device is always active and ready to respond to activity initiated by the master. Once the slave sequence is forked a series of writes and reads are performed on the `ahb2wb` DUT.

2.1.2 WB to SPI Example

The WB2SPI example demonstrates a block level environment. It is located in the `base_examples` group. This environment includes a register model based on the UVM register package. This block level environment is reused in the AHB2SPI chip level environment example. A specification for the `wb2spi` DUT can be found in the doc folder of the example.

This example demonstrates the following:

1. Block level environment that will be reused at the chip level
2. Block level UVM register model that will be reused at the chip level

WB2SPI Example: Test Bench



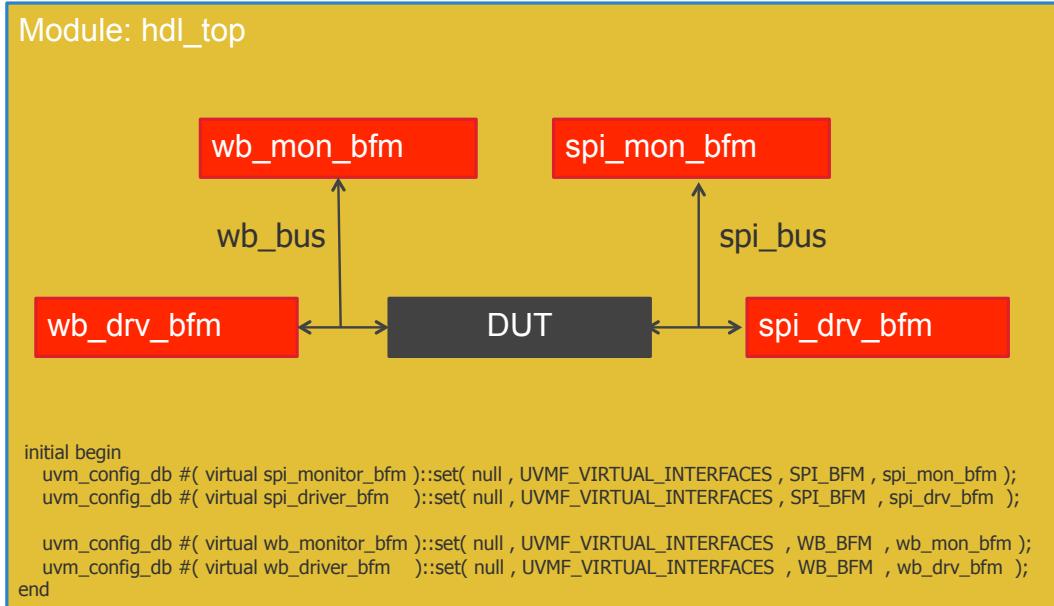
WB2SPI Example Block Diagrams

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As with all UVMF test benches, the WB2SPI test bench is composed of three top levels: `hdl_top`, `hvl_top` and `test_top`. The module named `hdl_top` contains the DUT, BFM's and signal bundle interfaces that tie them together. All content in `hdl_top` is synthesizable to support emulation. The module named `hvl_top` contains all content that must reside within a module but is not synthesizable. This includes importing the test package and calling `run_test` to start the UVM phases. The class named `test_top` is the top level UVM test class. It is selected using the `+UVM_TESTNAME` argument on the command line and constructed by the UVM factory.

WB2SPI Example: hdl_top



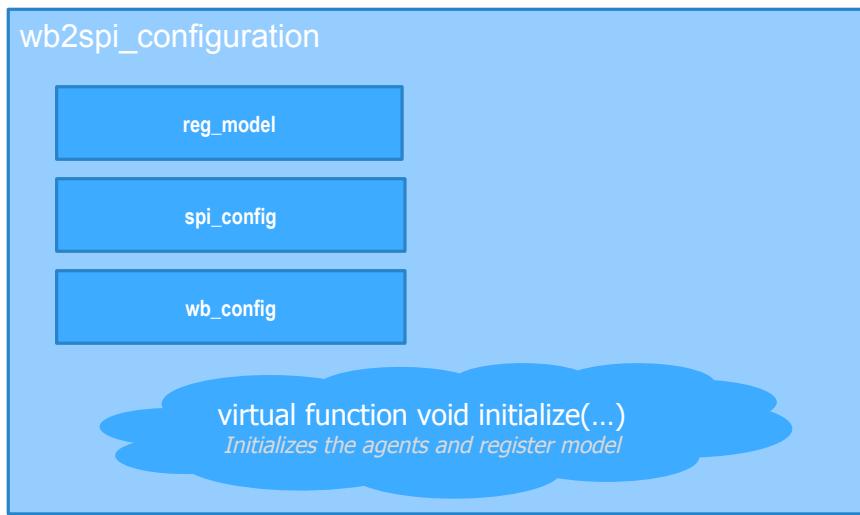
WB2SPI Example Block Diagrams

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The hdl_top module contains the DUT and BFM_s used to drive and monitor bus activity. The _drv_bfm interfaces provide signal stimulus. The _mon_bfm interfaces observe signal activity and capture signal information for broadcasting to the environment for prediction, scoreboard_{ing} and coverage collection. An interface containing all of the signals for the bus ties the monitor BFM, driver BFM and DUT signal ports together. Protocol signals are separated into an interface to enable block to top reuse of environments and monitor BFM_s. All BFM_s are placed into the uvm_config_db by hdl_top for retrieval by the appropriate agent configuration. This mechanism is described in the section on resource sharing and initialization within UVM Framework.

WB2SPI Example: Configuration



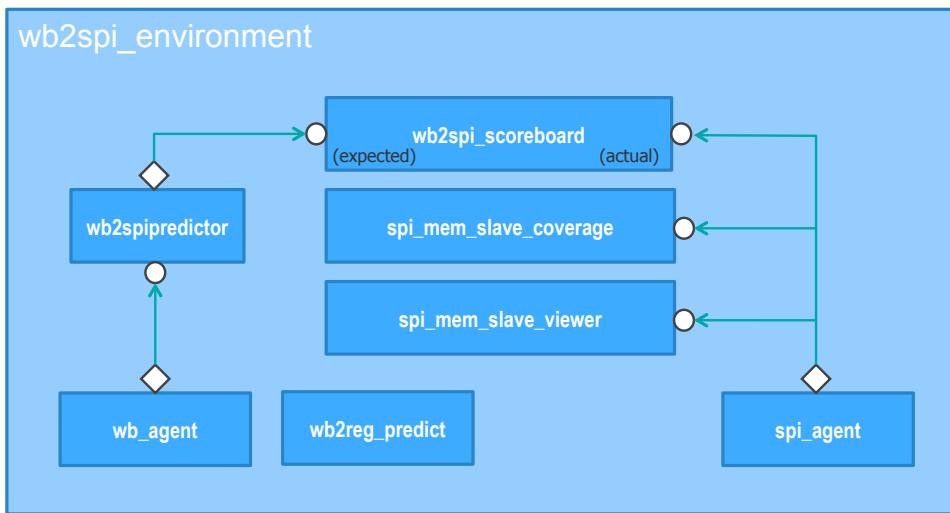
WB2SPI Example Block Diagrams

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The `wb2spi_configuration` class contains a configuration for each agent in the environment and the register model. The register model is a UVM register block for the `wb2spi` DUT. This register block will be a sub block of the `ahb2spi` register block used in the chip level simulation. A function named `initialize` provides the agent configurations with the active/passive state of the agent, the path to its agent in the environment and the string name of the interface to be retrieved from the `uvm_config_db`. The `wb2spi` configuration also contains DUT configuration specific variables that can be randomized as needed. The `wb2spi` configuration class is constructed, randomized and initialized before the environment build phase is executed. This ensures that the environment can be built according to the configuration for the simulation.

WB2SPI Example: Environment



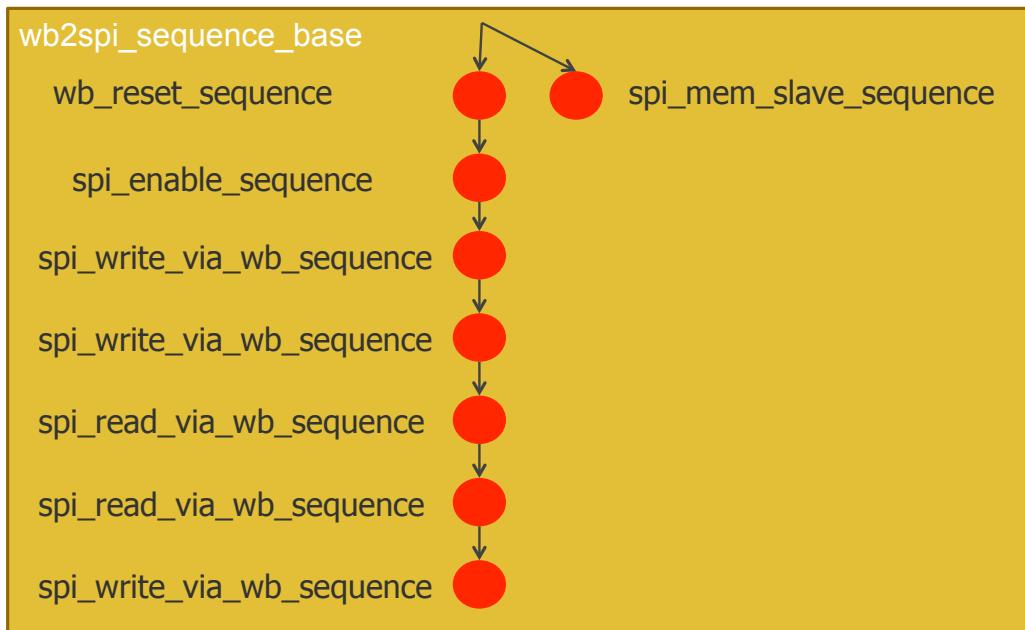
WB2SPI Example Block Diagrams

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The wb2spi environment contains the agents, predictor, scoreboard, coverage and transaction viewing components shown in the above diagram. The wishbone agent interacts with the wb_drv_bfm and wb_mon_bfm. It receives stimulus information from sequences in the top level sequence. Bus operations are observed and broadcasted to the wb2spi predictor. The predictor creates an expected SPI transaction based on DUT configuration and input from the wishbone bus. Output from the wb2spi predictor are sent to the scoreboard to be queued until DUT activity is received for comparison. The SPI agent interacts with the spi_drv_bfm and spi_mon_bfm. It receives stimulus information from sequences in the top level sequence. Bus operations are observed and broadcasted to the wb2spi scoreboard, coverage component and transaction viewing component. The coverage component records functional coverage of SPI operations. The transaction viewing component provides a transaction viewing stream of SPI memory slave transactions. The monitor within the SPI agent provides transaction viewing of the base SPI transfer. This allows for viewing of raw SPI transfers as well as the functional meaning of each bit within the raw SPI transfer.

WB2SPI Example: Top Level Sequence



WB2SPI Example Block Diagrams

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The top level sequence, named wb2spi_sequence_base, orchestrates and controls all stimulus within the simulation. The stimulus flow is shown in the diagram above. The first sequence to be started is the SPI memory slave sequence. This sequence is forked off at the beginning because it will remain active throughout the simulation. This is because a slave device is always active and ready to respond to activity initiated by the master. Once the slave sequence is forked the wishbone reset sequence is started. This causes the wb_drv_bfm to assert and then release reset. Once the reset sequence has completed a series of writes and reads are performed on the wb2spi DUT. The format of the SPI transfer as a memory slave is shown in the table below.

SPI Slave Bus Protocol

Signal	Data [7]	Data [6:4]	Data [3:0]
MOSI	RW 1: Write, 0: Read	Address[2:0]	Data[3:0]
MISO	STATUS (prev command) 1:Success, 0:Error	Address[2:0]	Data[3:0]

2.1.3 AHB to SPI Example

The AHB2SPI example demonstrates a chip level environment. It is located in the base_examples group. This chip level environment reuses the AHB2WB and WB2SPI block level environments. This environment includes a register model based on the UVM register package. This chip level register model contains a register block for the WB2SPI block level environment.

This example demonstrates the following:

1. Chip level environment that reuses block level environments
2. Chip level UVM register model that reuses a block level UVM register model

AHB2SPI Example: Test Bench



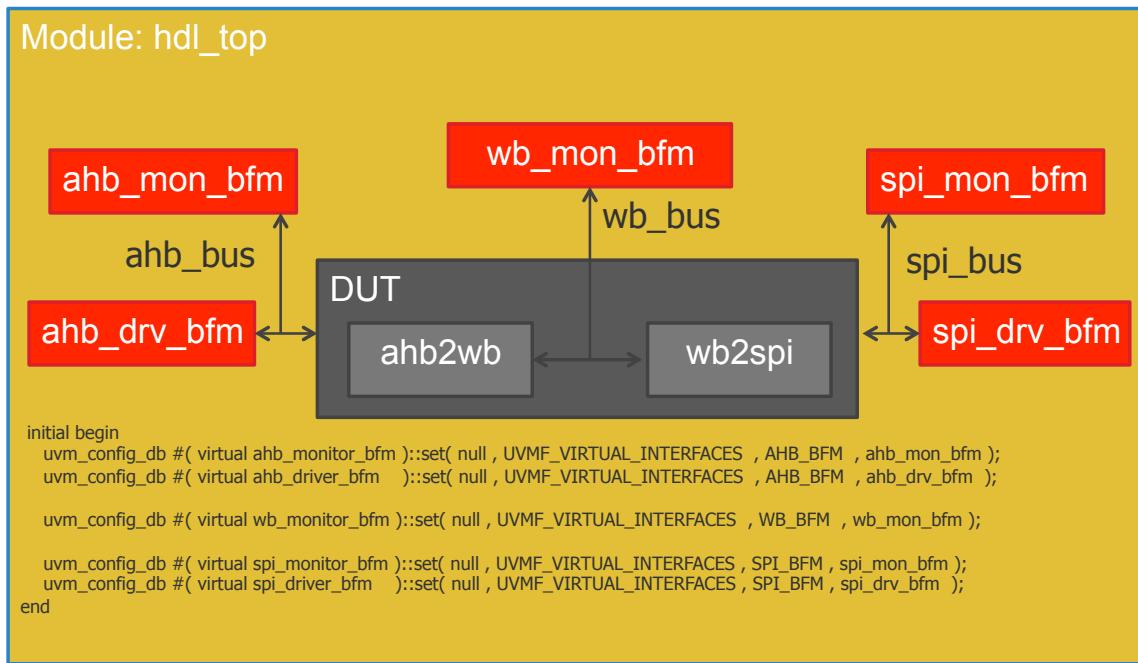
WB2SPI Example Block Diagrams

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As with all UVMF test benches, the AHB2SPI test bench is composed of three top levels: hdl_top, hvl_top and test_top. The module named hdl_top contains the DUT, BFM's and signal bundle interfaces that tie them together. All content in hdl_top is synthesizable to support emulation. The module named hvl_top contains all content that must reside within a module but is not synthesizable. This includes importing the test package and calling run_test to start the UVM phases. The class named test_top is the top level UVM test class. It is selected using the +UVM_TESTNAME argument on the command line and constructed by the UVM factory.

AHB2SPI Example: hdl_top



WB2SPI Example Block Diagrams

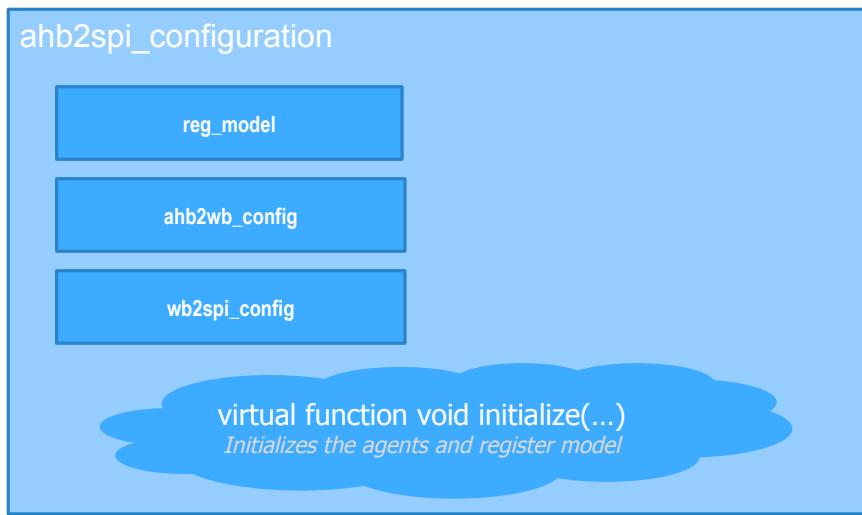
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The `hdl_top` module contains the DUT and BFM^s used to drive and monitor bus activity. The `_drv_bfm` interfaces provide signal stimulus. The `_mon_bfm` interfaces observe signal activity and capture signal information for broadcasting to the environment for prediction, scoreboard^{ing} and coverage collection. An interface containing all of the signals for the bus ties the monitor BFM, driver BFM and DUT signal ports together. Protocol signals are separated into an interface to enable block to top reuse of environments and monitor BFM^s. All BFM^s are placed into the `uvm_config_db` by `hdl_top` for retrieval by the appropriate agent configuration. This mechanism is described in the section on resource sharing and initialization within UVM Framework.

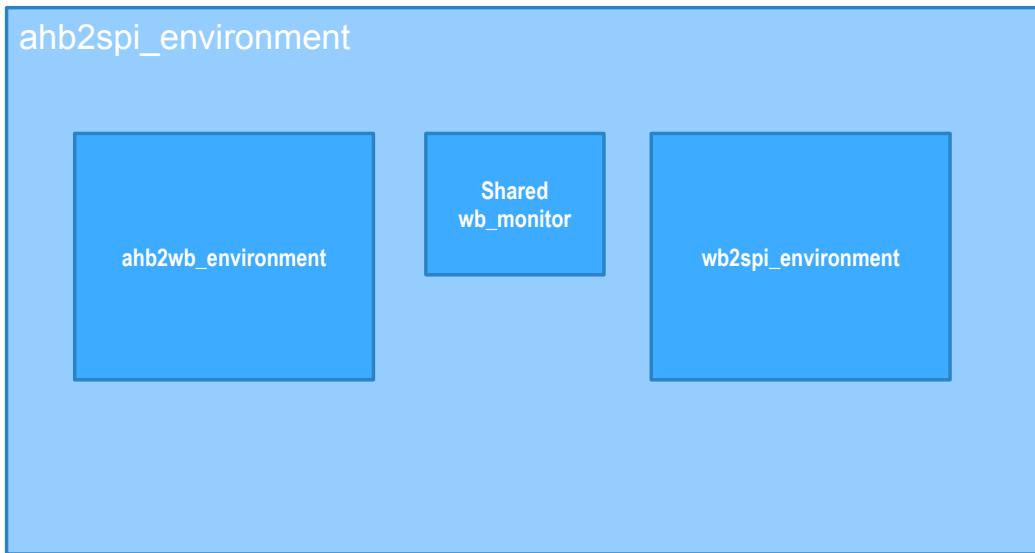
In this example the wishbone bus is internal to the DUT and driven by RTL within the DUT. A wishbone signal bundle interface, `wb_bus`, is connected to the wishbone bus in the DUT in order to observe bus activity. This can be done using either the SystemVerilog bind construct or hierarchically connecting the signal bundle into the DUT. This wishbone signal bundle is connected to two wishbone monitor BFM^s. This is to provide the wishbone agent within each of the block level environments a wishbone monitor BFM virtual interface handle. This allows independent prediction, scoreboard^{ing} and coverage for each block level environment.

AHB2SPI Example: Configuration



The `ahb2spi_configuration` class contains a configuration for each block level environment within this chip level environment and a register model. The register model is a UVM register block for the `ahb2spi` DUT. This register block contains a `wb2spi` register block for use by the `wb2spi` block level environment. A function named `initialize` provides the environment configurations with the simulation level, BLOCK/CHIP, the hierarchical path down to the chip level environment and an array of string names of the interface to be retrieved from the `uvm_config_db`. The `ahb2spi` configuration also contains DUT configuration specific variables that can be randomized as needed. The `ahb2spi` configuration class is constructed, randomized and initialized before the environment build phase is executed. This ensures that the environment can be built according to the configuration for the simulation. Randomization occurs down through the configuration classes. The `post_randomize` of `ahb2spi_configuration` randomizes `ahb2wb_config` and `wb2spi_config` applying implication constraints to enforce lower level value options based on upper level values randomly selected.

AHB2SPI Example: Environment



WB2SPI Example Block Diagrams

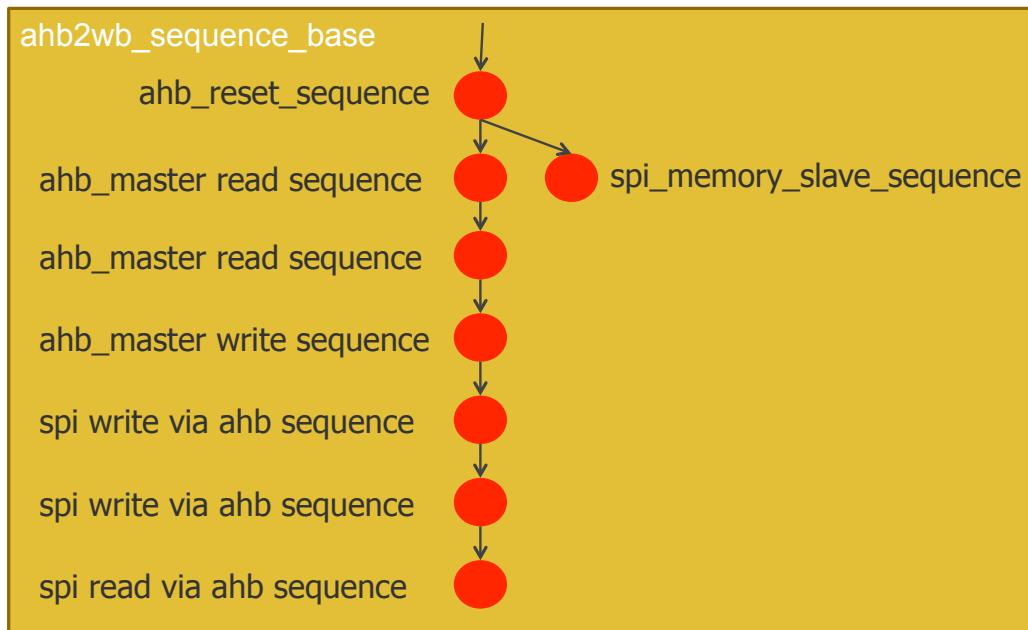
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The ahb2spi environment contains the ahb2wb environment and the wb2spi environment. These two block level environments perform the same prediction, scoreboarding and coverage provided when run in the block level bench. Stimulus is driven into the design via the ahb interface. The wishbone interface is now buried in the DUT. It is observed by both environments for prediction, scoreboarding and coverage. Data is sent out through the SPI interface of the DUT. The ahb2wb_environment is configured by the ahb2spi_configuration. The ahb2wb_environment is configured by the ahb2wb_configuration. The wb2spi_environment is configured by the wb2spi_configuration.

The ahb2spi environment creates a wb_monitor to be shared between the two environments that need to observe the wb bus. This wb monitor is constructed by the ahb2spi environment and placed into the uvm_config_db for retrieval by the wb agent within each block level environment. The shared wb_monitor is connected to the single wb_monitor_bfm. WB transactions observed by the wb_monitor_bfm are sent to the shared wb_monitor and broadcasted within each environment.

AHB2SPI Example: Top Level Sequence



AHB2WB Example Block Diagrams

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The top level sequence, named `ahb2spi_sequence_base`, orchestrates and controls all stimulus within the simulation. The stimulus flow is shown in the diagram above. The first sequence to be started is the ahb reset sequence. This causes the `ahb_drv_bfm` to assert and then release reset. Once the reset sequence has completed then the SPI memory slave sequence is started. This sequence is forked off because it will remain active throughout the simulation. This is because a slave device is always active and ready to respond to activity initiated by the master. Once the slave sequence is forked a series of writes and reads are performed on the DUT through the ahb port. These operations write and read the SPI memory slave attached to the SPI port of the DUT.

2.1.4 GPIO Example

The GPIO example demonstrates the use of a parameterized interface. The `WRITE_PORT_WIDTH` and `READ_PORT_WIDTH` parameters are used to instantiate the BFM interfaces, agent, configuration, and sequence classes. The value for these parameters are defined in the `gpio_example_parameters_pkg`.

This example demonstrates the following:

1. The creation and instantiation of a parameterized interface

GPIO Example: Test Bench



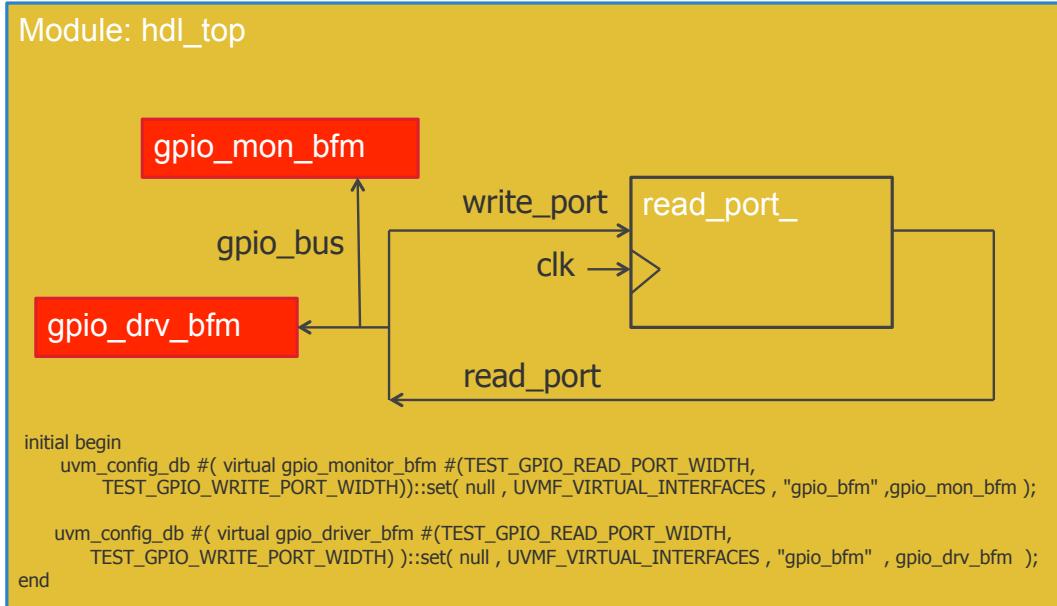
GPIO Example Block Diagrams

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As with all UVMF test benches, the GPIO test bench is composed of three top levels: `hdl_top`, `hvl_top` and `test_top`. The module named `hdl_top` contains the DUT, BFM`s` and signal bundle interfaces that tie them together. All content in `hdl_top` is synthesizable to support emulation. The module named `hvl_top` contains all content that must reside within a module but is not synthesizable. This includes importing the test package and calling `run_test` to start the UVM phases. The class named `test_top` is the top level UVM test class. It is selected using the `+UVM_TESTNAME` argument on the command line and constructed by the UVM factory.

GPIO Example: hdl_top



GPIO Example Block Diagrams

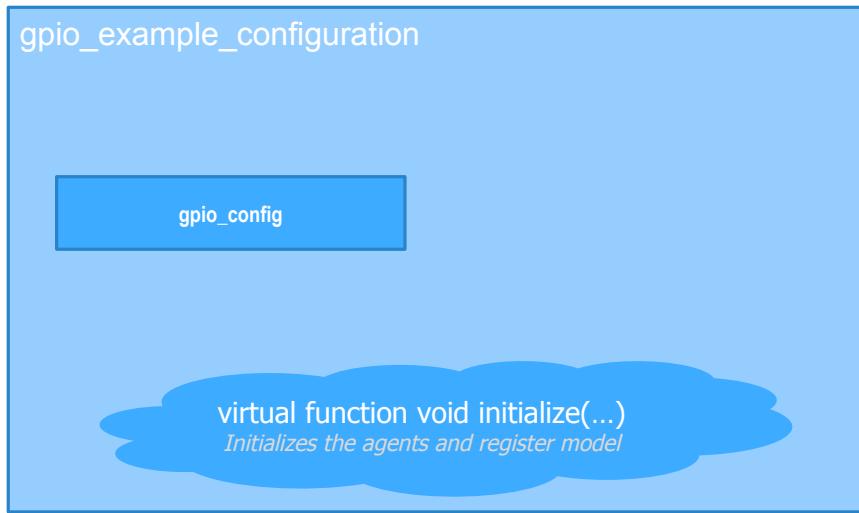
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The hdl_top module contains the DUT and BFM interfaces used to drive and monitor bus activity. The _drv_bfm interfaces provide signal stimulus. The _mon_bfm interfaces observe signal activity and capture signal information for broadcasting to the environment for prediction, scoreboarding and coverage collection. An interface containing all of the signals for the bus ties the monitor BFM, driver BFM and DUT signal ports together. Protocol signals are separated into an interface to enable block to top reuse of environments and monitor BFM. All BFM are placed into the uvm_config_db by hdl_top for retrieval by the appropriate agent configuration. This mechanism is described in the section on resource sharing and initialization within UVM Framework.

In this example the DUT is a simple register named read_port_. The input to the register is the write_port of the gpio_bus. On each clock edge the value on write_port is output on read_port_. The read_port_value is then assigned to the read_port of the gpio_bus. This inserts a one clock delay between the write_port output and read_port input. This loopback delay is only for demonstration purposes.

GPIO Example: Configuration



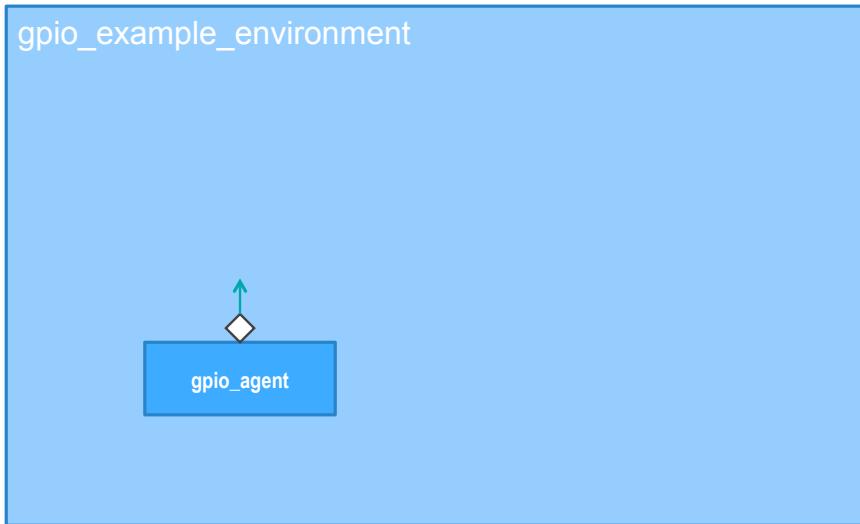
GPIO Example Block Diagrams

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The `gpio_example_configuration` class contains a configuration object for the GPIO agent in the environment. A function named `initialize` provides the agent configuration with the active/passive state of the agent, the path to its agent in the environment and the string name of the interface to be retrieved from the `uvm_config_db`.

GPIO Example: Environment



GPIO Example Block Diagrams

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The gpio_example_environment only contains the gpio_agent. This is because the purpose of this example is to demonstrate the use of a parameterized interface, agent, configuration and sequence.

GPIO Example: Top Level Sequence

```
58 // ****
59 virtual task body();
60
61     gpio_seq = new("gpio_seq");
62     gpio_seq.start(gpio_sequencer);
63     gpio_config.wait_for_num_clocks(2); //#20ns;
64     gpio_seq.bus_a = 16'h1234;
65     gpio_seq.bus_b = 16'habcd;
66     `uvm_info("GPIO", gpio_seq.convert2string(), UVM_MEDIUM)
67     gpio_seq.write_gpio();
68     gpio_config.wait_for_num_clocks(2); //#20ns;
69     gpio_seq.read_gpio();
70     gpio_config.wait_for_num_clocks(2); //#20ns;
71     `uvm_info("GPIO", gpio_seq.convert2string(), UVM_MEDIUM)
72
73
74 endtask
```

GPIO Example Block Diagrams

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The sequence used in this example is different from most sequences in that it is started at the beginning of the simulation and remains throughout the simulation. Writing values to the GPIO write_port and reading values from the GPIO read_port are done through tasks in this sequence. The sequence, named gpio_seq, is an extension to the gpio_sequence located in the gpio_pkg. This extension defines bit assignments to the write_port and read_port. In this case bus_a and bus_b are assigned to the write_port, bus_c and bus_d are assigned from the read_port. The flow of the top level sequence is outlined below:

Initialization:

Line 61: Construct the gpio_seq sequence.

Line 62: Start the gpio_seq sequence. This sequence remains resident throughout the simulation.

Line 63: Wait for two clocks using the wait_for_num_clocks task within the gpio_agents configuration class.

Write operation:

Line 64 and 65: Set the values of bus_a and bus_b variables.

Line 66: Display the variable values in the sequence item within gpio_seq.

Line 67: Write the new values of bus_a and bus_b to the GPIO write_port

Line 68: Wait for two clocks using the wait_for_num_clocks task within the gpio_agents configuration class.

Read operation:

Line 69: Read the values currently on the GPIO write_port and read_port.

Line 70: Wait for two clocks using the wait_for_num_clocks task within the gpio_agents configuration class.

Line 71: Display the variable values in the sequence item within gpio_seq.

2.1.5 Questa VIP Examples

The Questa VIP examples provide UVM Framework environments with instantiations of Questa VIP. They reside in the vip_examples group. These examples can be used to understand where constituent pieces of Questa VIP reside in the environment. They can also be used as a starting point for designs that have standard protocols.

2.1.5.1 AXI4 Example

This example demonstrates the various features of the QVIP AXI4 as listed below. This example can be used as a production environment by substituting a design for either axi4_master, axi4_slave or both.

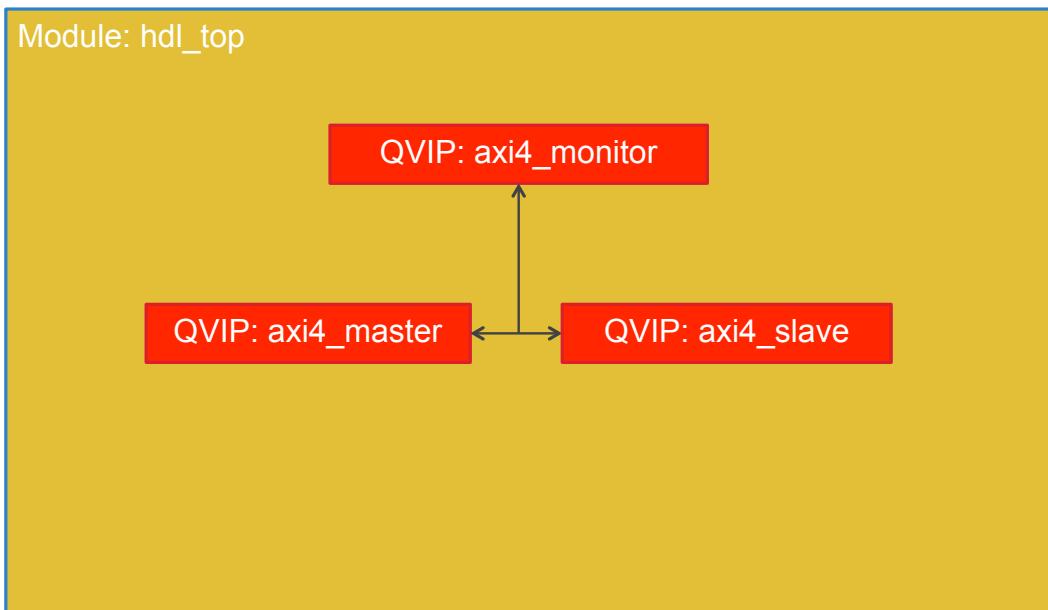
This example demonstrates the following:

1. Block level environment with a QVIP AXI4 master connected to a QVIP AXI4 slave with a QVIP AXI4 monitor observing bus activity.

The table below lists the interfaces and classes used from the QVIP Library and where they are located in the environment.

Component Description	Component Used	Location in UVMF
SystemVerilog interface	Axi4_master Axi4_slave Axi4_monitor	Hdl_top.sv
Configuration	Axi4_vip_config	Vip_axi4_configuration.svh
Agent	Axi4_agent	Vip_axi4_environment.svh
Sequence	Axi4_out_of_order_sequence	Qvip_axi4_bench_sequence_base.svh

QVIP AXI4 Example: hdl_top



AHB2WB Example Block Diagrams

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2.2 Running UVMF Example Benches

The UVMF examples will run on Windows and Linux. UVMF examples are run from the sim directory located under the *exampleGroup/project_benches/benchName* directory. The examples can be run in either command line or GUI mode. The sections below describe how to run the examples in Linux and Windows.

2.2.1 Running the Examples in Linux

Makefiles are provided under the sim directory of each example bench for running on Linux. Example benches are under the project_benches directory. Under each example bench is the sim directory where simulations are run. When in the sim directory do the following to run a simulation:

Set environment variables listed in the Makefiles section of this document.

Run one of the two following commands:

```
make cli  
make debug
```

The cli make target runs the sim in command line mode. The debug make target runs the sim in GUI mode. You can view signals and transactions in debug mode.

2.2.2 Running the Examples in Windows

There are no .do files provided for running in Windows. For running on windows a .do file can be generated using the makefile and a windows make utility. To generate a do file using a windows make utility perform the following steps:

Set environment variables listed in the Makefiles section of this document.

Enter the sim directory of the example you wish to run

run the following command to make a command line mode do file:

```
make -n cli >> make.cli.do
```

run the following command to make a GUI mode do file:

```
make -n debug >> make.debug.do
```

To run in command line mode execute make.cli.do

To run in GUI mode execute make.debug.do

2.3 Running the Examples on Veloce

By default, the makefiles are configured to run in simulation mode. The following make variables are used to run in emulation. Add these variables to the make command in the format shown as indicated.

This variable is used to run emulation:

```
USE_VELOCE = 1 (default is 0, i.e. pure simulation mode)
```

This variable enables emulatable VIP (VTL) use in lieu of pure simulation VIP (QVIP)

```
USE_VTL = 1 (default is 0, i.e. QVIP mode)
```

This variable enables the legacy TBX flow instead of the Veloce OS3 emulation flow:

```
USE_LEGACY_TBX_FLOW = 1 (default is 0, i.e. OS3 flow)
```

```
make [cli|debug] [USE_VELOCE=1] [USE_VTL=1] [USE_LEGACY_FLOW=1]
```

Note that the combination USE_VELOCE = 1 and USE_VTL = 0 is invalid. In the presence of VIP the use of emulation (USE_VELOCE = 1) implies the use of emulation-ready VIP (USE_VTL = 1). The reverse is not true, i.e. emulation-ready VIP can also be used in pure simulation.

2.4 Running the Examples using Questa Verification Run Manager

Questa Verification Run Manager (VRM) is a utility built into Questa that facilitates the execution of regressions in a highly automated way. In addition to being able to build and run simulations, it also easily integrates with grid management software like LSF, automates the process of determining PASS/FAIL for individual runs and automatically manages the collection and merging of coverage data as well as many other capabilities.

The UVMF examples are shipped with a reference VRM control file (RMDB) that illustrates some of the basic VRM capabilities for each bench. Each bench's sim directory contains a link to a common default.rmdb file which controls VRM and a test list control file unique to each bench. To invoke a VRM regression simply invoke the command "vrun" in a bench's sim directory.

When invoked for a given bench, VRM will compile the test bench and run the tests and seeds specified in the test list file in parallel. All of the data and log files for a given run can be found in the generated VRMDATA directory.

2.5 Viewing the Examples using Questa Visualizer

The Mentor Visualizer Debug Environment is Mentor's next generation debugger GUI. If installed and licensed it can be invoked in post-simulation debug mode against any of the UVMF test benches through the makefiles.

To run a simulation with Visualizer enabled, set the USE_VIS variable to 1 on all make command lines for a given test.

To run a simulation with Visualizer, logging SV and UVM constructs in addition to RTL waves, set USE_VIS and USE_VIS_UVM to 1 on all make command lines for a given test.

Once a simulation is complete, invoke Visualizer by running "make vis".

3 Makefiles

The UVMF uses a two level makefile structure. Individual packages have a makefile that contains make targets for compiling the package and associated modules. The simulation bench makefile includes the makefiles for all packages used by the bench as well as the reuse makefile. This gives the bench makefile access to the make targets needed to compile required packages located under verification_ip. The bench makefile also contains make targets for all packages located under the projects tb directory.

3.1 Package Makefile

Each package located under the verification_ip directory has a makefile that contains the make targets required to compile the package. These makefiles are included in the simulation bench makefile depending on which packages under verification_ip are used by the bench. Including each package makefile in the bench makefile allows project bench access to make targets for all packages under verification_ip that are required by the bench.

3.2 Reuse Makefile

The reuse makefile is located in scripts. This makefile contains common makefile variables and conditionals used to create commands for compiling and running example UVMF code. The reuse makefile is included by each project bench makefile

3.3 Simulation Bench Makefile

Each project bench contains a makefile located in the sim directory under project_benches. This makefile includes the reuse makefile for compiling required code located under verification_ip. The bench makefile also contains make targets for all packages and modules located under the tb directory.

3.4 User Makefile Variables

3.4.1 Environment variables used for directory structure control

The makefile in verification_ip/scripts contains the following variables that can be set using environment variables. These variables are used to indicate the location of code to be used by UVMF.

UVMF_HOME : This variable points to the home directory of UVMF core code. This represents released, non-user modified, code. This directory should contain the uvmf_base_pkg, common, scripts and base_examples directories. Example:
/tools/Questa/10.5/questasim/examples/UVM_Framework/UVMF_3.6c

UVMF_VIP_LIBRARY_HOME : This variable points to the directory where reusable UVMF IP is located. It should point to and include the verification_ip directory. Example:
/repository/simulation/reuse/project_name/verification_ip

UVMF_PROJECT_DIR : This variable points to the directory where project benches are located. It should point to and include the project_benches directory. Example:
/projects/simulation/project_name/project_benches

3.4.2 Command Line Makefile Variables

The makefile in the project_benches/bench/sim directory contains the following make variables that can be set from the command line. These variables have default values that can be seen in the makefile. To change the values of a makefile variable use the following format: TEST_NAME=my_test

TEST_NAME, TEST_SEED, TEST_VERBOSITY, UVM_CLI_ARGS, USE_VELOCE,
USE_LEGACY_TBX_FLOW, DEBUG_DO_COMMANDS

3.4.3 Adding Command Switches to Existing Flow

The makefile in the project_benches/bench/sim directory contains the following make variables that can be used to add switches to the vcom, vlog, vopt, and vsim commands. Add the desired switches to the variable in the makefile. Do not add switches using the command line format listed above.

VCOM_ARGS, VLOG_ARGS, VELANALYZE_ARGS, VELANALYZE_HVL_ARGS,
BATCH_VOPT_ARGS, DEBUG_VOPT_ARGS, COMMON_VSIM_ARGS, BATCH_VSIM_ARGS,
DEBUG_VSIM_ARGS

4 Using the Python Templates

4.1 Overview

Python based templates are provided by UVMF for rapid code development. Three code generation templates are provided: interface, environment and bench. The interface template generates the files, infrastructure and interconnect required for an interface package. The environment template generates the files, infrastructure and interconnect required for an environment package. The bench template generates the files, infrastructure and interconnect required for a project bench. The code generated by the templates can be simulated as is. This provides a starting point for adding required design and protocol specific code.

The templates have been run on the following python releases: 2.6, 2.7. Confirm the python version on machine is at least 2.6 using the following command: `python -V`

It is important to note that python uses spaces, indentation, to group code blocks. Each line of template configuration files should start at the beginning of the line with no whitespace, indentation.

The input to the generator is a Python configuration script that imports the `uvmf_gen.py` Python module as well as specifying the work to be done. Example configuration scripts for generating UVMF code using the templates is located under `templates/python/examples`.

4.2 Installation and operation

Instructions on installation and operation of the python based UVMF code generators is located in `templates/python/templates README`

5 Developing an Interface Package using the Python Templates

5.1 Format and input required by the template

The UVM Framework includes an example interface template. It is located in the `templates/python` directory. The name of the example interface template is `abc_if_config.py`. The template requires the following information: interface name, signals, transaction variables and configuration variables. The format of the interface template is given below. The items listed should be included in the interface configuration file in the order listed.

This line invokes a python shell .

```
#! /usr/bin/env python
```

This line imports the python code that creates the required data structures and generates the output files.

```
import uvmf_gen
```

This line creates the data structure used to create the interface files. The argument to the `InterfaceClass` function is the name of the interface. The name given will have `_pkg` appended to it to form the

```
package name.  
intf = uvmf_gen.InterfaceClass('abc')
```

The following lines show how to specify the clock and reset signal for the interface. These signals do not need to be added using the addPort function shown below.

```
intf.clock = 'paClk'  
intf.reset = 'paRst'
```

The addPort function is required for each signal in the interface. The arguments to the addPort identify the name, width and direction of the signal. The options for the direction are input, output and inout.

```
intf.addPort('abc_wdata',8,'input')  
intf.addPort('abc_addr',16,'input')  
intf.addPort('abc_rdata',8,'output')
```

The addHdlTypedef function is used to create typedefs that are synthesizable, used in the driver_bfm. The types are added to the correct file and can be used by transaction class variables and configuration class variables. The arguments to addHdlTypedef are name, type.

```
intf.addHdlTypedef('my_byte_t','byte')  
intf.addHdlTypedef('my_word_t','bit [15:0] ')  
intf.addHdlTypedef('colors_t','enum { red, green, blue, yellow, white,  
black }')
```

The addHvlTypedef function is used to create typedefs that are NOT synthesizable. These include class specializations. The types are added to the correct file and can be used by transaction class variables and configuration class variables. The arguments to addHvlTypedef are name, type.

```
intf.addHvlTypedef('my_object_t','uvm_object')
```

The addHdlParamDef function specifies parameters for inclusion in typedefs_hdl file:

```
addHdlParamDef(<name>,<type>,<value>)  
intf.addHdlParamDef('NUM_FILTERS','int','20')  
intf.addHdlParamDef('NUM_TAPS','int','12')
```

The addTransVar function is required for each variable needed by the transaction class. The variables in the transaction class reflect the untimed information used during a transfer on the bus. The arguments required by the addTransVar include the name of the variable, variable type and indication that this variable is to be randomized.

```
intf.addTransVar('abc_trnVar1','byte',isrand=False)  
intf.addTransVar('abc_trnVar2','int',isrand=True)  
intf.addTransVar('abc_trnVar3','bit [15:0]',isrand=False)
```

The addConfigVar function is required for each variable needed by the configuration class. The variables in the configuration class control the operation of the BFM within the limits of the protocol specification. An example of a configuration variable for the SPI protocol is whether the BFM uses the positive or negative edge of the clock. For this protocol option a variable named use_posedge can be created of type bit. This variable can be randomized to test designs that can operate on either edge of sclk.

```
intf.addConfigVar('abc_cfgVar1','bit',isrand=False)
intf.addConfigVar('abc_cfgVar2','int',isrand=True)
intf.addConfigVar('abc_cfgVar3','bit [3:0]',isrand=False)
```

The create function initiates the generation of all interface files in the correct location.

```
intf.create()
```

5.2 Steps for using the template

- 1) Set the environment variables as described above
- 2) Create the interface template file as described above
- 3) Execute the interface template
- 4) Use the list below to add protocol specific code to the new interface package.

5.3 Adding protocol specific code

The following list identifies areas where protocol specific code needs to be added to the new interface package. The following files listed assume the interface generated is named abc_pkg. The UVMF_CHANGE_ME string can be used to identify locations for code addition or changes within various files.

- 1) src/abc_transaction.svh: Add constraints for transaction variables that characterize valid values for these variables.
- 2) src/abc_configuration.svh: Add constraints for configuration variables that characterize valid values for these variables.
- 3) src/abc_driver_bfm.sv: Implement protocol driving in the provided do_write task. The entry point into the driver BFM is the access task. If needed, replace the do_write task with the task needed and call this task from the access task. Example tasks include do_read, do_burst, do_transfer, etc.
- 4) src/abc_monitor_bfm.sv: Implement protocol monitoring in the provided do_monitor task.
- 5) Add new sequences as needed. All new sequences should be extended from abc_sequence_base.

6 Developing an Environment Package using the Python Templates

6.1 Format and input required by the template

The UVM Framework includes an example environment template. It is located in the templates/python directory. The name of the example environment template is abc_prj_env_config.py. The template requires the following information: environment

name and agents contained in the environment. The format of the environment template is given below. The items listed should be included in the environment configuration file in the order listed.

This line invokes a python shell .

```
#! /usr/bin/env python
```

This line imports the python code that creates the required data structures and generates the output files.

```
import uvmf_gen
```

This line creates the data structure used to create the environment files. The argument to the EnvironmentClass function is the name of the environment. The name given will have _env_pkg appended to it to form the package name.

```
env = uvmf_gen.EnvironmentClass('abc_prj')
```

The addAgent function is required for each agent needed in the environment. The arguments to the addAgent function are the agent instance name and the agent type. The name given for the agent type should not include the _pkg that is used in the interface package name. In the example below four agents of the abc_pkg type will be added to this environment.

```
addAgent(<agent_handle_name>,<agent_type_name>,<clock_name>,<reset_name>)
env.addAgent('abc_in' , 'abc', 'paClk','paRst')
env.addAgent('abc_out' , 'abc', 'paClk','paRst')
env.addAgent('abc_ctrl','abc', 'paClk','paRst')
env.addAgent('abc_mm' , 'abc', 'paClk','paRst')
```

The create function initiates the generation of all interface files in the correct location.

```
env.create()
```

6.2 Steps for using the template

- 1) Set the environment variables as described above
- 2) Create the environment template file as described above
- 3) Execute the environment template
- 4) Use the list below to add DUT specific code to the new environment package.

6.3 Adding DUT specific code

The following list identifies areas where DUT specific code needs to be added to the new environment package. The following files listed assumes the environment generated is named abc_prj_env_pkg. The UVMF_CHANGE_ME string can be used to identify locations for code addition or changes within various files.

- 1) src/abc_prj_configuration.svh: Configure agents as required by the DUT.
- 2) src/abc_prj_environment.svh: Add prediction and scoreboarding as required by the data flow and checking needs of the DUT.

- 3) Add new sequences as needed in the src directory. All new sequences should be extended from abc_prj_sequence_base. Be sure to add new sequences to the environment package: abc_prj_env_pkg.sv

7 Developing a Project Bench using the Python Templates

7.1 Format and input required by the template

The UVM Framework includes an example project bench template. It is located in the templates/python directory. The name of the example bench template is abc_ben_config.py. The template requires the following information: bench name and agents contained in the environment used in the bench. The format of the bench template is given below. The items listed should be included in the bench configuration file in the order listed.

This line invokes a python shell .

```
#! /usr/bin/env python
```

This line imports the python code that creates the required data structures and generates the output files.

```
import uvmf_gen
```

This line creates the data structure used to create the bench files. The arguments to the BenchClass function are the name of the bench and the name of the environment. The name given for the environment will have _env_pkg appended to it to form the package name.

```
ben = uvmf_gen.BenchClass('abc_ben','abc_prj')
```

The addAgent function is required for each agent needed in the bench. The arguments to the addAgent function are the agent instance name and the agent type. The name given for the agent type should not include the _pkg that is used in the interface package name. In the example below four agents of the abc_pkg type will be added to this environment.

```
addAgent(<agent_handle_name>,<agent_type_name>,<clock_name>,<reset_name>)
ben.addAgent('abc_in' , 'abc', 'paClk','paRst')
ben.addAgent('abc_out' , 'abc', 'paClk','paRst')
ben.addAgent('abc_ctrl','abc', 'paClk','paRst')
ben.addAgent('abc_mm' , 'abc', 'paClk','paRst')
```

The create function initiates the generation of all interface files in the correct location.

```
ben.create()
```

7.2 Steps for using the template

- 1) Set the environment variables as described above

- 2) Create the bench template file as described above. It is important to note that the order of agents in the bench template must match the order of agents in the environment template for the environment this bench will instantiate.
- 3) Execute the bench template
- 4) Use the list below to add DUT specific code to the new bench.

7.3 Adding DUT specific code

The following list identifies areas where DUT specific code needs to be added to the new bench. The following files listed assumes the bench generated is named abc_ben. The UVMF_CHANGE_ME string can be used to identify locations for code addition or changes within various files.

- 1) abc_ben/tb/test bench/hdl_top.sv: Instantiate the DUT and connect ports to the signals in the interface busses, _bus.
- 2) Add new sequences as needed in the abc_ben/tb/sequences/src directory. All new sequences should be extended from abc_ben_sequence_base. Be sure to add new sequences to the environment package: tb/sequences/abc_ben_sequence_pkg.sv

7.4 Important Notes regarding environment and bench templates

It is important to note that the environment and bench templates are currently for generating block level environments and benches. The current environment template can be used to generate higher level environments if the addAgent function is used to identify sub environments. This requires some modification of the environments configuration class. The current bench template can be used to generate a bench for higher level environments. This requires careful thought regarding the agents added to the bench and distribution of interface identifiers throughout the environment.

It is also important to note that when generating a block level bench the list of agents should match the list used to create the block level environment package.

8 Resource Sharing within UVM Framework

8.1 Overview

The UVM Framework uses uvm_config_db as the mechanism for sharing resources within the test. The resources shared include virtual interface handles, sequencer handles and agent configuration handles. The information used to place resources into and retrieve resources from the uvm_config_db are listed in the resource table. The resource table is described in the following section.

It is important to note that the code listed below is automatically generated when using the python scripts to generate an interface package, environment package or project bench. The table below can be created from the python generated code for use by test writers.

The example table and code below is from the ahb2spi example.

8.2 The Resource Table

The resource table is used to collect all information required to access resources associated with an interface. The “Port Description” column is a listing and description of each interface in the design that is either actively driven or passively monitored. The “Port Type” column identifies the name of the BFM interfaces for the port. They are the declared name of the interface BFM. The “Transaction Type” column identifies the transaction type that is sent to the sequencer for that interface. The “Port Name” column lists a unique string variable for each interface listed. The “Port Name” variable must be unique from all other “Port Name” values in the column.

Port Description	Port Type	Transaction Type	Port Name
AHB Interface	ahb_monitor_bfm ahb_driver_bfm	ahb_transaction	“AHB_BFM”
WB Interface	wb_monitor_bfm	wb_transaction	“AHB2WB_WB_BFM”
WB Interface	wb_monitor_bfm	wb_transaction	“WB2SPI_WB_BFM”
SPI Interface	spi_monitor_bfm spi_driver_bfm	spi_transaction	“SPI_BFM”

8.3 Sharing and Accessing Environment Resources

8.3.1 Virtual Interface Handles

The resource table has the information needed to access virtual interface handles for the monitor BFM and driver BFM. The fields used are in red and green. The “Port Type” field is used in the uvm_config_db Type field. The scope for all virtual interface handles is ‘null, UVMF_VIRTUAL_INTERFACES’. This creates a generic scope for all virtual interface handles. The “Port Name” field is used for the uvm_config_db Field name variable. This provides a unique identifier to differentiate between multiple BFM entries of the same type.

Interface Resource Sharing – AHB2SPI Example

Port Description	Port Type	Transaction Type	Port Name
AHB Interface	ahb_monitor_bfm ahb_driver_bfm	ahb_transaction	"AHB_BFM"
WB Interface	wb_monitor_bfm	wb_transaction	"AHB2WB_WB_BFM"
WB Interface	wb_monitor_bfm	wb_transaction	"AHB2WB_WB_BFM"
SPI Interface	spi_monitor_bfm spi_driver_bfm	spi_transaction	"SPI_BFM"

- Top module places virtual interface into uvm_config_db
 - Type: `ahb_monitor_bfm` or `ahb_driver_bfm`
 - Scope: `null`, `UVMF_VIRTUAL_INTERFACES`
 - Field name: "`AHB_BFM`"
- To retrieve virtual interface from uvm_config_db
 - Type: `ahb_monitor_bfm` or `ahb_driver_bfm`
 - Scope: `null`, `UVMF_VIRTUAL_INTERFACES`
 - Field name: "`AHB_BFM`"

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The code for placing a virtual interface handle into the uvm_config_db is shown below. It is located in hdl_top.sv of the ahb2wb example project_bench.

```
94 initial begin // tbx vif_binding_block
95   import uvm_pkg::uvm_config_db;
96
97   uvm_config_db #( virtual ahb_monitor_bfm )::
98     set( null , UVMF_VIRTUAL_INTERFACES , AHB_BFM , ahb_mon_bfm );
99   uvm_config_db #( virtual ahb_driver_bfm )::
100    set( null , UVMF_VIRTUAL_INTERFACES , AHB_BFM , ahb_drv_bfm );
101
102  uvm_config_db #( virtual wb_monitor_bfm )::
103    set( null , UVMF_VIRTUAL_INTERFACES , AHB2WB_WB_BFM , ahb2wb_wb_mon_bfm );
104  uvm_config_db #( virtual wb_monitor_bfm )::
105    set( null , UVMF_VIRTUAL_INTERFACES , WB2SPI_WB_BFM , wb2spi_wb_mon_bfm );
106
107  uvm_config_db #( virtual spi_monitor_bfm )::
108    set( null , UVMF_VIRTUAL_INTERFACES , SPI_BFM , spi_mon_bfm );
109  uvm_config_db #( virtual spi_driver_bfm )::
110    set( null , UVMF_VIRTUAL_INTERFACES , SPI_BFM , spi_drv_bfm );
111
112 end
```

The retrieval of the virtual interface handle is located in the agent configuration. The code below is from uvmf_parameterized_agent_configuration_base.svh

```

106 virtual function void initialize(
107           uvmf_active_passive_t activity,
108           string agent_path,
109           string interface_name);
110   active_passive      = activity;
111   this.interface_name = interface_name;
112
113 // Checking the config_db
114 void'(uvm_config_db #(uvm_bitstream_t):::
115   get(null,interface_name,"enable_transaction_viewing",enable_transaction_viewing));
116
117 if( !uvm_config_db #( MONITOR_BFM_BIND_T )::
118   get( null , UVMF_VIRTUAL_INTERFACES , interface_name , monitor_bfm ) )
119   `uvm_error("Config Error" ,
120   $sformatf("uvm_config_db #( MONITOR_BFM_BIND_T )::get cannot find resource %s",interface_name) )
121
122 if ( activity == ACTIVE ) begin
123   if( !uvm_config_db #( DRIVER_BFM_BIND_T )::
124     get( null , UVMF_VIRTUAL_INTERFACES , interface_name , driver_bfm ) )
125     `uvm_error("Config Error" ,
126     $sformatf("uvm_config_db #( DRIVER_BFM_BIND_T )::get cannot find resource %s",interface_name) )
127 end
128
129 endfunction

```

8.3.2 Sequencer Handles

The resource table has the information needed to access sequencer handles in the simulation. The fields used are in red and green. The “Transaction Type” field is used in the uvm_config_db Type field. The scope for all virtual interface handles is ‘null, UVMF_SEQUENCERS’. This creates a generic scope for all sequencer handles. The “Port Name” field is used for the uvm_config_db Field name variable. This provides a unique identifier to differentiate between multiple sequencer entries of the same type.

Sequencer Resource Sharing – AHB2SPI Example

Port Description	Port Type	Transaction Type	Port Name
AHB Interface	ahb_monitor_bfm ahb_driver_bfm	ahb_transaction	"AHB_BFM"
WB Interface	wb_monitor_bfm	wb_transaction	"AHB2WB_WB_BFM"
WB Interface	wb_monitor_bfm	wb_transaction	"AHB2WB_WB_BFM"
SPI Interface	spi_monitor_bfm spi_driver_bfm	spi_transaction	"SPI_BFM"

- Agent places interface sequencer into uvm_config_db
 - Type: uvm_sequencer#(ahb_transaction)
 - Scope: null , UVMF_SEQUENCERS
 - Field name: "AHB_BFM"
- To retrieve sequencer from uvm_config_db
 - Type: uvm_sequencer#(ahb_transaction)
 - Scope: null , UVMF_SEQUENCERS
 - Field name: "AHB_BFM"

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The code for placing a sequencer handle into the uvm_config_db is shown below. It is located in uvmf_parameterized_agent.svh.

```
136     uvm_config_db #( sequencer_t )::  
137         set( null , UVMF_SEQUENCERS , configuration.interface_name, sequencer );  
138         driver = DRIVER_T::type_id::create({agent_name,"_driver"},this);
```

The retrieval of the sequencer handle is located in the top level sequence. The code below is from ahb2spi_sequence_base.svh

```
60     if( !uvm_config_db #( uvm_sequencer #(ahb_transaction) )::  
61         get( null , UVMF_SEQUENCERS , AHB_BFM , ahb_sequencer ) )  
62         `uvm_error("Config Error",  
63             "uvm_config_db #( uvm_sequencer #(ahb_transaction) )::get cannot find resource ahb_sequ  
64     if( !uvm_config_db #( uvm_sequencer #(spi_transaction) )::  
65         get( null , UVMF_SEQUENCERS , SPI_BFM , spi_sequencer ) )  
66         `uvm_error("Config Error",  
67             "uvm_config_db #( uvm_sequencer #(spi_transaction) )::get cannot find resource spi_sequ
```

8.3.3 Agent Configuration Handles

The agent configuration can be retrieved from the uvm_config_db using the same value from the "Port Name" column of the resource table. The scope for all agent configurations is 'null, UVMF_CONFIGURATIONS'. The code below is from

ahb_configuration.svh. The configuration places itself in the uvm_config_db using the interface name variable in line 82.

```
74 // ****
75 virtual function void initialize(uvmf_active_passive_t activity,
76                               string agent_path,
77                               string interface_name);
78
79     super.initialize( activity, agent_path, interface_name );
80
81     uvm_config_db #( ahb_configuration )::set( null ,agent_path,      UVMF_AGENT_CONFIG, this );
82     uvm_config_db #( ahb_configuration )::set( null ,UVMF_CONFIGURATIONS, interface_name, this );
83
84 endfunction
```

The code below is from ahb2spi_sequence_base.svh. The ahb agents configuration class is retrieved from uvm_config_db in lines 69-70.

```
69 if( !uvm_config_db #( ahb_configuration )::
70     get( null ,UVMF_CONFIGURATIONS, AHB_BFM, ahb_config ) )
71     `uvm_error("Config Error" ,
72             "uvm_config_db #( ahb_configuration )::get cannot find resource ahb_config" )
```

8.4 Turning on transaction viewing for selected interfaces

The resource table can be used to enable transaction viewing for selected interfaces without recompilation of batch mode simulations. The “Port Name” field of the resource table is used to enable transaction viewing for a single, group or all interfaces. Use the UVM command line processing line shown below as an example. The plusarg is added to the vsim command.

Enabling Interface Transaction Viewing

Port Description	Port Type	Transaction Type	Port Name
AHB Interface	ahb_monitor_bfm ahb_driver_bfm	ahb_transaction	" AHB_BFM "
WB Interface	wb_monitor_bfm	wb_transaction	" AHB2WB_WB_BFM "
WB Interface	wb_monitor_bfm	wb_transaction	" AHB2WB_WB_BFM "
SPI Interface	spi_monitor_bfm spi_driver_bfm	spi_transaction	" SPI_BFM "

— Use the UVM Command Line Interface to turn on transaction viewing for:

- A selected interface:
`+uvm_set_config_int="AHB_BFM",enable_transaction_viewing,1`
- Interface groups:
`+uvm_set_config_int="AHB2*",enable_transaction_viewing,1`
- All interfaces:
`+uvm_set_config_int=*,enable_transaction_viewing,1`

9 Environment and Interface Initialization within the UVM Framework

9.1 Overview

The UVM Framework is architected for reuse. One key characteristic of reuse is self-containment. Reusable components automatically get needed resources, construct and configure children components and make internal resources available to other components. The two mechanisms for applying this are the initialize function and set_config function.

The initialize function passes information down through the configuration object hierarchy. This information configures environments and agents in a simulation. It begins at the top level UVM test and ends at agent configurations. It is the mechanism by which all agents are initialized.

The set_config function passes configuration object handles down through the environment hierarchy.

It is important to note that the code listed below is automatically generated when using the python scripts to generate an interface package, environment package or project bench.

9.2 Top-down initialization through the initialize function

The initialize function passes information down through the configuration hierarchy. It starts at the top level UVM test and ends at the agent configurations. The configuration class for each agent in a simulation is initialized using this mechanism. At the top level UVM test and environment level the initialize function passes the following information: simulation level, hierarchical path down to the configurations environment and an array of string names that uniquely identify each interface in the design. At the agent level the initialize function passes the following information: active/passive state of the agent, hierarchical path to the configurations agent and unique string identifying the agents handle to the interface BFM (driver BFM and monitor BFM).

The following initialize flow is from the ahb2wb example.

The code below is from test_top.svh. Keep in mind that the build_phase function of this component completes before the environment build_function is executed. This allows for the configurations to be constructed and initialized before the environment hierarchy is constructed.

This function performs the following flow.

Line 55: Create an array of strings that contains the unique names of each interface BFM in the simulation.

Line 57: Pass the simulation level, BLOCK, path to the environment, uvm_test_top.environment, and the array of interface identifiers to the environments configuration object using the initialize function.

```
53 // ****
54 virtual function void build_phase(uvm_phase phase);
55   string interface_names[] = {AHB_BFM, WB_BFM} ;
56   super.build_phase(phase);
57   configuration.initialize(BLOCK, "uvm_test_top.environment", interface_names );
58 endfunction
```

The code below is from ahb2wb_configuration.svh. It is executed by test_top.svh. It is passed the simulation level, BLOCK, the hierarchy down to the environment, "uvm_test_top.environment", and the array of interface names. Additional optional argument to this function, register_model, is for block to top use of a UVM register model. Additional optional argument to this function, interface_activity, is for setting agent active/passive state from test_top.

This function performs the following flow:

Line 66: This conditional is true if the simulation is a block level simulation.

Lines 67-68: The agents active/passive state are both set to active since the simulation is block level. This is because both inputs, ahb and wb, are primary inputs to the DUT at this simulation level and must be driven by the driver BFM. The environment path is appended with the agent name within the environment to create a full path to the agent. This identifies to the configuration the path to its agent. The string names are distributed to the agents in the environment. The configuration for the ahb agent gets the first string. The configuration for the wishbone agent gets the second string.

Line 69: This conditional is true if the simulation is a chip level simulation.

Lines 70-71: The activity state for the ahb agent is active since at chip level simulation the ahb is a primary input to the DUT. The activity state for the wishbone agent is passive since at the chip level simulation the wishbone interface is not a primary input to the dut. The wishbone interface is driven by adjacent RTL. Therefore, no driver BFM is required to stimulate this port. The environment path is appended with the agent name within the environment to create a full path to the agent. This identifies to the configuration the path to its agent. The string names are distributed to the agents in the environment. The configuration for the ahb agent gets the first string. The configuration for the wishbone agent gets the second string.

Line 72: This conditional is true if the simulation is a system level simulation.

Lines 73-74: The activity state for the ahb agent is passive since at the system level simulation the ahb interface is not a primary input to the dut. The ahb interface is driven by adjacent RTL. The activity state for the wishbone agent is passive since at the system level simulation the wishbone interface is not a primary input to the dut. The wishbone interface is driven by adjacent RTL. Therefore, no driver BFM is required to stimulate this port. The environment path is appended with the agent name within the environment to create a full path to the agent. This identifies to the configuration the path to its agent. The string names are distributed to the agents in the environment. The configuration for the ahb agent gets the first string. The configuration for the wishbone agent gets the second string.

Lines 75-76: Generate an error if an unknown sim_level value is passed to this function.

```

59 // ****
60 function void initialize(uvmf_sim_level_t sim_level,
61                         string environment_path,
62                         string interface_names [],
63                         uvm_reg_block register_model = null,
64                         uvmf_active_passive_t interface_activity[] = null);
65
66   if ( sim_level == BLOCK ) begin
67     ahb_config.initialize( ACTIVE, {environment_path,".a_agent"}, interface_names[0]);
68     wb_config.initialize ( ACTIVE, {environment_path,".b_agent"}, interface_names[1]);
69   end else if ( sim_level == CHIP ) begin
70     ahb_config.initialize( ACTIVE, {environment_path,".a_agent"}, interface_names[0]);
71     wb_config.initialize ( PASSIVE,{environment_path,".b_agent"}, interface_names[1]);
72   end else if ( sim_level == SYSTEM ) begin
73     ahb_config.initialize( PASSIVE, {environment_path,".a_agent"}, interface_names[0]);
74     wb_config.initialize ( PASSIVE, {environment_path,".b_agent"}, interface_names[1]);
75   end else begin
76     `uvm_fatal("CONFIGURATION", "Unknown sim_level in ahb2wb_configuration::set_activity()")
77   end
78 endfunction

```

The code below is from ahb_configuration.svh. It is executed by ahb2wb_configuration.svh. It is passed the active/passive state, the hierarchy down to the agent, “uvm_test_top.environment.a_agent”, and the interface name.

This function performs the following flow:

Line 79: Call to super.initialize to execute the initialize function in uvmf_parameterized_agent_configuration_base.svh. The flow of this function is described in the next code section.

Line 81: This configuration object places itself in the uvm_config_db for the agent identified by agent_path to retrieve.

Line 82: This configuration object places itself in the uvm_config_db using the string that identifies the interface BFM used for this agent. This creates an automatic association between an interface and its configuration.

```

74 // ****
75 virtual function void initialize(uvmf_active_passive_t activity,
76                                 string agent_path,
77                                 string interface_name);
78
79   super.initialize( activity, agent_path, interface_name );
80
81   uvm_config_db #( ahb_configuration )::set( null ,agent_path,      UVMF_AGENT_CONFIG, this );
82   uvm_config_db #( ahb_configuration )::set( null ,UVMF_CONFIGURATIONS, interface_name, this );
83
84 endfunction

```

The code below is from uvmf_parameterized_agent_configuration_base.svh. It is executed by ahb_configuration.svh. It is passed the active/passive state, the hierarchy down to the agent, “uvm_test_top.environment.a_agent”, and the interface name.

This function performs the following flow:

Lines 110-111: Set the local activity level and interface string name variables from the arguments to the function call.

Lines 114-115: Check the uvm_config_db for command line setting of the enable_transaction_viewing flag for this interface.

Lines 117-120: Retrieve the handle to the monitor BFM. Generate an error if the get function fails.

Lines 122-126: If the agent is configured as active then retrieve the handle to the driver BFM. Generate an error if the get function fails.

```
106 virtual function void initialize(
107                                     uvmf_active_passive_t activity,
108                                     string agent_path,
109                                     string interface_name);
110   active_passive      = activity;
111   this.interface_name = interface_name;
112
113 // Checking the config_db
114 void'(uvm_config_db #(uvm_bitstream_t):::
115     get(null,interface_name,"enable_transaction_viewing",enable_transaction_viewing));
116
117 if( !uvm_config_db #( MONITOR_BFM_BIND_T )::
118     get( null , UVMF_VIRTUAL_INTERFACES , interface_name , monitor_bfm ) )
119     `uvm_error("Config Error",
120               $sformatf("uvm_config_db #( MONITOR_BFM_BIND_T )::get cannot find resource %s",interface_name) )
121
122 if( activity == ACTIVE ) begin
123   if( !uvm_config_db #( DRIVER_BFM_BIND_T )::
124     get( null , UVMF_VIRTUAL_INTERFACES , interface_name , driver_bfm ) )
125     `uvm_error("Config Error",
126               $sformatf("uvm_config_db #( DRIVER_BFM_BIND_T )::get cannot find resource %s",interface_name) )
127 end
128
129 endfunction
```

9.3 Top-down passing of environment configuration through the set_config function.

All environments should be extended from the uvmf_environment_base. The set_config function from this class is shown below. This function is used by test_top and all lower environments to pass in the environments configuration handle.

```
49 // FUNCTION : set_config
50 function void set_config( CONFIG_T cfg );
51   configuration = cfg;
52 endfunction
```

The following set_config flow is from the ahb2spi example.

The code below is from uvmf_test_base.svh. This call is made in the build_phase and happens automatically for any test_top derived from uvmf_test_base. This call is performed on the top level environment. If the environment is not a block level, i.e. chip level or above, then the set_config for lower level environments must be done by the top level environment as shown in the next code example.

```
93     environment.set_config(configuration);
```

The code below is from ahb2spi_environment.svh. The build phase of this chip level environment uses set_config to pass configuration handles into lower level environments.

This function performs the following flow:

Line 59: Construct the ahb2wb environment.

Line 60: Pass the ahb2wb_config handle into the ahb2wb environment using set_config.

Line 62: Construct the wb2spi environment.

Line 63: Pass the wb2spi_config handle into the wb2spi environment using set_config.

```
55 // ****
56 virtual function void build_phase(uvm_phase phase);
57     super.build_phase(phase);
58
59     ahb2wb_env = ahb2wb_environment::type_id::create("ahb2wb_env",this);
60     ahb2wb_env.set_config( configuration.ahb2wb_config );
61
62     wb2spi_env = wb2spi_environment::type_id::create("wb2spi_env",this);
63     wb2spi_env.set_config( configuration.wb2spi_config );
64
65 endfunction
```

10 Enabling Transaction Viewing within the UVM Framework

10.1 Overview

The code that is responsible for transaction viewing in the waveform viewer is in three locations: agent configuration, agent monitor and transaction class. The agent configuration contains a variable that turns transaction viewing on and off. The agent monitor creates the transaction viewing stream and calls the function in the transaction class that adds the transaction to the stream. The transaction class adds itself to the transaction stream.

10.2 UVM Framework transaction viewing flow

10.2.1 Creating a transaction stream

The transaction stream is a handle to which all transactions to be viewed are added. This stream is created in the monitor extended from the uvmf_monitor_base. The following code in uvmf_monitor_base creates the stream.

```

// FUNCTION: start_of_simulation_phase
virtual function void start_of_simulation_phase(uvm_phase phase);
  if (configuration.enable_transaction_viewing)
    transaction_viewing_stream = $create_transaction_stream({.."get_full_name()",".", "txn_stream"});
endfunction

```

The stream is automatically created in the start_of_simulation_phase and is conditional on the enable_transaction_viewing flag in the agent configuration. The name of the stream is the full hierarchical path to the monitor with ".txn_stream" appended. This stream can be found in the Questa object window when viewing objects within the monitor.

10.2.2 Adding a transaction to the stream

Transactions to be viewed in the waveform viewer must be added to a transaction stream. The function that adds a transaction is located in the transaction class. The following code from the run_phase of the uvmf_monitor_base calls the add_to_wave function of the transaction class. The add_to_wave function adds the trans class to the transaction stream.

```

if ( configuration.enable_transaction_viewing )
  trans.add_to_wave(transaction_viewing_stream);

```

The add_to_wave function of the wb_transaction class of the wb_pkg is shown below.

```

56 //*****+
57 virtual function void add_to_wave(int transaction_viewing_stream_h);
58   if ( transaction_view_h == 0)
59     transaction_view_h = $begin_transaction(transaction_viewing_stream_h,op.name(),start_time);
60   if ( op == WB_RESET ) $add_color( transaction_view_h, "red" );
61   else if ( op == WB_WRITE ) $add_color( transaction_view_h, "blue" );
62   else if ( op == WB_READ ) $add_color( transaction_view_h, "green" );
63   super.add_to_wave(transaction_view_h);
64   $add_attribute(transaction_view_h, op, "op");
65   $add_attribute(transaction_view_h, addr, "addr");
66   $add_attribute(transaction_view_h, data, "data");
67   $add_attribute(transaction_view_h, byte_select, "byte_select");
68   $end_transaction(transaction_view_h,end_time);
69   $free_transaction(transaction_view_h);
70 endfunction

```

The following is a description of the operations performed by the add_to_wave function:

Lines 58-59: The transaction_view_h is a handle to the transaction viewing object for this transaction within the transaction stream. Each transaction in the stream has a unique transaction viewing handle. If the handle is null then a new handle is generated using the begin_transaction system call. The start_time argument of the begin_transaction call determines the start time of the transaction in the waveform viewer.

Lines 60-62: These lines set the color of the transaction within the waveform viewer based on the transaction operation type.

Line 63: This line executes the add_to_wave function in the base class. It adds variables in the base class, uvmf_transaction_base, to the waveform viewer.

Lines 64-67: The add_attribute system function adds transaction variables to the waveform viewer. The second argument is the data variable to be added. The third argument identifies the variable value.

Line 68: The end_transaction system function call sets the end time of the transaction in the waveform viewer.

Line 69: The free_transaction system function call closes the transaction viewing handle on the stream and completes the process of adding the transaction.

10.3 Switches for enabling transaction viewing

10.3.1 UVM Reporting Detail setting

The UVM recording detail of the simulation can be set in either of the two mechanisms listed below:

Add the following line to the UVM test case in any phase prior to and including the run_phase:

```
set_config_int("*","recording_detail",UVM_FULL);
```

Add the following line to the vsim command line:

```
+uvm_set_config_int=*,recording_detail,UVM_FULL
```

10.3.2 Command line switches

```
-uvmcontrol=all -msgmode both  
+uvm_set_config_int=*,enable_transaction_viewing,1
```

10.3.3 Adding transaction viewing stream to the waveform viewer

The line below adds the transaction viewing stream, txn_stream, in the wishbone agent monitor component with the hierarchical path listed. The transaction stream of any UVMF based monitor can be added to the waveform in the same manner.

```
add wave -noupdate /uvm_root/uvm_test_top/environment/wb_agent/wb_agent_monitor/txn_stream
```

11 Creating the Top Level Modules

11.1.1 Hdl_top

The module named hdl_top, located in tb/test bench directory, contains the signal bundle interfaces, interface BFM s and DUT. It also includes the uvm_config_db::set calls to pass virtual interface handles to the UVM. The UVMF uses a two top architecture, hdl_top and hvl_top, to support emulation. Hdl_top is synthesized into the emulator. Hvl_top is run on the host simulator.

11.1.1.1 Instantiating Interfaces

A UVMF interface is divided into three pieces; the signal bundle, monitor BFM and driver BFM. Each instance of a protocol interface requires an instantiation of the signal bundle and monitor BFM. Each active instance of a protocol interface requires the instantiation of a driver BFM. The following code is from the instantiation of the interfaces in hdl_top from the ALU example.

```
48  alu_out_if      alu_out_bus(.clk(),.rst(),.done(),.result());
49  alu_out_monitor_bfm alu_out_mon_bfm(alu_out_bus);
50  alu_out_driver_bfm alu_out_drv_bfm(alu_out_bus);
51
52  alu_in_if       alu_in_bus(.clk(),.rst(),.valid(),.ready(),.op(),.a(),.b());
53  alu_in_monitor_bfm alu_in_mon_bfm(alu_in_bus);
54  alu_in_driver_bfm alu_in_drv_bfm(alu_in_bus);
```

Lines 48 and 52 instantiate the alu_in_if and alu_out_if signal bundles respectively. Lines 49 and 53 instantiate the alu_in_if and alu_out_if monitor BFM s. Lines 50 and 54 instantiate the alu_in_if and alu_out_if driver BFM s. The monitor and driver BFM port lists require a reference to the signal bundle. This allows the monitor BFM to observe signals in the signal bundle and the driver BFM to drive signals in the signal bundle.

11.1.1.2 Instantiating a Verilog DUT

A verilog DUT is instantiated using the following format. The code is from the instantiation of the DUT in hdl_top from the ALU example.

```
59  alu #(.OP_WIDTH(8), .RESULT_WIDTH(16)) DUT (
60    .clk  (alu_in_bus.clk) ,
61    .rst  (alu_in_bus.rst) ,
62    .ready (alu_in_bus.ready) ,
63    .valid (alu_in_bus.valid) ,
64    .op    (alu_in_bus.op) ,
65    .a     (alu_in_bus.a) ,
66    .b     (alu_in_bus.b) ,
67    .done  (alu_out_bus.done) ,
68    .result (alu_out_bus.result) );
```

Line 59 defines the module type, alu, and instance name, DUT. Parameters for the module are defined in the parenthesis following the #. Lines 60 through 68 list the ports of the alu module. The parenthesis following each port name identify the signal to be connected to the port. For each port connection the interface signal bundle and signal within the signal bundle is identified using hierarchical notation.

11.1.1.3 Instantiating a VHDL DUT

The format for instantiating a VHDL DUT is identical to instantiating a verilog DUT with the exception of line 59. In line 59 the work library, VHDL entity and VHDL architecture must be specified. The following line replaces line 59:

```
\workLib.entity(architecture) #(.OP_WIDTH(8), .RESULT_WIDTH(16)) DUT (
```

11.1.2 Hvl_top

The module named hvl_top, located in tb/test bench directory, imports the test package and contains the call to run_test which executes the UVM phases. The UVMF uses a two top architecture, hdl_top and hvl_top, to support emulation. Hdl_top is synthesized into the emulator. Hvl_top is run on the host simulator.

The code below is from hvl_top from the ALU example.

```
41 import uvm_pkg::*;
42 import alu_test_pkg::*;
43
44 module hvl_top;
45
46   initial run_test();
47
48 endmodule
```

Line 42 imports the alu test package which contains all alu tests. The call to run_test in line 46 starts execution of all UVM phases.

12 Creating Test Scenarios

12.1 Overview

A test scenario is a series of stimulus used to configure and stimulate the design. A test scenario can be created by writing a new test, a new sequence or both. If the desired stimulus does not exist in a sequence package then a new sequence must be created. The new sequence can be selected using either a new test or using the UVM command line processor. This section describes the creation of a new sequence, creation of a new test and how to select the sequence using either the new test or the UVM command line processor.

12.2 Creating a New Sequence

12.2.1 Creating a New Interface Sequence

If a bus operation needs to be created that is protocol specific and not design specific then a new interface sequence should be created. The new sequence should be extended from the _sequence_base class located in the interface package. The new sequence should be added to the interface package. The steps below describe how to create a new interface sequence and add the sequence to the package. It assumes the name of the interface package is abc_pkg and that the name of the new sequence is new_sequence.

- 1) In the abc_pkg/src folder create a file named new_sequence.svh
- 2) In new_sequence.svh add a class that extends abc_sequence_base. At a minimum this sequence should contain a factory registration macro and constructor.
- 3) Add the desired behavior to this sequence.
- 4) Include the new sequence in abc_pkg.sv after the inclusion of abc_sequence_base.svh

12.2.2 Creating a New Environment Sequence

If a sequence needs to be created that is design specific and may be reused at block and chip level simulation then a new environment sequence should be created. The new sequence should be extended from the _sequence_base class located in the environment package. The new sequence should be added to the environment package. The steps below describe how to create a new environment sequence and add the sequence to the package. It assumes the name of the environment package is abc_env_pkg and that the name of the new sequence is new_sequence.

- 1) In the abc_env_pkg/src folder create a file named new_sequence.svh
- 2) In new_sequence.svh add a class that extends abc_env_sequence_base. At a minimum this sequence should contain a factory registration macro and constructor.
- 3) Add the desired behavior to this sequence.
- 4) Include the new sequence in abc_env_pkg.sv after the inclusion of abc_env_sequence_base.svh

12.2.3 Creating a New Top Level Sequence

The top level sequence controls the flow and order of all lower level sequences. If a sequence needs to be created that is design specific and will not be reused at block and chip level simulation then a new top level sequence should be created. The new sequence should be extended from the _sequence_base class located in the sequence package of the bench. The new sequence should be added to the sequence package. The steps below describe how to create a new top level sequence and add the sequence to the package. It assumes the name of the bench sequence package is abc2def_sequences_pkg and that the name of the new sequence is new_sequence.

- 1) In the tb/sequences/abc2def_sequences/src folder create a file named new_sequence.svh
- 2) In new_sequence.svh add a class that extends abc2def_sequence_base. At a minimum this sequence should contain a factory registration macro and constructor.
- 3) Add the desired behavior to this sequence.
- 4) Include the new sequence in abc2def_sequences_pkg.sv after the inclusion of abc2def_sequence_base.svh

12.3 Creating a New Test

All UVMF test packages have a test named test_top. This test contains the top level configuration, top level environment and top level sequence. Test_top constructs and

connects the components. It also starts the sequence identified in the class definition of test_top. A new test case is created by extending test_top. The steps below describe how to create a new test class. It assumes the name of the test package is abc2def_test_pkg and the name of the new test is new_test. Each example in UVMF has an example derived test named example_derived_test.

- 1) In the tb/tests/src folder create a new file named new_test.svh
- 2) In new_test.svh add a class that extends test_top. At a minimum this test should contain a factory registration macro, constructor and build_phase function.
- 3) Add the desired factory overrides to this sequence in the build_phase. The factory overrides should be prior to super.build_phase(phase).
- 4) Include the new test in abc2def_test_pkg.sv after the inclusion of test_top.svh

12.4 Selecting a New Test Scenario using the UVM Factory

12.4.1 Using a New Test Class

The TEST_NAME makefile variable is used to select the test. This variable is used to set the UVM_TESTNAME command line variable. The default value for the TEST_NAME variable is test_top. To select another test add TEST_NAME=new_test to the make command line.

12.4.2 Using the UVM Command Line Processor

The UVM command line processor can be used to override any class or object within the simulation. This includes overriding sequences. To select a new test scenario by performing an override using the UVM command line processor add the following to the vsim command line:

```
+uvm_set_type_override=requested_type_class_name,override_type_class_name
```

13 Adding agents to an existing UVMF bench and environment

13.1 Adding a UVMF based agent

When adding a UVMF based agent to an existing UVMF based bench and environment the following files must be modified.

13.1.1 Bench modifications

13.1.1.1 Parameters package

The parameters package under the tb/parameters directory contains the unique strings used to identify interface resources within the uvm_config_db. Add a new parameter for a new unique string that will be used to identify the new interface.

13.1.1.2 HDL top

The hdl_top.sv module under the tb/testbench directory instantiates the interface signal bundle, monitor BFM and driver BFM. It also places the BFM's into the uvm_config_db for retrieval by agent configurations. Instantiate the signal bundle, monitor BFM and driver BFM for the new interface. Add the uvm_config_db::set call for the BFM's using the parameter defined in the parameters package as the field_name argument of the set call.

13.1.1.3 Test top

The test_top class under tb/tests/src passes the string identifiers for the interfaces to the environments configuration class through the initialize call of the configuration (Line 57 in the code example below). This is done through the string array named interface_names. Add the parameter, defined in the parameters package, to the end of this array by adding it to the end of the declaration in line 55.

```
40▼ class test_top extends uvmf_test_base #(  
41    .CONFIG_T(ahb2wb_configuration),  
42    .ENV_T(ahb2wb_environment),  
43    .TOP_LEVEL_SEQ_T(ahb2wb_sequence_base)  
44▼ );  
45  
46  `uvm_component_utils( test_top );  
47  
48▼ // ****  
49  function new( string name = "", uvm_component parent = null );  
50    super.new( name ,parent );  
51  endfunction  
52  
53▼ // ****  
54  virtual function void build_phase(uvm_phase phase);  
55    string interface_names[] = {AHB_BFM, WB_BFM} ;  
56    super.build_phase(phase);  
57    configuration.initialize(BLOCK, "uvm_test_top.environment", interface_names );  
58  endfunction  
59  
60 endclass
```

Be sure to add an import of the interface package to the test package declaration in tb/tests.

13.1.1.4 Sequence package

The following code must be added to the virtual sequence base located in the tb/sequences/src directory.

Add a handle to the agent sequencer. Example code is provided below.

```
uvm_sequencer #(wb_transaction ) wb_sequencer;
```

In the constructor add the uvm_config_db::get call to retrieve the sequencer handle. Example code is provided below.

```
if( !uvm_config_db #( uvm_sequencer #(ahb_transaction ))::get(null,UVMFSEQUENCERS , AHB_BFM , ahb_sequencer )
`uvm_error("Config Error","uvm_config_db #( uvm_sequencer #(ahb_transaction ))::get cannot find resource ahb_sequencer")
```

Add a handle to the agent configuration. Example code is provided below.

```
wb_configuration wb_config;
```

In the constructor add the uvm_config_db::get call to retrieve the configuration handle. Example code is provided below.

```
if( !uvm_config_db #( wb_configuration )::get( null ,UVMFCONFIGURATIONS , WB_BFM , wb_config ) )
`uvm_error("Config Error" , "uvm_config_db #( wb_configuration )::get cannot find resource wb_config")
```

Instantiate, construct and start interface sequences as needed.

Be sure to add an import of the interface package to the sequence package declaration located in tb/tests.

13.1.2 Environment modifications

13.1.2.1 Configuration

Instantiate a configuration class for the agent. Example code is provided below.

```
wb_configuration wb_config;
```

Construct the agent configuration in the constructor of the environment configuration. Be sure the string name given to the create call matches the instance name of the configuration. Example code is provided below.

```
49 |     wb_config = wb_configuration::type_id::create("wb_config");
```

The environment configuration initializes agent configurations. This is done through the initialize call on each agent configuration. One argument to the initialize function of the agent configuration is the string identifier of the interface. The entries of the interface_names array are distributed among the agents. Each agent receives the string identifier for the interface handle that agent will use. Be sure each agent receives the correct identifier as defined when the interface_names array was initialized in test_top.svh.

The second argument to an agent configurations initialize call defines the hierarchical path to the agent. This is used to make the agent configuration available to the agent through the uvm_config_db. The full path is created by concatenating the path down to the environment, provided by the environment_path variable, to the string name of the agent. The string name used here must match the string name given to the agent in the construction of the agent. Construction of the agent is described in the next section.

```

60▼  function void initialize(uvmf_sim_level_t sim_level,
61                      string environment_path,
62                      string interface_names [],
63                      uvm_reg_block register_model = null,
64                      uvmf_active_passive_t interface_activity[] = null);
65
66▼  if ( sim_level == BLOCK ) begin
67    ahb_config.initialize( ACTIVE, {environment_path,".a_agent"}, interface_names[0]);
68    wb_config.initialize ( ACTIVE, {environment_path,".b_agent"}, interface_names[1]);
69▼  end else if ( sim_level == CHIP ) begin
70    ahb_config.initialize( ACTIVE, {environment_path,".a_agent"}, interface_names[0]);
71    wb_config.initialize ( PASSIVE,{environment_path,".b_agent"}, interface_names[1]);
72▼  end else if ( sim_level == SYSTEM ) begin
73    ahb_config.initialize( PASSIVE, {environment_path,".a_agent"}, interface_names[0]);
74    wb_config.initialize ( PASSIVE, {environment_path,".b_agent"}, interface_names[1]);
75  end else begin
76    `uvm_fatal("CONFIGURATION", "Unknown sim_level in ahb2wb_configuration::set_activity()")
77  end
78 endfunction

```

Be sure to add an import of the interface package to the environment package declaration located in verification_ip/environment_packages.

13.1.2.2 Environment

Agents are instantiated in the environment. Instantiate the new agent in the environment file located in the verification_ip/environment_packages directory. Example code is provided below.

45 **wb_agent_t wb_agent;**

Construct the agent in the environments build_phase. Example code is provided below.

70 **wb_agent = wb_agent_t::type_id::create("wb_agent",this);**

Connect the agent to other components as required. The example code below connects the wb_agent to the predictor.

```
92     wb_agent.monitored_ap.connect(wb2spi_predictor.analysis_export);
```

Be sure to add an import of the interface package to the environment package declaration located in verification_ip/environment_packages.

13.2 Adding a QVIP agent

There are four major components for each QVIP protocol. They are the agent, configuration, sequence and interface. The sections below describe where each of these constituent pieces are placed within a UVMF bench and environment. The component names are different for each protocol. Partial or descriptive names will be used to identify components. The example below will cover the steps required to add QVIP from examples within the QVIP installation into a UVMF bench and environment.

13.2.1 Agent

The agent has a _agent suffix and is typically located in env.svh within the QVIP install example. The agent must be instantiated and constructed in the environment located under verification_ip/environment_packages. Each agent has a handle to its configuration. The name of this handle is cfg. This handle can be directly assigned from the agent configuration within the environment configuration. For example code from the environment illustrates the assignment:

```
function void env::build_phase(uvm_phase phase);  
  
    env_cfg = env_config_t::get_config(this);  
    master = axi_agent_t::type_id::create("master", this);  
    slave = axi_agent_t::type_id::create("slave", this);  
  
    master.cfg = env_cfg.master;  
    slave.cfg = env_cfg.slave;  
  
endfunction
```

13.2.2 Configuration

The agent configuration has a _vip_config suffix and is typically located in env_config.svh within the QVIP install example. The agent configuration must be instantiated and constructed in the environment configuration located under verification_ip/environment_packages.

The agent configuration has various assignments and function calls that are used to configure the agent. This code is typically located in test.svh within the QVIP install example. This code must be moved into the environment configuration and executed after the agent configuration is constructed.

The generic package, mvc_pkg, and protocol specific package, mgc_..., must be imported in the environment package located under verification_ip/environment_packages.

13.2.3 Sequence

13.2.4 Interface

14 Appendix A: UVM classes used within UVMF

14.1 Overview

14.2 UVM Component Classes Used

uvm_test, uvm_env, uvm_agent, uvm_sequencer, uvm_driver, uvm_monitor, uvm_subscriber, uvm_scoreboard, uvm_analysis_port, uvm_port_component_base, uvm_port_list, uvm_report_server, uvm_reg_predictor

14.3 UVM Data Classes Used

uvm_object, uvm_sequence_item, uvm_sequence, uvm_tlm_analysis_fifo

14.4 UVM Phases Used

Build_phase, Connect_phase, End_of_elaboration_phase, Start_of_simulation_phase, Run_phase, Extract_phase, Check_phase, Report_phase

14.5 UVM Macros Used

uvm_component_utils, uvm_component_param_utils, uvm_object_utils, uvm_object_param_utils, uvm_info, uvm_warning, uvm_error, uvm_fatal, uvm_analysis_imp_decl

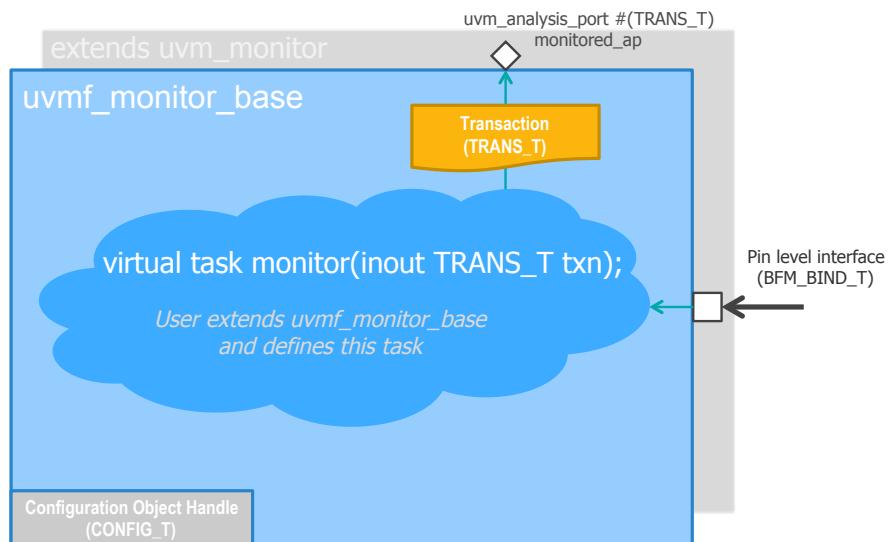
14.6 Miscellaneous UVM Features Used

Uvm_config_db, UVM factory, Phase_ready_to_end, Raise_objection, Drop_objection

15 Appendix B: UVMF Base Package Block Diagrams

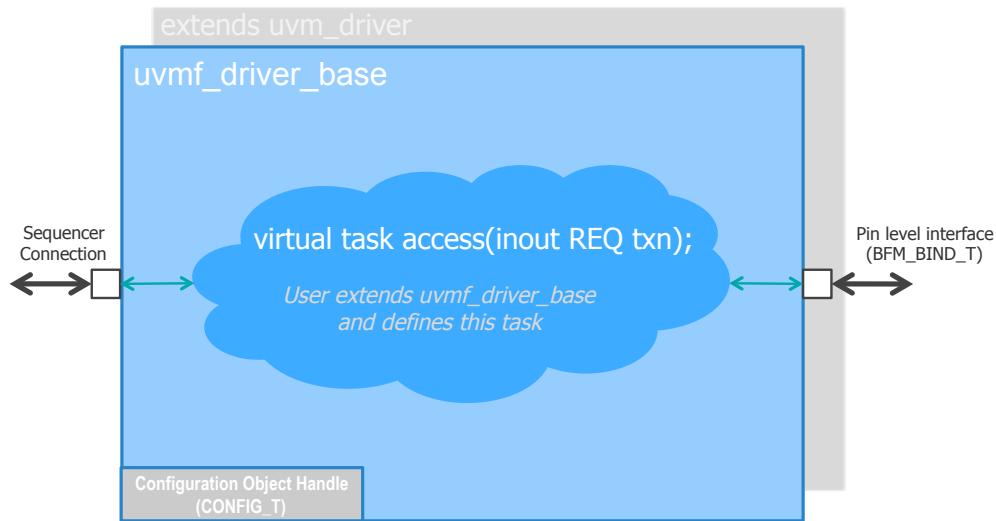
15.1 Monitor Base

UVMF Monitor Base



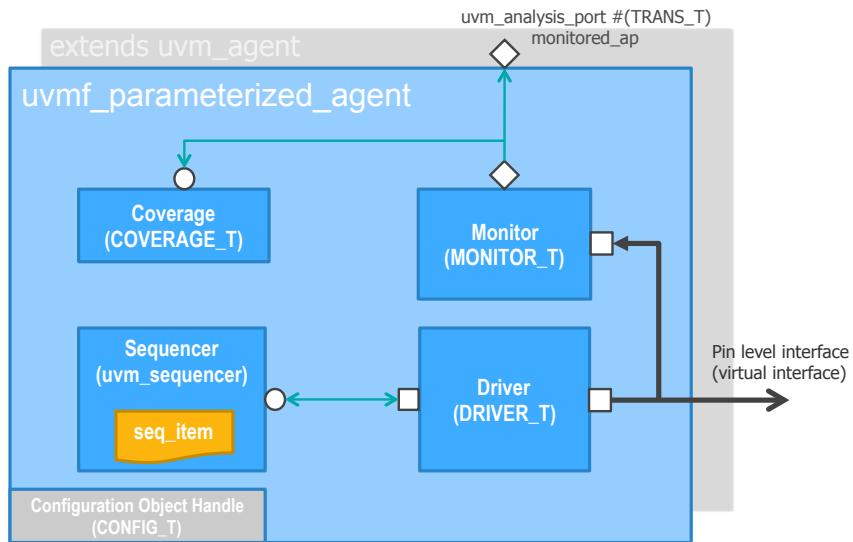
15.2 Driver Base

UVMF Driver Base



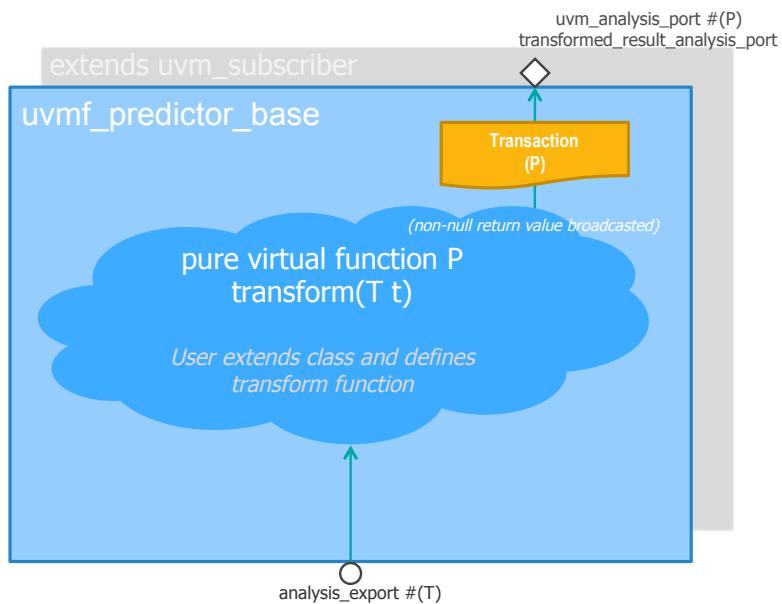
15.3 Parameterized Agent

UVMF Parameterized Agent



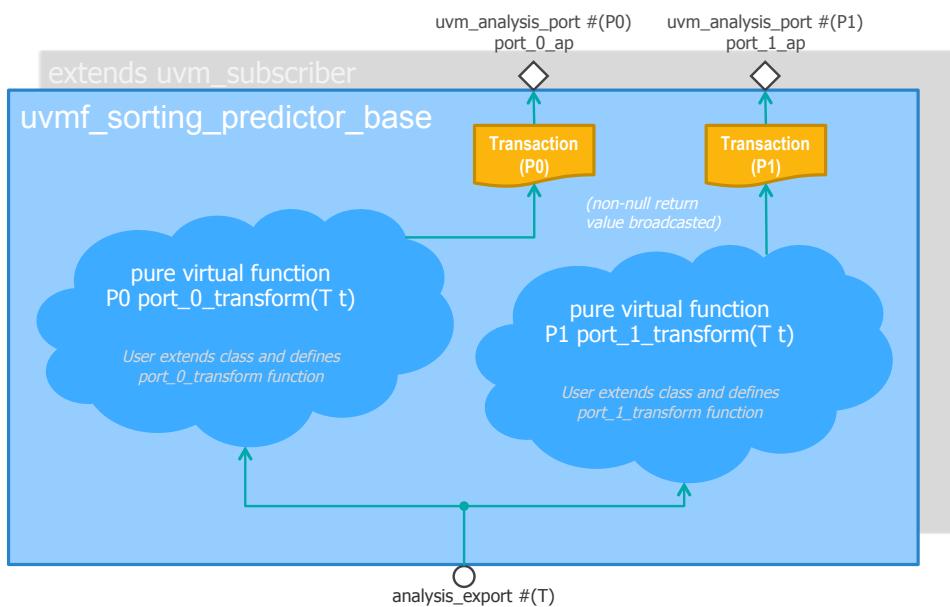
15.4 Predictor Base

UVMF Predictor Base



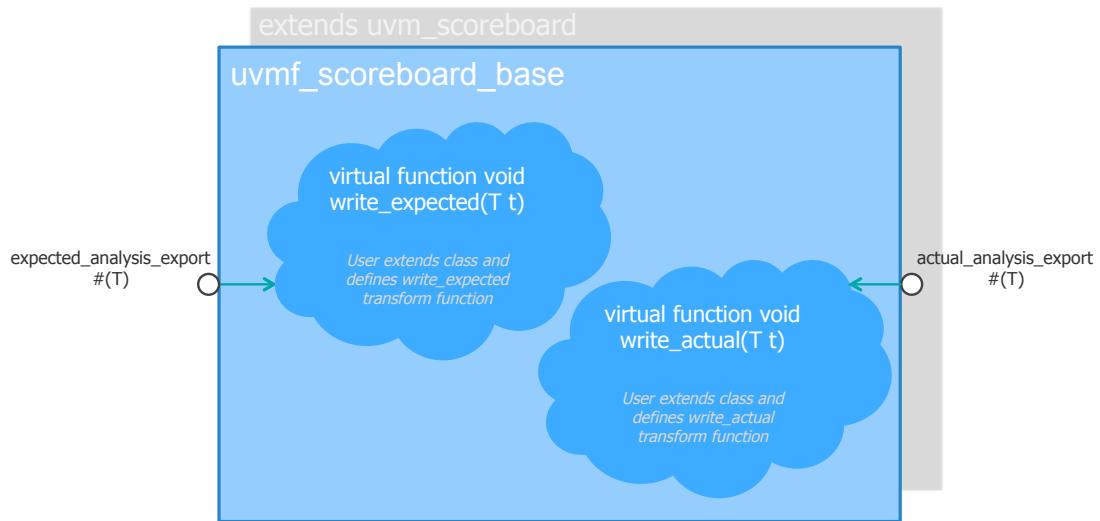
15.5 Sorting Predictor Base

UVMF Sorting Predictor Base



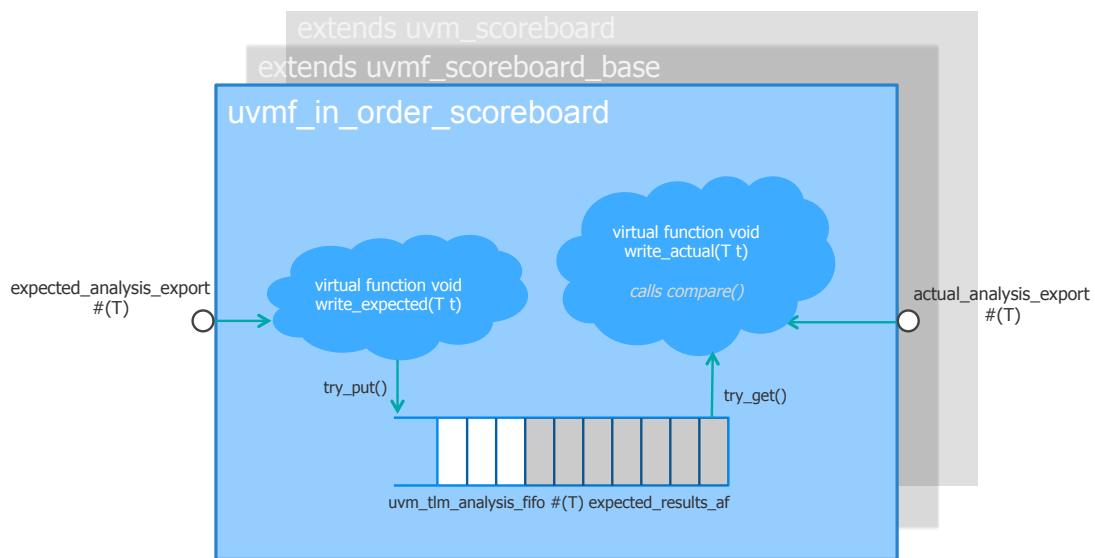
15.6 Scoreboard Base

UVMF Scoreboard Base



15.7 In Order Scoreboard

UVMF In-Order Scoreboard



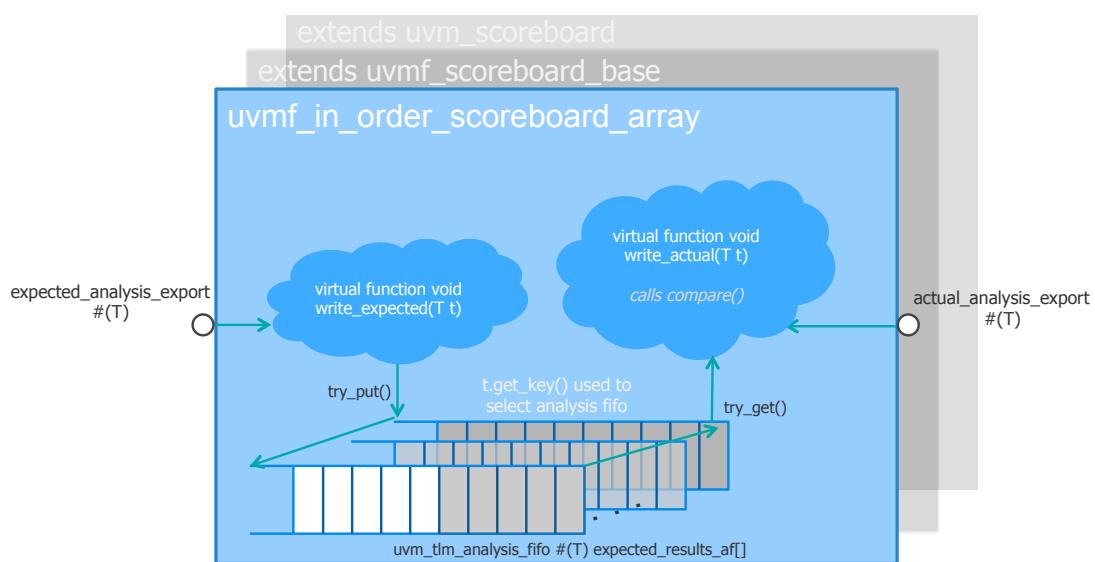
12 UVMF Base Package Component Block Diagrams

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15.8 In Order Scoreboard Array

UVMF In-Order Scoreboard Array



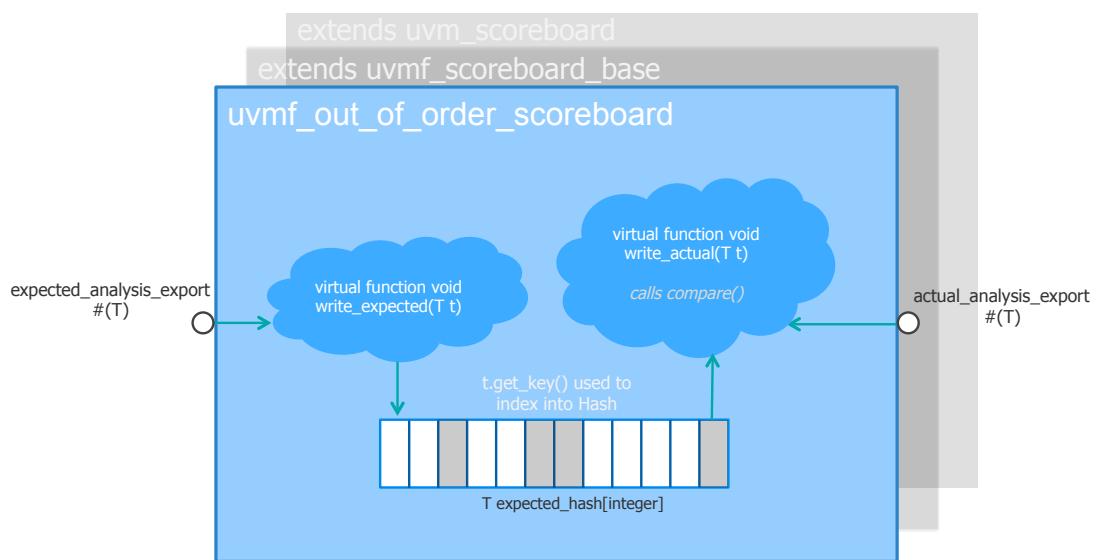
13 UVMF Base Package Component Block Diagrams

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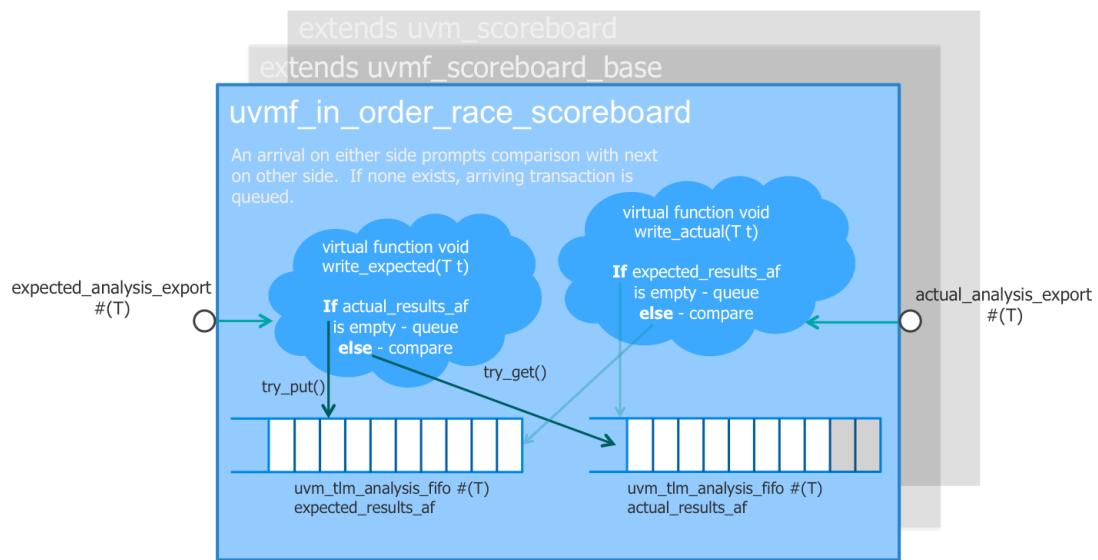
15.9 Out of Order Scoreboard

UVMF Out-of-Order Scoreboard



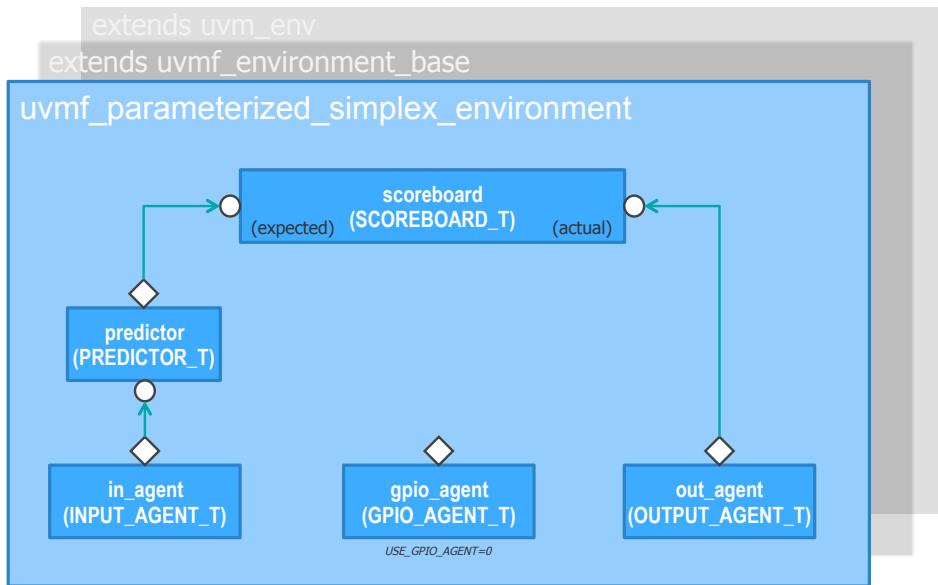
15.10 In Order Race Scoreboard

UVMF In-Order Race Scoreboard



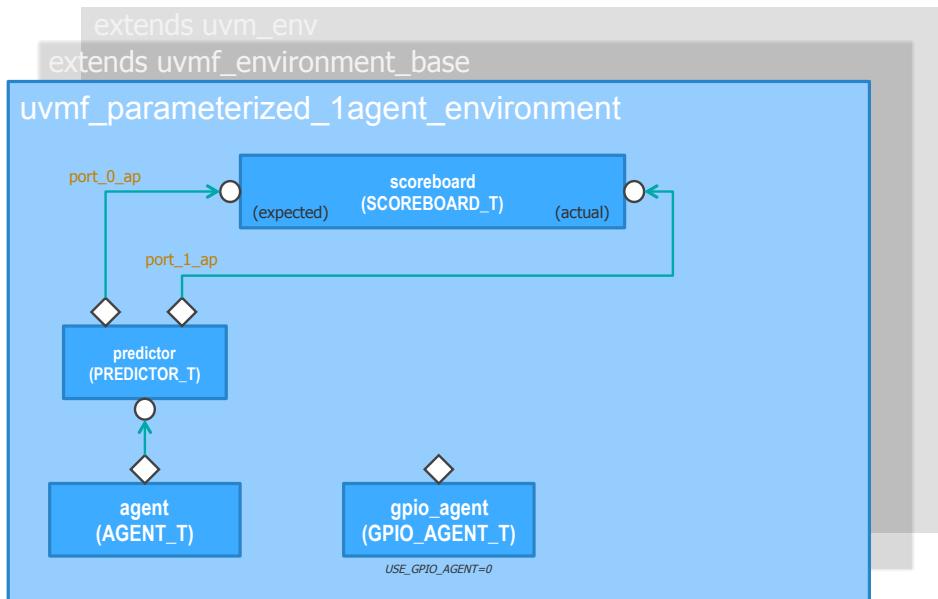
15.11 Parameterized Simplex Environment

UVMF Parameterized Simplex Environment



15.12 Parameterized One Agent Environment

UVMF Parameterized 1 Agent Environment



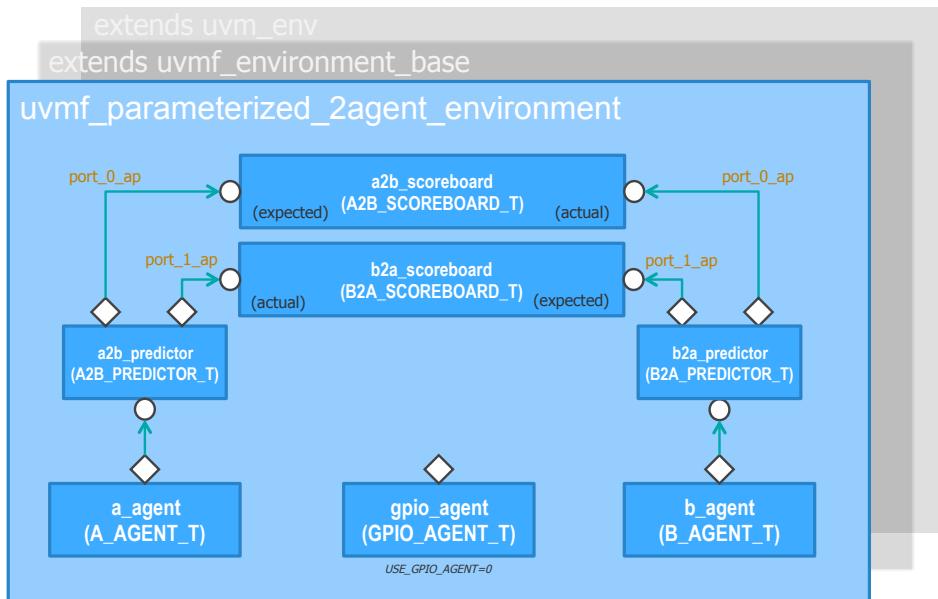
7 UVMF Base Package Component Block Diagrams

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15.13 Parameterized Two Agent Environment

UVMF Parameterized 2 Agent Environment



15.14 Parameterized Three Agent Environment

UVMF Parameterized 3 Agent Environment

