# HEXACUBE COUNTERS CHALLENGE

The overall functioning contains 4 verilog files. Module for clock divider function(oneHz_gen.v), Module to control counter function(digits.v), Module to control seven segment display(seg7_control.v), Top level module(top.v).

## oneHz_gen.v

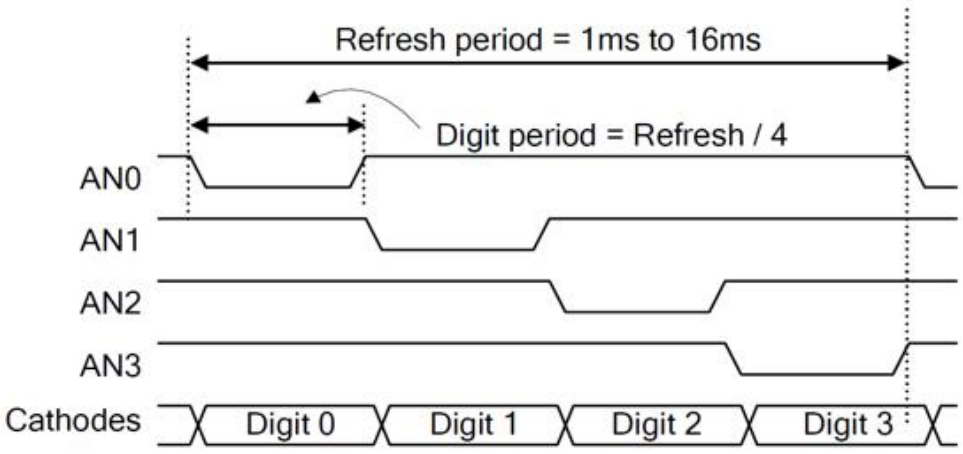
1Hz is generated from a 50MHz clock by making use of a counter, ctr_reg which counts till 25,000,000 and then it toggles a new clock signal to obtain a clock signal of frequency 1Hz. The formula used to obtain the counter value is (50MHz / 1Hz / 2). ctr_reg is declared as 26 bit register to hold the given value.

## digits.v

The two digits of the seven segment display which are required for counting from 00 to 99 are declared as “ones” and “tens”. The logic used here is initially ones digit will be counted either from 0 to 9 or 9 to 0 depending on upcounting or downcounting. For upcounting when the ones digit reaches 9, the tens digit will be incremented by 1 and ones digit will be made 0. If both ones and tens digits are 9, then both digits are set to 0 and the buzzer will be turned on for 1 second. If reset is pressed both ones and tens goes to 0 and counting is continued from there. If load is pressed ones digit is set to 0 and tens digit is set to 9, and counting is continued.
For downcounting when the ones digit reaches 0, the tens digit will be decremented by 1 and ones digit will made 9. If both ones and tens digits are 0, then both digits are set to 9 and the buzzer will be turned on for 1 second. If reset is pressed both ones and tens goes to 9 and counting is continued from there. If load is pressed ones digit is set to 0 and tens digit is set to 1, and counting is continued.
Stop is included as pushbutton which when pressed and held will stay at the same digit and when released will continue counting.

## seg7_control.v

This file contains the logic for controlling digit select and digit timer. Digit select is a 2 bit counter for selecting each of 4 digits. Digit timer is a counter for digit refresh. For each of the four digits to appear bright and continuously illuminated, all four digits should be driven once every 1 to 16ms. So we have a refresh period of 4ms within the range and each digit must be ON for 1/4 period of the refresh period I.e,. each digit must be ON for 1ms.




Four digit scanning display controller timing diagram.

Thus counter for digit refresh will be 50,000. This is calculated as (20ns x counter)=1ms. 20ns is the period of 50MHz clock. Thus based on when the digit timer reaches this value, the digit select is incremented by 1 to select the next digit. The value “ones” is displayed on first seven segment display, “tens” is displayed on the second display whereas on third and fourth seven segment displays a dash is displayed by activating the “g” segment.

## top.v

It is the top level module that instantiates all the modules.

## Factors that are working and not working:

The display on seven segment is proper.
Down counting is working fine when included in the “else” condition. Upcounting doesn’t work when included in “if” condition.
If the upcounting is put within else condition by change “if(updown)” to “if(updown==0)” then upcounting will work fine and downcounting will not work.
Load is working fine. Reset is working fine. Stop button when pressed and held the value will remain constant and when the button is released the counting continues.
During rollover the buzzer will ring for 1 second.