Deadlines and activities

Week of Oct 30:

Activity: Work on the controller design, and prelab activities for tasks 1 and 2

Deliverable: **November 6 (Monday 12pm)**: Submit the following:

- ALU (from Task1),
- Instruction Memory (from Task1),
- All tables for control signals (from Tasks 1 and 2)
- single_cycle_datapath_Task1.pptx : Slides 9, 11,
- single_cycle_datapath_Task2.pptx: slides 4, 7

Week of Nov 6:

Activity: During the lab integrate the controller and the datapath components. Continue working outside the lab hours to complete your design. Suggested approach: A top module for datapath, and another top module that integrates the datapath with the controller.

Deliverable: **November 10 (Friday)** Submit the following:

- Only the completed controller module (.v) covering instructions from task1 and 2.

Week of Nov 13:

Activity: **In the lab demonstrate both Tasks 1 and 2.**

Deliverable: November 17 (Friday), submit the .v files on D2L

Instructor will release Task 3 specification

Week of November 20 (Exam 3 on Monday):

Activity: Continue with Task 3 to execute a given application on your datapath.

Week of November 27:

Activity: Lab Practical and outside the lab continue on Task 3.

Week of December 4:

Activity: FPGA based demo of Task 3. Students in Thursday and Friday sections will make an appointment with one of the TAs to complete the demo.

Deliverable: Dec 4 (Monday) 9am all .v files for Task 3.