**GPIO**

Verification Environment and Test Plan

Table Of Contents

1. Introduction………………………………………………………………………………..
   1. Document Overview…………………………………………………………………..
   2. Terms and Definitions………………………………………………………………....
2. Testbench Overview………………………………………………………………………..
   1. Verification Objective………………………………………………………………….
   2. Verification Architecture………………………………………………………………
3. Test Bench Components…………………………………………………………………..
   1. Scoreboard……………………………………………………………………………..
   2. Interface………………………………………………………………………………..
   3. Agents.............................................................................................................................

3.3.1 Sequencer..............................................................................................................

3.3.2 Driver.....................................................................................................................

3.3.3 Monitor..................................................................................................................

4. Signal Description...............................................................................................................

**1.INTRODUCTION**

## 1.1 Document Overview

This document describes the Verification environment and Test plan for the GPIO. It identifies the various components that form the GPIO Verification Environment and defines the test bench features and test scenarios. GPIO is a block in the PULPino project which is used to connect the particular pheripheral device with the core

1.2 Terms and Definitions

Table 1:Terms and Definitions

| Abbreviation / Term | Expansion / Definition |
| --- | --- |
| GPIO | General Purpose Input Output |
| UVM | Universal Verification Methodology |
| DUT | Design Under Test |
| MON | Monitor |
| TB | Test Bench |
| ASIC | Application Specific Integrated Circuit |
|  | |

**2.** **TEST BENCH OVERVIEW**

2.1 Verification Objective

The primary objective is to develop a verification environment for the GPIO , to perform a block level verification of each component with possible test cases using UVM Methodology. The idea of using the Universal verification methodology [UVM] is to preserve a single environment for block level verification.

2.2 Verification Architecture

TOP

TEST

ENV

SCOREBOARD(TB LOGIC)

SEQS

Active agent

Passive agent

MON

MON

SEQ

DRVR

**3. Test Bench Components**

* 1. Score board

Scoreboards are used for checking the data integrity. Expected data is collected from the respective monitor and compared with the actual data coming from peripheral monitor

* 1. Interface

The Interface construct in SystemVerilog is used specifically to encapsulate the communication between blocks. This is a SystemVerilog language construct used to connect the DUT to the Testbench. All the connection signals are defined here and are used by the testbench to drive and sample the data to/from the DUT.

3.3 Agents

Active and passive agents were used here. Active agent contains sequencer,driver and monitor.Passive agent contains monitor only from that monitor we were monitoring the DUT output.

3.3.1 Sequencer

Sequencer is a UVM component through which sequences are send to driver.Sequencer and driver will maintain a handshake mechanism for passing sequences to DUT.

3.3.2 Driver

Driver drives the GPIO data to DUT through GPIO interface

3.3.3 Monitor

The input that is given to DUT through driver is monitored by the monitor in the active agent to implement the input checker at score board

4 GPIO Signal Description

|  |  |  |
| --- | --- | --- |
| Signal | Direction | Description |
| gpio\_in[31:0] | output | Transmit data |
| gpio\_out[31:0] | input | Receive data |
| gpio\_dir[31:0] | input | Request to send |
| pad\_cfg[5:0][31:0] | input | Pad configuration |
| interrupt | input | Interrupt |