Case Study for 32-bit Pipelined CPU design with New ALU Architecture

12/02/2016

A20345929

Namsik Kong

1. INTRODUCTION

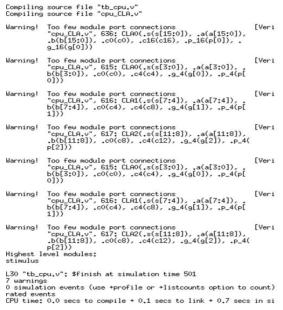
This Report will describes the "Case Study for 32-bit Pipelined CPU design with New ALU Architecture". The objective of this project is to understand a 32-bit Pipelined Central Processing Unit (CPU). As the name of the design declares, the word length of the data used in the circuits is 32 bits. Furthermore, since this circuit is pipelined, more than one instruction can be executed simultaneously. The operation of the circuit is synchronized by an externally set clock signal. Also the instruction signals for addressing the memory file, selecting the Arithmetic Logic Unit (ALU) operands and specifying the operation of the ALU are also external. The correct synchronization of those signals with the critical data path delay of the circuit that will determine the minimum operating period is one of the objectives of the project.

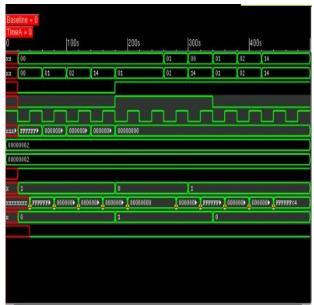
2. ANALYSIS

- CASE STUDY 1

1) Generate the display screenshot or the text output of the RTL simulation and the screenshot from simvision with provided test bench (tb_cpu.v)

(1) cpu_CLA.v





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Compiling source file "tb_cpu.v" Compiling source file "cpu_CRA.v"

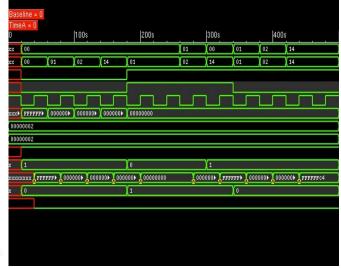
Warning! Too few module port connections "opu_CRR.v", 557; cra0(.sum(7:0]), .c_out(c7), .c_out(c7), .c_in(c_in))

Too few module port connections [Verilog-TFNPC] cpu_CRR,v", 558: craf(_sum(sum[15:8]), _c_out(_cf5), _a(a[15:8]), _b(b[15:8]), _c_in(c7))

Warning! Too few module port connections "cpu_CRR,v", 559; cra2(,sum(sum[23:16]), .c_out(
Highest level modules:
stimulus

L30 "tb_cpu.v": \$finish at simulation time 501 3 warnings 0 simulation events (use +profile or +listcounts option to count) + 21024 accele

rated events CPU time; 0.0 secs to compile + 0.1 secs to link + 0.7 secs in simulation



(3) cpu_CSA.v

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Compiling source file "tb_cpu.v" Compiling source file "cpu_CSA.v"

Warning! Too few module port connections [Verilog-TFNPC] "cpu_CSA,v", 598; cs0.15(.s(s[15:0]), .cout(c), a(a[15:0]), b(s[15:0]), .cin(cin))

Too few module port connections "cpu_CSA,v", 582: cs0_3(.s(s[3:0]), .cout(c[0]), .a(a[3:0]), .b(b[3:0]), .cin(cin)) [Verilog-TFNPC] Warning!

Too few module port connections [Verilog-TFNPC] "cpu_CSA,v", 583; cs4_7(.s(s[7:4]), .cout(c[1]), .a(a[7:4]), .b(b[7:4]), .cin(c[0])) Warning!

Warning!

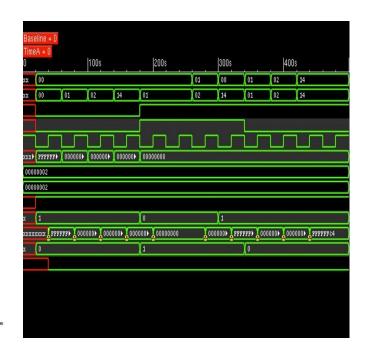
Too few module port connections "cpu_CSA,v", 584; cs8_11(,s(s[11:8]), _cout(c[2]) , _a(a[11:8]), _b(b[11:8]), _cin(c[1]))

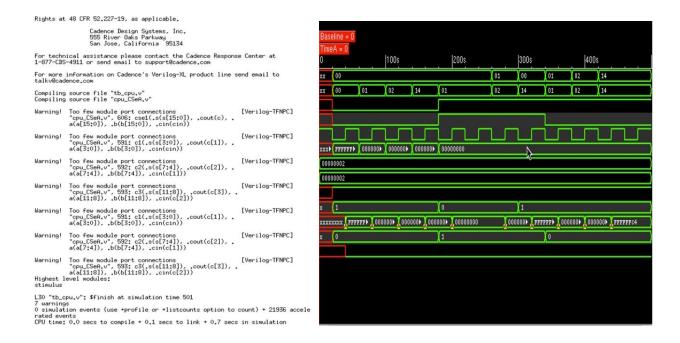
Warning! Too few module port connections [Verilog-TFNPC] "cpu_CSA.v", 582; cs0_3(.s(s[3:0]), .cout(c[0]), .d(a[3:0]), .b(b[3:0]), .cin(cin)) Too few module port connections "cpu_CSA.v", 583; cs4_7(.s(s[7:4]), .cout(c[1]), .a(a[7:4]), .b(b[7:4]), .cin(c[0])) [Verilog-TFNPC]

Warning! Too few module port connections [Verilog-TFNPC] "cpu_CSA,v", 584; cs8_i1(_s(s[i1:8]), _cout(c[2]) , _a(s[i1:8]), _b(b[i1:8]), _cin(c[i])) Highest level modules:

L30 "tb_cpu.v": \$finish at simulation time 501
7 warnings
0 simulation events (use *profile or *listcounts option to count) + 21065 accele

rated events CPU time: 0.0 secs to compile + 0.1 secs to link + 0.7 secs in simulation





2) Synthesize the design and summarize cell.rep and timing.rep

(1) cpu_CLA.v

Beginning Mapping Optimizations (Medium effort) (Incremental)	☐ cell.rep ×				↑ timing.rep x		
	VI CIT CUI VA	TUVINE	guccium	J.131100 II	7		
Beginning Incremental Implementation Selection	o/tr/t10/b1	TBUFX2	gscl45nm	3.754400 n	d/(3/1203/U2/1 (AUKZAI)	0.07	0.04 [
	o/tr/t11/b1	TBUFX2	ascl45nm	3.754400 n	a/l3/f274/U5/Y (XNOR2X1)	0.06	6.11 r
Beginning Delay Optimization Phase	o/tr/t12/b1	TBUFX2	ascl45nm	3.754400 n	a/l3/f274/U2/Y (XOR2X1)	0.07	6.18 r
	o/tr/t13/b1	TBUFX2	gscl45nm	3.754400 n	a/l3/f283/U5/Y (XNOR2X1)	0.06	6.24 r
ELAPSED WORST NEG TOTAL NEG DESIGN TIME AREA SLACK SLACK RULE COST ENDPOINT	o/tr/t14/b1	TBUFX2	gscl45nm	3.754400 n	a/l3/f283/U2/Y (XOR2X1)	0.07	6.31 r
	o/tr/t15/b1	TBUFX2	gscl45nm	3.754400 n	a/l3/f292/U5/Y (XNOR2X1)	0.06	6.37 r
0:00:02 48566.4 0.00 0.0 3.0 0:00:03 48566.4 0.00 0.0 3.0	o/tr/t16/b1	TBUFX2	ascl45nm	3.754400 n	a/13/f292/U2/Y (XOR2X1)	0.07	6.44 r
0:00:03 48566.4 0.00 0.0 3.0	o/tr/t17/b1	TBUFX2	gscl45nm	3.754400 n		0.04	6.48 f
	o/tr/t18/b1	TBUFX2	ascl45nm	3.754400 n	a/l3/h301/U2/Y (XOR2X1)		
Beginning Design Rule Fixing (max_capacitance)	o/tr/t19/b1	TBUFX2	ascl45nm	3.754400 n	a/U26/Y (A0I22X1)	0.03	6.52 r
ELAPSED MORST NEG TOTAL NEG DESIGN	o/tr/t20/b1	TBUFX2	gscl45nm gscl45nm	3.754400 n	U219/Y (BUFX2)	0.04	6.56 r
TIME AREA SLACK SLACK RULE COST ENIPPOINT		TBUFX2		3.754400 n	U64/Y (AND2X1)	0.07	6.62 r
0:00:03 48566.4 0.00 0.0 3.0	o/tr/t21/b1		gscl45nm		U1729/Y (INVX1)	0.10	6.73 f
Loading db file '/apps/FreePIK45/osu_scc/lib/files/gscl45nm.db'	o/tr/t22/b1	TBUFX2	gscl45nm	3.754400 n	mb/ram/mer12/m0/m31/U3/Y (A0I22X1)	0.05	6.78 r
Optimization Complete	o/tr/t23/b1	TBUFX2	gscl45nm	3.754400 n	U3762/Y (INVX1)	0.02	6.80 f
Warning: Design 'cpu' contains 1 high-fanout nets, A fanout number of 1000 will be used for del	o/tr/t24/bl	TBUFX2	gscl45nm	3.754400 n	mb/ram/mer12/ll/me31/qout_reg/D (DFFPOSX1)	0.00	6.80 f
ay calculations involving these nets. (TIM-134)	o/tr/t25/b1	TBUFX2	gscl45nm	3.754400 n	data arrival time	0.00	6.80
Net 'clk': 1624 load(s), 1 driver(s)	o/tr/t26/b1	TBUFX2	gscl45nm	3.754400 n	data dilivat time		0.00
check_design	o/tr/t27/b1	TBUFX2	gscl45nm	3.754400 n	alock all fator adock	22.00	22.00
#report_constraint -all_violators	o/tr/t28/b1	TBUFX2	gscl45nm	3.754400 n	clock clk (rise edge)	33.00	33.00
set filename [format "%s%s"	o/tr/t29/b1	TBUFX2	gscl45nm	3.754400 n	clock network delay (ideal)	0.00	33.00
write -f verilog -output \$filename	o/tr/t30/b1	TBUFX2	gscl45nm	3.754400 n	mb/ram/mer12/ll/me31/qout_reg/CLK (DFFPOSX1)	0.00	33.00 r
Writing verilog file '/howe/ykim/ece429/project/cpu_CLA/cpu,vh'. 1	o/tr/t31/b1	TBUFX2	gscl45nm	3.754400 n	library setup time	-0.06	32.94
set filename [format "%x%s"	wb/bd/me0/gout reg	DFFP0SX1	gscl45nm	7.978100 n	data required time		32.94
write_sdc \$filename	wb/bd/mel/qout reg	DFFPOSX1	gscl45nm	7.978100 n			
1 #set filename [format "%s%s" %aw_toplevel ".db"]	wb/bd/me2/gout_reg	DFFP0SX1	gscl45nm	7.978100 n	data required time		32.94
Murite -f db -hier -output \$filename -xg_force_db redirect timing.rep { report_timing }	wb/bd/me3/gout_reg	DFFP0SX1	gscl45nm	7.978100 n	data arrival time		-6.80
redirect cell,rep { report_cell }	wb/bd/me4/gout_reg	DFFP0SX1	ascl45nm	7.978100 n	uata arrivat time		-0,00
redirect power.rep { report_power } quit	wb/ bd/ me4/ qout_reg			7.970100 11			
H-7000	Total 14359 cells			48566.448185	slack (MET)		26.14
Thank you Element Time = 2400 EE	10(01 14339 (6(12			40300.440103			

(2) cpu_CRA.v

Beginning Mapping Optimizations (Medium effort) (Incremental)	☐ cell.rep ×				∬ timing rep ×		
Beginning Incremental Implementation Selection	0/11/110/01	IBUFAZ	gsct45nm	3./34400 N	d/L3/T203/U2/1 (AUKZAI)	8.87	0.84 F
	o/tr/t11/b1	TBUFX2	gscl45nm	3.754400 n	a/l3/f274/U5/Y (XNOR2X1)	0.06	6.11 r
Beginning Delay Optimization Phase	o/tr/t12/b1	TBUFX2	gscl45nm	3.754400 n	a/13/f274/U2/Y (XOR2X1)	0.07	6.18 r
	o/tr/t13/b1	TBUFX2	gscl45nm	3.754400 n	a/13/f283/U5/Y (XNOR2X1)	0.06	6.24 r
ELAPSED WORST NEG TOTAL NEG DESIGN TIME AREA SLACK SLACK RULE COST ENDPOINT	o/tr/t14/b1	TBUFX2	gscl45nm	3.754400 n	a/l3/f283/U2/Y (XOR2X1)	0.07	6.31 r
0:00:02 48610.1 0.00 0.0 2.9	o/tr/t15/bl	TBUFX2	gscl45nm	3.754400 n	a/l3/f292/U5/Y (XNOR2X1)	0.06	6.37 r
0:00:03 48610.1 0.00 0.0 2.9	o/tr/t16/b1	TBUFX2	gscl45nm	3.754400 n	a/l3/f292/U2/Y (XOR2X1)	0.07	6.44 r
0:00:03 48610.1 0.00 0.0 2.9	o/tr/t17/b1	TBUFX2	gscl45nm	3.754400 n	a/l3/h301/U2/Y (XOR2X1)	0.04	6.48 f
Beginning Design Rule Fixing (max_capacitance)	o/tr/t18/b1	TBUFX2	gscl45nm	3.754400 n	1.00E-0.078038170E-0.00E-0.78038090CTE-		
acquiring sessin rate (interpretation)	o/tr/t19/b1	TBUFX2	gscl45nm	3.754400 n	a/U26/Y (A0I22X1)	0.03	6.52 r
ELAPSED WORST NEG TOTAL NEG DESIGN	o/tr/t20/bl	TBUFX2	gscl45nm	3.754400 n	U220/Y (BUFX2)	0.04	6.56 r
TIME AREA SLACK SLACK RULE COST ENDPOINT	o/tr/t21/b1	TBUFX2	gscl45nm	3.754400 n	U65/Y (AND2X1)	0.07	6.62 r
0:00:03 48610.1 0.00 0.0 2.9	o/tr/t22/b1	TBUFX2	gscl45nm	3.754400 n	U1794/Y (INVX1)	0.10	6.73 f
oading db file '/apps/FreePDK45/osu_soc/lib/files/gscl45nm.db'	o/tr/t23/b1	TBUFX2	gscl45nm	3.754400 n	mb/ram/merl2/m0/m31/U3/Y (A0I22X1)	0.05	6.78 r
Optimization Complete	o/tr/t24/bl	TBUFX2	gscl45nm	3.754400 n	U3794/Y (INVX1)	0.02	6.80 f
arning: Design 'cpu' contains 1 high-fanout nets. A fanout number of 1000 will be	used 0/tr/t25/b1	TBUFX2	gscl45nm	3.754400 n	mb/ram/mer12/ll/me31/qout_reg/D (DFFPOSX1)	0.00	6.80 f
for delay calculations involving these nets. (TIM-134) Net 'clk': 1624 load(s), 1 driver(s)	o/tr/t26/b1	TBUFX2	gscl45nm	3.754400 n	data arrival time	17/17/	6.80
heck design	o/tr/t27/bl	TBUFX2	gscl45nm	3.754400 n	data dirarat tane		0.00
	o/tr/t28/b1	TBUFX2	gscl45nm	3.754400 n	clock clk (rise edge)	33.00	33.00
report_constraint -all_violators et filename [format "%s%s" \$my_toplevel ".vh"]	o/tr/t29/bl	TBUFX2	gscl45nm	3.754400 n		0.00	33.00
pu.vh rite -f verilog -output \$filename	o/tr/t30/bl	TBUFX2	gscl45nm	3.754400 n	clock network delay (ideal)	187.850	
riting verilog file '/home/ykim/ece429/project/cpu_CRA/cpu.vh'.	o/tr/t31/b1	TBUFX2	gscl45nm	3.754400 n	mb/ram/mer12/ll/me31/qout_reg/CLK (DFFPOSX1)	0.00	33.00 r
et filename [format "%s%s" \$mu_toplevel ".sdc"]	wb/bd/meθ/qout_reg	DFFP0SX1	gscl45nm	7.978100 n	library setup time	-0.06	32.94
pu.sdc rite_sdc \$filename	wb/bd/mel/qout_reg	DFFP0SX1	gscl45nm	7.978100 n	data required time		32.94
potential total social properties	wb/bd/me2/qout_reg	DFFP0SX1	gscl45nm	7.978100 n			
set filename [format "%s%s" \$my_toplevel ".db"] write -f db -hier -output \$filename -xg_force_db	wb/bd/me3/qout_reg	DFFP0SX1	gscl45nm	7.978100 n	data required time		32.94
edirect timing.rep { report_timing } edirect cell.rep { report_cell }	wb/bd/me4/qout_reg	DFFP0SX1	gscl45nm	7.978100 n	data arrival time		-6.80
edirect power.rep { report_power }							
uit	Total 14390 cells			48610.093084	slack (MET)		26.14
hank you	1				arnes (ner)		20.14

(3) cpu_CSA.v

	⊕ cell.rep ×				☐ timing.rep x		
Beginning Incremental Implementation Selection	0/11/110/01	IBULY7	gsct45nm	3./54400 N	d/ L3/T203/U2/T (AUKZA1)	U.U/	0.84 F
beginning incremental implementation selection	o/tr/t11/b1	TBUFX2	gscl45nm	3.754400 n	a/l3/f274/U5/Y (XNOR2X1)	0.06	6.11 r
Beginning Delay Optimization Phase	o/tr/t12/b1	TBUFX2	gscl45nm	3.754400 n	a/l3/f274/U2/Y (XOR2X1)	0.07	6.18 r
***************************************	o/tr/t13/b1	TBUFX2	gscl45nm	3.754400 n	a/l3/f283/U5/Y (XNOR2X1)	0.06	6.24 r
ELAPSED MORST NEG TOTAL NEG DESIGN TIME AREA SLACK SLACK RULE COST ENDPOINT	o/tr/t14/b1	TBUFX2	gscl45nm	3.754400 n	a/l3/f283/U2/Y (XOR2X1)	0.07	6.31 r
	o/tr/t15/b1	TBUFX2	gscl45nm	3.754400 n	a/13/f292/U5/Y (XNOR2X1)	0.06	6.37 r
0;00;02 48878,1 0,00 0,0 2,9 0;00;03 48878,1 0,00 0,0 2,9	o/tr/t16/b1	TBUFX2	gscl45nm	3.754400 n			6.44 r
0:00:03 49878,1 0.00 0.0 2.9	o/tr/t17/b1	TBUFX2	gscl45nm	3.754400 n	a/l3/f292/U2/Y (XOR2X1)	0.07	
P	o/tr/t18/b1	TBUFX2	gscl45nm	3.754400 n	a/l3/h301/U2/Y (XOR2X1)	0.04	6.48 f
Beginning Design Rule Fixing (max_capacitance)	o/tr/t19/b1	TBUFX2	gscl45nm	3.754400 n	a/U26/Y (A0I22X1)	0.03	6.52 r
ELAPSED WORST NEG TOTAL NEG DESIGN	o/tr/t20/bl	TBUFX2	gscl45nm	3.754400 n	U222/Y (BUFX2)	0.04	6.56 r
TIME AREA SLACK SLACK RULE COST ENDPOINT	o/tr/t21/b1	TBUFX2	gscl45nm	3.754400 n	U67/Y (AND2X1)	0.07	6.62 r
0;00;03 49878,1 0,00 0,0 2,9	o/tr/t22/b1	TBUFX2	gscl45nm	3.754400 n	U1832/Y (INVX1)	0.10	6.73 f
Loading db file '/apps/FreePDK45/osu_soc/lib/files/gscl45nm.db'	o/tr/t23/b1	TBUFX2	gscl45nm	3.754400 n	mb/ram/mer12/m0/m31/U3/Y (A0I22X1)	0.05	6.78 r
Optimization Complete	o/tr/t24/bl	TBUFX2	gscl45nm	3.754400 n	U3835/Y (INVX1)	0.02	6.80 f
Warning: Design 'cpu' contains 1 high-fanout nets. A fanout number of 1000 will be u	sed o/tr/t25/b1	TBUFX2	gscl45nm	3.754400 n	mb/ram/mer12/ll/me31/qout reg/D (DFFPOSX1)	0.00	6.80 f
for delay calculations involving these nets. (TIM-134) Net 'clk': 1624 load(s), 1 driver(s)	o/tr/t26/b1	TBUFX2	gscl45nm	3.754400 n	data arrival time	0.00	6.80
1 check_design	o/tr/t27/bl	TBUFX2	gscl45nm	3.754400 n	data dilivat time		0.00
1 #report constraint -all violators	o/tr/t28/b1	TBUFX2	gscl45nm	3.754400 n	cleak alk (sice adae)	22.00	22.00
set filename [format "%s%s" \$my_toplevel ".vh"]	o/tr/t29/bl	TBUFX2	gscl45nm	3.754400 n	clock clk (rise edge)	33.00	33.00
cpu.vh write -f verilog -output \$filename	o/tr/t30/b1	TBUFX2	gscl45nm	3.754400 n	clock network delay (ideal)	0.00	33.00
Writing verilog file '/home/ykim/ece429/project/cpu_CSA/cpu.vh'.	o/tr/t31/b1	TBUFX2	gscl45nm	3.754400 n	mb/ram/mer12/ll/me31/qout_reg/CLK (DFFPOSX1)	0.00	33.00 r
set filename [format "%s%s" \$my_toplevel ".sdc"]	wb/bd/me0/gout reg	DFFP0SX1	gscl45nm	7.978100 n	library setup time	-0.06	32.94
cpu.sdc write_sdc \$filename	wb/bd/mel/qout reg	DFFP0SX1	gscl45nm	7.978100 n	data required time		32.94
1 *set filename [format "%s%s" \$my_toplevel ".db"]	wb/bd/me2/gout reg	DFFP0SX1	gscl45nm	7.978100 n			
<pre>#urite -f db -hier -output \$filename -xg_force_db redirect timing.rep { report_timing }</pre>	wb/bd/me3/gout_reg	DFFP0SX1	gscl45nm	7.978100 n	data required time		32.94
redirect child, rep (report_cell) redirect power, rep (report_power) quit	wb/bd/me4/qout_reg	DFFP0SX1	gscl45nm	7.978100 n	data arrival time		-6.80
Elapsed Time = 2:31.85, CPU_Time = 146.062	Total 14479 cells			48878.063377	slack (MET)		26.14

	∏ cell rep ×				No.		
	0/11/110/01	IBUFAZ	qsct45nm	5./54400 N	⊕ timing rep ×		
. Beginning Incremental Implementation Selection	o/tr/t11/b1	TBUFX2	gscl45nm	3.754400 n	8/L3/1203/UZ/1 (AUKZAL)	0.07	0.04 [
	o/tr/t12/b1	TBUFX2	gscl45nm	3.754400 n	a/l3/f274/U5/Y (XNOR2X1)	0.06	6.11 r
Beginning Delay Optimization Phase	o/tr/t13/b1	TBUFX2	gscl45nm	3.754400 n	a/l3/f274/U2/Y (XOR2X1)	0.07	6.18 r
ELAPSED WORST NEG TOTAL NEG DESIGN	o/tr/t13/b1	TBUFX2	gscl45nm	3.754400 n	a/l3/f283/U5/Y (XNOR2X1)	0.06	6.24 r
TIME AREA SLACK SLACK RULE COST ENIPOINT	o/tr/t15/b1	TBUFX2	gscl45nm	3.754400 n	a/l3/f283/U2/Y (XOR2X1)	0.07	6.31 r
0:00:01 49150.7 0.00 0.0 3.0	o/tr/t16/b1	TBUFX2	gscl45nm	3.754400 n	a/l3/f292/U5/Y (XNOR2X1)	0.06	6.37 r
0;00;02 49150,7 0,00 0,0 3,0	o/tr/t17/b1	TBUFX2	gscl45nm gscl45nm	3.754400 n	a/l3/f292/U2/Y (XOR2X1)	0.07	6.44 r
0:00:03 49150.7 0.00 0.0 3.0	o/tr/t18/b1	TBUFX2	gscl45nm gscl45nm	3.754400 n	a/l3/h301/U2/Y (XOR2X1)	0.04	6.48 f
Beginning Design Rule Fixing (max_capacitance)	o/tr/t19/b1	TBUFX2		0. 35 1100		0.03	6.52 r
and the state of t	.,,,	TBUFX2	gscl45nm	3.754400 n 3.754400 n	a/U26/Y (A0I22X1)		
ELAPSED WORST NEG TOTAL NEG DESIGN	o/tr/t20/bl	TBUFX2	gscl45nm	3.754400 n	U243/Y (BUFX2)	0.04	6.56 r
TIME AREA SLACK SLACK RULE COST ENDPOINT	o/tr/t21/b1		gscl45nm		U74/Y (AND2X1)	0.07	6.62 r
0:00:03 49150,7 0.00 0.0 3.0 Loading db file '/apps/FreePIK45/osu_soc/lib/files/gscl45mm.db'	o/tr/t22/b1	TBUFX2	gscl45nm	3.754400 n	U1844/Y (INVX1)	0.10	6.73 f
	o/tr/t23/b1	TBUFX2	gscl45nm	3.754400 n	mb/ram/mer12/m0/m31/U3/Y (A0I22X1)	0.05	6.78 r
Optimization Complete	o/tr/t24/b1	TBUFX2	gscl45nm	3.754400 n	U3884/Y (INVX1)	0.02	6.80 f
Warning; Design 'cpu' contains 1 high-fanout nets, A fanout number of 1000 will be used for de ay calculations involving these nets, (TIM-134)		TBUFX2	gscl45nm	3.754400 n	mb/ram/mer12/ll/me31/qout_reg/D (DFFPOSX1)	0.00	6.80 f
Net 'clk': 1624 load(s), 1 driver(s)	o/tr/t26/b1	TBUFX2	gscl45nm	3.754400 n	data arrival time		6.80
1 check_design	o/tr/t27/bl	TBUFX2	gscl45nm	3.754400 n	***************************************		
1 Hreport_constraint -all_violators	o/tr/t28/b1	TBUFX2	gscl45nm	3.754400 n	clock clk (rise edge)	33.00	33.00
set filename [format "%s%s" \$my_toplevel ".vh"]	o/tr/t29/b1	TBUFX2	gscl45nm	3.754400 n	clock network delay (ideal)	0.00	33.00
cpu.vh write -f verilog -output \$filename	o/tr/t30/bl	TBUFX2	gscl45nm	3.754400 n		0.00	
Writing verilog file '/home/ykim/ece429/project/cpu_CSeA/cpu.vh'.	o/tr/t31/b1	TBUFX2	gscl45nm	3.754400 n	mb/ram/mer12/ll/me31/qout_reg/CLK (DFFPOSX1)		33.00 r
set filename [format "%s%s" \$my_toplevel ".sdc"]	wb/bd/me0/qout_reg	DFFP0SX1	gscl45nm	7.978100 n	library setup time	-0.06	32.94
cpu.sdc write_sdc \$filename	wb/bd/mel/qout_reg	DFFP0SX1	gscl45nm	7.978100 n	data required time		32.94
1 Wset filename [format "%s%s" \$mu_toplevel ".db"]	wb/bd/me2/qout_reg	DFFP0SX1	gscl45nm	7.978100 n			
#write -f db -hier -output \$filename -xg_force_db	wb/bd/me3/qout_reg	DFFP0SX1	gscl45nm	7.978100 n	data required time		32.94
redirect timing.rep { report_timing } redirect cell.rep { report_cell }	wb/bd/me4/qout_reg	DFFP0SX1	gscl45nm	7.978100 n	data arrival time		-6.80
redirect power,rep { report_power }							
quit	Total 14577 cells			49150.726672	slack (MET)		26.14
Thank you Elapsed Time = 2:28,99, CPU Time = 146,569	1						

3) Provide the display screenshot or the text output of the post-synthesis simulation and the screenshot from simvision

(1) cpu_CLA.v

```
Cadence Design Systems, Inc.
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San Jose, California 95134
                                                                                                                                                                                                                   300,000ps
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                                                                                                                                                              100,000ps
                                                                                                                                                                                        200,000ps
                                                                                                                                                                                                                                               400,000ps
For more information on Cadence's Verilog-XL product line send email to
talkv@cadence.com
                                                                                                                                                                                                        02 14 01 02 14
Compiling source file "gscl45nm.v"
Compiling source file "tb_cpu.v"
Compiling source file "cpu.vh"
Highest level modules:
BUFX4
CLKBUF1
CLKBUE2
                                                                                                                                    (XX) [FFFFF] (000000) (000000) (000000) (0000000
CLKBUF3
DFFNEGX1
                                                                                                                                    00000002
DFFSR
FAX1
HAX1
INVX2
INVX4
INVX8
LATCH
MUX2X1
                                                                                                                                    | 000000 | | FFFFFF | 000000 | 000000 | FFFFFFC4
NAND3X1
NOR3X1
0AI22X1
OR2X2
TBUFX1
stimulus
"gscl45nm.v", 299: Timing violation in stimulus.proj.\a/l3/rc30/qout_reg
$setup( negedge D:35999, posedge CLK:36000, 0.09 : 9 );
L30 "tb_cpu.v": $finish at simulation time 50100
\theta simulation events (use +profile or +listcounts option to count) + 199395 accelerated events + 345566 timing check events CPU time: \theta.1 secs to compile + \theta.2 secs to link + \theta.1 secs in simulation
```



(3) cpu_CSA.v

1-877-CDS-4911 or send email to support@cadence.com

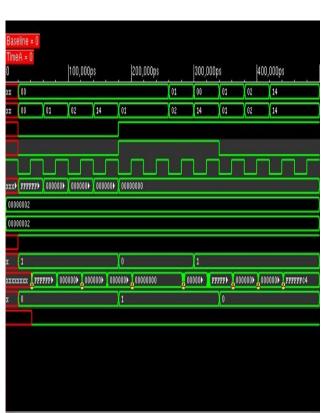
For more information on Cadence's Verilog-XL product line send email to talkv@cadence.com

```
Compiling source file "gscl45nm.v"
Compiling source file "tb_cpu.v"
Compiling source file "cpu.vh"
Highest level modules:
A0I21X1
BUFX4
CLKBUF1
CLKBUF2
CLKBUF3
DFFNEGX1
DFFSR
FAX1
HAX1
INVX2
TNVX4
INVX8
LATCH
MUX2X1
NOR3X1
0AT22X1
OR2X2
TRUEX1
stimulus
```

```
"gscl45nm.v", 299: Timing violation in stimulus.proj.\a/l3/rc30/qout_reg
   $setup( negedge D:35999, posedge CLK:36000, 0.09 : 9 );
```

L30 "tb_cpu.v": \$finish at simulation time 50100 θ simulation events (use +profile or +listcounts option to count) + 203407 accel erated events + 345558 timing check events CPU time: 0.1 secs to compile + 0.1 secs to link + 0.2 secs in simulation

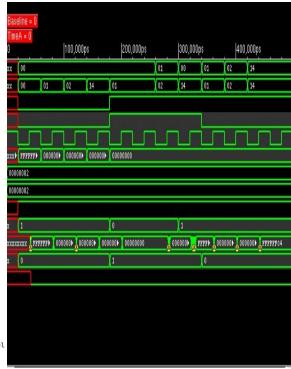




```
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1-877-CDS-4911 or send email to support@cadence.com
For more information on Cadence's Verilog-XL product line send email to
talkv@cadence.com
Compiling source file "gscl45nm.v"
Compiling source file "tb_cpu.v"
Compiling source file "cpu.vh"
Highest level modules:
A0I21X1
BUFX4
CLKBUF1
CLKBUF2
CLKBUF3
DFFNEGX1
DEESR
FAX1
HAX1
INVX2
INVX4
TNVX8
LATCH
MUX2X1
NAND3X1
NOR3X1
0AT22X1
OR2X2
```

"gscl45nm.v", 299: Timing violation in stimulus.proj.\a/l3/rc30/qout_reg \$setup(negedge D:35999, posedge CLK:36000, 0.09 : 9);

L30 "tb_cpu.v": \$finish at simulation time 50100 0 simulation events (use +profile or +listcounts option to count) + 207669 accelerated events + 345638 timing check events CPU time: 0.1 secs to compile + 0.1 secs to link + 0.1 secs in simulation



4) Summarize timing.rep.5.final. What is the maximum clock frequency this circuit can run

(1) cpu_CLA.v

TBUFX1 stimulus

(2) cpu_CRA.v

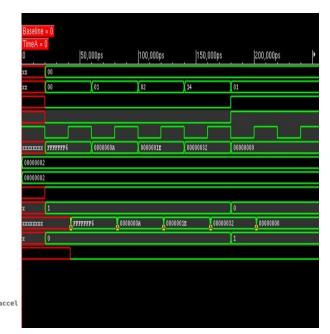
(3) cpu_CSA.v

(4) cpu_CSeA.v

5) Provide the display screenshot or the text output of the post-P&R simulation and the screenshot from simvision

(1) cpu_CLA.v

1-877-CDS-4911 or send email to support@cadence.com For more information on Cadence's Verilog-XL product line send email to talkv@cadence.com Compiling source file "gscl45nm.v"
Compiling source file "tb_cpu.v"
Compiling source file "final.v"
Highest level modules: BUFX4 CLKBUF2 CLKBUF3 DFFNEGX1 DFFSR FAX1 HAX1 INVX2 LATCH MUX2X1 NAND3X1 NOR3X1 OAI22X1 OR2X2 TBUFX1 "gscl45nm.v", 299: Timing violation in stimulus.proj.\a/l3/rc30/qout_reg \$setup(negedge D:36017, posedge CLK:36018, 0.09 : 9); L30 "tb_cpu.v": \$finish at simulation time 50100 θ simulation events (use +profile or +listcounts option to count) + 203917 accelerated events + 345566 timing check events CPU time: θ .1 secs to compile + θ .1 secs to link + θ .2 secs in simulation



(2) cpu_CRA.v

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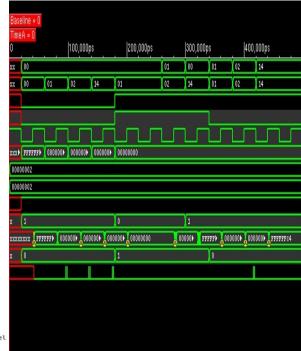
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Compiling source file "gscl45nm.v"
Compiling source file "tb_cpu.v"
Compiling source file "final.v"
Highest level modules:
AUIZIXI
BUFX4
CLKBUF1
CLKBUF2
CLKBUF3
DFFNEGX1
DFFSR
FAX1
HAX1
INVX2
INVX4
LATCH
PUXZX1
NAND3X1
NOR3X1
NOR3X1
OR2X2
TBUFX1
Stimulus

"gscl45nm.v", 299: Timing violation in stimulus.proj.\a/l3/rc30/qout_reg \$setup(negedge D:36017, posedge CLK:36018, 0.09 : 9);

L30 "tb_cpu.v": \$finish at simulation time 50100 0 simulation events (use +profile or +listcounts option to count) + 205645 accelerated events + 345566 timing check events CPU time: 0.1 secs to compile + 0.1 secs to link + 0.2 secs in simulation



(3) cpu_CSA.v

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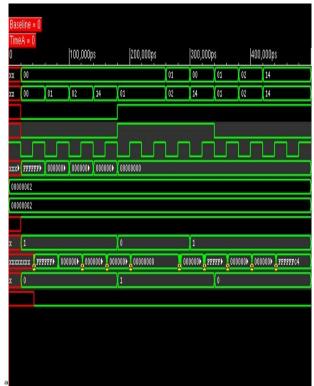
For more information on Cadence's Verilog-XL product line send email to talkv@cadence.com

Compiling source file "gscl45nm.v"
Compiling source file "tb_cpu.v"
Compling source file "final.v"
Highest level modules:
A0121X1
BUFXA
CLKBUF1
CLKBUF2
CLKBUF3
DFFNEGX1
DFFSR
FAX1
HAX1
INVX2
LATCH
MUX2X1
NOR3X1
OA122X1
OA122X1
OA122X1
TBUFX1
stimulus

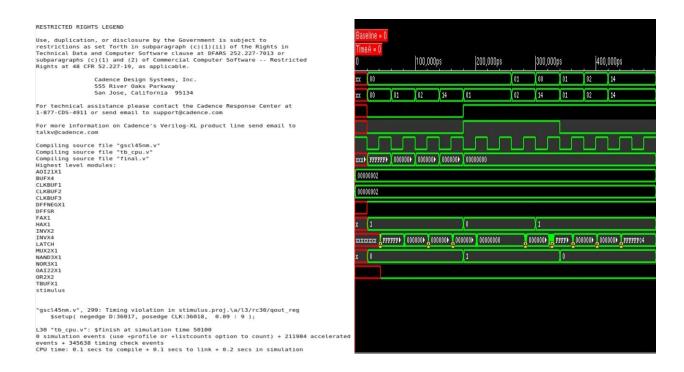
"gscl45nm.v", 299: Timing violation

"gscl45nm.v", 299: Timing violation in stimulus.proj.\a/l3/rc30/qout_reg \$setup(negedge D:36017, posedge CLK:36018, 0.09 : 9);

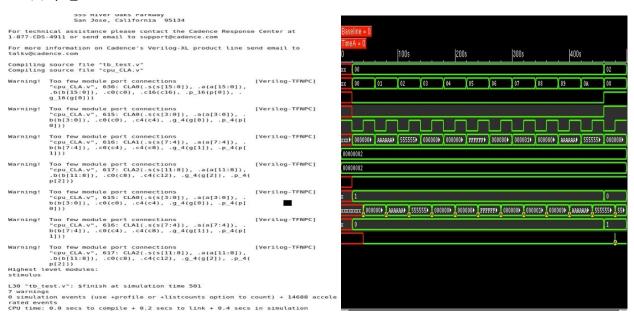
L30 "tb_cpu.v": \$finish at simulation time 50100
0 simulation events (use +profile or +listcounts option to count) + 207877
CPUI time: A 1 serve to commile the 1 serve to link + A 2 serve in simulation



(4) cpu_CSeA.v



- 6) Generate a new test bech file (tb_test.v) for the following instruction set
- See the attached file, "tb_test.v"
- 7) Provide the display screenshot and the text output of the RTL simulation and the screenshot from simvision for each cpu desgin (cpu_CRA.v, cpu_CLA.v, cpu_CSA.v, cpu_CSA.v) with the new generated test bench (tb_test.v)
- (1) cpu_CLA.v



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Compiling source file "cpu_CRA.v" Warning! Too few module port connections
 "cpu_CRA.v", 557: cra0(.sum[7:0]), .c_out(c7)
 , .a(a[7:0]), .b(b[7:0]), .c_in(c_in)) [Verilog-TFNPC] xxxxxxx [000000) [aaaaaa) [555555) [000000] [000000] [797977) [000000] [000001] [000000] [aaaaaa) [555555] [555 [Verilog-TFNPC] [Verilog-TFNPC] c_out(stimulus L30 "tb_test.v": \$finish at simulation time 501 3 warnings θ simulation events (use +profile or +listcounts option to count) + 16246 accele rated events CPU time: $\theta.\theta$ secs to compile + $\theta.1$ secs to link + $\theta.4$ secs in simulation

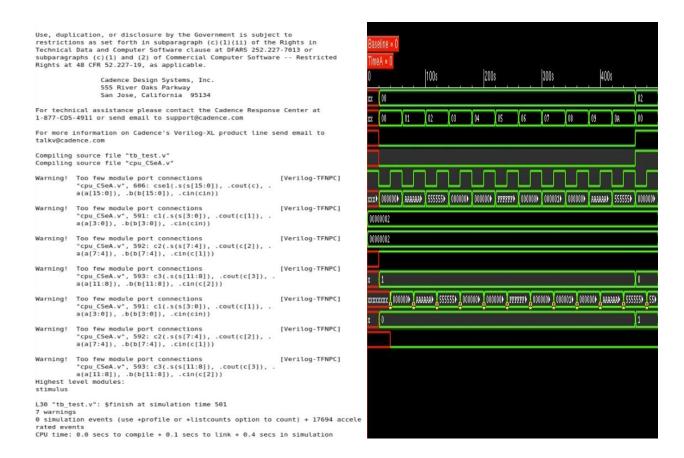
(3) cpu_CSA.v

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 "cpu_CSA.v", 598: cs0_15(.s(s[15:0]), .cout(c), .
 a(a[15:0]), .b(b[15:0]), .cin(cin)) Too few module port connections "cpu_CSA.v", 582: cs0_3(.s(s[3:0]), .cout(c[0]), .a(a[3:0]), .b(b[3:0]), .cin(cin)) Warning! Too few module port connections "cpu_CSA.v", 583: cs4_7(.s(s[7:4]), .cout(c[1]), .a(a[7:4]), .b(b[7:4]), .cin(c[0])) Warning! Too few module port connections "cpu_CSA.v", 584: cs8_l1(.s(s[11:8]), .cout(c[2]) , .a(a[11:8]), .b(b[11:8]), .cin(c[1])) Warning! Too few module port connections "cpu_CSA.v", 582: cs0_3(.s(s[3:0]), .cout(c[0]), .a(a[3:0]), .b(b[3:0]), .cin(cin)) Warning! [Verilog-TFNPC] Warning! Too few module port connections "cpu_C\$A.v", 583: cs4_7(.s{s[7:4]}, .cout(c[1]), .a(a[7:4]), .b(b[7:4]), .cin(c[0])) [Verilog-TFNPC] Warning! Too few module port connections
 "cpu_CSA.v", 584: cs8_l1(.s(s[11:8]), .cout(c[2])
 , .a(a[11:8]), .b(b[11:8]), .cin(c[1]))
Highest level modules: [Verilog-TFNPC]

rated events CPU time: $\theta.\theta$ secs to compile + $\theta.1$ secs to link + $\theta.4$ secs in simulation

100s 200s 300s 400s 01 104 105 06 Y 09 02 103 Y 07 Y 08 xxxx) 000000) | rarrar) | 555555) | 000000) | 000000) | pppppp) | 000000) | 000001) | 000000) | rarrar) | 555555) | 000000) 00000002 XXXXXXXX 000000) [RARRAR) [555555) [000000) [000000) [FPFFFF] [000000) [000001) [000000) [RARRARA] [555555) [55) 7 warnings θ simulation events (use +profile or +listcounts option to count) + 16304 accele

L30 "tb_test.v": \$finish at simulation time 501



8) Fill out the following performance comparison table after synthesis and analyze the results (explain the reasons of your comparison results)

		CLA(nS)	CRA(nS)	CSA(nS)	CSeA(nS)
	5555_5555 + 5	2.10	2.11	2.19	1.2
	AAAA_AAAA + 5555_5555	2.85	2.90	2.36	1.65
Path Delay for Each	0000_00C8 + 0000_012C	2.45	2.76	2.13	1.70
Operation (Post- Synthesis Gate-Level Delay)	5 + 0000_000A	2.69	2.59	2.18	1.69
	FFFF_FFFF - 0000_0001	2.68	2.4	2.24	2.07
	FFFF_FFFF + 0000_0001	2.55	2.32	2.28	1.85
	5555_5555 - 5	2.13	2.35	1.89	1.64
	AAAA_AAAB + 5555_5555	2.42	2.39	1.8	1.65

- As observed from above that more number of bits to be operated more delay will be there in path.
- CSeA take minimum path delay as it has less data to handle.
- CLA always takes less time to perform operation.

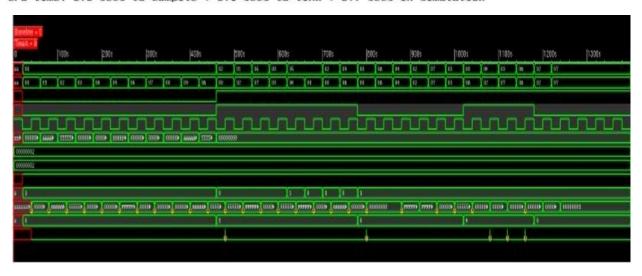
- CASE STUDY 2

- 1) Generate a new test bech file (tb_test_comp.v) for the following instruction set
- See the attached file, "tb_test_comp.v"
- 2) Provide the display screenshot or the text output of the RTL simulation and the screenshot from simvision with the test bench (tb_test_comp.v)
- See the attached file, "cpu_comp.v" which is modified for its right purpose.

```
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Compiling source file "tb_test_comp.v"
Compiling source file "cpu_comp.v"
Warning! Too few module port connections

"cpu_comp.v", 647: CLA0(.s(s[15:0]), .a(a[15:0])

, .b(b[15:0]), .c0(c0), .c16(c16), .p_16(p[0]), .
                                                                                                                             [Verilog-TFNPC]
                     g_16(g[0]))
Warning! Too few module port connections 
"cpu_comp.v", 626: CLAΘ(.s(s[3:0]), .a(a[: b(b[3:0]), .cΘ(cΘ), .c4(c4), .g_4(g[Θ]),
                                                                                                                              [Verilog-TFNPC]
                                                                                                 .a(a[3:0])
Warning! Too few module port connections
"cpu_comp.v", 627: CLA1(.s(s[7:4]), .a(a[7:4]),
b(b[7:4]), .c0(c4), .c4(c8), .g_4(g[1]), .p_4(p[
1]))
                                                                                                                              [Verilog-TFNPC]
                    Too few module port connections "cpu_comp.v", 628: CLA2(.s(s[11:8]), .a(a[11:8]), .b(b[11:8]), .c0(c8), .c4(c12), .g_4(g[2]), .p_4(p[2]))
                                                                                                                              [Verilog-TFNPC]
Warning!
                    Too few module port connections "cpu_comp.v", 626: CLA0(.s(s[3:0]), .a(a[3:0]), b(b[3:0]), .c0(c0), .c4(c4), .g_4(g[0]), .p_4(p[0])
Warning!
                                                                                                                              [Verilog-TFNPC]
                   Too few module port connections "cpu_comp.v", 627: CLA1(.s(s[7:4]), .a(a[7:4]), b(b[7:4]), .c0(c4), .c4(c8), .g_4(g[1]), .p_4(p[1]))
Warning!
                                                                                                                              [Verilog-TFNPC]
Warning! Too few module port connections
"cpu_comp.v", 628: CLA2(.s(s[11:8]), .a(a[11:8]),
, .b(b[11:8]), .c0(c8), .c4(c12), .g_4(g[2]), .
p_4(p[2]))
                                                                                                                              [Verilog-TFNPC]
Highest level modules:
stimulus
Please check Select Lines!
L31 "tb_test_comp.v": $finish at simulation time 1401
7 warnings
0 simulation events (use +profile or +listcounts option to count) + 131981 accelerated events
CPU time: 0.0 secs to compile + 0.1 secs to link + 0.7 secs in simulation
```



3) Synthesize the design and summarize cell.rep and timing.rep

```
Updating timing information
Information: Updating design information... (UID-85)
  Beginning Mapping Optimizations (Medium effort) (Incremental)
  Beginning Incremental Implementation Selection
  Beginning Delay Optimization Phase
                          WORST NEG TOTAL NEG DESIGN SLACK SLACK RULE COST

9.00 0.0 3.0
9.00 0.0 3.0
9.00 0.0 3.0
              49385.8 0.00
49385.8 0.00
49385.8 0.00
   ELAPSED
                                                                          ENDPOINT
     TIME
                                                    3.0
3.0
3.0
     0:00:01
  Beginning Design Rule Fixing (max_capacitance)
ELAPSED WORST NEG TOTAL NEG DESIGN
TIME AREA SLACK SLACK RULE COST END
6:00:02 49385.8 0.00 0.0 3.0
Loading db file '/apps/FreePDK45/osu_soc/lib/files/gscl45nm.db'
Warning: Design 'cpu' contains 1 high-fanout nets. A fanout number of 1000 will be used for delay calcu
lations involving these nets. (TIM-134)
Net 'clk': 1625 load(s), 1 driver(s)
#report_constraint -all_violators
set filename [format "%s%s" $my_toplevel ".vh"]
set filename i...
cpu.vh
write -f verilog -output $filename
Writing verilog file '/home/ykim/ece429/project/CASE2/cpu.vh'.
set filename [format "%s%s" $my_toplevel ".sdc"]
cpu.sdc
write_sdc $filename
#set filename [format "%s%s" $my_toplevel ".db"]
#write -f db -hier -output $filename -xg_force_db
redirect timing.rep { report_timing }
redirect cell.rep { report_cell }
redirect power.rep { report_power }

quit
Thank you...
Elapsed Time = 1:32.26, CPU Time = 84.779
 Cell rep x
mmOpn/ops/m0/qout_reg
mmOpn/ops/m1/qout_reg
mmOpn/outs/m0/qout_reg
mmOpn/outs/m1/qout_reg
mmOpn/outs/m2/qout_reg
                                                DFFP05X1
                                                                              gscl45nm
                                                                                                            7.978100
                                                                                                           7.978100
7.978100
                                                DFFP0SX1
                                                                              gscl45nm
                                                DFFP0SX1
                                                                              gscl45nm
                                                                                                                              n
                                                                                                           7.978100
7.978100
                                                DFFP0SX1
                                                                              gscl45nm
                                                DFFP0SX1
                                                                              gscl45nm
                                                                                                                             n
 o/tr/t0/bl
o/tr/t1/bl
                                                 TBUFX2
                                                                              gscl45nm
                                                                                                           3.754400 3.754400
                                                                              ascl45nm
                                                 TBUFX2
                                                                                                                             n
 o/tr/t2/b1
o/tr/t3/b1
                                                 TBUFX2
                                                                              gscl45nm
                                                                                                           3.754400
                                                                                                           3.754400
                                                 TBUFX2
                                                                              ascl45nm
                                                                                                                             n
 o/tr/t4/bl
                                                 TBUFX2
                                                                              gscl45nm
                                                                                                           3.754400
 o/tr/t5/b1
                                                                                                           3.754400
                                                                             gscl45nm
gscl45nm
                                                 TBUFX2
                                                                                                                             n
 o/tr/t6/bl
                                                                                                           3.754400
                                                 TBUFX2
                                                                                                                              n
                                                                             gscl45nm
gscl45nm
                                                                                                           3.754400
 o/tr/t7/bl
                                                 TBUFX2
                                                                                                                             n
 o/tr/t8/bl
                                                 TBUFX2
                                                                                                                             n
 o/tr/t9/b1
o/tr/t10/b1
                                                 TBUFX2
                                                                             gscl45nm
gscl45nm
                                                                                                           3.754400
                                                                                                           3.754400
                                                 TBUFX2
                                                                                                                             n
 o/tr/t11/b1
o/tr/t12/b1
                                                                             gscl45nm
gscl45nm
                                                 TRUEX2
                                                                                                           3.754400
                                                                                                           3.754400
                                                 TBUFX2
                                                                                                                             n
 o/tr/t13/b1
o/tr/t14/b1
                                                TRUEX2
                                                                              gscl45nm
                                                                                                           3.754400
                                                                              gscl45nm
                                                                                                           3.754400
                                                 TBUFX2
                                                                                                                             n
 o/tr/t15/b1
o/tr/t16/b1
                                                 TBUFX2
                                                                              gscl45nm
                                                                                                           3.754400
                                                                              gscl45nm
                                                                                                           3.754400
                                                 TBUFX2
                                                                                                                             n
 o/tr/t17/b1
o/tr/t18/b1
                                                 TBUFX2
                                                                              gscl45nm
                                                                                                           3.754400
                                                 TBUFX2
                                                                              gscl45nm
                                                                                                           3.754400
                                                                                                                             n
 o/tr/t19/b1
o/tr/t20/b1
                                                                              gscl45nm
                                                                                                           3.754400
                                                 TBUFX2
                                                                                                           3.754400
                                                 TBUFX2
                                                                              gscl45nm
                                                                                                                             n
 o/tr/t21/b1
                                                                              gscl45nm
                                                                                                           3.754400
                                                 TBUFX2
                                                                                                                              n
 o/tr/t22/bl
                                                                                                           3.754400
                                                 TBUFX2
                                                                              gscl45nm
                                                                                                                             n
 o/tr/t23/b1
                                                                              gscl45nm
                                                                                                           3.754400
 o/tr/t24/bl
```

wb/bd/me0/qout_reg
wb/bd/me1/qout_reg
wb/bd/me2/qout_reg
wb/bd/me3/qout_reg
wb/bd/me4/qout_reg 7.978100 7.978100 gscl45nm DFFP0SX1 ascl45nm n DFFP0SX1 gscl45nm 7.978100 49385.845973 Total 14678 cells

TRUFX2

TBUFX2

TBUFX2

TBUFX2

TBUFX2

TBUFX2

TRIIFX2

TBUFX2

DFFP0SX1

DFFP0SX1

DFFP0SX1

o/tr/t25/b1

o/tr/t26/bl o/tr/t27/bl

o/tr/t28/bl o/tr/t29/bl

o/tr/t30/bl o/tr/t31/bl

gscl45nm gscl45nm

gscl45nm gscl45nm

gscl45nm gscl45nm

gscl45nm gscl45nm

gscl45nm

gscl45nm

3.754400

3.754400

3.754400

3.754400

3.754400 3.754400

3.754400 3.754400

7.978100 7.978100

n

n

n

n

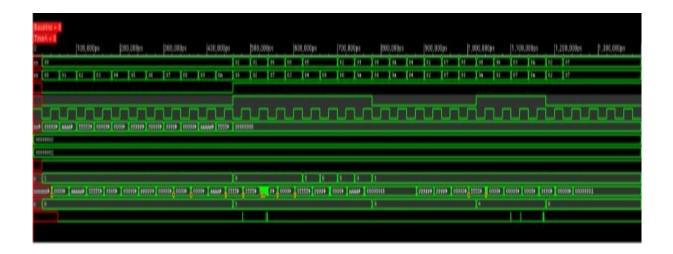
n

n

```
### Timing.rep * ### Ti
☐ timing.rep ×
                                                                                                                                                                                                                        0.06
                                                                                                                                                                                                                        0.07
                                                                                                                                                                                                                                                                                4.74 r
                                                                                                                                                                                                                                                                                4.80
                                                                                                                                                                                                                        0.06
                                                                                                                                                                                                                        0.07
                                                                                                                                                                                                                                                                                4.87
                                                                                                                                                                                                                        0.06
                                                                                                                                                                                                                                                                                4.93
                                                                                                                                                                                                                        0.07
                                                                                                                                                                                                                                                                                5.01
                                                                                                                                                                                                                       0.06
                                                                                                                                                                                                                                                                               5.07
                                                                                                                                                                                                                       0.07
                                                                                                                                                                                                                                                                                5.14
                                                                                                                                                                                                                                                                               5.20
                                                                                                                                                                                                                       0.06
                                                                                                                                                                                                                       0.07
                                                                                                                                                                                                                                                                               5.33
                                                                                                                                                                                                                       0.06
                                                                                                                                                                                                                        0.06
                                                                                                                                                                                                                                                                                5.40
                                                                                                                                                                                                                       0.05
                                                                                                                                                                                                                                                                               5.45
       01348/Y (X0R2X1)
a/l3/f2308/U5/Y (XNOR2X1)
a/l3/f2308/U5/Y (XOR2X1)
a/l3/f2308/U2/Y (XOR2X1)
a/l3/f247/U5/Y (XNOR2X1)
a/l3/f256/U5/Y (XNOR2X1)
a/l3/f256/U5/Y (XNOR2X1)
a/l3/f265/U5/Y (XNOR2X1)
a/l3/f265/U5/Y (XNOR2X1)
a/l3/f274/U5/Y (XNOR2X1)
a/l3/f274/U5/Y (XNOR2X1)
a/l3/f283/U5/Y (XNOR2X1)
a/l3/f283/U5/Y (XNOR2X1)
a/l3/f292/U5/Y (XNOR2X1)
a/l3/f292/U2/Y (XOR2X1)
u1784/Y (AND2X1)
                                                                                                                                                                                                                        0.07
                                                                                                                                                                                                                                                                               5.52
                                                                                                                                                                                                                        0.06
                                                                                          (XNOR2X1)
                                                                                                                                                                                                                                                                                5.58
                                                                                                                                                                                                                      0.07
                                                                                                                                                                                                                                                                               5.65
                                                                                                                                                                                                                       0.06
                                                                                                                                                                                                                                                                               5.71
                                                                                                                                                                                                                       0.07
                                                                                                                                                                                                                                                                                5.78
                                                                                                                                                                                                                      0.06
                                                                                                                                                                                                                                                                               5.85
                                                                                                                                                                                                                      0.07
                                                                                                                                                                                                                                                                               5.92
                                                                                                                                                                                                                     0.06
                                                                                                                                                                                                                                                                               5.98
                                                                                                                                                                                                                                                                               6.05
                                                                                                                                                                                                                      0.06
                                                                                                                                                                                                                                                                               6.11
                                                                                                                                                                                                                      0.07
                                                                                                                                                                                                                                                                               6.18
                                                                                                                                                                                                                      0.06
                                                                                                                                                                                                                                                                               6.25
                                                                                                                                                                                                                      0.07
                                                                                                                                                                                                                                                                                6.32
                                                                                                                                                                                                                     0.06
0.05
0.03
                                                                                                                                                                                                                                                                               6.38
                                                                                                                                                                                                                                                                               6.43
         U1784/Y
                                              (AND2X1)
                                                                                                                                                                                                                       0.03
                                                                                                                                                                                                                                                                                6.46
        a/l3/rc31/qout_reg/D (DFFPOSX1)
data arrival time
                                                                                                                                                                                                                     0.00
                                                                                                                                                                                                                                                                               6.46
                                                                                                                                                                                                                                                                              6.46
        clock clk (rise edge)
clock network delay (ideal)
a/l3/rc31/qout_reg/CLK (DFFPOSX1)
library setup time
data required time
                                                                                                                                                                                                                 33.00
                                                                                                                                                                                                                                                                         33.00
                                                                                                                                                                                                                  0.00
                                                                                                                                                                                                                                                                          33.00
                                                                                                                                                                                                                        0.00
                                                                                                                                                                                                                                                                          33.00
                                                                                                                                                                                                                                                                          32.94
                                                                                                                                                                                                                   -0.06
                                                                                                                                                                                                                                                                          32.94
                                                                                                _____
         data required time
                                                                                                                                                                                                                                                                       32.94
                                                                                                                                                                                                                                                                          -6.46
         data arrival time
                                                                       -----
         slack (MET)
```

4) Provide the display screenshot or the text output of the post-synthesis simulation and the screenshot from simvision

```
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 talkv@cadence.com
Compiling source file "gscl45nm.v"
Compiling source file "tb_test_comp.v"
Compiling source file "cpu.vh"
Highest level modules:
BUFX4
CLKBUF1
CLKBUF2
 CLKBUF3
DFFNEGX1
DFFSR
FAX1
HAX1
INVX2
INVX4
 INVX8
MUX2X1
 OAT22X1
 TBUFX1
L31 "tb_test_comp.v": $finish at simulation time 140100
0 simulation events (use +profile or +listcounts option to count) + 799830 accel
erated events + 953312 timing check events
CPU time: 0.1 secs to compile + 0.1 secs to link + 0.4 secs in simulation
```



5) Summarize timing.rep.5.final. What is the maximum clock frequency this circuit can run

6) Provide the display screenshot or the text output of the post-P&R simulation and the screenshot from simvision

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Compiling source file "gscl45nm.v"
Compiling source file "tb_test_comp.v"
Compiling source file "final.v"
Highest level modules:
BUFX4
CLKBUF1
CLKBUF2
CLKBUF3
DFFNEGX1
DFFSR
FAX1
HAX1
INVX2
MUX2X1
OAI22X1
OR2X2
TBUFX1

L31 "tb_test_comp.v": \$finish at simulation time 140100
0 simulation events (use +profile or +listcounts option to count) + 810904 accel
erated events + 953312 timing check events
CPU time: 0.1 secs to compile + 0.1 secs to link + 0.4 secs in simulation

