ECE429 Final Project

Case Study for 32-bit Pipelined CPU design with New ALU Architecture

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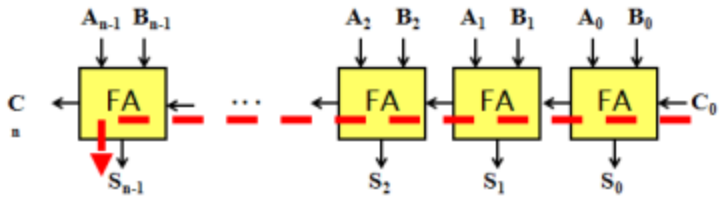
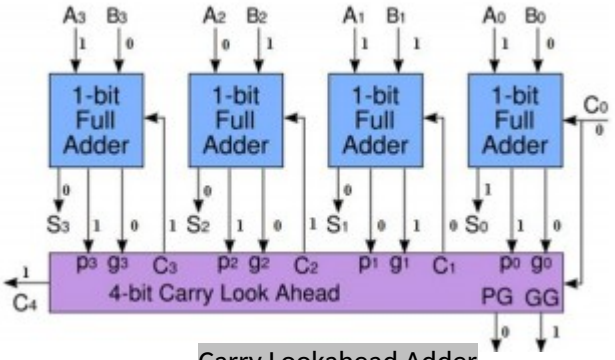
1. Introduction

1.1 Introduction

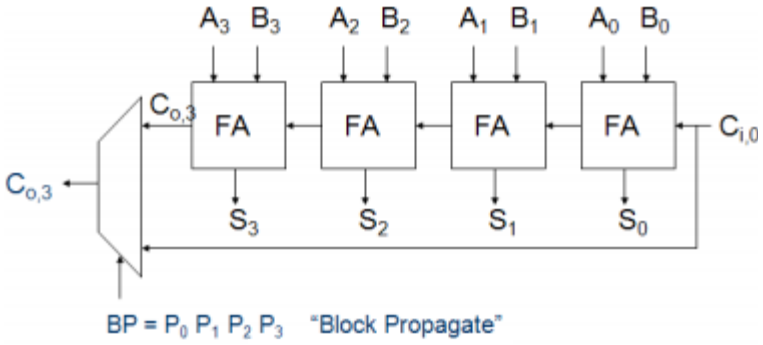
The objective of this final project is to understand a 32-bit pipelined CPU. Data is 32 bits long, and due to pipelining, more than one instruction can be executed at the same time. Synchronization is done via an external clock signal. The instruction signals for addressing the memory file, selecting the ALU operands, and specifying the operation of the ALU are also external. Correct synchronization of those signals determines the minimum operating period.



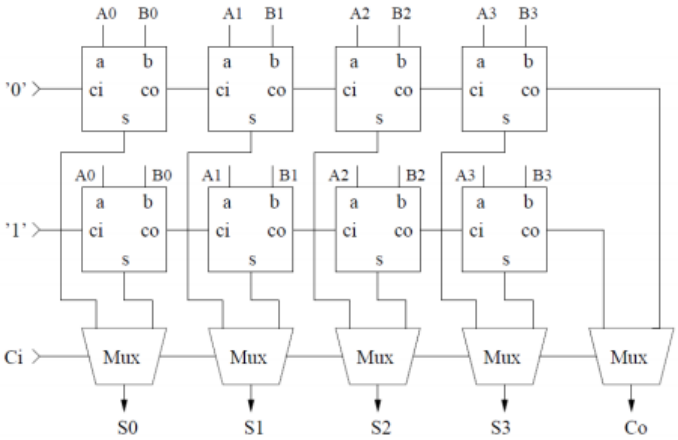
Carry Ripple Adder



Carry Lookahead Adder



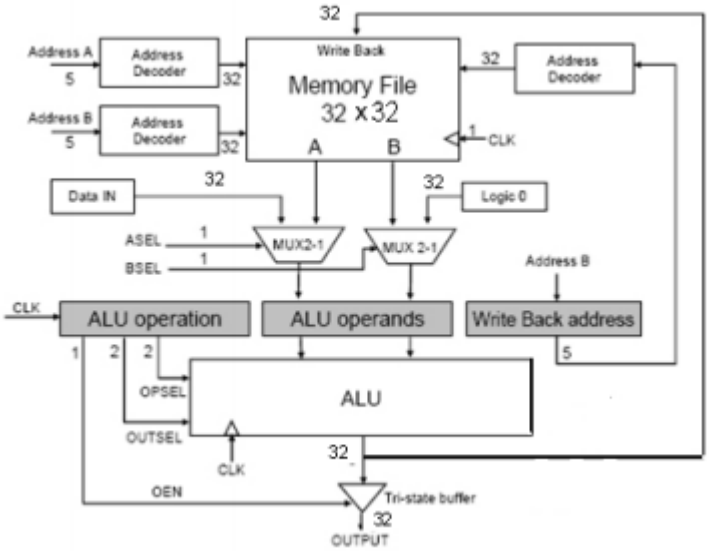
Carry Skip Adder



Carry Select Adder

1.2 Circuit Description

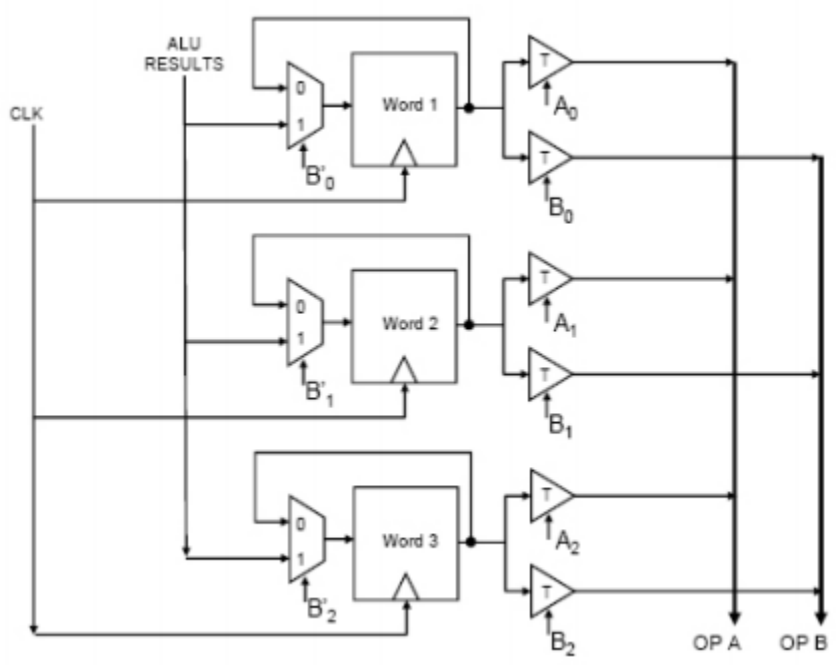
The primary blocks of the CPU are the memory file and the ALU. The external clock signal synchronizes the capture and release of data within the memory file block. Pipelining is accomplished through 2 separate cycles. In the first clock cycle, the two decoders decode the external address selection signals and read the memory ports. Multiplexer blocks also select ALU operation. In the next clock cycle, ALU executes and the result can be read, based upon the value of OEN (output enable) signal. ALU results can be written back in the memory file in Address B.



Overview of the primary blocks and signals

1.3 Memory File

The memory file stores 32 32-bit words. 2 read ports and one write port allow for words to be read in each clock cycle (specified by address A and B), and words to be written into in the next clock cycle. The storing element is a D register, and the output is connected to the two output ports of the memory file through tri-state buffers. The buffers are enabled by address signals A and B. Address B specifies the word address where ALU outputs can be stored as a write.



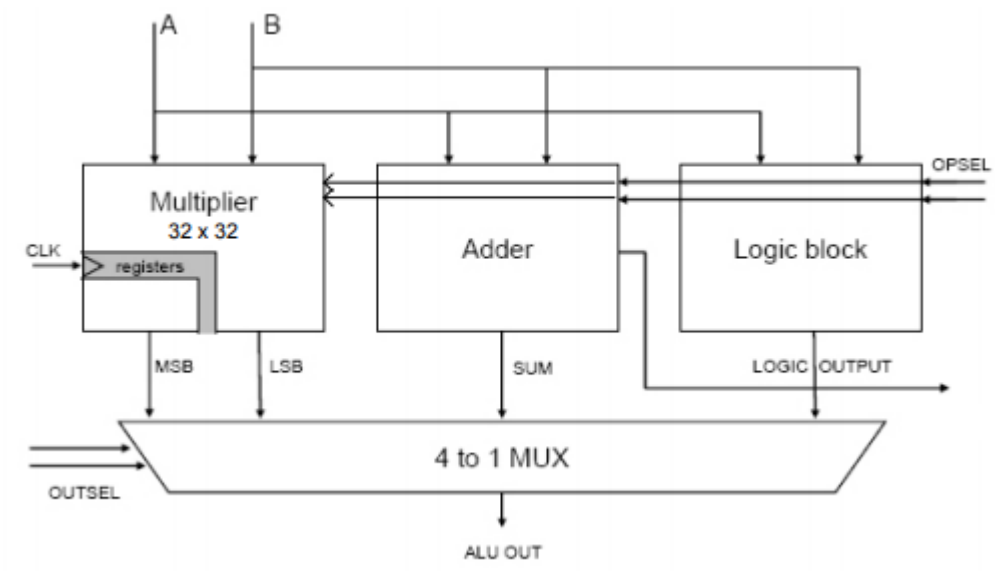
Memory File Configuration

1.4 Arithmetic Logic Unit (ALU)

The ALU can perform the following functions:

- Multiplication
- Addition
- Subtraction
- Logic OR function
- Logic AND function
- Logic XOR function
- Logix XNOR function

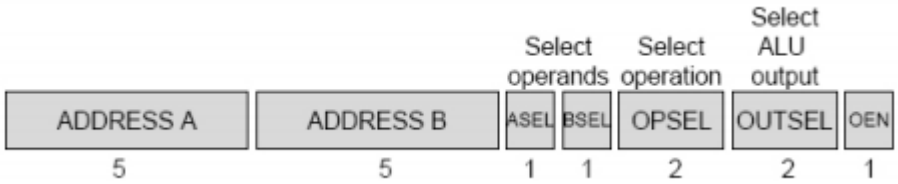
Note that multiplication required 3 clock cycles but is made possible by pipelining the multiplier unit. Also, ALU creates the control output signal for overflow, if needed by the CPU.



Block diagram of the ALU circuit

1.5 Synchronization

Instructions are determined by the external control signals. These signals specify the contents of the memory file and the operands of the ALU. In the second cycle, the control signals determine the operation to be executed by the ALU and thus the value of the ALU output. Results of the ALU are only available if the output enable signal is set. Control signals are set after a positive edge of the clock.



Instruction word contents

Case Study 1

32-bit CPU design with Different Adders – Carry Ripple Adder, Carry Lookahead Adder, Carry Skip Adder, and Carry Select Adder

2. Carry Ripple Adder

2.1 RTL Simulation

Figures 1 and 2 show the RTL simulation results and simvision waveform of CRA against the test bench tb_cpu.v. Besides a few warnings, no errors were encountered showing full functionality.

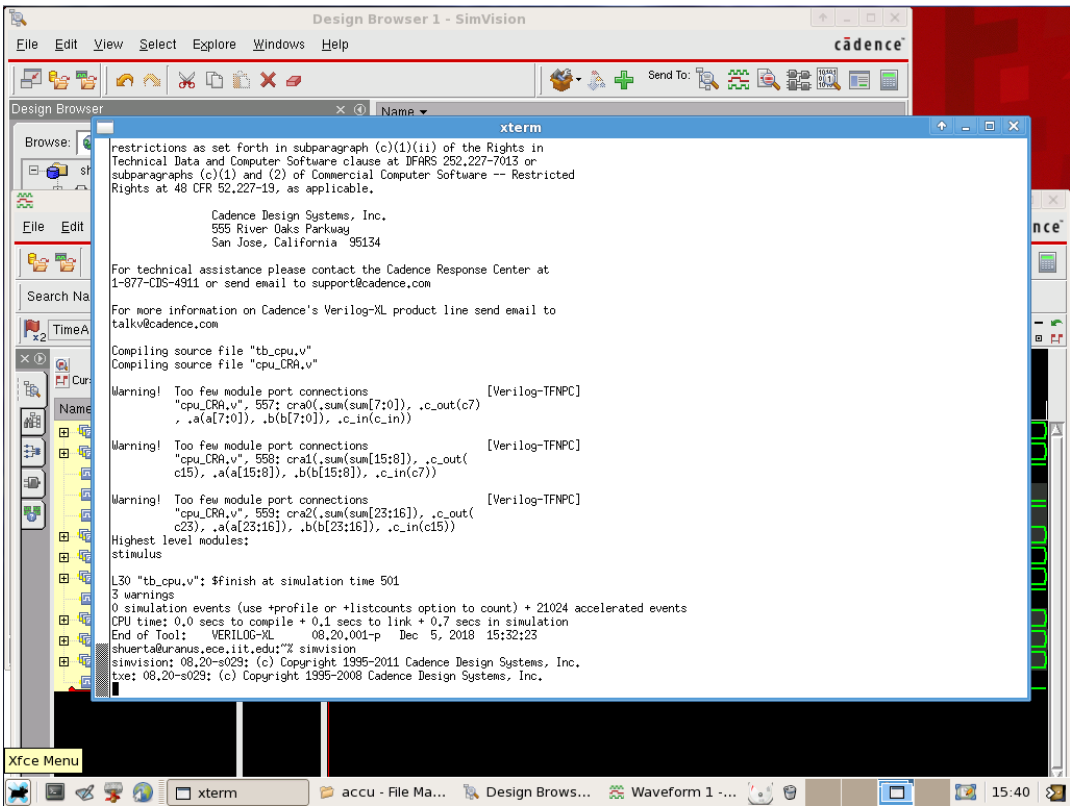


Figure 1: CRA RTL Simulation Results

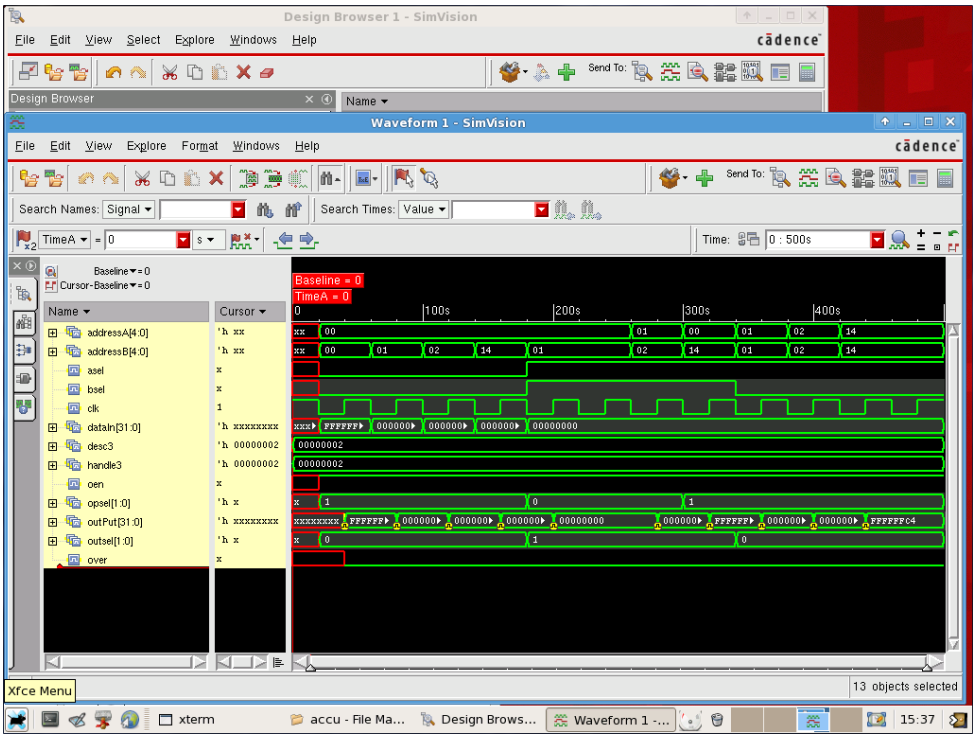


Figure 2: CRA Simvision

2.2 Synthesis

Design Compiler was ran and completed with no errors. Area and timing of the design found in cell.rep and timing.rep files show 14390 cells and a slack time of 29.14. The mapped circuit obtained in cpu.vh was simulated with Verilog models of standard cells and results shown.

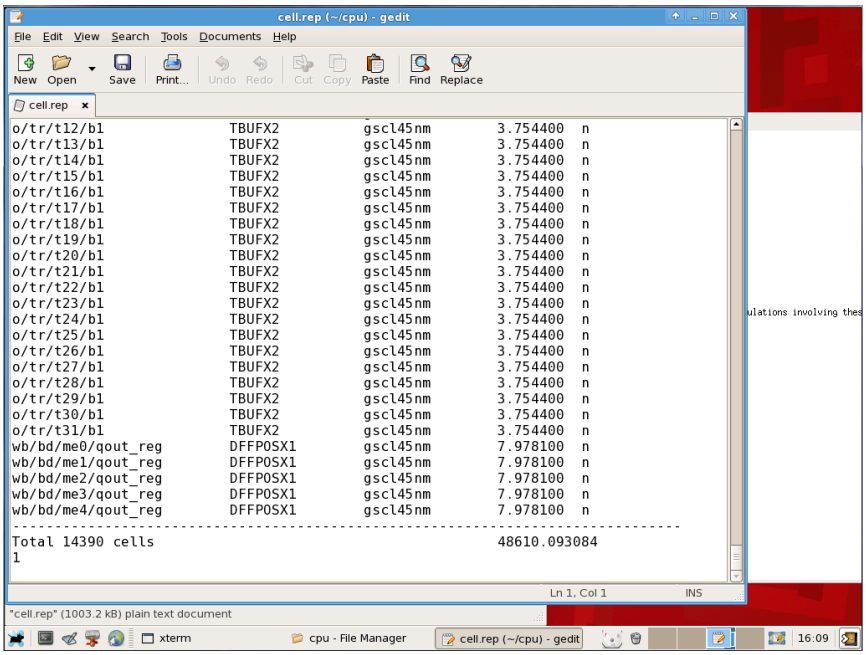


Figure 3: CRA cell.rep

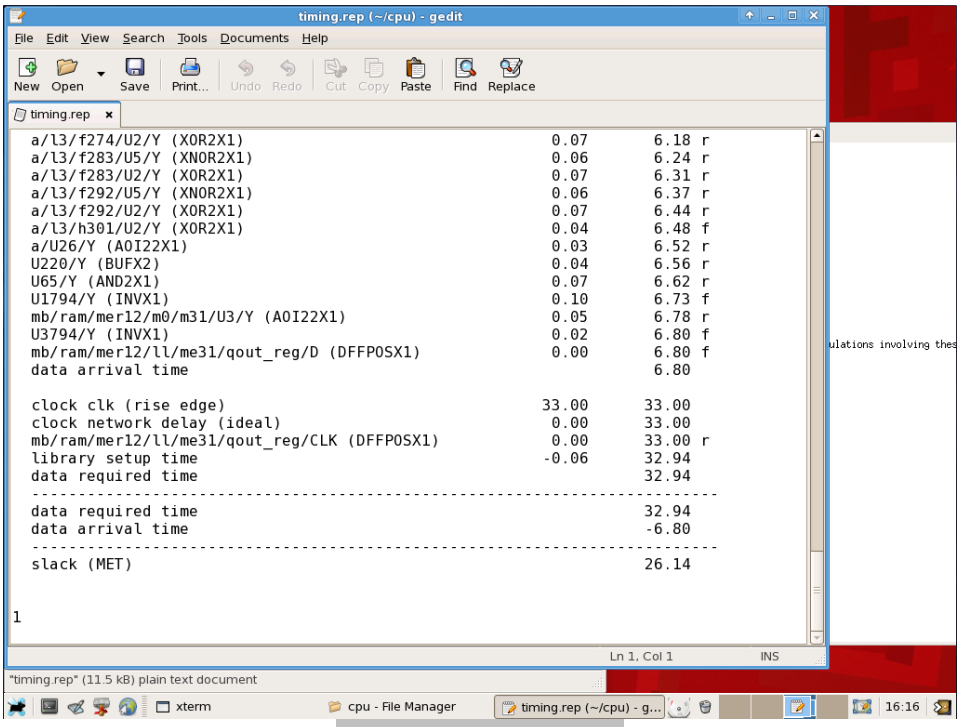


Figure 4: CRA timing.rep

2.3 Post-Synthesis Simulation

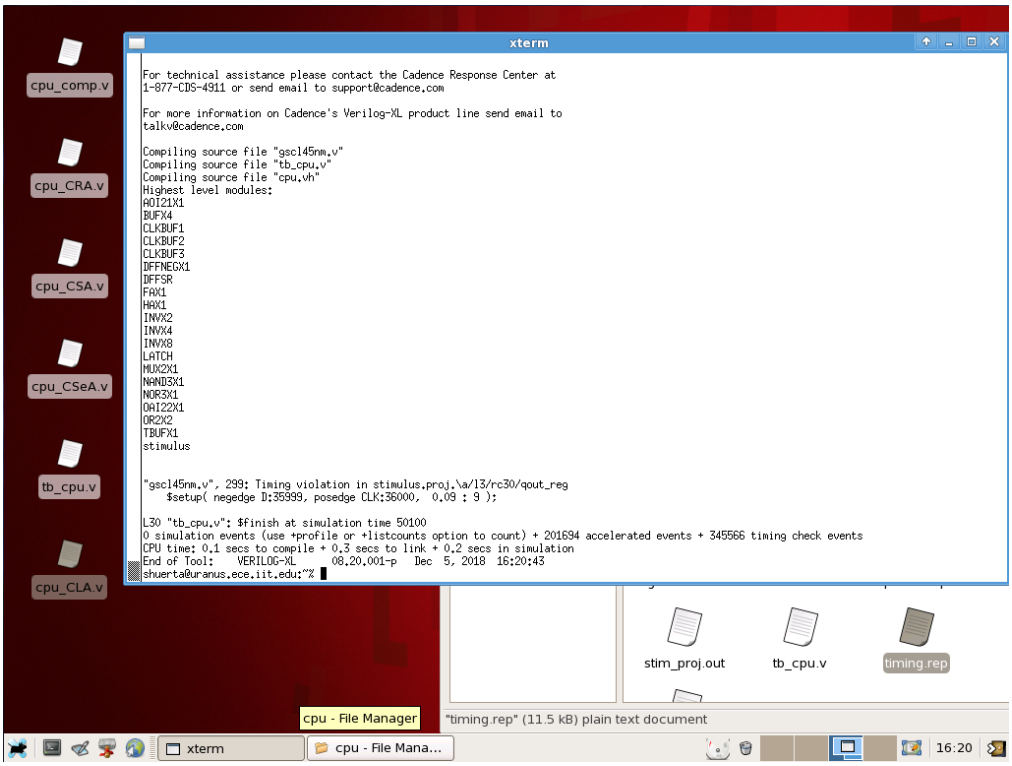


Figure 5: CRA Post-Synthesis Simulation

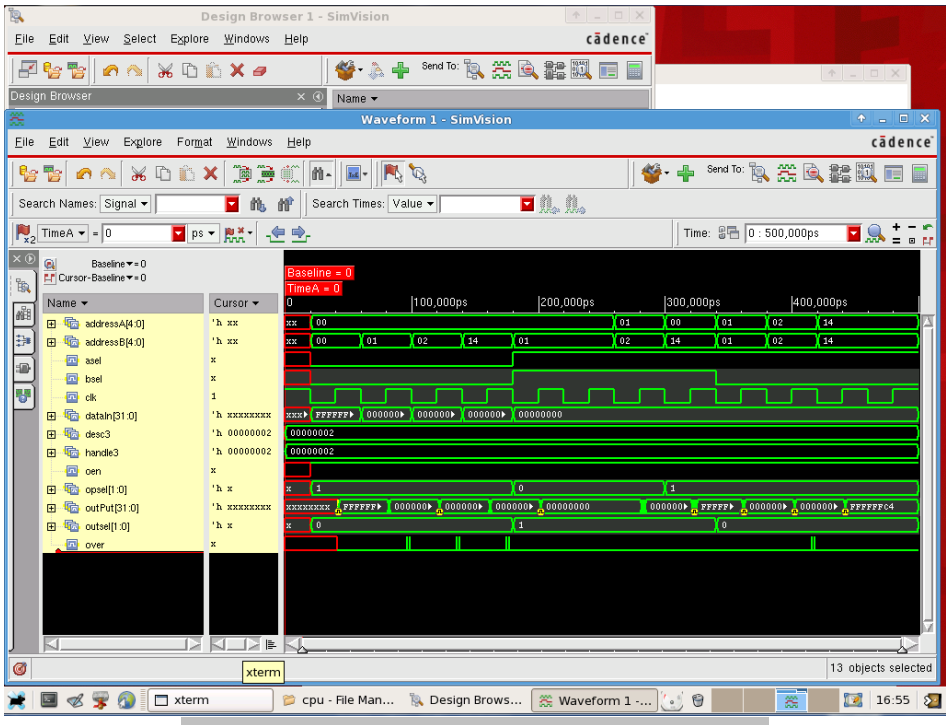
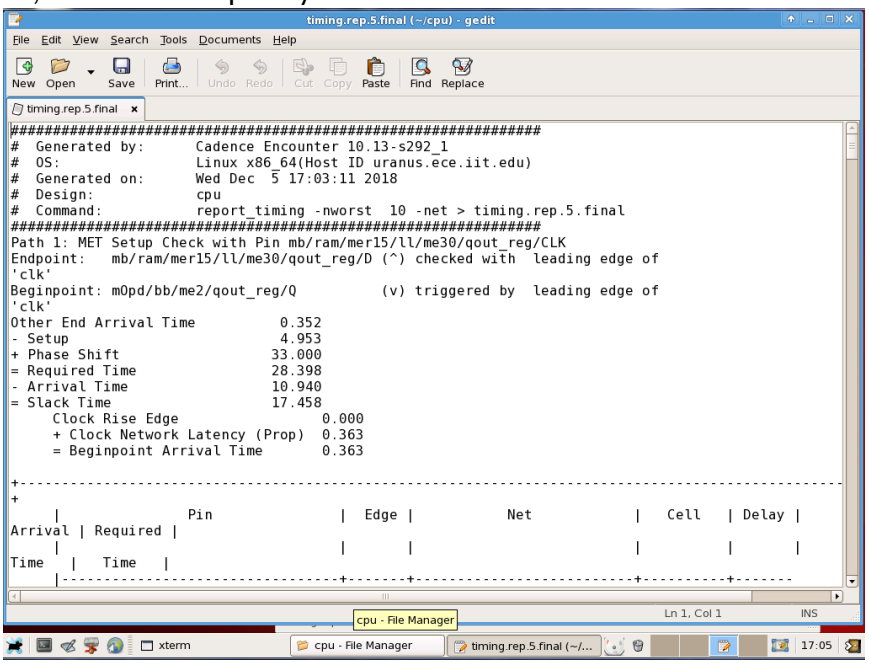


Figure 6: CRA Post-Synthesis Simulation Simvision

2.4 Maximum Clock Frequency

Having layouts for all standard cells, we placed and routed them for the final layout using Encounter. The output of this was used for a simulation, where slack time has decreased to 17.458, which is an improvement. Based off the required time of 28.398, max clock frequency was found to be 35.21MHz.



```
timing.rep.5.final (~/cpu) - gedit
File Edit View Search Tools Documents Help
New Open Save Print... Undo Redo Cut Copy Paste Find Replace
timing.rep.5.final
#############################################################
#  Generated by:      Cadence Encounter 10.13-s292_1
#  OS:                Linux x86_64(Host ID uranus.ece.iit.edu)
#  Generated on:      Wed Dec  5 17:03:11 2018
#  Design:            cpu
#  Command:           report_timing -nworst  10 -net > timing.rep.5.final
#############################################################
Path 1: MET Setup Check with Pin mb/ram/mer15/ll/me30/qout_reg/CLK
Endpoint:   mb/ram/mer15/ll/me30/qout_reg/D (^) checked with  leading edge of
'clk'
Beginpoint: mOpd/bb/me2/qout_reg/Q          (v) triggered by  leading edge of
'clk'
Other End Arrival Time          0.352
- Setup                         4.953
+ Phase Shift                  33.000
= Required Time                28.398
- Arrival Time                 10.940
= Slack Time                   17.458
     Clock Rise Edge                     0.000
     + Clock Network Latency (Prop)  0.363
     = Beginpoint Arrival Time       0.363

+-------------------------------------------------------------------------------------------------------
+
     |              Pin               |  Edge |          Net            |   Cell   | Delay |
Arrival | Required |
     |                                |       |                         |          |       |
Time   |   Time   |
     |--------------------------------+-------+-------------------------+----------+-------
Ln 1, Col 1   INS
cpu - File Manager
xterm   cpu - File Manager   timing.rep.5.final (~/...   17:05
```

Figure 6: CRA timing.rep.5.final

2.5 Post P&R Simulation

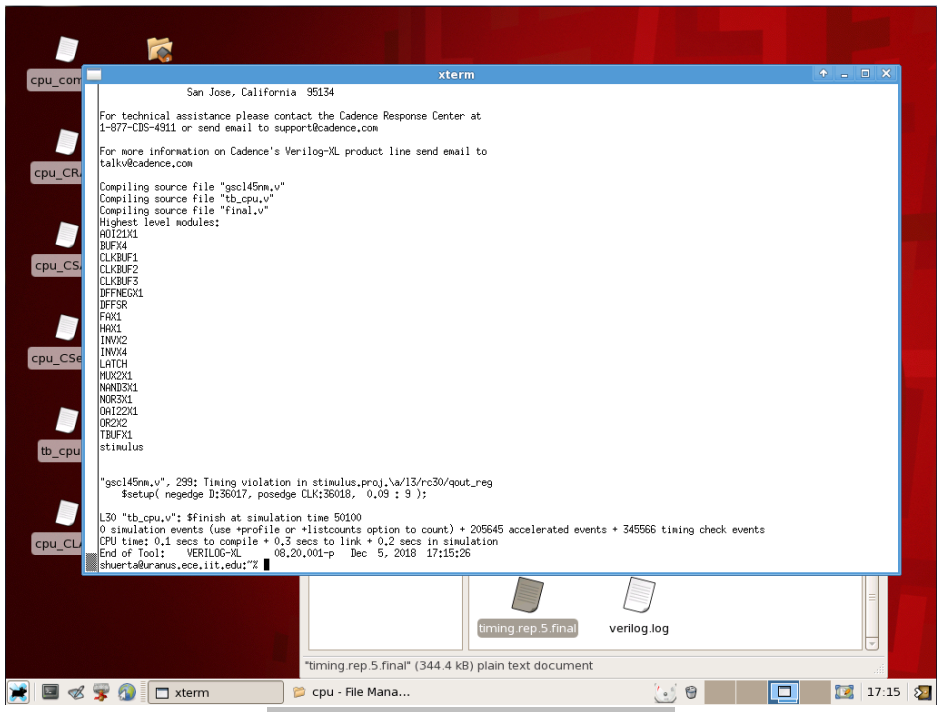


Figure 8: CRA Post P&R Simulation

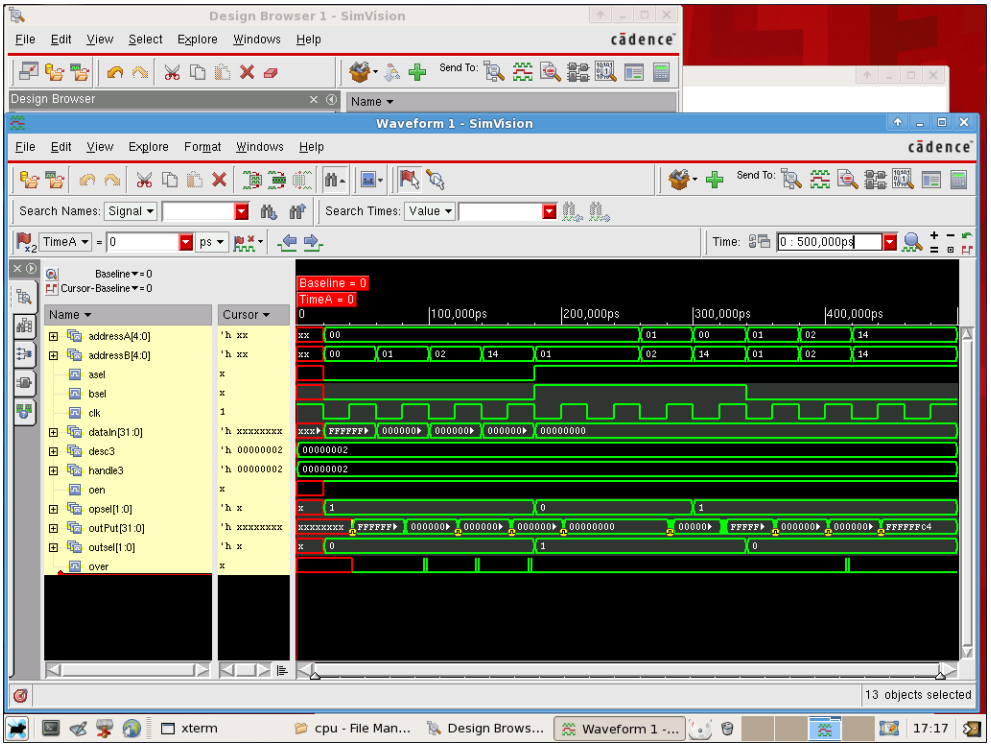


Figure 9: CRA Post P&R Simvision

2.6 New Test Bench

2.6.1 Appendix Figure A

2.7 New Test Bench Results

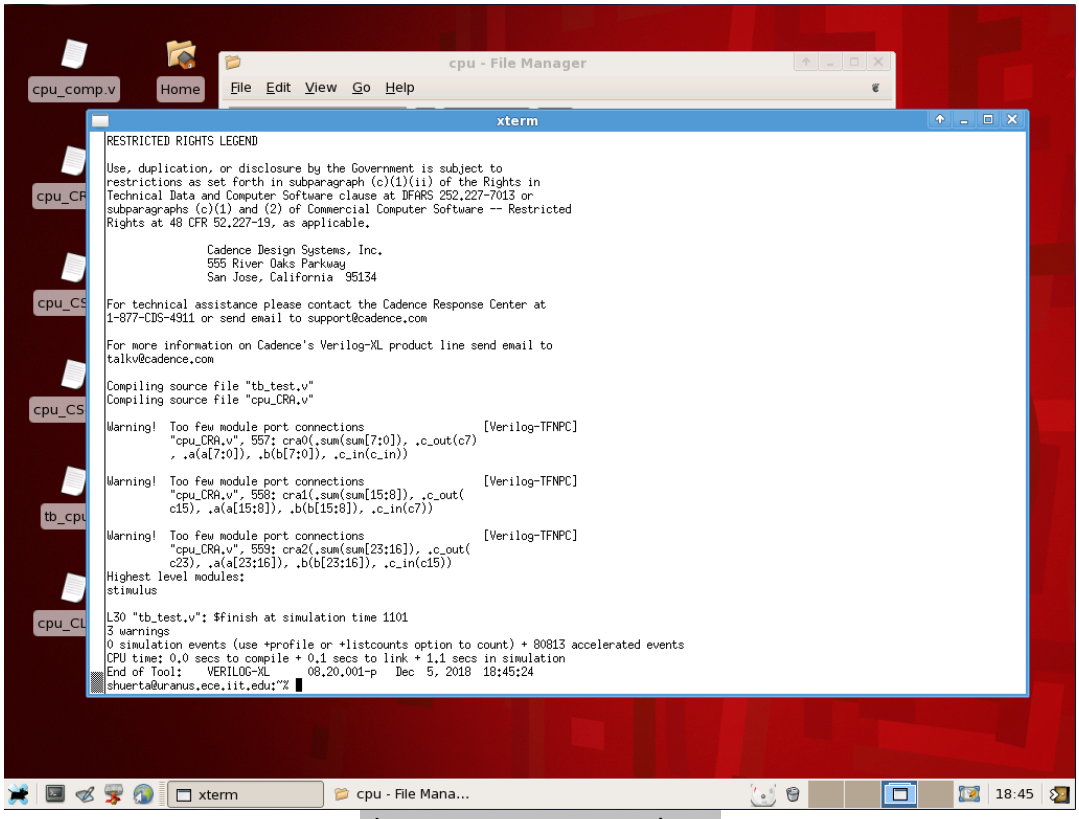


Figure 10: New Test Bench RLT

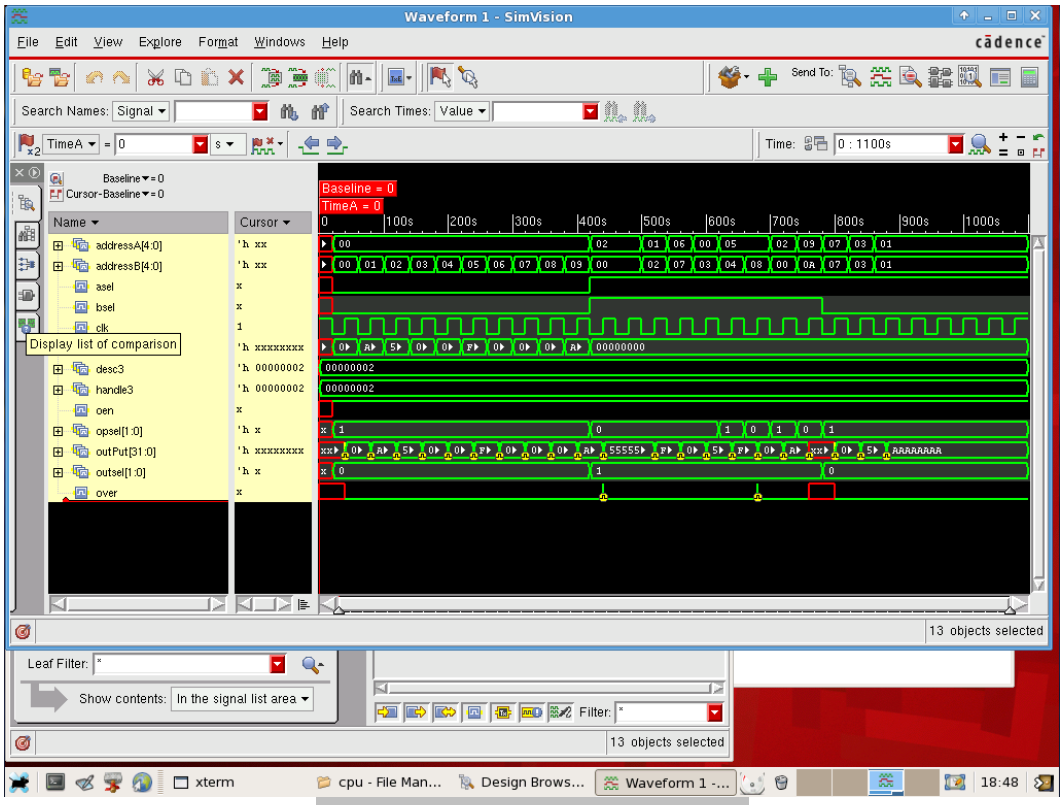


Figure 11: New Test Bench Simvision

3. Carry Lookahead Adder

3.1 RTL Simulation

Figures 12 and 13 show the RTL simulation results and simvision waveform of CLA against the test bench tb_cpu.v. Besides a few warnings, no errors were encountered showing full functionality.

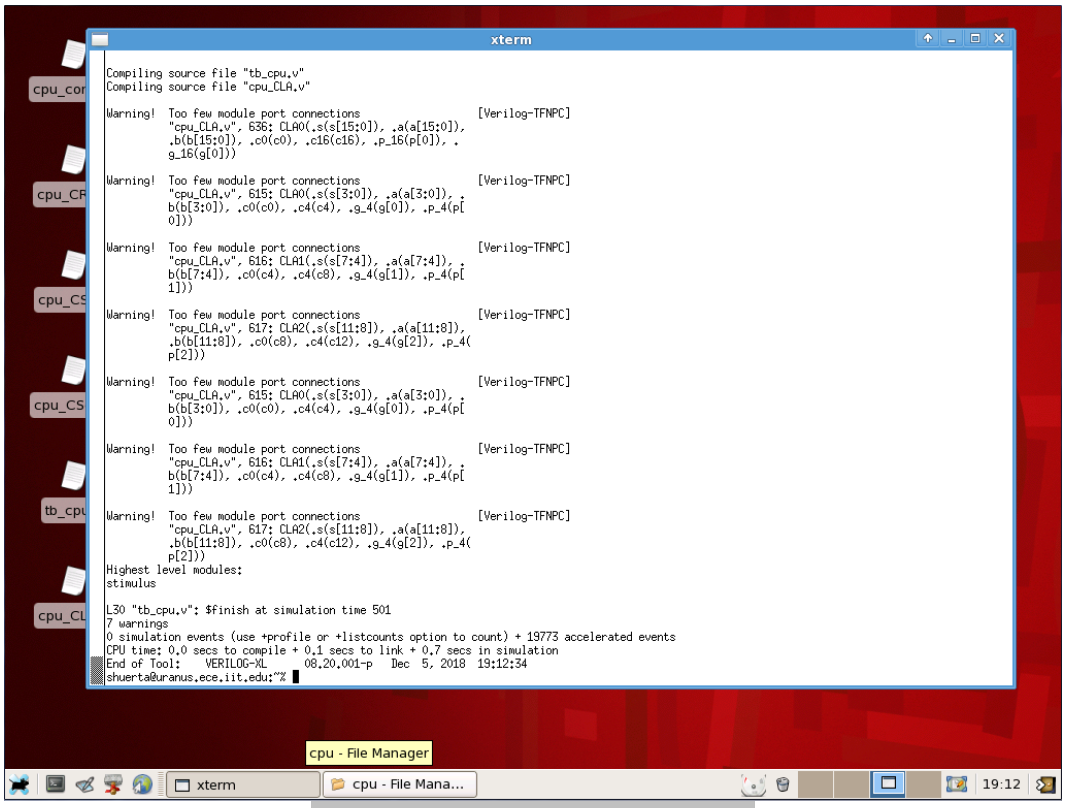


Figure 12: CLA RTL Simulation Results

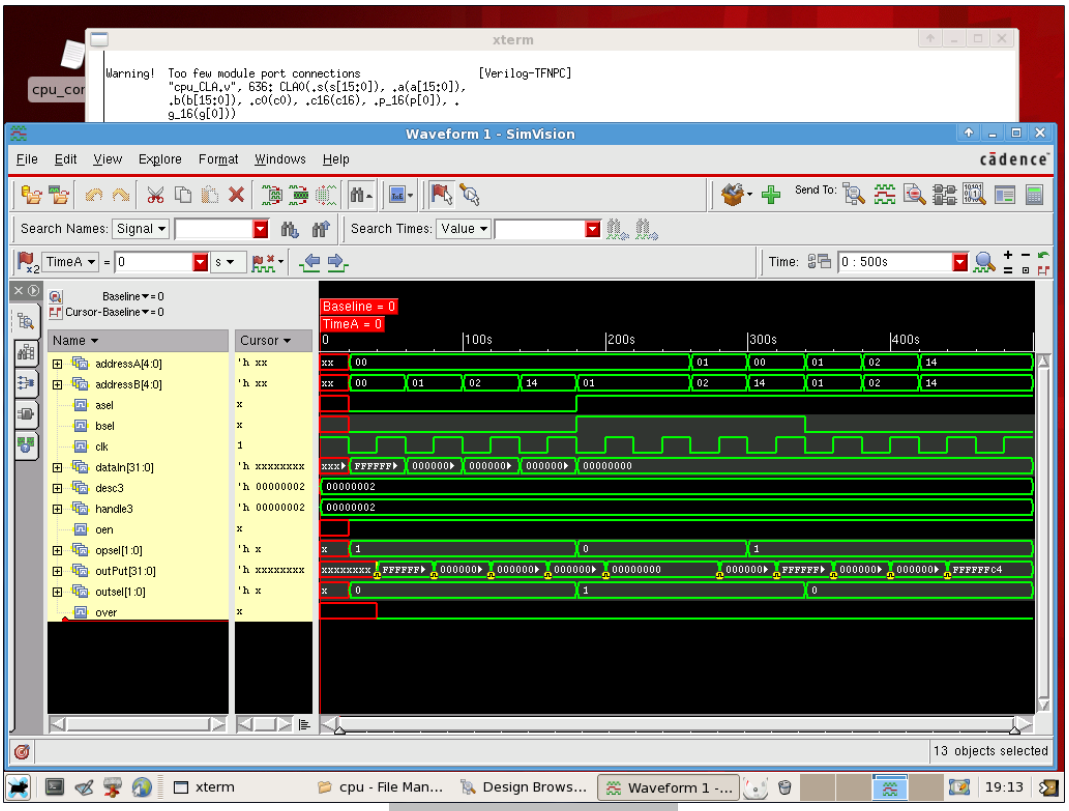
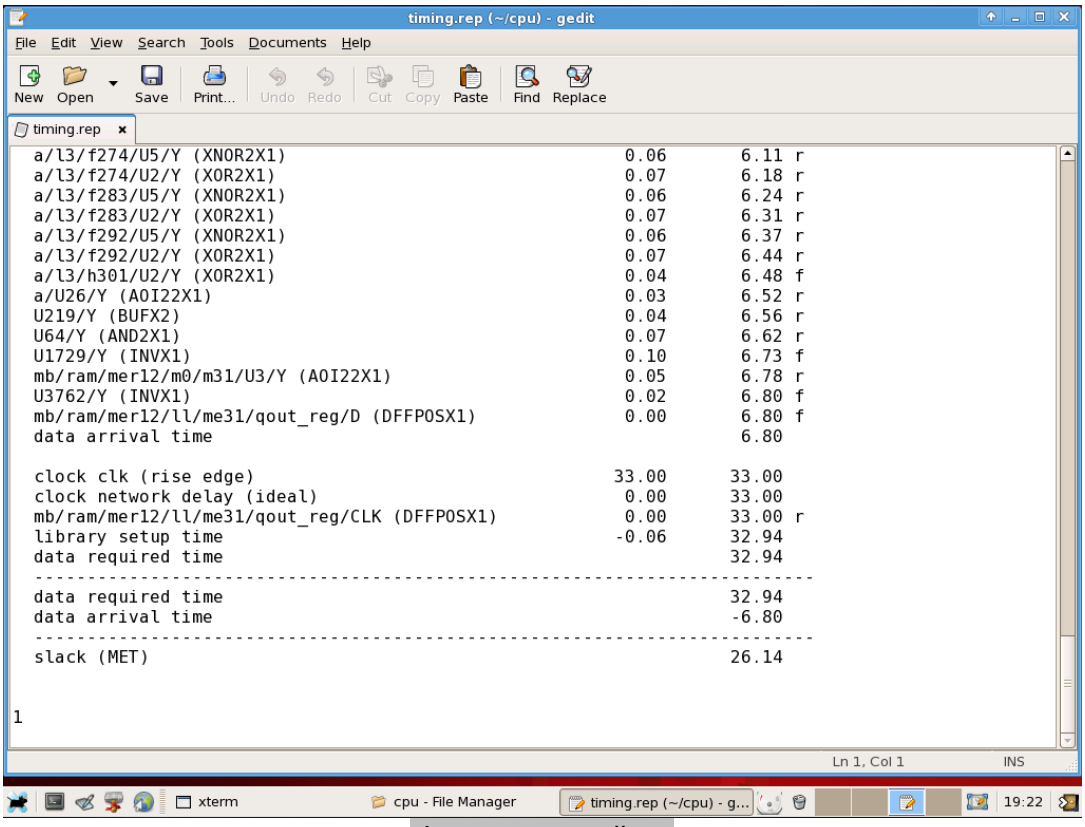


Figure 13: CLA Simvision

3.2 Synthesis

Design Compiler was ran and completed with no errors. Area and timing of the design found in cell.rep and timing.rep files show 14359 cells and a slack time of 26.14. The mapped circuit obtained in cpu.vh was simulated with Verilog models of standard cells and results shown.

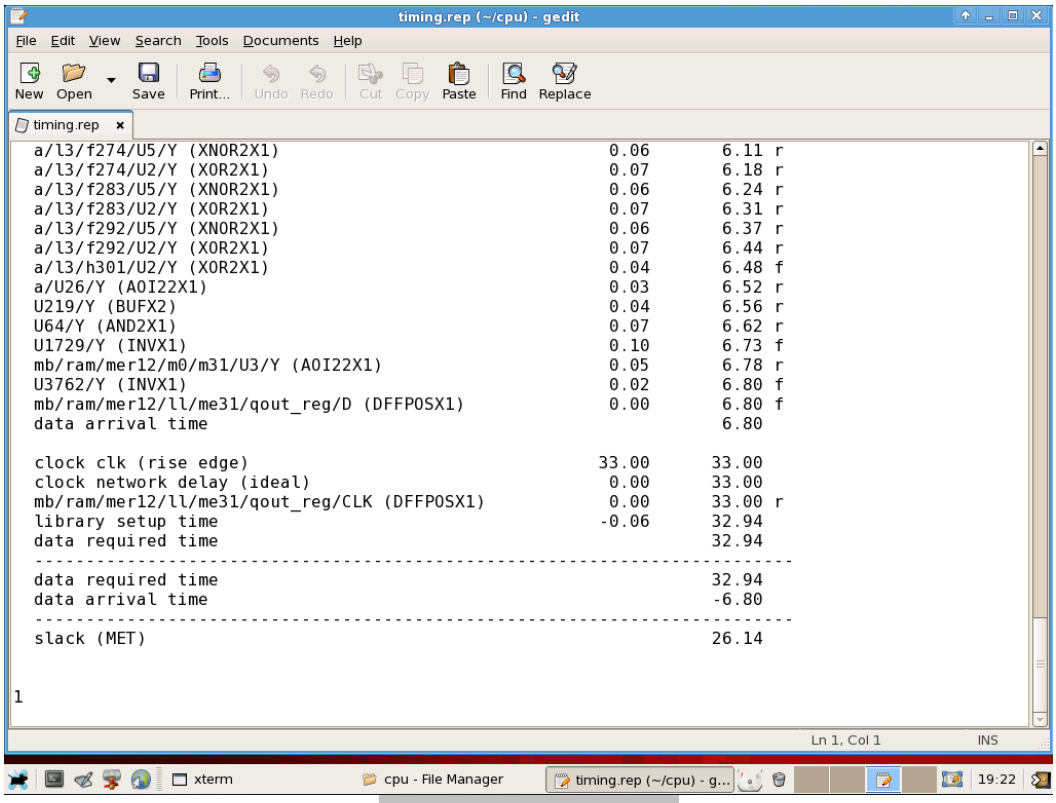


```
a/l3/f274/U5/Y (XNOR2X1)                                  0.06       6.11 r
a/l3/f274/U2/Y (XOR2X1)                                   0.07       6.18 r
a/l3/f283/U5/Y (XNOR2X1)                                  0.06       6.24 r
a/l3/f283/U2/Y (XOR2X1)                                   0.07       6.31 r
a/l3/f292/U5/Y (XNOR2X1)                                  0.06       6.37 r
a/l3/f292/U2/Y (XOR2X1)                                   0.07       6.44 r
a/l3/h301/U2/Y (XOR2X1)                                   0.04       6.48 f
a/U26/Y (AOI22X1)                                         0.03       6.52 r
U219/Y (BUFX2)                                            0.04       6.56 r
U64/Y (AND2X1)                                            0.07       6.62 r
U1729/Y (INVX1)                                           0.10       6.73 f
mb/ram/mer12/m0/m31/U3/Y (AOI22X1)                        0.05       6.78 r
U3762/Y (INVX1)                                           0.02       6.80 f
mb/ram/mer12/ll/me31/qout_reg/D (DFFPOSX1)                0.00       6.80 f
data arrival time                                                    6.80

clock clk (rise edge)                                    33.00      33.00
clock network delay (ideal)                               0.00      33.00
mb/ram/mer12/ll/me31/qout_reg/CLK (DFFPOSX1)              0.00      33.00 r
library setup time                                       -0.06      32.94
data required time                                                  32.94
---------------------------------------------------------------------------
data required time                                                  32.94
data arrival time                                                   -6.80
---------------------------------------------------------------------------
slack (MET)                                                         26.14


1
```

Figure 14: CLA cell.rep



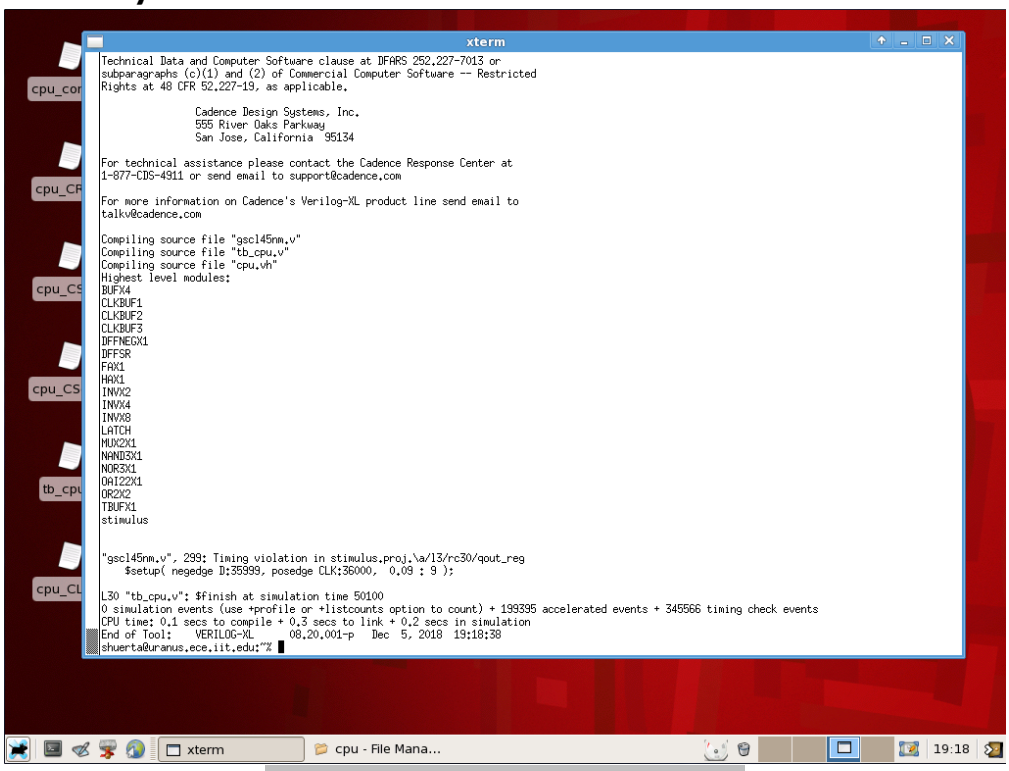
```
a/l3/f274/U5/Y (XNOR2X1)                                  0.06       6.11 r
a/l3/f274/U2/Y (XOR2X1)                                   0.07       6.18 r
a/l3/f283/U5/Y (XNOR2X1)                                  0.06       6.24 r
a/l3/f283/U2/Y (XOR2X1)                                   0.07       6.31 r
a/l3/f292/U5/Y (XNOR2X1)                                  0.06       6.37 r
a/l3/f292/U2/Y (XOR2X1)                                   0.07       6.44 r
a/l3/h301/U2/Y (XOR2X1)                                   0.04       6.48 f
a/U26/Y (AOI22X1)                                         0.03       6.52 r
U219/Y (BUFX2)                                            0.04       6.56 r
U64/Y (AND2X1)                                            0.07       6.62 r
U1729/Y (INVX1)                                           0.10       6.73 f
mb/ram/mer12/m0/m31/U3/Y (AOI22X1)                        0.05       6.78 r
U3762/Y (INVX1)                                           0.02       6.80 f
mb/ram/mer12/ll/me31/qout_reg/D (DFFPOSX1)                0.00       6.80 f
data arrival time                                                    6.80

clock clk (rise edge)                                    33.00      33.00
clock network delay (ideal)                               0.00      33.00
mb/ram/mer12/ll/me31/qout_reg/CLK (DFFPOSX1)              0.00      33.00 r
library setup time                                       -0.06      32.94
data required time                                                  32.94
---------------------------------------------------------------------------
data required time                                                  32.94
data arrival time                                                   -6.80
---------------------------------------------------------------------------
slack (MET)                                                         26.14


1
```

Figure 15: CLA timing.rep

3.3 Post-Synthesis Simulation



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For more information on Cadence's Verilog-XL product line send email to
talkv@cadence.com

Compiling source file "gscl45nm.v"
Compiling source file "tb_cpu.v"
Compiling source file "cpu.vh"
Highest level modules:
BUFX4
CLKBUF1
CLKBUF2
CLKBUF3
DFFNEGX1
DFFSR
FAX1
HAX1
INVX2
INVX4
INVX8
LATCH
MUX2X1
NAND3X1
NOR3X1
OAI22X1
OR2X2
TBUFX1
stimulus


"gscl45nm.v", 299: Timing violation in stimulus.proj.\a/l3/rc30/qout_reg
    $setup( negedge D:35999, posedge CLK:36000,  0.09 : 9 );

L30 "tb_cpu.v": $finish at simulation time 50100
0 simulation events (use +profile or +listcounts option to count) + 199395 accelerated events + 345566 timing check events
CPU time: 0.1 secs to compile + 0.3 secs to link + 0.2 secs in simulation
End of Tool:    VERILOG-XL    08.20.001-p   Dec  5, 2018  19:18:38
shuerta@uranus.ece.iit.edu:~%
```

Figure 16: CLA Post-Synthesis Simulation

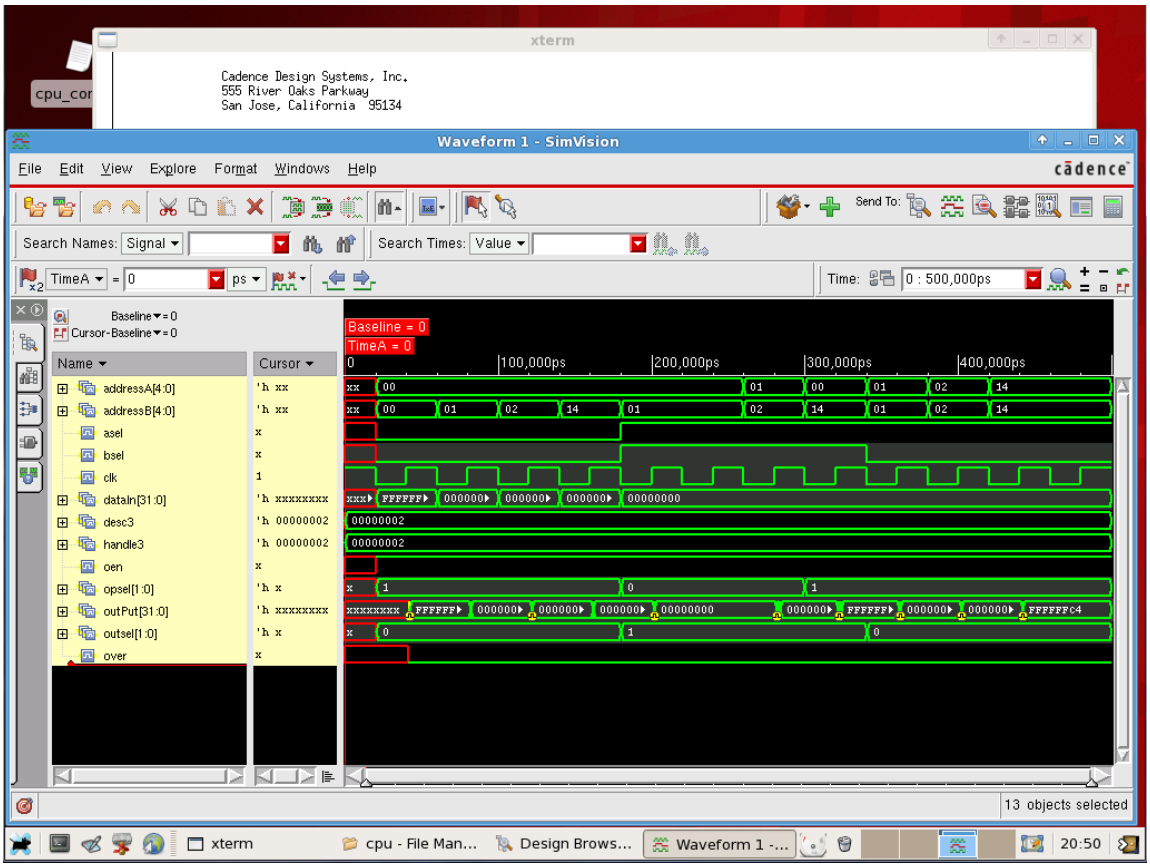


Figure 17: CLA Post-Synthesis Simulation Simvision

3.4 Maximum Clock Frequency

Having layouts for all standard cells, we placed and routed them for the final layout using Encounter. The output of this was used for a simulation, where slack time has decreased to 17.921, which is an improvement. Based off required time of 28.846, max clock frequency was found to be 34.67MHz.

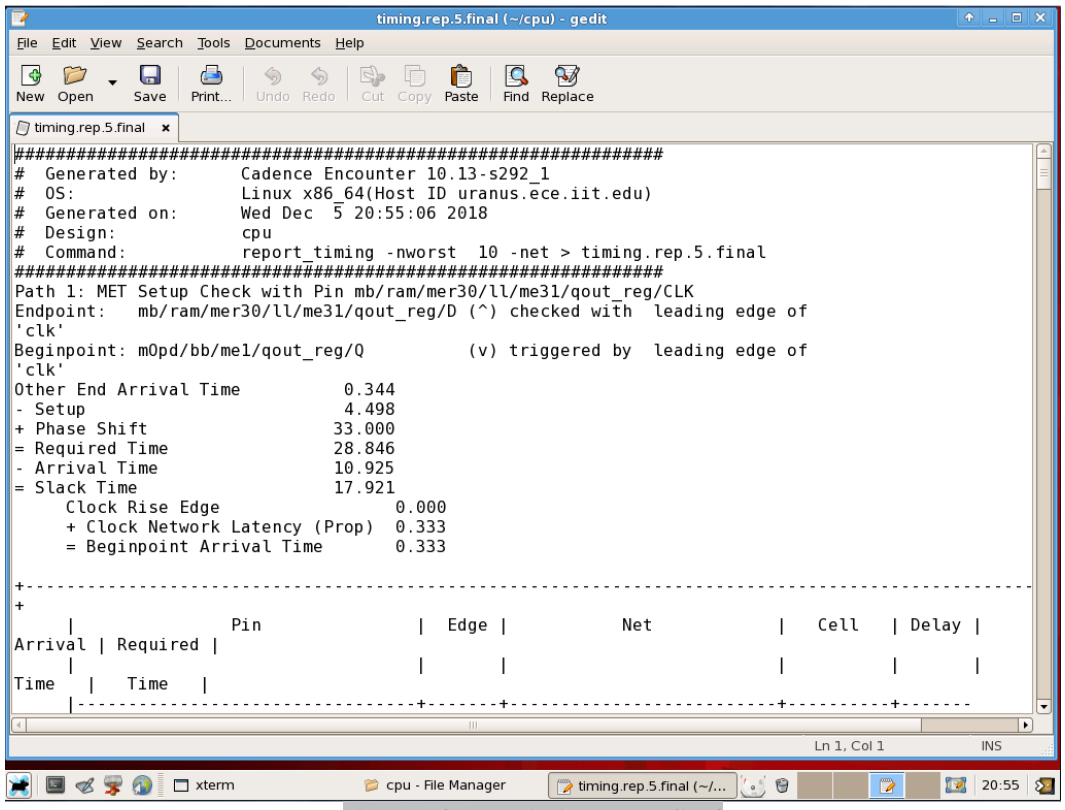


Figure 18: CLA timing.rep.5.final

3.5 Post P&R Simulation

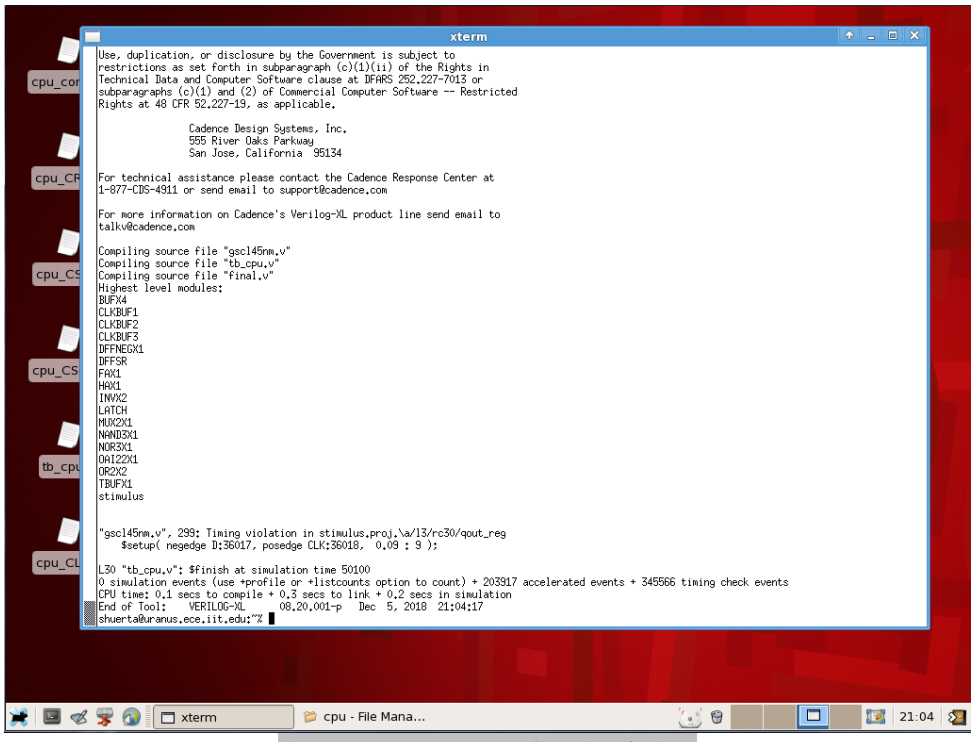


Figure 19: CLA Post P&R Simulation

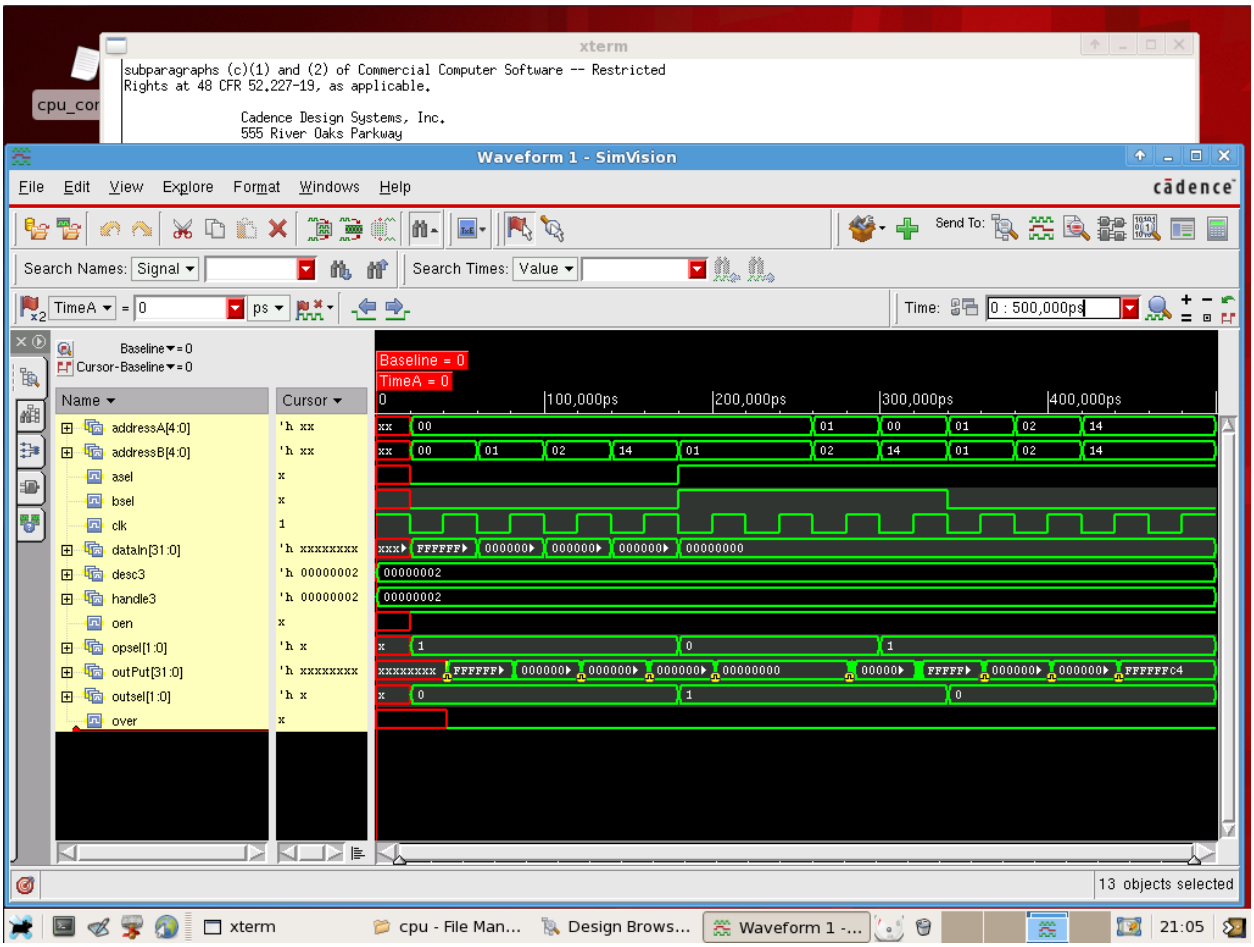


Figure 20: CLA Post P&R Simvision

3.6 New Test Bench

3.6.1 Appendix Figure A

3.7 New Test Bench Results

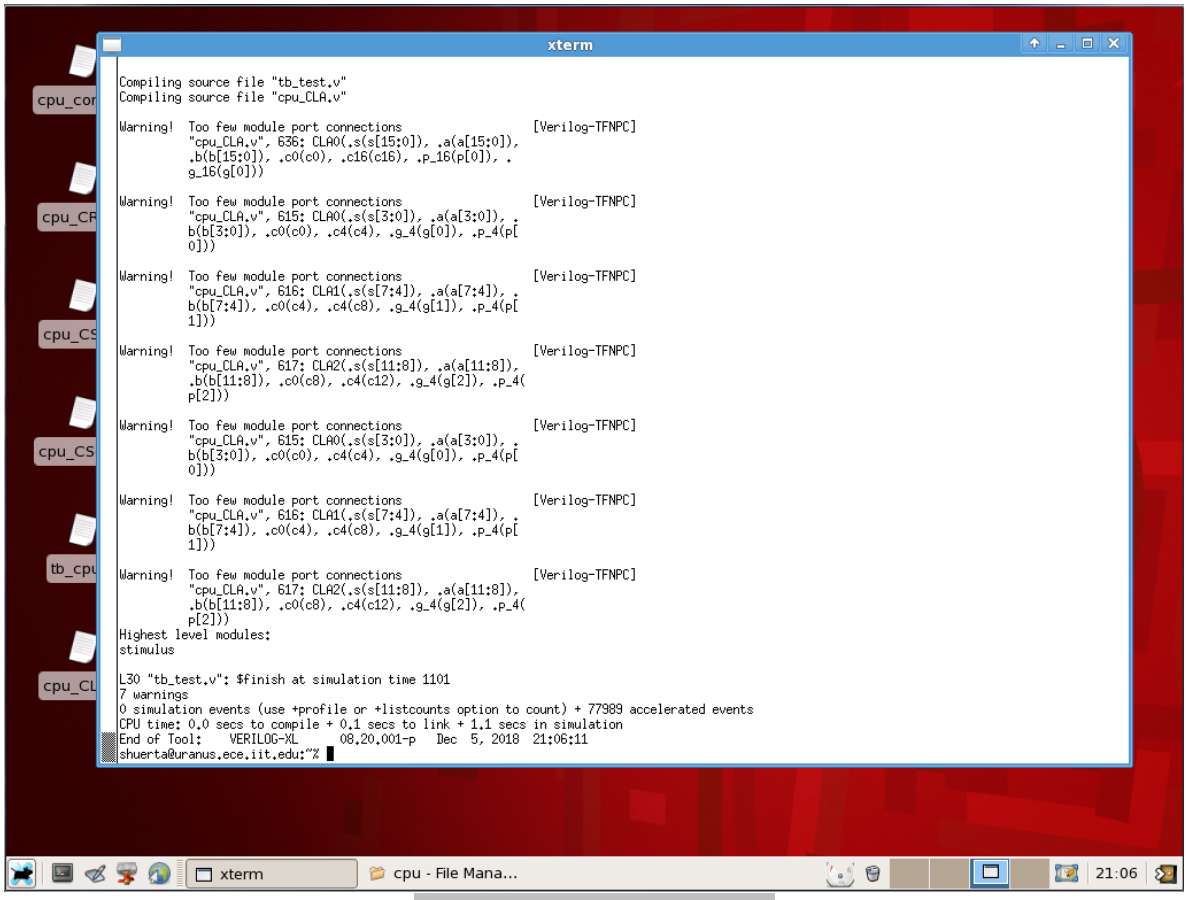


Figure 21: New Test Bench RLT

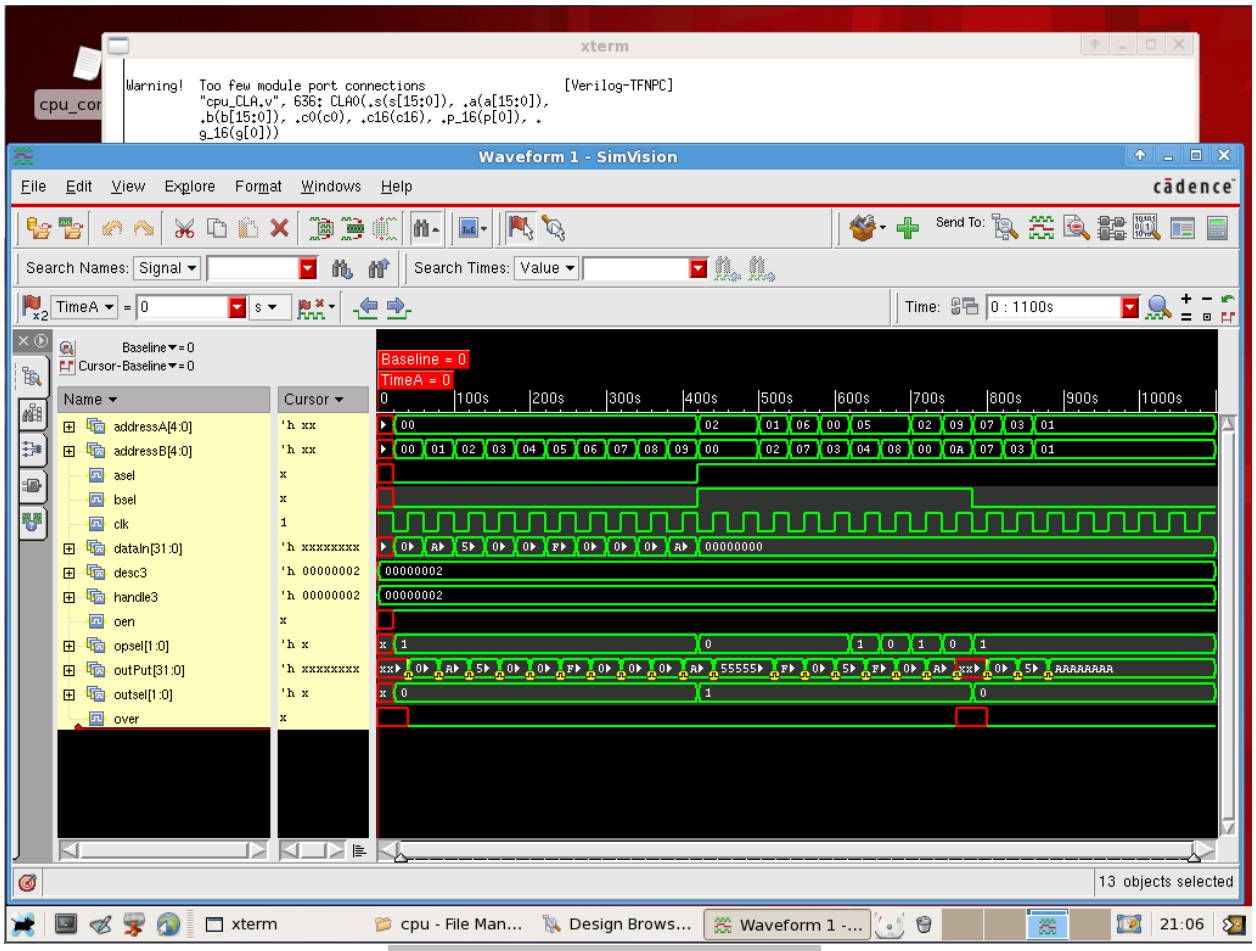


Figure 22: New Test Bench Simvision

4. Carry Skip Adder

4.1 RTL Simulation

Figures 23 and 24 show the RTL simulation results and simvision waveform of CSA against the test bench tb_cpu.v. Besides a few warnings, no errors were encountered showing full functionality.

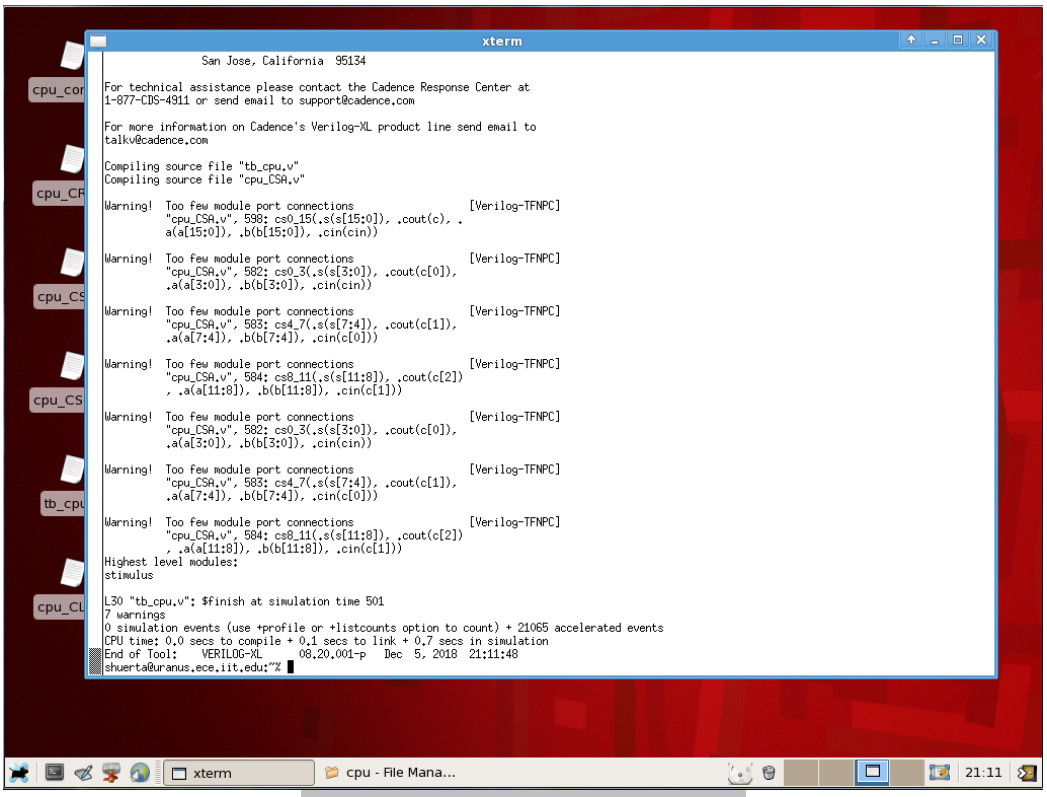


Figure 23: CSA RTL Simulation Results

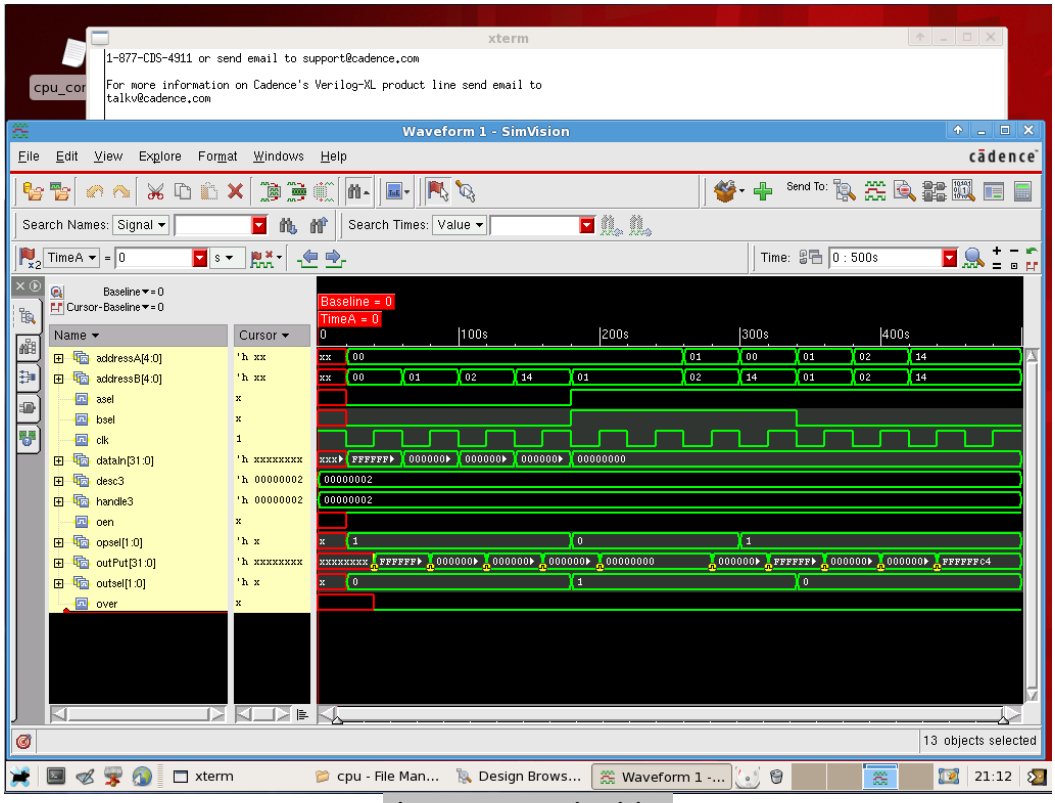
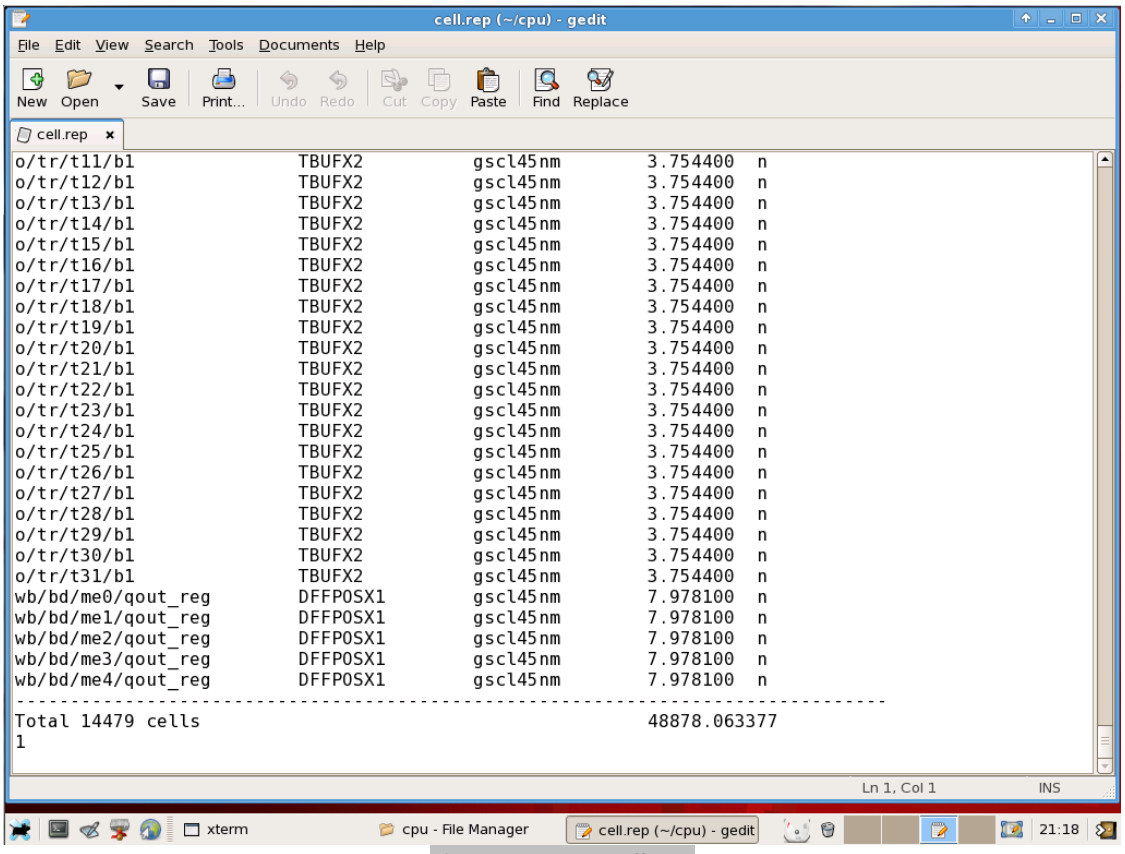


Figure 24: CSA Simvision

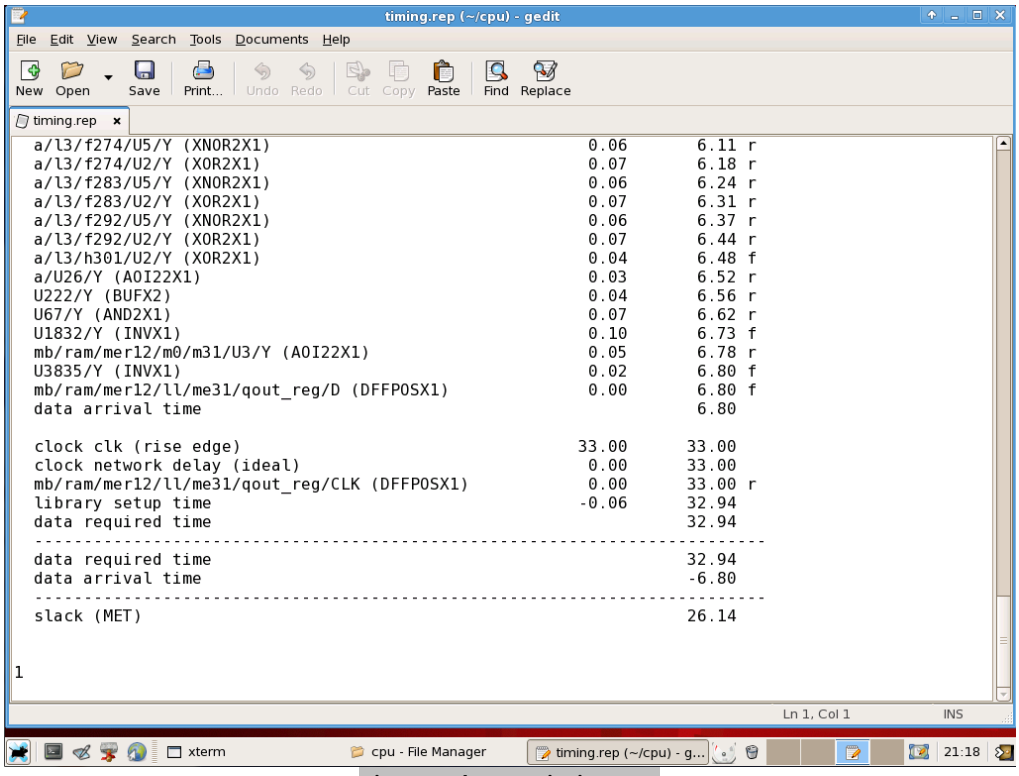
4.2 Synthesis

Design Compiler was ran and completed with no errors. Area and timing of the design found in cell.rep and timing.rep files show 14479 cells and a slack time of 26.14. The mapped circuit obtained in cpu.vh was simulated with Verilog models of standard cells and results shown.



```
o/tr/t11/b1                TBUFX2          gscl45nm        3.754400  n
o/tr/t12/b1                TBUFX2          gscl45nm        3.754400  n
o/tr/t13/b1                TBUFX2          gscl45nm        3.754400  n
o/tr/t14/b1                TBUFX2          gscl45nm        3.754400  n
o/tr/t15/b1                TBUFX2          gscl45nm        3.754400  n
o/tr/t16/b1                TBUFX2          gscl45nm        3.754400  n
o/tr/t17/b1                TBUFX2          gscl45nm        3.754400  n
o/tr/t18/b1                TBUFX2          gscl45nm        3.754400  n
o/tr/t19/b1                TBUFX2          gscl45nm        3.754400  n
o/tr/t20/b1                TBUFX2          gscl45nm        3.754400  n
o/tr/t21/b1                TBUFX2          gscl45nm        3.754400  n
o/tr/t22/b1                TBUFX2          gscl45nm        3.754400  n
o/tr/t23/b1                TBUFX2          gscl45nm        3.754400  n
o/tr/t24/b1                TBUFX2          gscl45nm        3.754400  n
o/tr/t25/b1                TBUFX2          gscl45nm        3.754400  n
o/tr/t26/b1                TBUFX2          gscl45nm        3.754400  n
o/tr/t27/b1                TBUFX2          gscl45nm        3.754400  n
o/tr/t28/b1                TBUFX2          gscl45nm        3.754400  n
o/tr/t29/b1                TBUFX2          gscl45nm        3.754400  n
o/tr/t30/b1                TBUFX2          gscl45nm        3.754400  n
o/tr/t31/b1                TBUFX2          gscl45nm        3.754400  n
wb/bd/me0/qout_reg         DFFPOSX1        gscl45nm        7.978100  n
wb/bd/me1/qout_reg         DFFPOSX1        gscl45nm        7.978100  n
wb/bd/me2/qout_reg         DFFPOSX1        gscl45nm        7.978100  n
wb/bd/me3/qout_reg         DFFPOSX1        gscl45nm        7.978100  n
wb/bd/me4/qout_reg         DFFPOSX1        gscl45nm        7.978100  n
--------------------------------------------------------------------------------
Total 14479 cells                                          48878.063377
1
```

Figure 25: CSA cell.rep



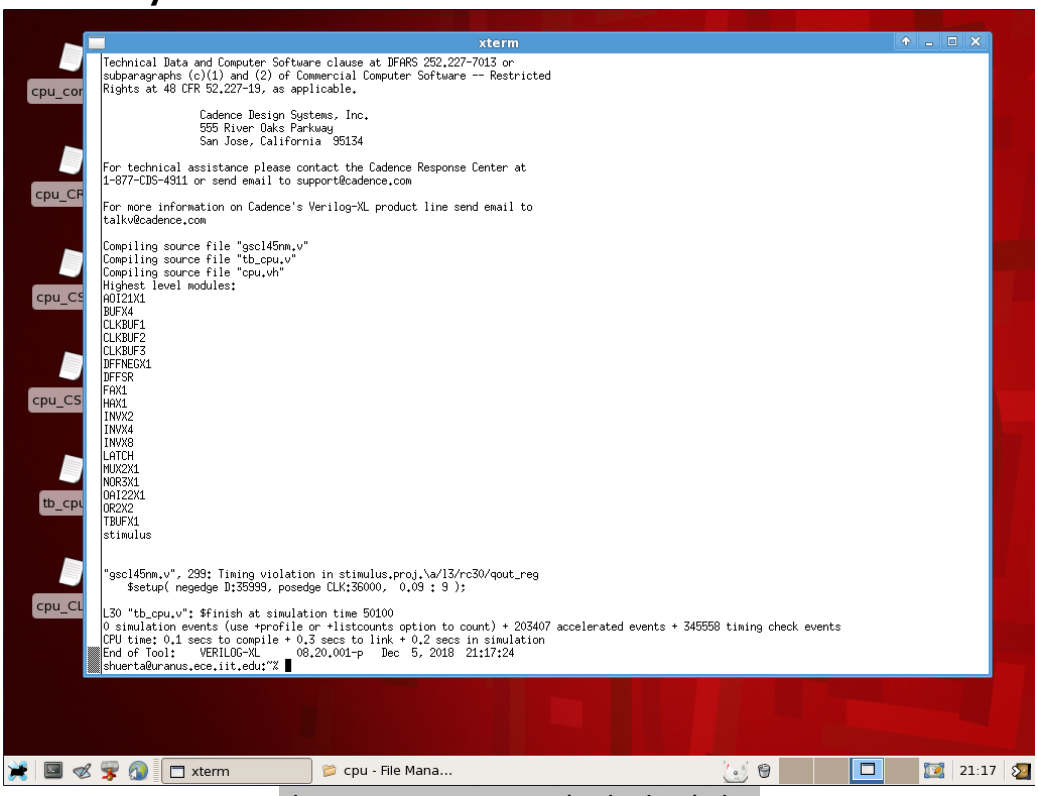
```
a/l3/f274/U5/Y (XNOR2X1)                                  0.06       6.11 r
a/l3/f274/U2/Y (XOR2X1)                                   0.07       6.18 r
a/l3/f283/U5/Y (XNOR2X1)                                  0.06       6.24 r
a/l3/f283/U2/Y (XOR2X1)                                   0.07       6.31 r
a/l3/f292/U5/Y (XNOR2X1)                                  0.06       6.37 r
a/l3/f292/U2/Y (XOR2X1)                                   0.07       6.44 r
a/l3/h301/U2/Y (XOR2X1)                                   0.04       6.48 f
a/U26/Y (AOI22X1)                                         0.03       6.52 r
U222/Y (BUFX2)                                            0.04       6.56 r
U67/Y (AND2X1)                                            0.07       6.62 r
U1832/Y (INVX1)                                           0.10       6.73 f
mb/ram/mer12/m0/m31/U3/Y (AOI22X1)                        0.05       6.78 r
U3835/Y (INVX1)                                           0.02       6.80 f
mb/ram/mer12/ll/me31/qout_reg/D (DFFPOSX1)                0.00       6.80 f
data arrival time                                                    6.80

clock clk (rise edge)                                    33.00      33.00
clock network delay (ideal)                               0.00      33.00
mb/ram/mer12/ll/me31/qout_reg/CLK (DFFPOSX1)              0.00      33.00 r
library setup time                                       -0.06      32.94
data required time                                                  32.94
-------------------------------------------------------------------------
data required time                                                  32.94
data arrival time                                                   -6.80
-------------------------------------------------------------------------
slack (MET)                                                         26.14


1
```

Figure 26: CSA timing.rep

4.3 Post-Synthesis Simulation



```
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                San Jose, California  95134

For technical assistance please contact the Cadence Response Center at
1-877-CDS-4911 or send email to support@cadence.com

For more information on Cadence's Verilog-XL product line send email to
talkv@cadence.com

Compiling source file "gscl45nm.v"
Compiling source file "tb_cpu.v"
Compiling source file "cpu.vh"
Highest level modules:
AOI21X1
BUFX4
CLKBUF1
CLKBUF2
CLKBUF3
DFFNEGX1
DFFSR
FAX1
HAX1
INVX2
INVX4
INVX8
LATCH
MUX2X1
NOR3X1
OAI22X1
OR2X2
TBUFX1
stimulus


"gscl45nm.v", 299: Timing violation in stimulus.proj.\a/l3/rc30/qout_reg
    $setup( negedge D:35999, posedge CLK:36000,  0.09 : 9 );

L30 "tb_cpu.v": $finish at simulation time 50100
0 simulation events (use +profile or +listcounts option to count) + 203407 accelerated events + 345558 timing check events
CPU time: 0.1 secs to compile + 0.3 secs to link + 0.2 secs in simulation
End of Tool:    VERILOG-XL,      08.20.001-p   Dec  5, 2018  21:17:24
shuerta@uranus.ece.iit.edu:~%
```

Figure 27: CSA Post-Synthesis Simulation

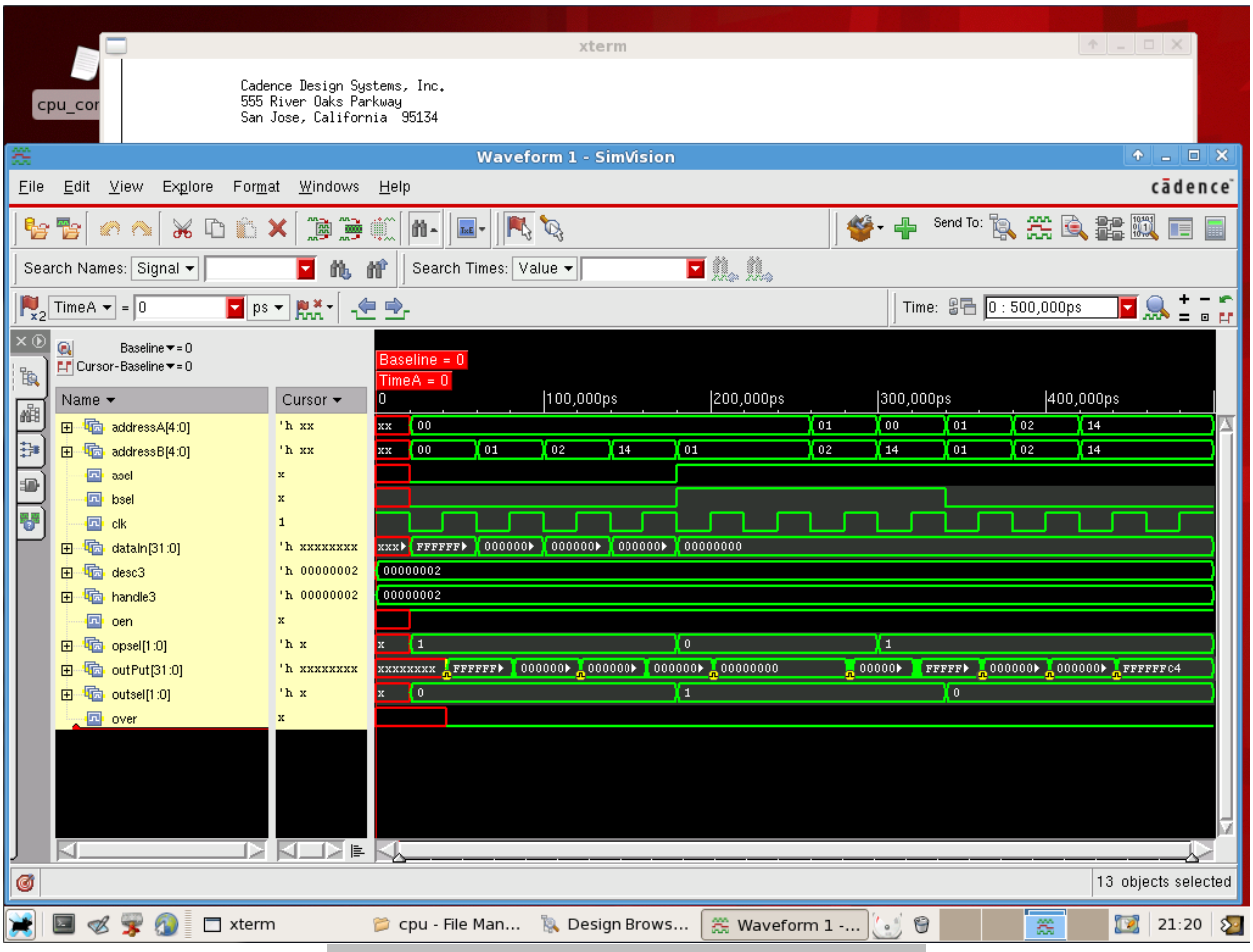


Figure 28: CSA Post-Synthesis Simulation Simvision

4.4 Maximum Clock Frequency

Having layouts for all standard cells, we placed and routed them for the final layout using Encounter. The output of this was used for a simulation, where slack time decreased to 18.318, which is an improvement. Based off the required time of 29.364, max clock frequency was found to be 34.06MHz.

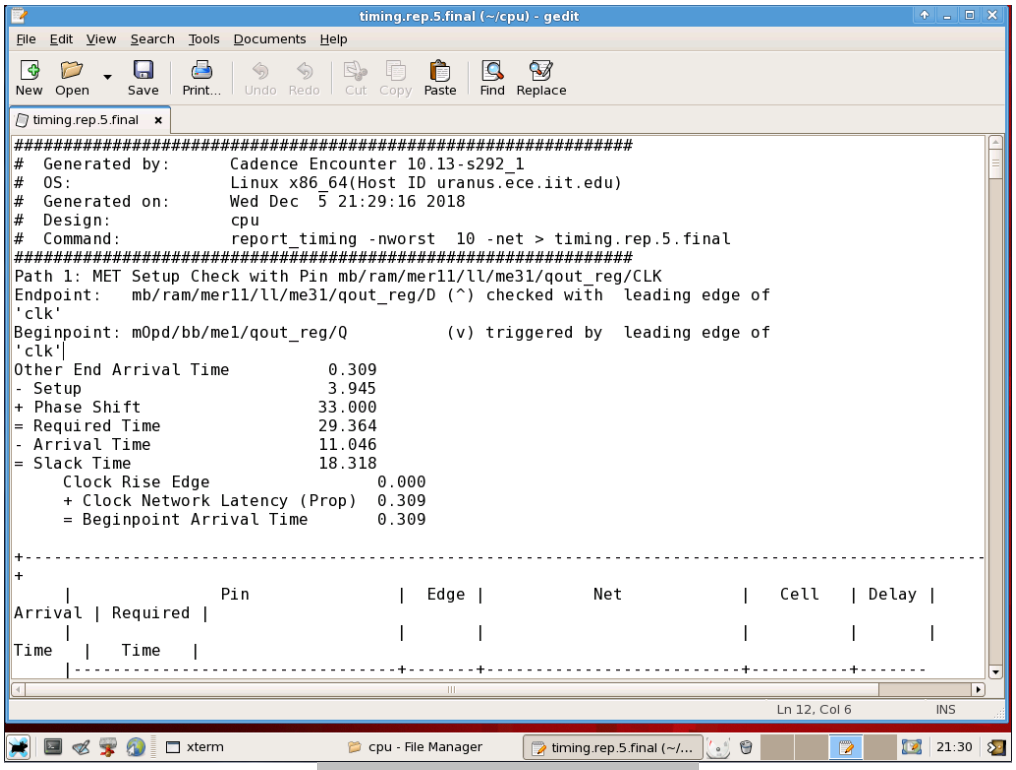


Figure 29: CSA timing.rep.5.final

4.5 Post P&R Simulation

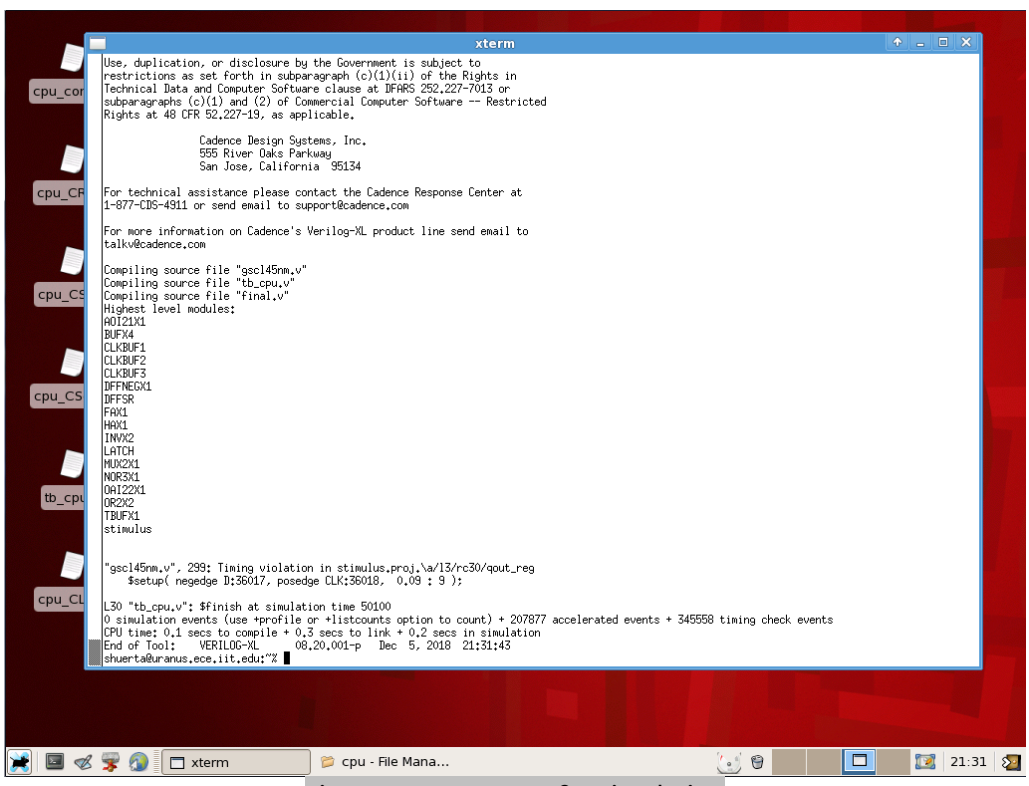


Figure 30: CSA Post P&R Simulation

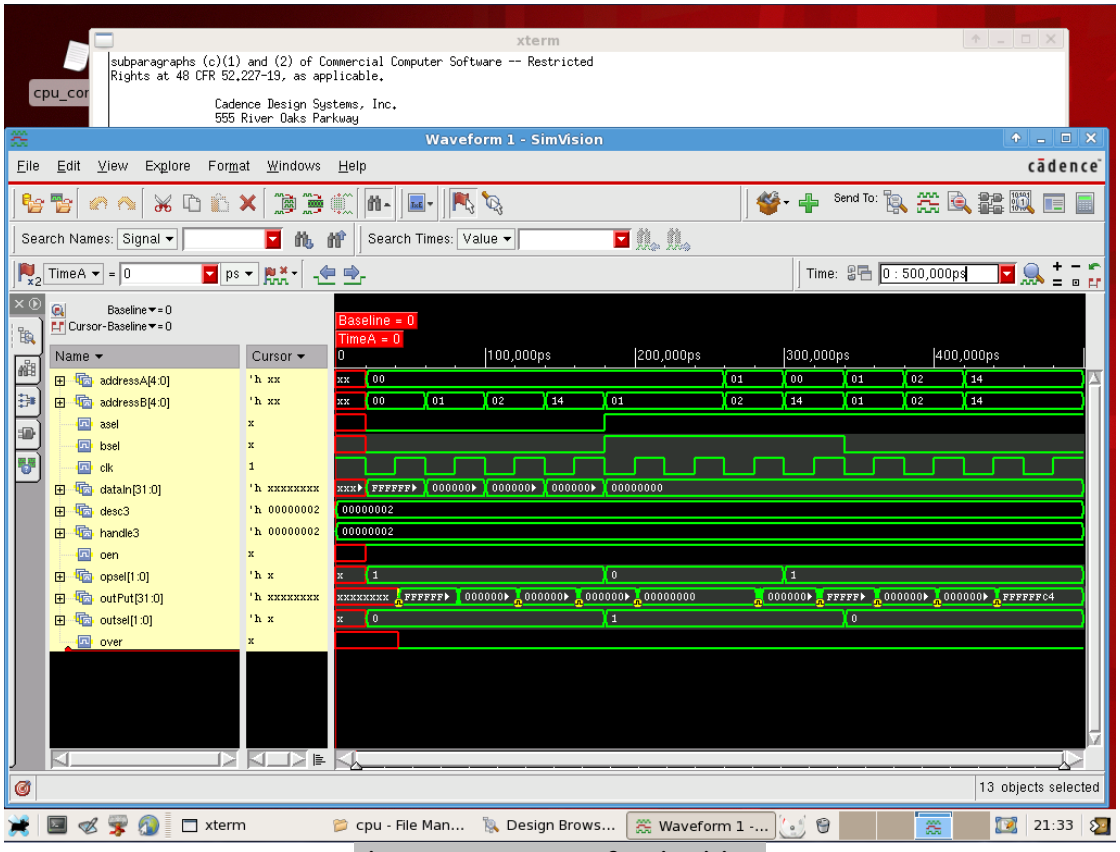


Figure 31: CSA Post P&R Simvision

4.6 New Test Bench

4.6.1 Appendix Figure A

4.7 New Test Bench Results

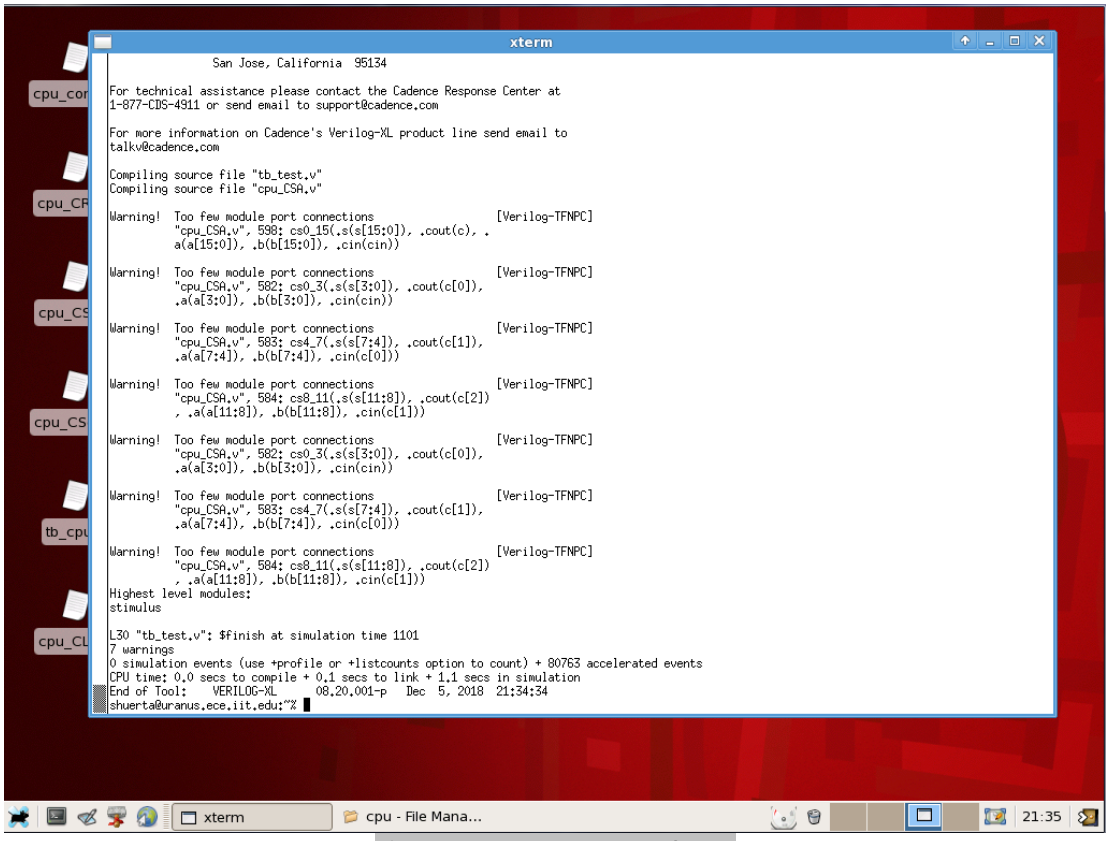


Figure 32: New Test Bench RLT

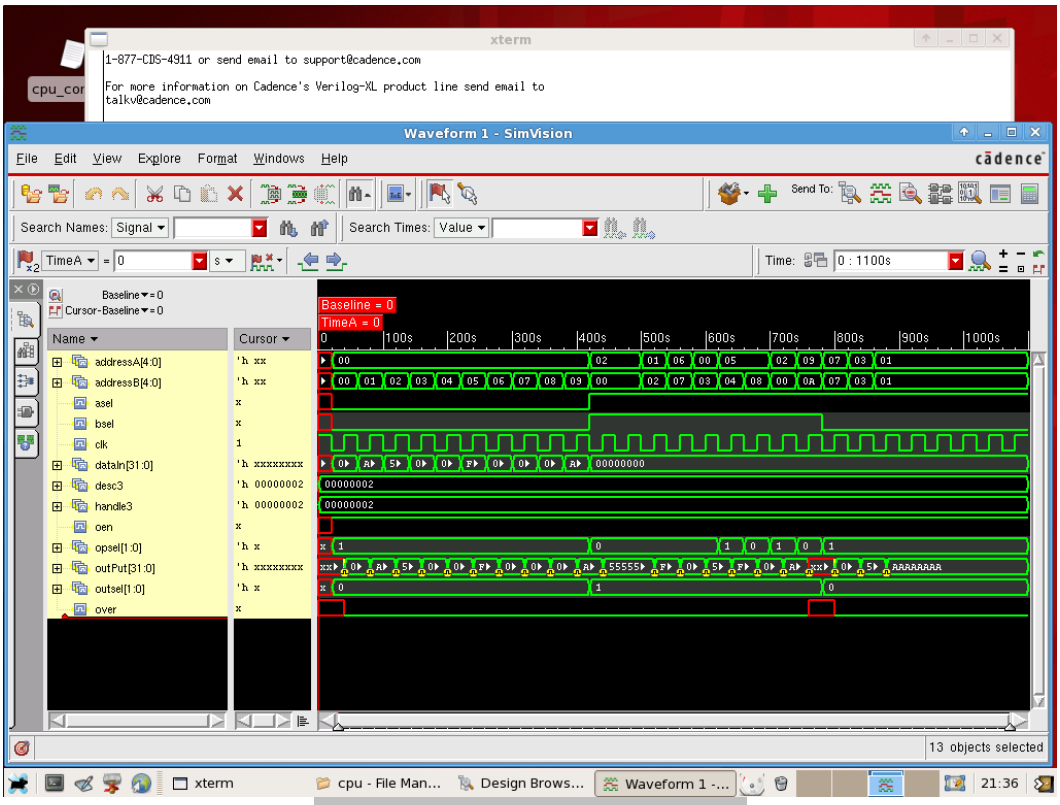


Figure 33: New Test Bench Simvision

5. Carry Select Adder

5.1 RTL Simulation

Figures 34 and 35 show the RTL simulation results and simvision waveform of CSeA against the test bench tb_cpu.v. Besides a few warnings, no errors were encountered showing full functionality.

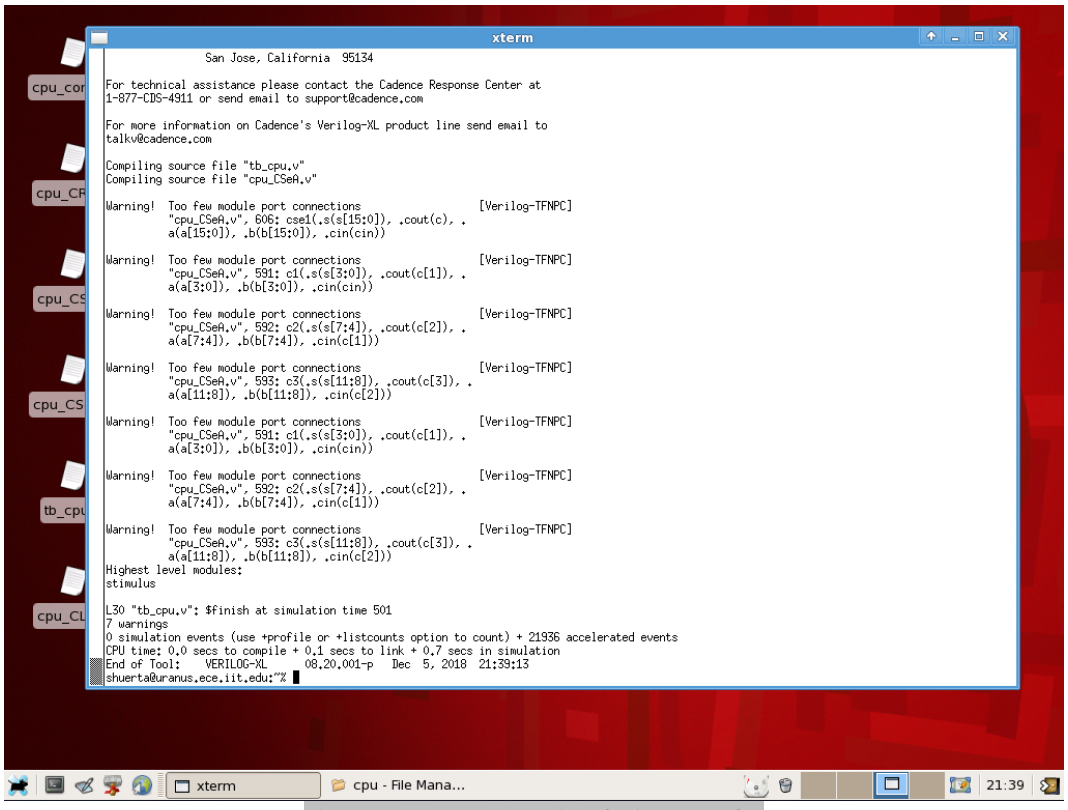


Figure 34: CSeA RTL Simulation Results

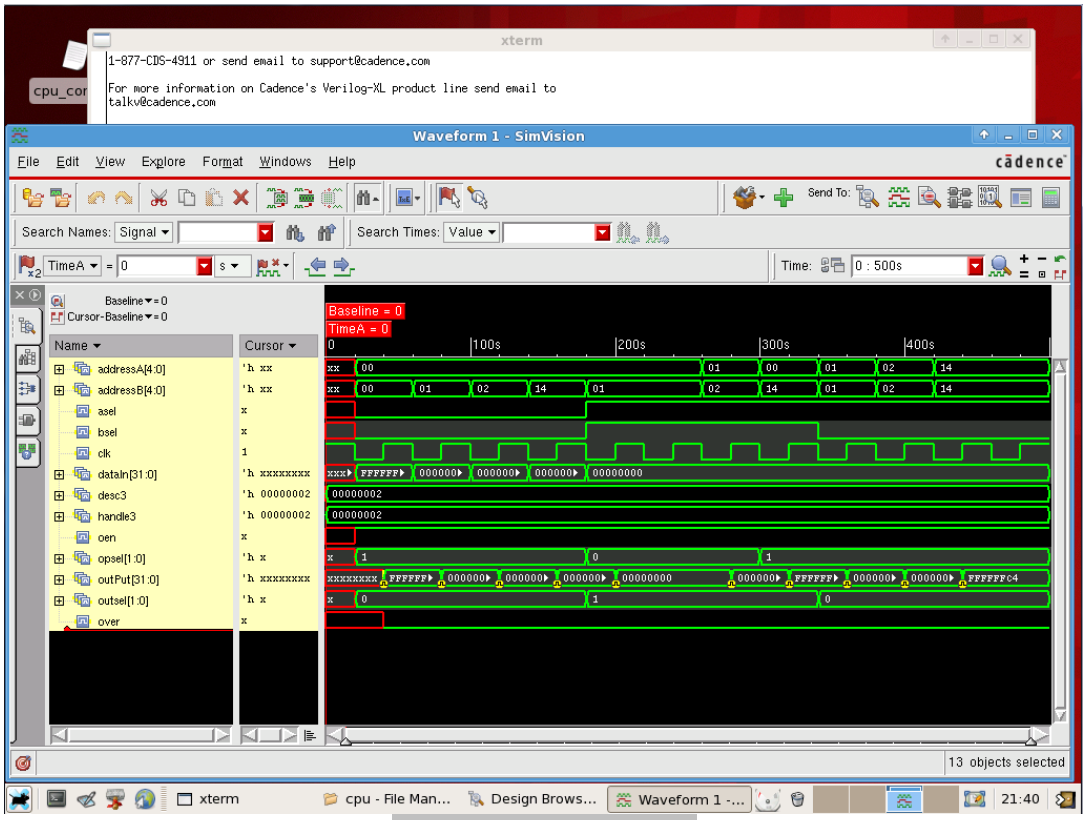
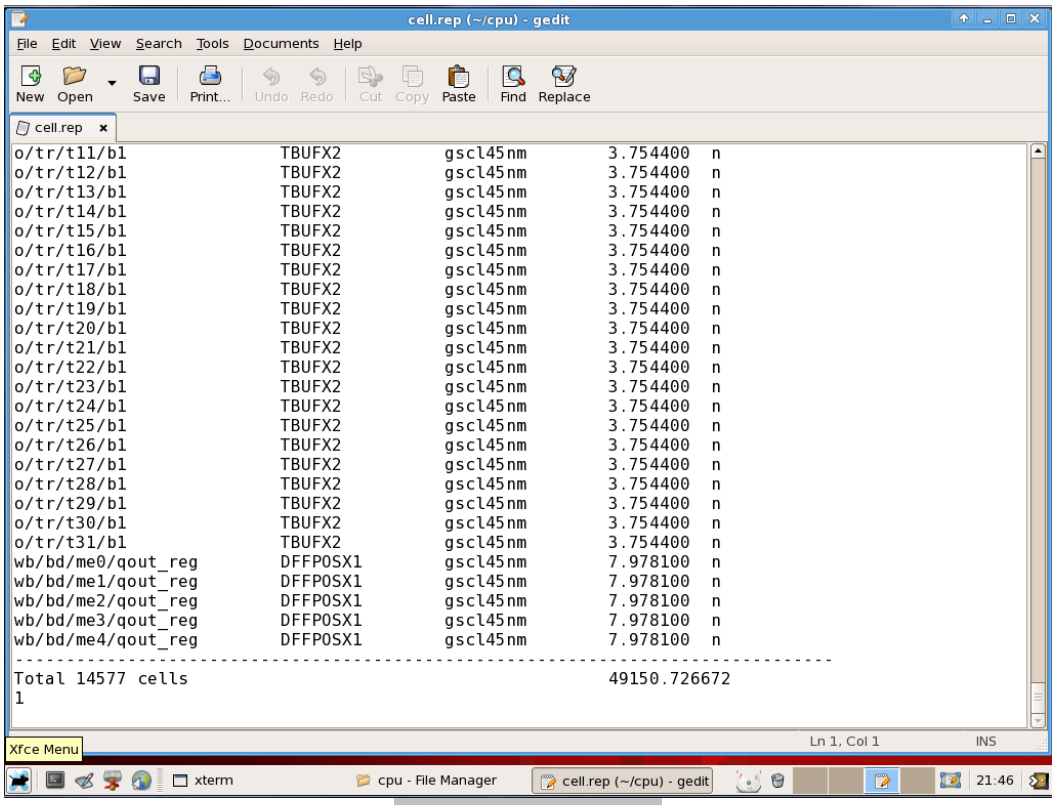


Figure 35: CSeA Simvision

5.2 Synthesis

Design Compiler was ran and completed with no errors. Area and timing of the design found in cell.rep and timing.rep files show 14577 cells and a slack time of 26.14. The mapped circuit obtained in cpu.vh was simulated with Verilog models of standard cells and results shown.



```
o/tr/t11/b1              TBUFX2          gscl45nm        3.754400  n
o/tr/t12/b1              TBUFX2          gscl45nm        3.754400  n
o/tr/t13/b1              TBUFX2          gscl45nm        3.754400  n
o/tr/t14/b1              TBUFX2          gscl45nm        3.754400  n
o/tr/t15/b1              TBUFX2          gscl45nm        3.754400  n
o/tr/t16/b1              TBUFX2          gscl45nm        3.754400  n
o/tr/t17/b1              TBUFX2          gscl45nm        3.754400  n
o/tr/t18/b1              TBUFX2          gscl45nm        3.754400  n
o/tr/t19/b1              TBUFX2          gscl45nm        3.754400  n
o/tr/t20/b1              TBUFX2          gscl45nm        3.754400  n
o/tr/t21/b1              TBUFX2          gscl45nm        3.754400  n
o/tr/t22/b1              TBUFX2          gscl45nm        3.754400  n
o/tr/t23/b1              TBUFX2          gscl45nm        3.754400  n
o/tr/t24/b1              TBUFX2          gscl45nm        3.754400  n
o/tr/t25/b1              TBUFX2          gscl45nm        3.754400  n
o/tr/t26/b1              TBUFX2          gscl45nm        3.754400  n
o/tr/t27/b1              TBUFX2          gscl45nm        3.754400  n
o/tr/t28/b1              TBUFX2          gscl45nm        3.754400  n
o/tr/t29/b1              TBUFX2          gscl45nm        3.754400  n
o/tr/t30/b1              TBUFX2          gscl45nm        3.754400  n
o/tr/t31/b1              TBUFX2          gscl45nm        3.754400  n
wb/bd/me0/qout_reg       DFFPOSX1        gscl45nm        7.978100  n
wb/bd/me1/qout_reg       DFFPOSX1        gscl45nm        7.978100  n
wb/bd/me2/qout_reg       DFFPOSX1        gscl45nm        7.978100  n
wb/bd/me3/qout_reg       DFFPOSX1        gscl45nm        7.978100  n
wb/bd/me4/qout_reg       DFFPOSX1        gscl45nm        7.978100  n
--------------------------------------------------------------------------------
Total 14577 cells                                        49150.726672
1
```

Figure 36: CRA cell.rep

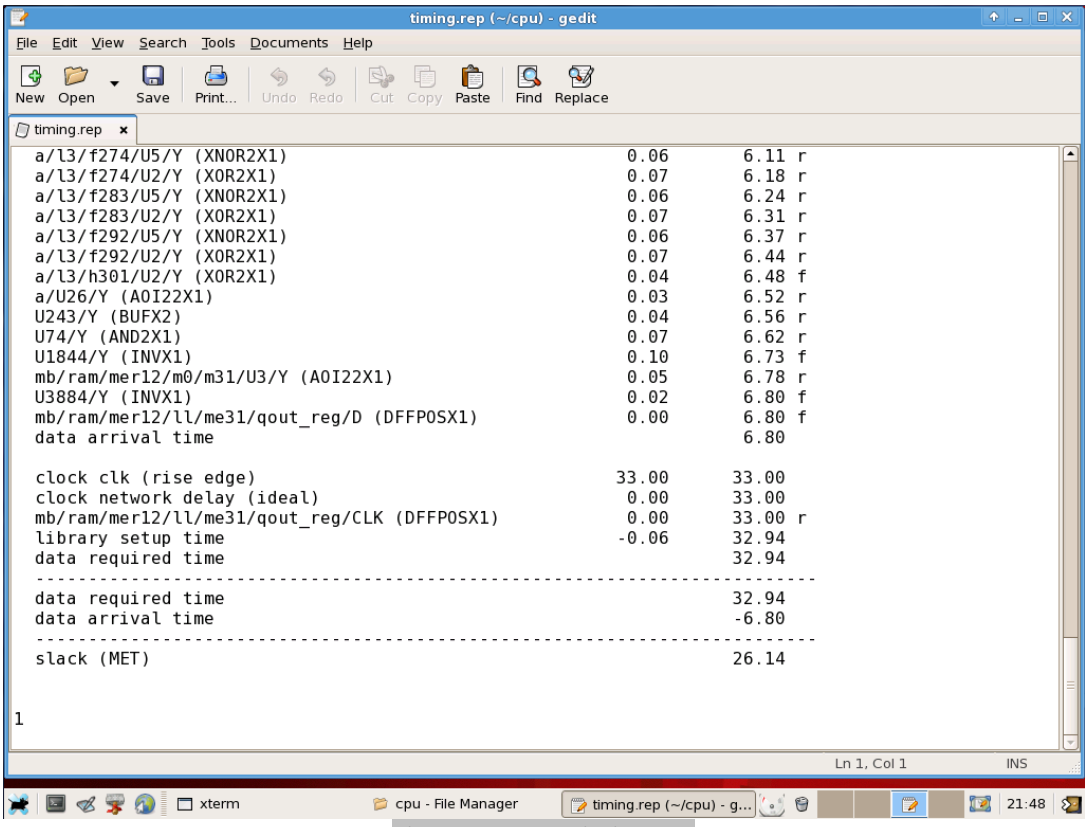


Figure 37: CRA timing.rep

5.3 Post-Synthesis Simulation

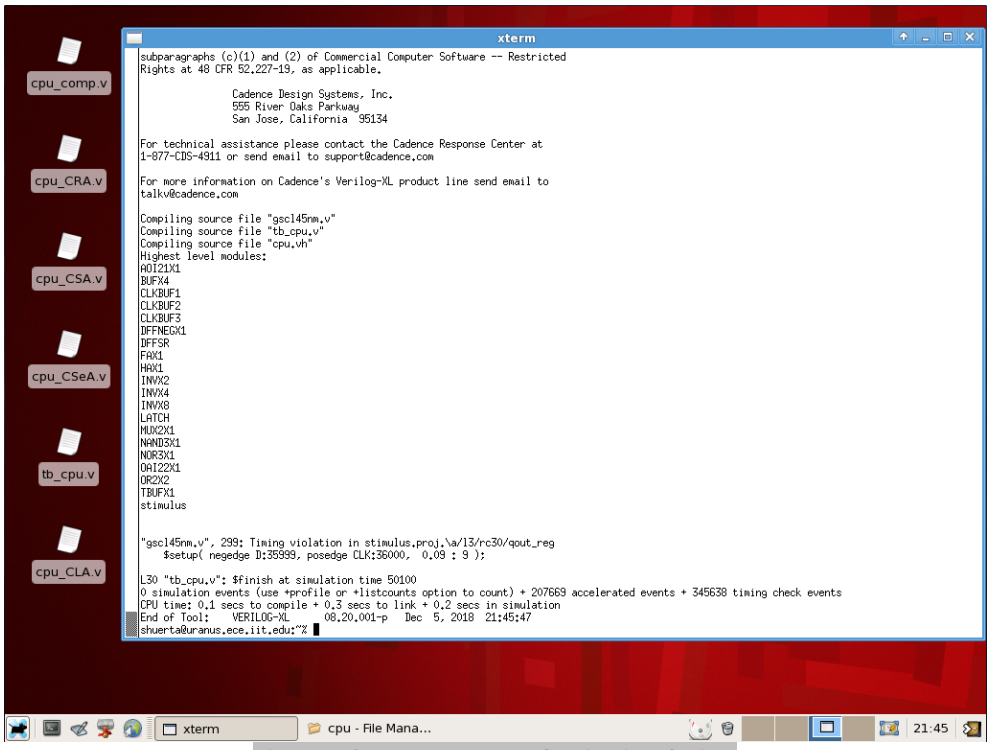


Figure 38: CRA Post-Synthesis Simulation

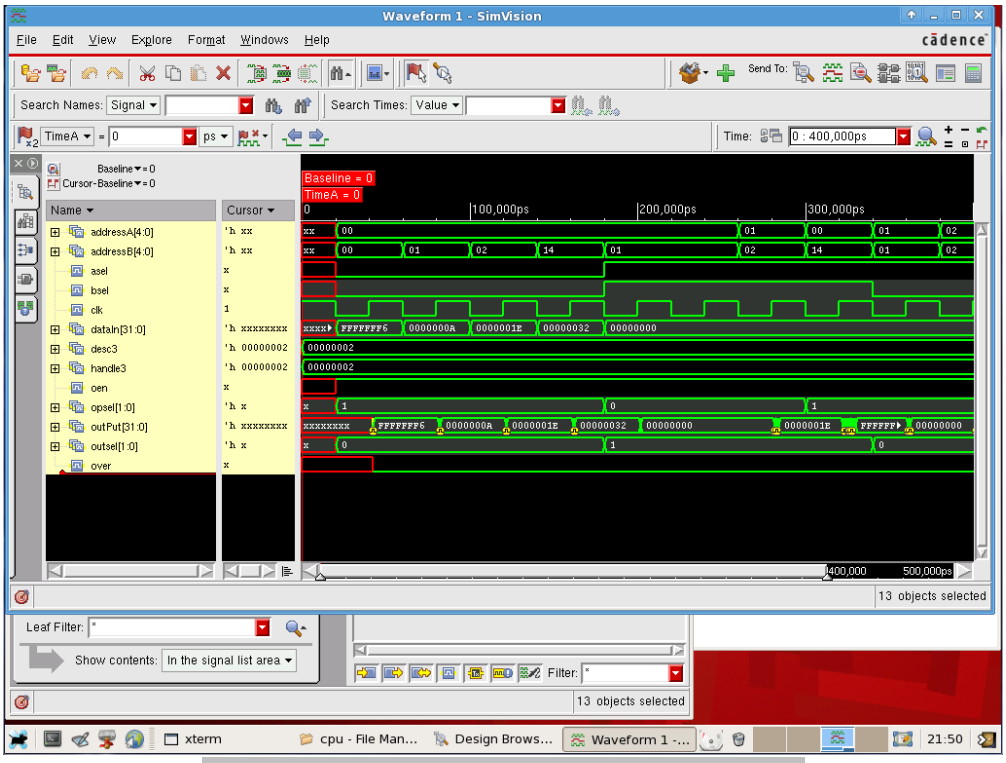


Figure 39: CRA Post-Synthesis Simulation Simvision

5.4 Maximum Clock Frequency

Having layouts for all standard cells, we placed and routed them for the final layout using Encounter. The output of this was used for a simulation, where slack time has decreased to 18.144, which is an improvement. Based off the required time of 29.259. max clock frequency was found to be 34.18MHz.

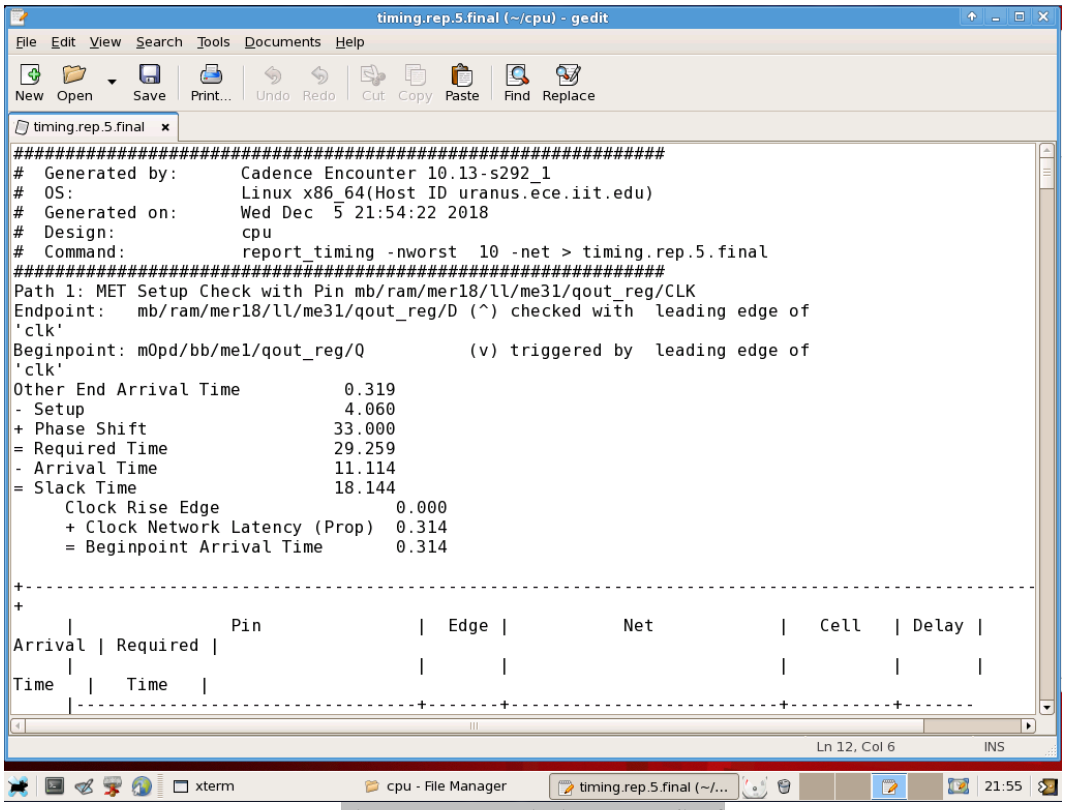


Figure 40: CRA timing.rep.5.final

5.5 Post P&R Simulation

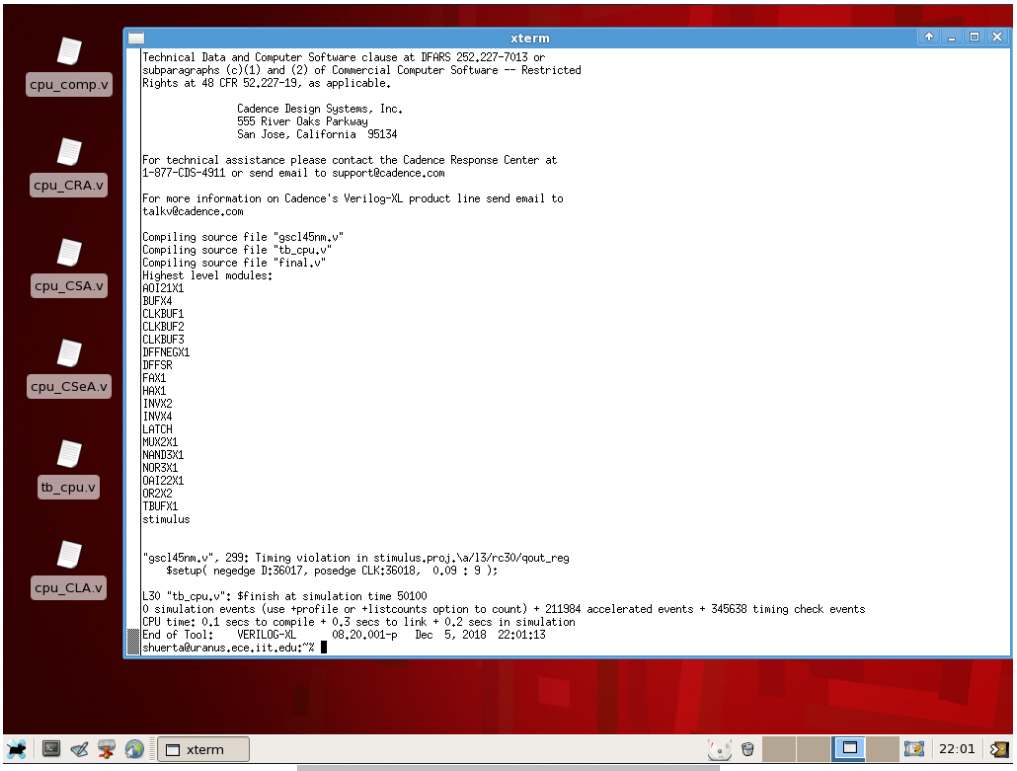


Figure 41: CRA Post P&R Simulation

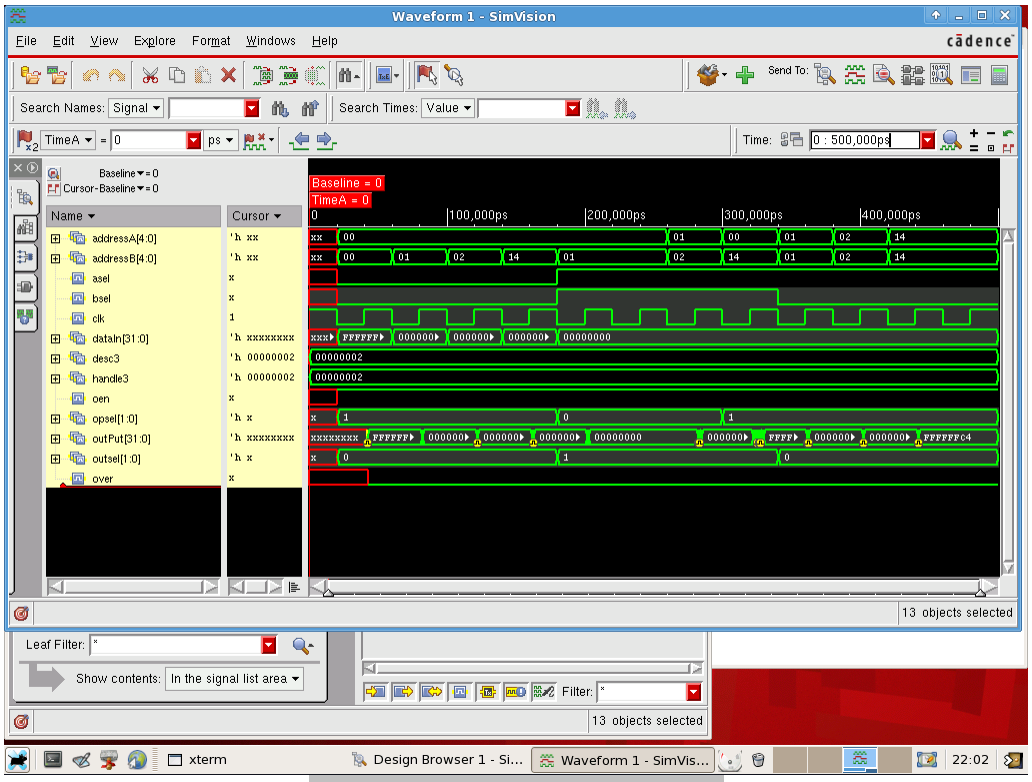


Figure 42: CRA Post P&R Simvision

5.6 New Test Bench

5.6.1 Appendix Figure A

5.7 New Test Bench Results

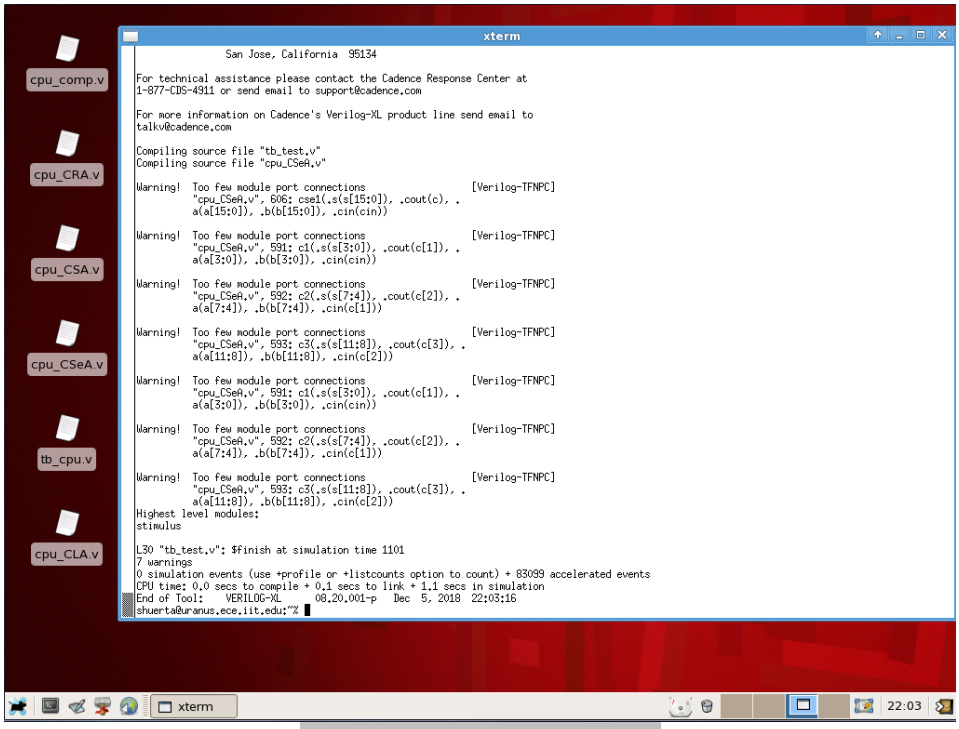


Figure 43: New Test Bench RLT

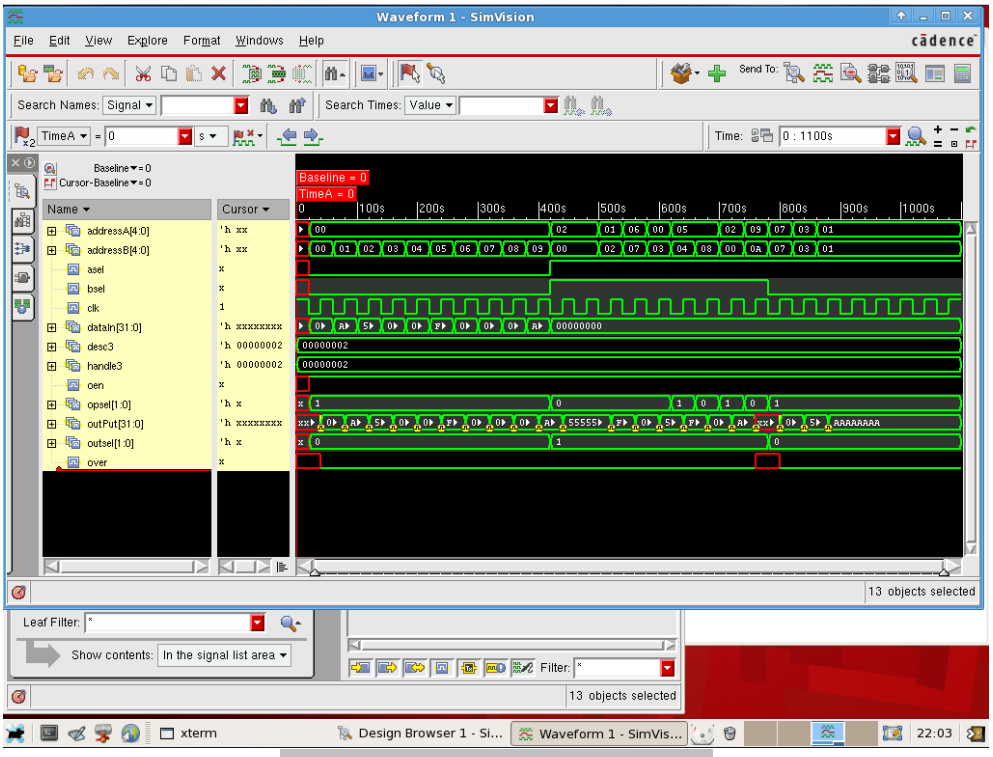


Figure 44: New Test Bench Simvision

Case Study 2

32-bit CPU design with New ALU Architecture

6. tb_test_comp.v

6.1.1 Appendix Figure B

6.2 RTL Simulation

Figures 45 and 46 show the RTL simulation results and simvision waveform of cpu_comp.v against the test bench tb_test_comp.v. Besides a few warnings, no errors were encountered showing full functionality.

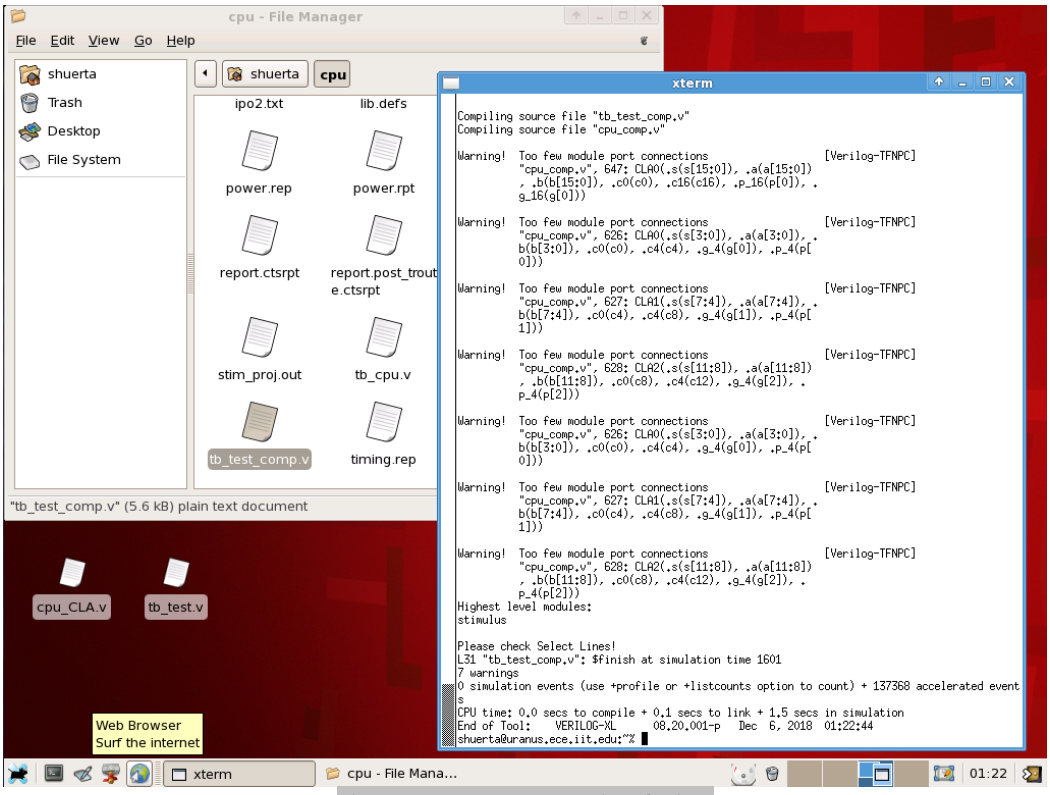


Figure 45: Comp RTL Simulation

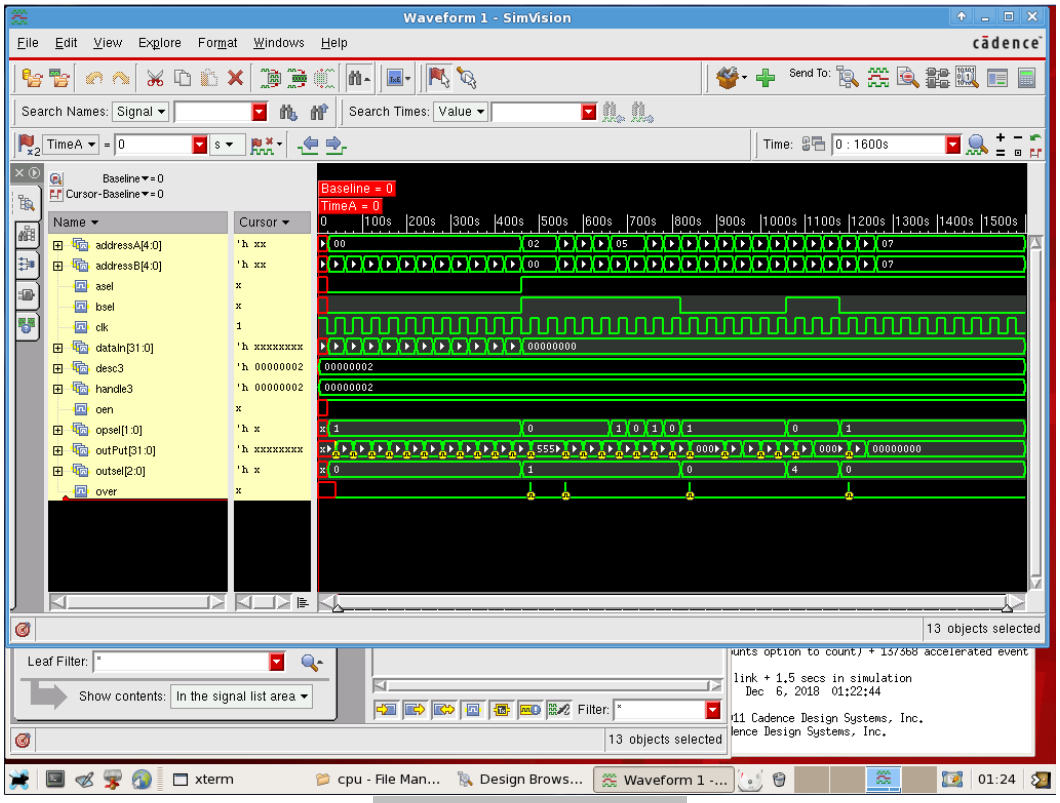


Figure 46: Comp Simvision

6.3 Synthesis

Design Compiler was ran and completed with no errors. Area and timing of the design found in cell.rep and timing.rep files show 14507 cells and a slack time of 26.48. The mapped circuit obtained in cpu.vh was simulated with Verilog models of standard cells and results shown.

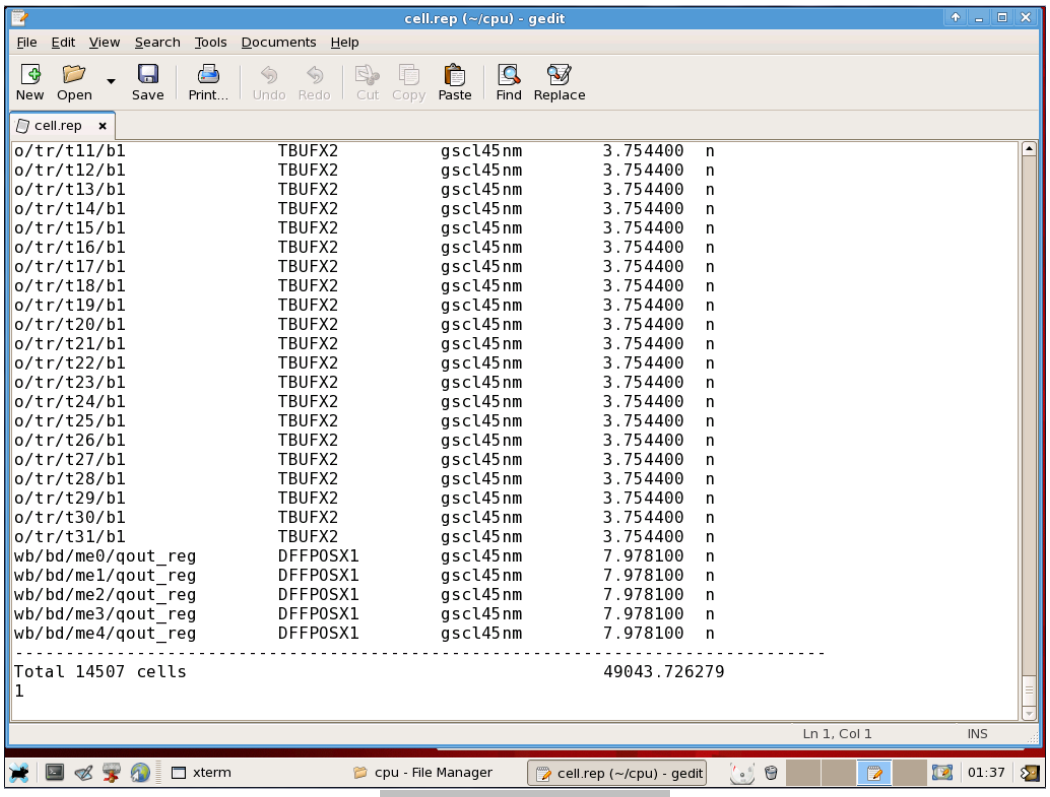
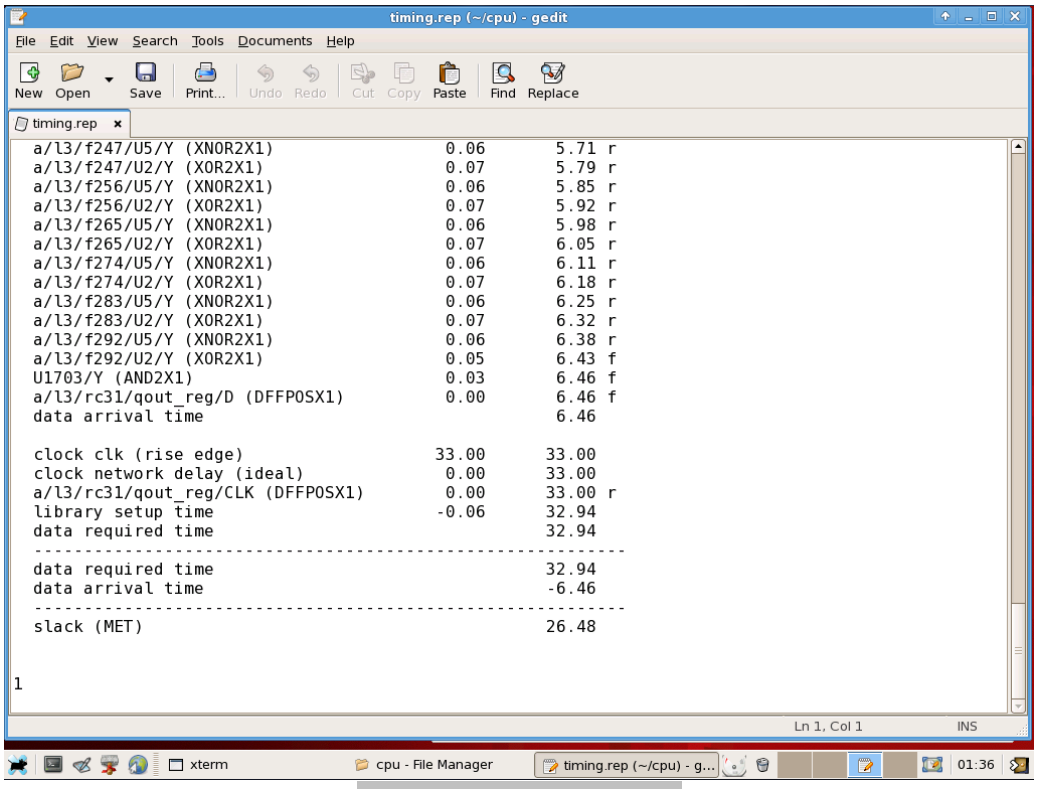


Figure 45: Comp cell.rep



```
  a/l3/f247/U5/Y (XNOR2X1)                 0.06       5.71 r
  a/l3/f247/U2/Y (XOR2X1)                  0.07       5.79 r
  a/l3/f256/U5/Y (XNOR2X1)                 0.06       5.85 r
  a/l3/f256/U2/Y (XOR2X1)                  0.07       5.92 r
  a/l3/f265/U5/Y (XNOR2X1)                 0.06       5.98 r
  a/l3/f265/U2/Y (XOR2X1)                  0.07       6.05 r
  a/l3/f274/U5/Y (XNOR2X1)                 0.06       6.11 r
  a/l3/f274/U2/Y (XOR2X1)                  0.07       6.18 r
  a/l3/f283/U5/Y (XNOR2X1)                 0.06       6.25 r
  a/l3/f283/U2/Y (XOR2X1)                  0.07       6.32 r
  a/l3/f292/U5/Y (XNOR2X1)                 0.06       6.38 r
  a/l3/f292/U2/Y (XOR2X1)                  0.05       6.43 f
  U1703/Y (AND2X1)                         0.03       6.46 f
  a/l3/rc31/qout_reg/D (DFFPOSX1)          0.00       6.46 f
  data arrival time                                   6.46

  clock clk (rise edge)                   33.00      33.00
  clock network delay (ideal)              0.00      33.00
  a/l3/rc31/qout_reg/CLK (DFFPOSX1)        0.00      33.00 r
  library setup time                      -0.06      32.94
  data required time                                 32.94
  -------------------------------------------------------------
  data required time                                 32.94
  data arrival time                                  -6.46
  -------------------------------------------------------------
  slack (MET)                                        26.48


1
```

Figure 48: Comp timing.rep

6.4 Post-Synthesis Simulation

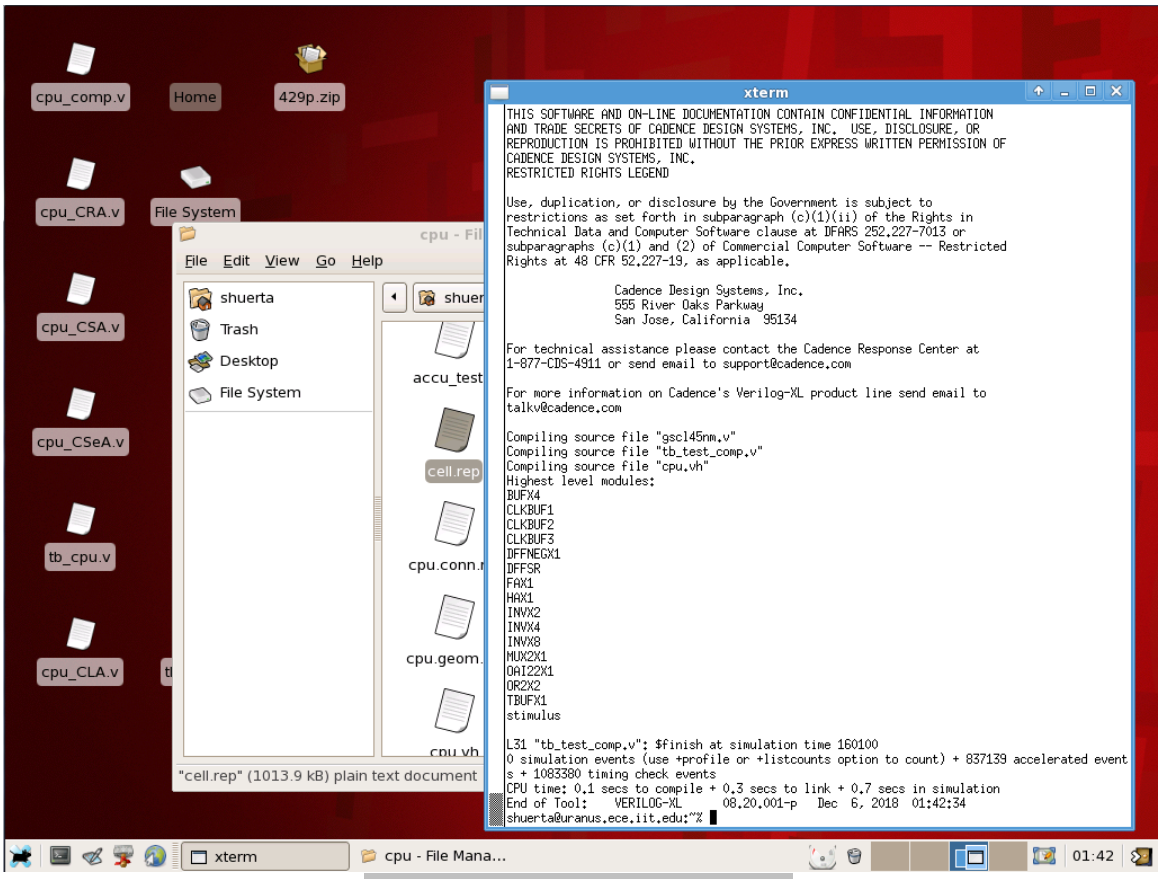


Figure 49: Post-Synthesis Simulation

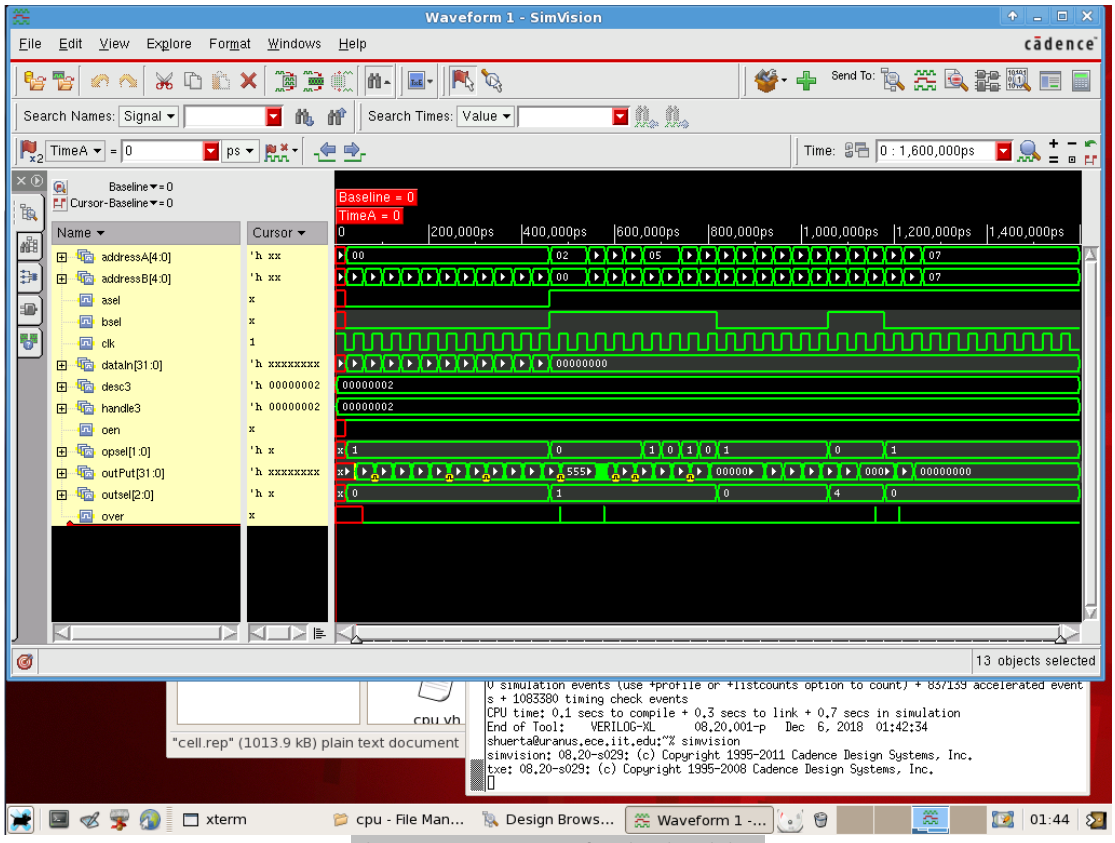
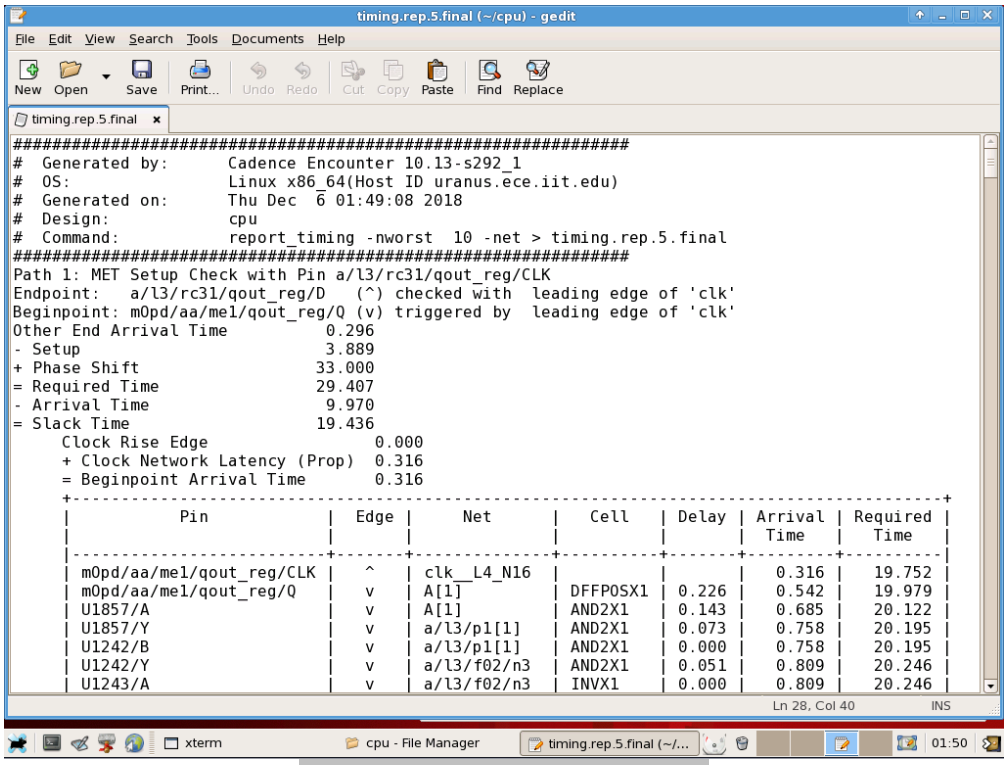


Figure 50: Post-Synthesis Simvision

6.5 Maximum Clock Frequency

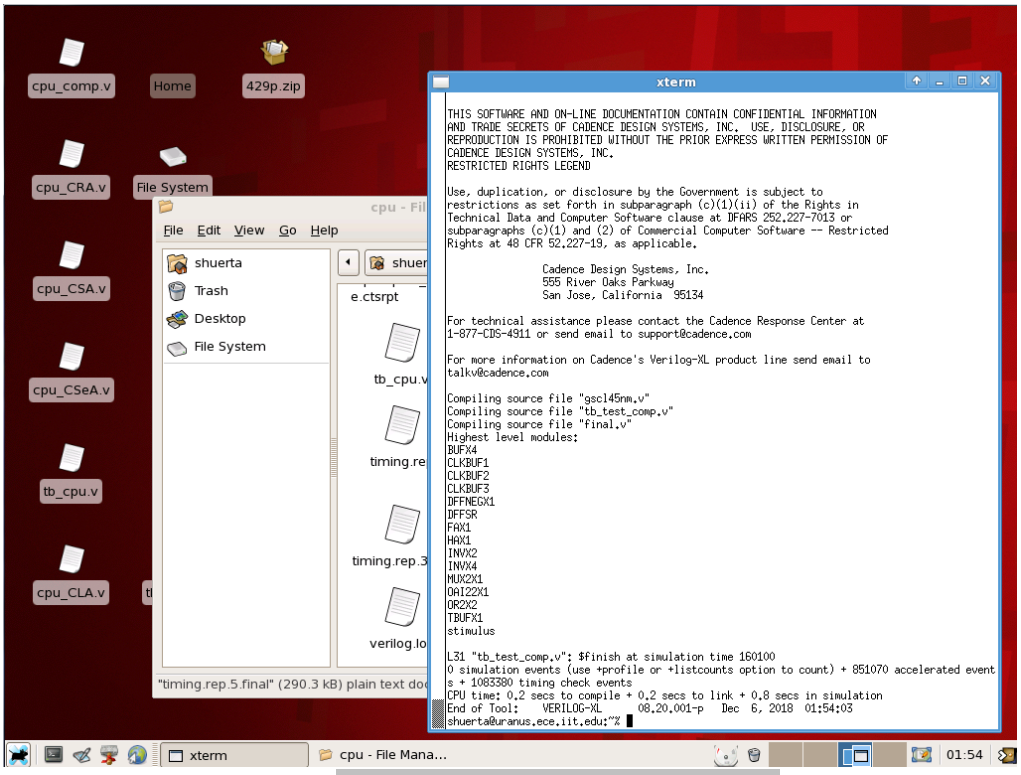
Having layouts for all standard cells, we placed and routed them for the final layout using Encounter. The output of this was used for a simulation, where slack time has decreased to 19.436, which is an improvement. Based off the required time of 29.407. max clock frequency was found to be 34.01MHz.



```
timing.rep.5.final (~/cpu) - gedit
File Edit View Search Tools Documents Help
New Open Save Print... Undo Redo Cut Copy Paste Find Replace
timing.rep.5.final
#############################################################
#  Generated by:      Cadence Encounter 10.13-s292_1
#  OS:                Linux x86_64(Host ID uranus.ece.iit.edu)
#  Generated on:      Thu Dec  6 01:49:08 2018
#  Design:            cpu
#  Command:           report_timing -nworst  10 -net > timing.rep.5.final
#############################################################
Path 1: MET Setup Check with Pin a/l3/rc31/qout_reg/CLK
Endpoint:   a/l3/rc31/qout_reg/D   (^) checked with  leading edge of 'clk'
Beginpoint: mOpd/aa/me1/qout_reg/Q (v) triggered by  leading edge of 'clk'
Other End Arrival Time          0.296
- Setup                         3.889
+ Phase Shift                  33.000
= Required Time                29.407
- Arrival Time                  9.970
= Slack Time                   19.436
     Clock Rise Edge                     0.000
     + Clock Network Latency (Prop)  0.316
     = Beginpoint Arrival Time       0.316
     +-------------------------------------------------------------------------------------+
     |           Pin            |  Edge |     Net      |   Cell   | Delay | Arrival | Required |
     |                          |       |              |          |       |  Time   |   Time   |
     |--------------------------+-------+--------------+----------+-------+---------+----------|
     | mOpd/aa/me1/qout_reg/CLK |   ^   | clk__L4_N16  |          |       |   0.316 |   19.752 |
     | mOpd/aa/me1/qout_reg/Q   |   v   | A[1]         | DFFPOSX1 | 0.226 |   0.542 |   19.979 |
     | U1857/A                  |   v   | A[1]         | AND2X1   | 0.143 |   0.685 |   20.122 |
     | U1857/Y                  |   v   | a/l3/p1[1]   | AND2X1   | 0.073 |   0.758 |   20.195 |
     | U1242/B                  |   v   | a/l3/p1[1]   | AND2X1   | 0.000 |   0.758 |   20.195 |
     | U1242/Y                  |   v   | a/l3/f02/n3  | AND2X1   | 0.051 |   0.809 |   20.246 |
     | U1243/A                  |   v   | a/l3/f02/n3  | INVX1    | 0.000 |   0.809 |   20.246 |
Ln 28, Col 40   INS
xterm   cpu - File Manager   timing.rep.5.final (~/...   01:50
```

Figure 51: Comp Timing.rep.5.final

6.6 Post P&R Simulation



```
xterm
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talkv@cadence.com

Compiling source file "gscl45nm.v"
Compiling source file "tb_test_comp.v"
Compiling source file "final.v"
Highest level modules:
BUFX4
CLKBUF1
CLKBUF2
CLKBUF3
DFFNEGX1
DFFSR
FAX1
HAX1
INVX2
INVX4
MUX2X1
OAI22X1
OR2X2
TBUFX1
stimulus

L31 "tb_test_comp.v": $finish at simulation time 160100
0 simulation events (use +profile or +listcounts option to count) + 851070 accelerated event
s + 1083380 timing check events
CPU time: 0.2 secs to compile + 0.2 secs to link + 0.8 secs in simulation
End of Tool:    VERILOG-XL      08.20.001-p   Dec  6, 2018  01:54:03
shuerta@uranus.ece.iit.edu:~%
```

Figure 52: Comp Post P&R Simulation

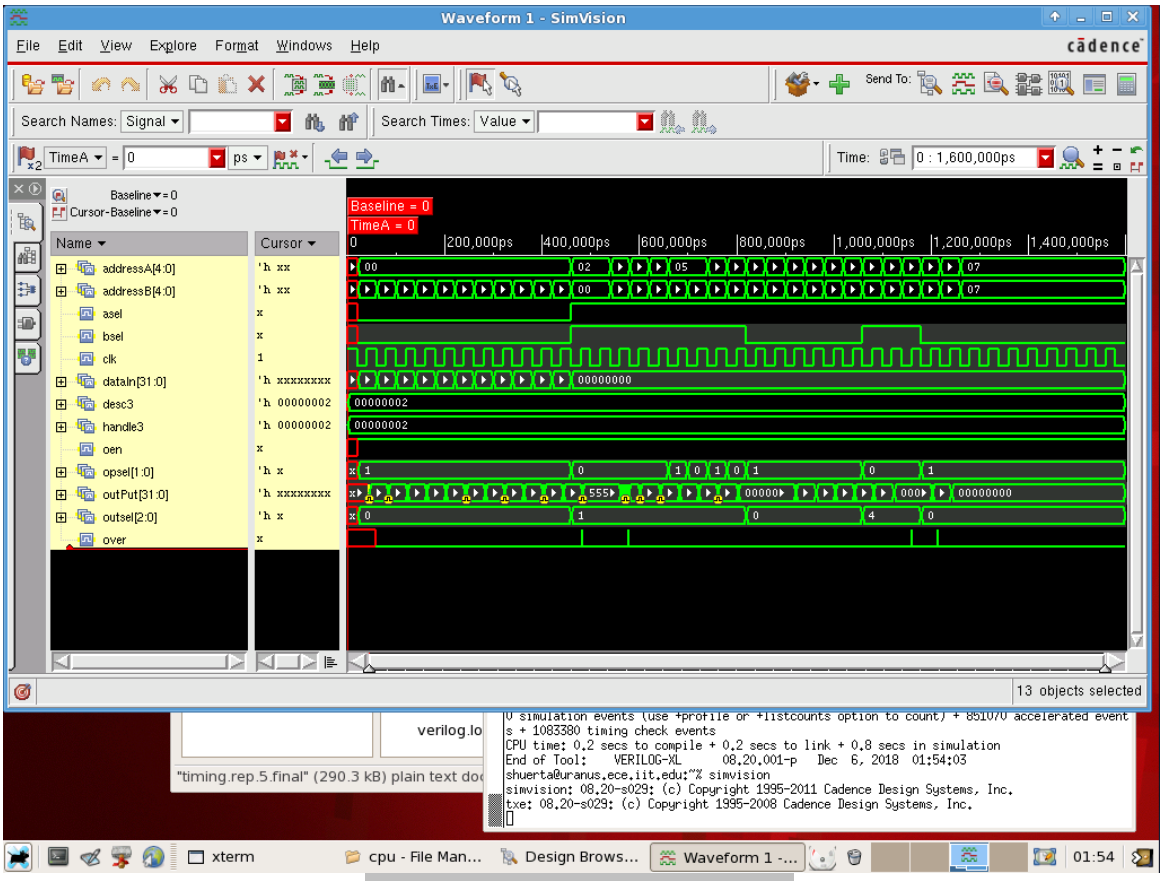

Figure 53: Comp Post P&R Simvision

8. APPENDIX

```
module stimulus;

parameter T = 20;

reg [31:0] dataIn;
reg [1:0] opsel, outsel;
reg [4:0] addressA, addressB;
reg asel, bsel, oen, clk;

wire [31:0] outPut;
wire over;


integer handle3,desc3;

// Instantiate the design block counter
cpu proj(addressA, addressB, dataIn, asel,bsel, clk,
opsel, outsel, oen, outPut, over);
initial
begin
clk = 1'b1;
forever #T  clk = ~clk;
end
```

```
initial
 begin
handle3 = $fopen ("stim_proj.out");
  $shm_open("shm.db",1);
  $shm_probe(stimulus,"AS");
  #1100  $shm_close();
  #1 $finish;
  end


always
begin
desc3=handle3;
#1 $fdisplay(desc3, $time,"clk=%b, addressA=%d,
addressB=%d, dataIn=%d, opsel=%d, outsel=%d, asel=
%d, bsel=%d, oen=%d, OUT=%d", clk, addressA,
addressB, dataIn, opsel, outsel,asel, bsel, oen, outPut);

end

 // Stimulate the Input Signals
initial
 begin
```

```
// 1. store (5) in [0]

#T

addressA = 5'b00000;

addressB = 5'b00000;

dataIn = 32'h000_0006;

opsel = 2'b01;

outsel =2'b00;

asel = 0;

bsel = 0;

oen = 1;

#(T*2)

// 2. store (AAAA_AAAA) in [1]

addressA = 5'b00000;

addressB = 5'b00001;

dataIn = 32'hAAAA_AAAA;

opsel = 2'b01;

outsel =2'b00;

asel = 0;

bsel = 0;

oen = 1;

#(T*2)

// 3. store (5555_5555) in [2]

addressA = 5'b00000;

addressB = 5'b00010;

dataIn = 32'h5555_5555;

opsel = 2'b01;

outsel =2'b00;

asel = 0;

bsel = 0;

oen = 1;

#(T*2)

// 4. store (0000_000A) in [3]

addressA = 5'b00000;

addressB = 5'b00011;

dataIn = 32'h0000_000A;

opsel = 2'b01;

outsel =2'b00;

asel = 0;

bsel = 0;

oen = 1;

#(T*2)

// 5. store (0000_0001) in [4]

addressA = 5'b00000;

addressB = 5'b00100;

dataIn = 32'h0000_0001;

opsel = 2'b01;

outsel =2'b00;

asel = 0;

bsel = 0;

oen = 1;

#(T*2)

// 6. store (FFFF_FFFF) in [5]

addressA = 5'b00000;
```

```
addressB = 5'b00101;

dataIn = 32'hFFFF_FFFF;

opsel = 2'b01;

outsel =2'b00;

asel = 0;

bsel = 0;

oen = 1;

#(T*2)

// 7. store (0000_00C8) in [6]

addressA = 5'b00000;

addressB = 5'b00110;

dataIn = 32'h0000_00C8;

opsel = 2'b01;

outsel =2'b00;

asel = 0;

bsel = 0;

oen = 1;

#(T*2)

// 8. store (0000_012C) in [7]

addressA = 5'b00000;

addressB = 5'b00111;

dataIn = 32'h0000_012C;

opsel = 2'b01;

outsel =2'b00;

asel = 0;

bsel = 0;

oen = 1;
```

```
#(T*2)

// 9. store (0000_0001) in [8]

addressA = 5'b00000;

addressB = 5'b01000;

dataIn = 32'h0000_0001;

opsel = 2'b01;

outsel =2'b00;

asel = 0;

bsel = 0;

oen = 1;

#(T*2)

// 10. store (AAAA_AAAB) in [9]

addressA = 5'b00000;

addressB = 5'b01001;

dataIn = 32'hAAAA_AAAB;

opsel = 2'b01;

outsel =2'b00;

asel = 0;

bsel = 0;

oen = 1;

#(T*2)

// 11. ADD [2][0]

addressA = 5'd2;

addressB = 5'd0;

dataIn = 32'd0;

opsel = 2'b00;
```

```
outsel =2'b01;

asel = 1;

bsel = 1;

oen = 1;

#(T*2)

#(T*2)

// 12. ADD [1][2]

addressA = 5'd1;

addressB = 5'd2;

dataIn = 32'd0;

opsel = 2'b00;

outsel =2'b01;

asel = 1;

bsel = 1;

oen = 1;

#(T*2)

// 13. ADD [6][7]

addressA = 5'd6;

addressB = 5'd7;

dataIn = 32'd0;

opsel = 2'b00;

outsel =2'b01;

asel = 1;

bsel = 1;

oen = 1;

#(T*2)

// 14. ADD [0][3]

addressA = 5'd0;

addressB = 5'd3;

dataIn = 32'd0;

opsel = 2'b00;

outsel =2'b01;

asel = 1;

bsel = 1;

oen = 1;

#(T*2)

// 15. SUB [5][4]

addressA = 5'd5;

addressB = 5'd4;

dataIn = 32'd0;

opsel = 2'b01;

outsel =2'b01;

asel = 1;

bsel = 1;

oen = 1;

#(T*2)

// 16. ADD [5][8]

addressA = 5'd5;

addressB = 5'd8;

dataIn = 32'd0;

opsel = 2'b00;

outsel =2'b01;

asel = 1;
```

```
bsel = 1;

oen = 1;

#(T*2)

// 17. SUB [2][0]

addressA = 5'd2;

addressB = 5'd0;

dataIn = 32'd0;

opsel = 2'b01;

outsel =2'b01;

asel = 1;

bsel = 1;

oen = 1;

#(T*2)

// 18. ADD [9][10]

addressA = 5'd9;

addressB = 5'd10;

dataIn = 32'd0;

opsel = 2'b00;

outsel =2'b01;

asel = 1;

bsel = 1;

oen = 1;

#(T*2)

// 19. READ [7]

addressA = 5'd7;

addressB = 5'd7;

dataIn = 32'd0;

opsel = 2'b01;

outsel =2'b00;

asel = 1;

bsel = 0;

oen = 1;

#(T*2)

// 20. READ [3]

addressA = 5'd3;

addressB = 5'd3;

dataIn = 32'd0;

opsel = 2'b01;

outsel =2'b00;

asel = 1;

bsel = 0;

oen = 1;

#(T*2)

// 21. READ [1]

addressA = 5'd1;

addressB = 5'd1;

dataIn = 32'd0;

opsel = 2'b01;

outsel =2'b00;

asel = 1;

bsel = 0;

oen = 1;

end
```

```
endmodule
```

Figure A: Test Bench

```
module stimulus;

parameter T = 20;

reg [31:0] dataIn;
reg [1:0] opsel;
reg [2:0] outsel;
reg [4:0] addressA, addressB;
reg asel, bsel, oen, clk;

wire [31:0] outPut;
wire over;


integer handle3,desc3;

// Instantiate the design block counter
cpu proj(addressA, addressB, dataIn, asel,bsel, clk,
opsel, outsel, oen, outPut, over);
initial
begin
clk = 1'b1;
forever #T  clk = ~clk;
end

initial
 begin
handle3 = $fopen ("stim_proj.out");
  $shm_open("shm.db",1);
  $shm_probe(stimulus,"AS");
  #1600  $shm_close();
  #1 $finish;
  end


always
begin
desc3=handle3;
#1 $fdisplay(desc3, $time,"clk=%b, addressA=%d,
addressB=%d, dataIn=%d, opsel=%d, outsel=%d, asel=
%d, bsel=%d, oen=%d, OUT=%d", clk, addressA,
addressB, dataIn, opsel, outsel,asel, bsel, oen, outPut);

end

 // Stimulate the Input Signals
initial
 begin

// 1. store (5) in [0]

#T

addressA = 5'b00000;

addressB = 5'b00000;

dataIn = 32'h000_0006;

opsel = 2'b01;

outsel =3'b000;

asel = 0;

bsel = 0;

oen = 1;


#(T*2)

// 2. store (AAAA_AAAA) in [1]


addressA = 5'b00000;

addressB = 5'b00001;

dataIn = 32'hAAAA_AAAA;

opsel = 2'b01;

outsel =3'b000;

asel = 0;

bsel = 0;

oen = 1;


#(T*2)
```

```
// 3. store (5555_5555) in [2]

addressA = 5'b00000;

addressB = 5'b00010;

dataIn = 32'h5555_5555;

opsel = 2'b01;

outsel =3'b000;

asel = 0;

bsel = 0;

oen = 1;

#(T*2)

// 4. store (0000_000A) in [3]

addressA = 5'b00000;

addressB = 5'b00011;

dataIn = 32'h0000_000A;

opsel = 2'b01;

outsel =3'b000;

asel = 0;

bsel = 0;

oen = 1;

#(T*2)

// 5. store (0000_0001) in [4]

addressA = 5'b00000;

addressB = 5'b00100;

dataIn = 32'h0000_0001;

opsel = 2'b01;

outsel =3'b000;

asel = 0;

bsel = 0;

oen = 1;

#(T*2)

// 6. store (FFFF_FFFF) in [5]

addressA = 5'b00000;

addressB = 5'b00101;

dataIn = 32'hFFFF_FFFF;

opsel = 2'b01;

outsel =3'b000;

asel = 0;

bsel = 0;

oen = 1;

#(T*2)

// 7. store (0000_00C8) in [6]

addressA = 5'b00000;

addressB = 5'b00110;

dataIn = 32'h0000_00C8;

opsel = 2'b01;

outsel =3'b000;

asel = 0;

bsel = 0;

oen = 1;

#(T*2)

// 8. store (0000_012C) in [7]

addressA = 5'b00000;

addressB = 5'b00111;
```

```
dataIn = 32'h0000_012C;

opsel = 2'b01;

outsel =3'b000;

asel = 0;

bsel = 0;

oen = 1;

#(T*2)

// 9. store (0000_0001) in [8]

addressA = 5'b00000;

addressB = 5'b01000;

dataIn = 32'h0000_0001;

opsel = 2'b01;

outsel =3'b000;

asel = 0;

bsel = 0;

oen = 1;

#(T*2)

// 10. store (AAAA_AAAB) in [9]

addressA = 5'b00000;

addressB = 5'b01001;

dataIn = 32'hAAAA_AAAB;

opsel = 2'b01;

outsel =3'b000;

asel = 0;

bsel = 0;

oen = 1;
```

```
#(T*2)

// 11. store (5555_5555) in [10]

addressA = 5'b00000;

addressB = 5'b01010;

dataIn = 32'h5555_5555;

opsel = 2'b01;

outsel =3'b000;

asel = 0;

bsel = 0;

oen = 1;

#(T*2)

// 12. ADD [2][0]

addressA = 5'd2;

addressB = 5'd0;

dataIn = 32'd0;

opsel = 2'b00;

outsel =3'b001;

asel = 1;

bsel = 1;

oen = 1;

#(T*2)

#(T*2)

// 13. ADD [1][2]

addressA = 5'd1;

addressB = 5'd2;

dataIn = 32'd0;

opsel = 2'b00;
```

```
outsel =3'b001;

asel = 1;

bsel = 1;

oen = 1;

#(T*2)

// 14. ADD [6][7]

addressA = 5'd6;

addressB = 5'd7;

dataIn = 32'd0;

opsel = 2'b00;

outsel =3'b001;

asel = 1;

bsel = 1;

oen = 1;

#(T*2)

// 15. ADD [0][3]

addressA = 5'd0;

addressB = 5'd3;

dataIn = 32'd0;

opsel = 2'b00;

outsel =3'b001;

asel = 1;

bsel = 1;

oen = 1;

#(T*2)

// 16. SUB [5][4]
```

```
addressA = 5'd5;

addressB = 5'd4;

dataIn = 32'd0;

opsel = 2'b01;

outsel =3'b001;

asel = 1;

bsel = 1;

oen = 1;

#(T*2)

// 17. ADD [5][8]

addressA = 5'd5;

addressB = 5'd8;

dataIn = 32'd0;

opsel = 2'b00;

outsel =3'b001;

asel = 1;

bsel = 1;

oen = 1;

#(T*2)

// 18. SUB [2][0]

addressA = 5'd2;

addressB = 5'd0;

dataIn = 32'd0;

opsel = 2'b01;

outsel =3'b001;

asel = 1;

bsel = 1;
```

```
oen = 1;

#(T*2)

// 19. ADD [9][10]

addressA = 5'd9;

addressB = 5'd10;

dataIn = 32'd0;

opsel = 2'b00;

outsel =3'b001;

asel = 1;

bsel = 1;

oen = 1;

#(T*2)

// 20. READ [8]

addressA = 5'd8;

addressB = 5'd8;

dataIn = 32'd0;

opsel = 2'b01;

outsel =3'b000;

asel = 1;

bsel = 0;

oen = 1;

#(T*2)

// 21. READ [10]

addressA = 5'd10;

addressB = 5'd10;

dataIn = 32'd0;

opsel = 2'b01;

outsel =3'b000;

asel = 1;

bsel = 0;

oen = 1;

#(T*2)

// 22. READ [4]

addressA = 5'd4;

addressB = 5'd4;

dataIn = 32'd0;

opsel = 2'b01;

outsel =3'b000;

asel = 1;

bsel = 0;

oen = 1;

#(T*2)

// 23. READ [2]

addressA = 5'd2;

addressB = 5'd2;

dataIn = 32'd0;

opsel = 2'b01;

outsel =3'b000;

asel = 1;

bsel = 0;

oen = 1;

#(T*2)

// 24. READ [7]
```

```
addressA = 5'd7;

addressB = 5'd7;

dataIn = 32'd0;

opsel = 2'b01;

outsel =3'b000;

asel = 1;

bsel = 0;

oen = 1;

#(T*2)

// 25. READ [3]

addressA = 5'd3;

addressB = 5'd3;

dataIn = 32'd0;

opsel = 2'b01;

outsel =3'b000;

asel = 1;

bsel = 0;

oen = 1;

#(T*2)

// 26. CMP [8][10]

addressA = 5'd8;

addressB = 5'd10;

dataIn = 32'd0;

opsel = 2'b00;

outsel =3'b100;

asel = 1;

bsel = 1;

oen = 1;

#(T*2)

// 27. CMP [4][2]

addressA = 5'd4;

addressB = 5'd2;

dataIn = 32'd0;

opsel = 2'b00;

outsel =3'b100;

asel = 1;

bsel = 1;

oen = 1;

#(T*2)

// 28. CMP [3][7]

addressA = 5'd3;

addressB = 5'd7;

dataIn = 32'd0;

opsel = 2'b00;

outsel =3'b100;

asel = 1;

bsel = 1;

oen = 1;

#(T*2)

// 29. READ [10]

addressA = 5'd10;

addressB = 5'd10;

dataIn = 32'd0;

opsel = 2'b01;

outsel =3'b000;
```

```
asel = 1;

bsel = 0;

oen = 1;

#(T*2)

// 30. READ [2]


addressA = 5'd2;

addressB = 5'd2;

dataIn = 32'd0;

opsel = 2'b01;

outsel =3'b000;

asel = 1;

bsel = 0;

oen = 1;
```

```
#(T*2)

// 31. READ [7]


addressA = 5'd7;

addressB = 5'd7;

dataIn = 32'd0;

opsel = 2'b01;

outsel =3'b000;

asel = 1;

bsel = 0;

oen = 1;

end
endmodule
```

Figure B: Test Bench with Comparator