ECE 429 Final project

Case Study for 32-bit Pipelined CPU design with New ALU Architecture

12/02/2016

A20345929

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1. INTRODUCTION

This Report will describes the “Case Study for 32-bit Pipelined CPU design with New ALU Architecture”. The objective of this project is to understand a 32-bit Pipelined Central Processing Unit (CPU). As the name of the design declares, the word length of the data used in the circuits is 32 bits. Furthermore, since this circuit is pipelined, more than one instruction can be executed simultaneously. The operation of the circuit is synchronized by an externally set clock signal. Also the instruction signals for addressing the memory file, selecting the Arithmetic Logic Unit (ALU) operands and specifying the operation of the ALU are also external. The correct synchronization of those signals with the critical data path delay of the circuit that will determine the minimum operating period is one of the objectives of the project.

2. ANALYSIS

- CASE STUDY 1

1) Generate the display screenshot or the text output of the RTL simulation and the screenshot from simvision with provided test bench (tb_cpu.v)

(1) cpu_CLA.v

```
Compiling source file "tb_cpu.v"
Compiling source file "cpu_CLA.v"

Warning!  Too few module port connections                    [Veri
          "cpu_CLA.v", 636: CLA0(.s(s[15:0]), .a(a[15:0]),
          .b(b[15:0]), .c0(c0), .c16(c16), .p_16(p[0]), .
          g_16(g[0]))

Warning!  Too few module port connections                    [Veri
          "cpu_CLA.v", 615: CLA0(.s(s[3:0]), .a(a[3:0]), .
          b(b[3:0]), .c0(c0), .c4(c4), .g_4(g[0]), .p_4(p[
          0]))

Warning!  Too few module port connections                    [Veri
          "cpu_CLA.v", 616: CLA1(.s(s[7:4]), .a(a[7:4]), .
          b(b[7:4]), .c0(c4), .c4(c8), .g_4(g[1]), .p_4(p[
          1]))

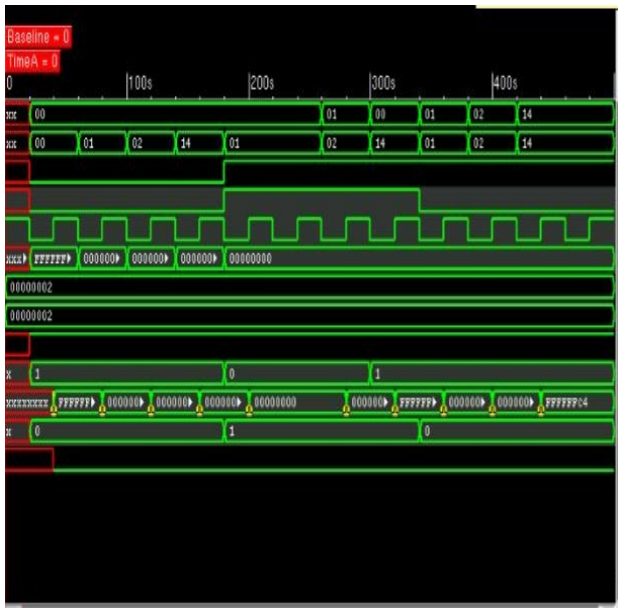
Warning!  Too few module port connections                    [Veri
          "cpu_CLA.v", 617: CLA2(.s(s[11:8]), .a(a[11:8]),
          .b(b[11:8]), .c0(c8), .c4(c12), .g_4(g[2]), .p_4(
          p[2]))

Warning!  Too few module port connections                    [Veri
          "cpu_CLA.v", 615: CLA0(.s(s[3:0]), .a(a[3:0]), .
          b(b[3:0]), .c0(c0), .c4(c4), .g_4(g[0]), .p_4(p[
          0]))

Warning!  Too few module port connections                    [Veri
          "cpu_CLA.v", 616: CLA1(.s(s[7:4]), .a(a[7:4]), .
          b(b[7:4]), .c0(c4), .c4(c8), .g_4(g[1]), .p_4(p[
          1]))

Warning!  Too few module port connections                    [Veri
          "cpu_CLA.v", 617: CLA2(.s(s[11:8]), .a(a[11:8]),
          .b(b[11:8]), .c0(c8), .c4(c12), .g_4(g[2]), .p_4(
          p[2]))
Highest level modules:
stimulus

L30 "tb_cpu.v": $finish at simulation time 501
7 warnings
0 simulation events (use +profile or +listcounts option to count)
rated events
CPU time: 0.0 secs to compile + 0.1 secs to link + 0.7 secs in si
```



(2) cpu_CRA.v

```
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talkv@cadence.com

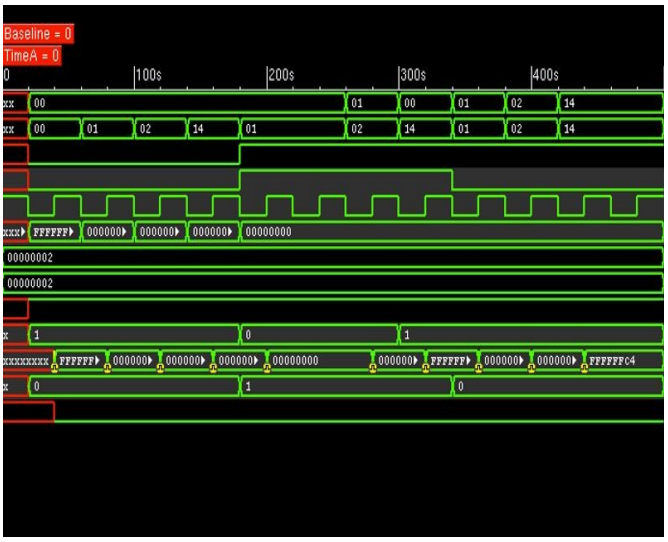
Compiling source file "tb_cpu.v"
Compiling source file "cpu_CRA.v"

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CRA.v", 557: cra0(.sum(sum[7:0]), .c_out(c7)
          , .a(a[7:0]), .b(b[7:0]), .c_in(c_in))

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CRA.v", 558: cra1(.sum(sum[15:8]), .c_out(
          c15), .a(a[15:8]), .b(b[15:8]), .c_in(c7))

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CRA.v", 559: cra2(.sum(sum[23:16]), .c_out(
          c23), .a(a[23:16]), .b(b[23:16]), .c_in(c15))
Highest level modules:
stimulus

L30 "tb_cpu.v": $finish at simulation time 501
3 warnings
0 simulation events (use +profile or +listcounts option to count) + 21024 accele
rated events
CPU time: 0.0 secs to compile + 0.1 secs to link + 0.7 secs in simulation
```



(3) cpu_CSA.v

```
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Compiling source file "tb_cpu.v"
Compiling source file "cpu_CSA.v"

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CSA.v", 598: cs0_15(.s(s[15:0]), .cout(c), .
          a(a[15:0]), .b(b[15:0]), .cin(cin))

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CSA.v", 582: cs0_3(.s(s[3:0]), .cout(c[0]),
          .a(a[3:0]), .b(b[3:0]), .cin(cin))

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CSA.v", 583: cs4_7(.s(s[7:4]), .cout(c[1]),
          .a(a[7:4]), .b(b[7:4]), .cin(c[0]))

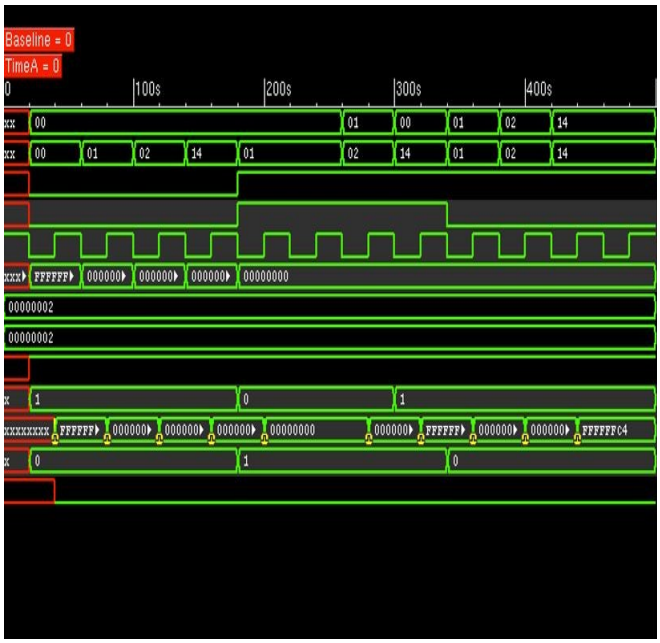
Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CSA.v", 584: cs8_11(.s(s[11:8]), .cout(c[2])
          , .a(a[11:8]), .b(b[11:8]), .cin(c[1]))

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CSA.v", 582: cs0_3(.s(s[3:0]), .cout(c[0]),
          .a(a[3:0]), .b(b[3:0]), .cin(cin))

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CSA.v", 583: cs4_7(.s(s[7:4]), .cout(c[1]),
          .a(a[7:4]), .b(b[7:4]), .cin(c[0]))

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CSA.v", 584: cs8_11(.s(s[11:8]), .cout(c[2])
          , .a(a[11:8]), .b(b[11:8]), .cin(c[1]))
Highest level modules:
stimulus

L30 "tb_cpu.v": $finish at simulation time 501
7 warnings
0 simulation events (use +profile or +listcounts option to count) + 21065 accele
rated events
CPU time: 0.0 secs to compile + 0.1 secs to link + 0.7 secs in simulation
```



(4) cpu_CSeA.v

```
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Compiling source file "tb_cpu.v"
Compiling source file "cpu_CSeA.v"

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CSeA.v", 606: cse1(.s(s[15:0]), .cout(c), .
          a(a[15:0]), .b(b[15:0]), .cin(cin))

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CSeA.v", 591: c1(.s(s[3:0]), .cout(c[1]), .
          a(a[3:0]), .b(b[3:0]), .cin(cin))

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CSeA.v", 592: c2(.s(s[7:4]), .cout(c[2]), .
          a(a[7:4]), .b(b[7:4]), .cin(c[1]))

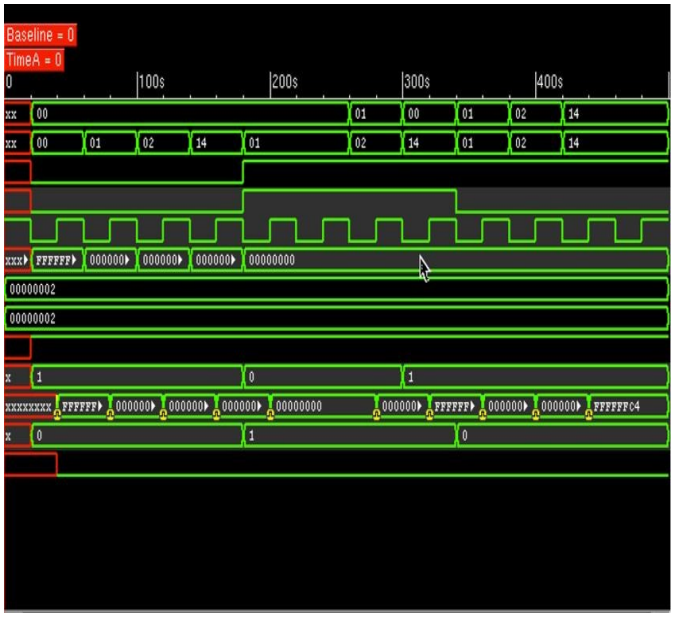
Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CSeA.v", 593: c3(.s(s[11:8]), .cout(c[3]), .
          a(a[11:8]), .b(b[11:8]), .cin(c[2]))

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CSeA.v", 591: c1(.s(s[3:0]), .cout(c[1]), .
          a(a[3:0]), .b(b[3:0]), .cin(cin))

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CSeA.v", 592: c2(.s(s[7:4]), .cout(c[2]), .
          a(a[7:4]), .b(b[7:4]), .cin(c[1]))

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CSeA.v", 593: c3(.s(s[11:8]), .cout(c[3]), .
          a(a[11:8]), .b(b[11:8]), .cin(c[2]))
Highest level modules:
stimulus

L30 "tb_cpu.v": $finish at simulation time 501
7 warnings
0 simulation events (use +profile or +listcounts option to count) + 21936 accele
rated events
CPU time: 0.0 secs to compile + 0.1 secs to link + 0.7 secs in simulation
```



2) Synthesize the design and summarize cell.rep and timing.rep

(1) cpu_CLA.v

```
Beginning Mapping Optimizations  (Medium effort)  (Incremental)
--------------------------------

Beginning Incremental Implementation Selection
----------------------------------------------

Beginning Delay Optimization Phase
----------------------------------

 ELAPSED            WORST NEG TOTAL NEG  DESIGN
   TIME      AREA      SLACK     SLACK   RULE COST         ENDPOINT
-------  ---------  --------- --------- --------- ------------------------
  0:00:02   48566.4      0.00       0.0       3.0
  0:00:03   48566.4      0.00       0.0       3.0
  0:00:03   48566.4      0.00       0.0       3.0


Beginning Design Rule Fixing  (max_capacitance)
-----------------------------

 ELAPSED            WORST NEG TOTAL NEG  DESIGN
   TIME      AREA      SLACK     SLACK   RULE COST         ENDPOINT
-------  ---------  --------- --------- --------- ------------------------
  0:00:03   48566.4      0.00       0.0       3.0
Loading db file '/apps/FreePDK45/osu_soc/lib/files/gscl45nm.db'

 Optimization Complete
 ---------------------
Warning: Design 'cpu' contains 1 high-fanout nets. A fanout number of 1000 will be used for del
ay calculations involving these nets. (TIM-134)
    Net 'clk': 1624 load(s), 1 driver(s)
1
check_design
1
#report_constraint -all_violators
set filename [format "%s%s"  $my_toplevel ".vh"]
cpu.vh
write -f verilog -output $filename
Writing verilog file '/home/ykim/ece429/project/cpu_CLA/cpu.vh'.
1
set filename [format "%s%s"  $my_toplevel ".sdc"]
cpu.sdc
write_sdc $filename
1
#set filename [format "%s%s"  $my_toplevel ".db"]
#write -f db -hier -output $filename -xg_force_db
redirect timing.rep { report_timing }
redirect cell.rep { report_cell }
redirect power.rep { report_power }
quit

Thank you...
```

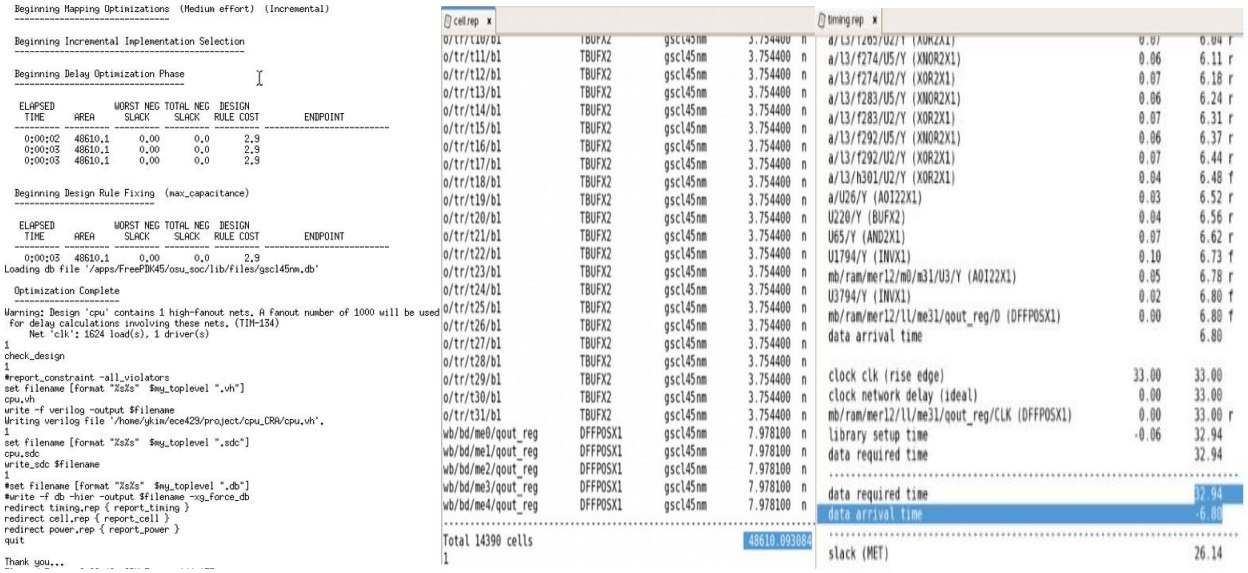
cell.rep

o/tr/t10/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t11/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t12/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t13/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t14/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t15/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t16/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t17/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t18/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t19/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t20/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t21/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t22/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t23/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t24/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t25/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t26/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t27/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t28/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t29/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t30/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t31/b1	TBUFX2	gscl45nm	3.754400	n
wb/bd/me0/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me1/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me2/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me3/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me4/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
Total 14359 cells				48566.448185

timing.rep

a/l3/f283/U5/Y (XNOR2X1)	0.06	6.11 r
a/l3/f274/U5/Y (XNOR2X1)	0.07	6.18 r
a/l3/f274/U2/Y (XOR2X1)	0.06	6.24 r
a/l3/f283/U5/Y (XNOR2X1)	0.07	6.31 r
a/l3/f283/U2/Y (XOR2X1)	0.06	6.37 r
a/l3/f292/U5/Y (XNOR2X1)	0.07	6.44 r
a/l3/f292/U2/Y (XOR2X1)	0.04	6.48 f
a/l3/h301/U2/Y (XOR2X1)	0.03	6.52 r
a/U26/Y (AOI22X1)	0.04	6.56 r
U219/Y (BUFX2)	0.07	6.62 r
U64/Y (AND2X1)	0.10	6.73 f
U1729/Y (INVX1)	0.05	6.78 r
mb/ram/mer12/m0/m31/U3/Y (AOI22X1)	0.02	6.80 f
U3762/Y (INVX1)	0.00	6.80 f
mb/ram/mer12/ll/me31/qout_reg/D (DFFPOSX1)		6.80
data arrival time		6.80
clock clk (rise edge)	33.00	33.00
clock network delay (ideal)	0.00	33.00
mb/ram/mer12/ll/me31/qout_reg/CLK (DFFPOSX1)	0.00	33.00 r
library setup time	-0.06	32.94
data required time		32.94
data required time		32.94
data arrival time		-6.80
slack (MET)		26.14

(2) cpu_CRA.v



```
Beginning Mapping Optimizations  (Medium effort)  (Incremental)
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Beginning Incremental Implementation Selection
-----------------------------------------------

Beginning Delay Optimization Phase
-----------------------------------

 ELAPSED            WORST NEG TOTAL NEG  DESIGN
   TIME     AREA      SLACK     SLACK   RULE COST         ENDPOINT
 --------- --------- --------- --------- --------- --------------------------
   0:00:02   48610.1      0.00       0.0       2.9
   0:00:03   48610.1      0.00       0.0       2.9
   0:00:03   48610.1      0.00       0.0       2.9


Beginning Design Rule Fixing  (max_capacitance)
-----------------------------

 ELAPSED            WORST NEG TOTAL NEG  DESIGN
   TIME     AREA      SLACK     SLACK   RULE COST         ENDPOINT
 --------- --------- --------- --------- --------- --------------------------
   0:00:03   48610.1      0.00       0.0       2.9
Loading db file '/apps/FreePDK45/osu_soc/lib/files/gscl45nm.db'

  Optimization Complete
  ---------------------
Warning: Design 'cpu' contains 1 high-fanout nets. A fanout number of 1000 will be used
 for delay calculations involving these nets. (TIM-134)
    Net 'clk': 1624 load(s), 1 driver(s)
1
check_design
1
#report_constraint -all_violators
set filename [format "%s%s"  $my_toplevel ".vh"]
cpu.vh
write -f verilog -output $filename
Writing verilog file '/home/ykim/ece429/project/cpu_CRA/cpu.vh'.
1
set filename [format "%s%s"  $my_toplevel ".sdc"]
cpu.sdc
write_sdc $filename
1
#set filename [format "%s%s"  $my_toplevel ".db"]
#write -f db -hier -output $filename -xg_force_db
redirect timing.rep { report_timing }
redirect cell.rep { report_cell }
redirect power.rep { report_power }
quit

Thank you...
```

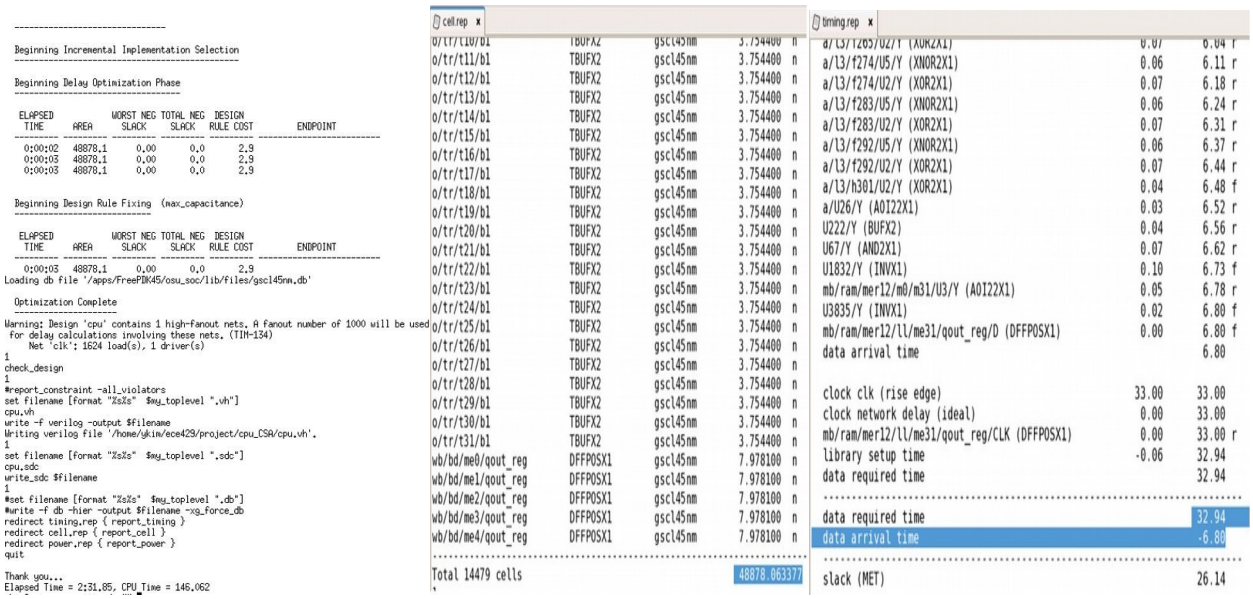
cell.rep

o/tr/t10/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t11/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t12/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t13/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t14/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t15/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t16/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t17/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t18/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t19/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t20/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t21/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t22/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t23/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t24/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t25/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t26/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t27/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t28/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t29/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t30/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t31/b1	TBUFX2	gscl45nm	3.754400	n
wb/bd/me0/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me1/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me2/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me3/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me4/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
Total 14390 cells			48610.093084	
1				

timing.rep

a/l3/f265/U2/Y (XOR2X1)	0.07	6.04 r
a/l3/f274/U5/Y (XNOR2X1)	0.06	6.11 r
a/l3/f274/U2/Y (XOR2X1)	0.07	6.18 r
a/l3/f283/U5/Y (XNOR2X1)	0.06	6.24 r
a/l3/f283/U2/Y (XOR2X1)	0.07	6.31 r
a/l3/f292/U5/Y (XNOR2X1)	0.06	6.37 r
a/l3/f292/U2/Y (XOR2X1)	0.07	6.44 r
a/l3/h301/U2/Y (XOR2X1)	0.04	6.48 f
a/U26/Y (AOI22X1)	0.03	6.52 r
U220/Y (BUFX2)	0.04	6.56 r
U65/Y (AND2X1)	0.07	6.62 r
U1794/Y (INVX1)	0.10	6.73 f
mb/ram/mer12/m0/m31/U3/Y (AOI22X1)	0.05	6.78 r
U3794/Y (INVX1)	0.02	6.80 f
mb/ram/mer12/ll/me31/qout_reg/D (DFFPOSX1)	0.00	6.80 f
data arrival time		6.80
clock clk (rise edge)	33.00	33.00
clock network delay (ideal)	0.00	33.00
mb/ram/mer12/ll/me31/qout_reg/CLK (DFFPOSX1)	0.00	33.00 r
library setup time	-0.06	32.94
data required time		32.94
data required time		32.94
data arrival time		-6.80
slack (MET)		26.14

(3) cpu_CSA.v



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Beginning Incremental Implementation Selection
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Beginning Delay Optimization Phase
-----------------------------------

 ELAPSED            WORST NEG TOTAL NEG  DESIGN
   TIME     AREA      SLACK     SLACK   RULE COST         ENDPOINT
 --------- --------- --------- --------- --------- --------------------------
   0:00:02   48878.1      0.00       0.0       2.9
   0:00:03   48878.1      0.00       0.0       2.9
   0:00:03   48878.1      0.00       0.0       2.9


Beginning Design Rule Fixing  (max_capacitance)
-----------------------------

 ELAPSED            WORST NEG TOTAL NEG  DESIGN
   TIME     AREA      SLACK     SLACK   RULE COST         ENDPOINT
 --------- --------- --------- --------- --------- --------------------------
   0:00:03   48878.1      0.00       0.0       2.9
Loading db file '/apps/FreePDK45/osu_soc/lib/files/gscl45nm.db'

  Optimization Complete
  ---------------------
Warning: Design 'cpu' contains 1 high-fanout nets. A fanout number of 1000 will be used
 for delay calculations involving these nets. (TIM-134)
    Net 'clk': 1624 load(s), 1 driver(s)
1
check_design
1
#report_constraint -all_violators
set filename [format "%s%s"  $my_toplevel ".vh"]
cpu.vh
write -f verilog -output $filename
Writing verilog file '/home/ykim/ece429/project/cpu_CSA/cpu.vh'.
1
set filename [format "%s%s"  $my_toplevel ".sdc"]
cpu.sdc
write_sdc $filename
1
#set filename [format "%s%s"  $my_toplevel ".db"]
#write -f db -hier -output $filename -xg_force_db
redirect timing.rep { report_timing }
redirect cell.rep { report_cell }
redirect power.rep { report_power }
quit

Thank you...
Elapsed Time = 2:31.85, CPU_Time = 146.062
```

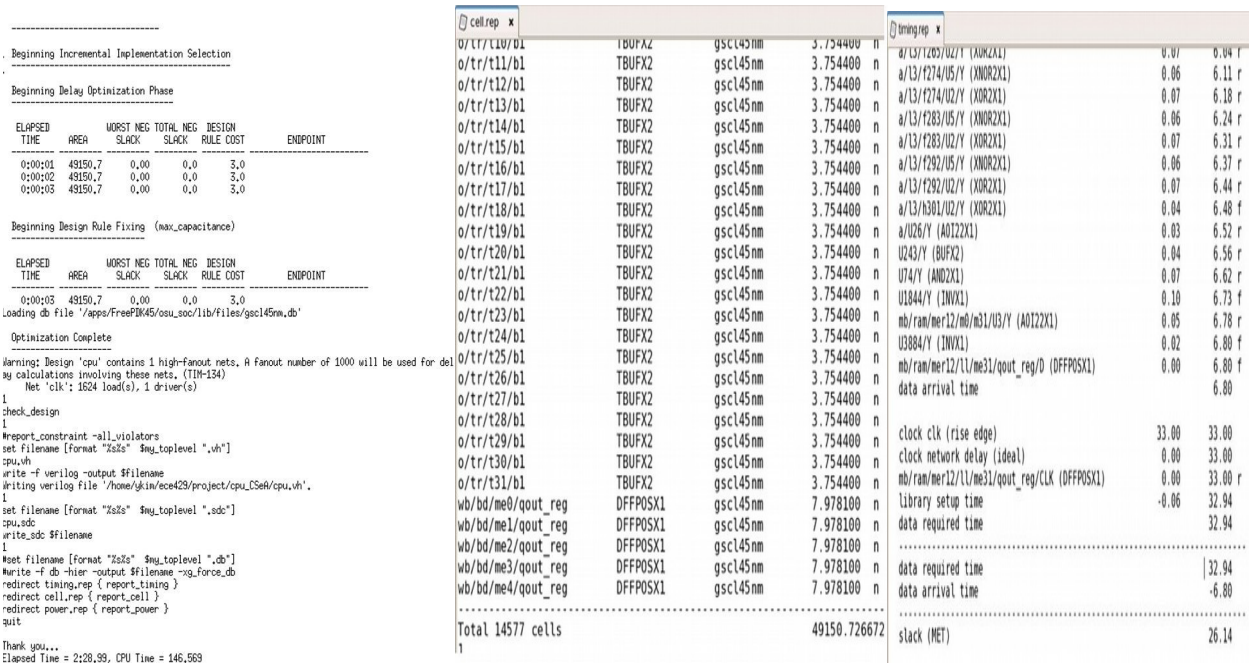
cell.rep

o/tr/t10/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t11/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t12/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t13/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t14/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t15/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t16/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t17/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t18/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t19/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t20/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t21/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t22/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t23/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t24/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t25/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t26/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t27/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t28/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t29/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t30/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t31/b1	TBUFX2	gscl45nm	3.754400	n
wb/bd/me0/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me1/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me2/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me3/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me4/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
Total 14479 cells			48878.063377	

timing.rep

a/l3/f265/U2/Y (XOR2X1)	0.07	6.04 r
a/l3/f274/U5/Y (XNOR2X1)	0.06	6.11 r
a/l3/f274/U2/Y (XOR2X1)	0.07	6.18 r
a/l3/f283/U5/Y (XNOR2X1)	0.06	6.24 r
a/l3/f283/U2/Y (XOR2X1)	0.07	6.31 r
a/l3/f292/U5/Y (XNOR2X1)	0.06	6.37 r
a/l3/f292/U2/Y (XOR2X1)	0.07	6.44 r
a/l3/h301/U2/Y (XOR2X1)	0.04	6.48 f
a/U26/Y (AOI22X1)	0.03	6.52 r
U222/Y (BUFX2)	0.04	6.56 r
U67/Y (AND2X1)	0.07	6.62 r
U1832/Y (INVX1)	0.10	6.73 f
mb/ram/mer12/m0/m31/U3/Y (AOI22X1)	0.05	6.78 r
U3835/Y (INVX1)	0.02	6.80 f
mb/ram/mer12/ll/me31/qout_reg/D (DFFPOSX1)	0.00	6.80 f
data arrival time		6.80
clock clk (rise edge)	33.00	33.00
clock network delay (ideal)	0.00	33.00
mb/ram/mer12/ll/me31/qout_reg/CLK (DFFPOSX1)	0.00	33.00 r
library setup time	-0.06	32.94
data required time		32.94
data required time		32.94
data arrival time		-6.80
slack (MET)		26.14

(4) cpu_CSeA.v



```
Beginning Incremental Implementation Selection

Beginning Delay Optimization Phase

  ELAPSED            WORST NEG TOTAL NEG  DESIGN
    TIME      AREA     SLACK     SLACK   RULE COST        ENDPOINT
  --------  --------  --------  --------  ---------  -------------------------
    0:00:01   49150.7      0.00       0.0        3.0
    0:00:02   49150.7      0.00       0.0        3.0
    0:00:03   49150.7      0.00       0.0        3.0

Beginning Design Rule Fixing  (max_capacitance)

  ELAPSED            WORST NEG TOTAL NEG  DESIGN
    TIME      AREA     SLACK     SLACK   RULE COST        ENDPOINT
  --------  --------  --------  --------  ---------  -------------------------
    0:00:03   49150.7      0.00       0.0        3.0
Loading db file '/apps/FreePDK45/osu_soc/lib/files/gscl45nm.db'

  Optimization Complete

Warning: Design 'cpu' contains 1 high-fanout nets. A fanout number of 1000 will be used for del
ay calculations involving these nets. (TIM-134)
    Net 'clk': 1624 load(s), 1 driver(s)
1
check_design
1
#report_constraint -all_violators
set filename [format "%s%s"  $my_toplevel ".vh"]
cpu.vh
write -f verilog -output $filename
Writing verilog file '/home/ykim/ece429/project/cpu_CSeA/cpu.vh'.
1
set filename [format "%s%s"  $my_toplevel ".sdc"]
cpu.sdc
write_sdc $filename
1
#set filename [format "%s%s"  $my_toplevel ".db"]
#write -f db -hier -output $filename -xg_force_db
redirect timing.rep { report_timing }
redirect cell.rep { report_cell }
redirect power.rep { report_power }
quit

Thank you...
Elapsed Time = 2:28.99, CPU Time = 146.569
```

cell.rep

o/tr/t10/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t11/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t12/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t13/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t14/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t15/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t16/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t17/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t18/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t19/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t20/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t21/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t22/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t23/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t24/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t25/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t26/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t27/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t28/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t29/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t30/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t31/b1	TBUFX2	gscl45nm	3.754400	n
wb/bd/me0/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me1/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me2/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me3/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me4/qout_reg	DFFPOSX1	gscl45nm	7.978100	n

Total 14577 cells 49150.726672

1

timing.rep

a/l3/f285/U2/Y (XNOR2X1)	0.07	6.04 r
a/l3/f274/U5/Y (XNOR2X1)	0.06	6.11 r
a/l3/f274/U2/Y (XOR2X1)	0.07	6.18 r
a/l3/f283/U5/Y (XNOR2X1)	0.06	6.24 r
a/l3/f283/U2/Y (XOR2X1)	0.07	6.31 r
a/l3/f292/U5/Y (XNOR2X1)	0.06	6.37 r
a/l3/f292/U2/Y (XOR2X1)	0.07	6.44 r
a/l3/h301/U2/Y (XOR2X1)	0.04	6.48 f
a/U26/Y (AOI22X1)	0.03	6.52 r
U243/Y (BUFX2)	0.04	6.56 r
U74/Y (AND2X1)	0.07	6.62 r
U1844/Y (INVX1)	0.10	6.73 f
mb/ram/mer12/m0/m31/U3/Y (AOI22X1)	0.05	6.78 r
U3884/Y (INVX1)	0.02	6.80 f
mb/ram/mer12/ll/me31/qout_reg/D (DFFPOSX1)	0.00	6.80 f
data arrival time		6.80
clock clk (rise edge)	33.00	33.00
clock network delay (ideal)	0.00	33.00
mb/ram/mer12/ll/me31/qout_reg/CLK (DFFPOSX1)	0.00	33.00 r
library setup time	-0.06	32.94
data required time		32.94
data required time		32.94
data arrival time		-6.80
slack (MET)		26.14

3) Provide the display screenshot or the text output of the post-synthesis simulation and the screenshot from simvision

(1) cpu_CLA.v

```
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                San Jose, California  95134

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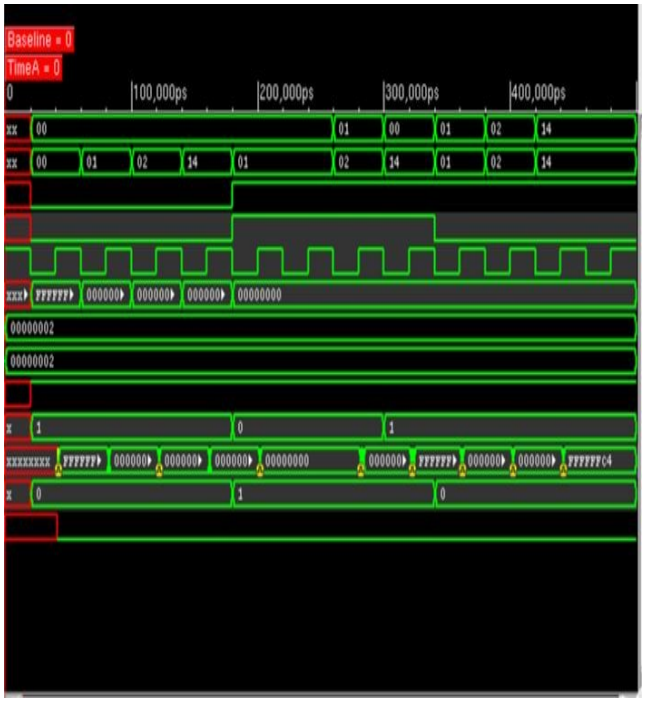
talkv@cadence.com

Compiling source file "gscl45nm.v"
Compiling source file "tb_cpu.v"
Compiling source file "cpu.vh"
Highest level modules:
BUFX4
CLKBUF1
CLKBUF2
CLKBUF3
DFFNEGX1
DFFSR
FAX1
HAX1
INVX2
INVX4
INVX8
LATCH
MUX2X1
NAND3X1
NOR3X1
OAI22X1
OR2X2
TBUFX1
stimulus


"gscl45nm.v", 299: Timing violation in stimulus.proj.\a/l3/rc30/qout_reg
    $setup( negedge D:35999, posedge CLK:36000,  0.09 : 9 );

L30 "tb_cpu.v": $finish at simulation time 50100
0 simulation events (use +profile or +listcounts option to count) + 199395 accel
erated events + 345566 timing check events
CPU time: 0.1 secs to compile + 0.2 secs to link + 0.1 secs in simulation
```



(2) cpu_CRA.v

```
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                San Jose, California  95134

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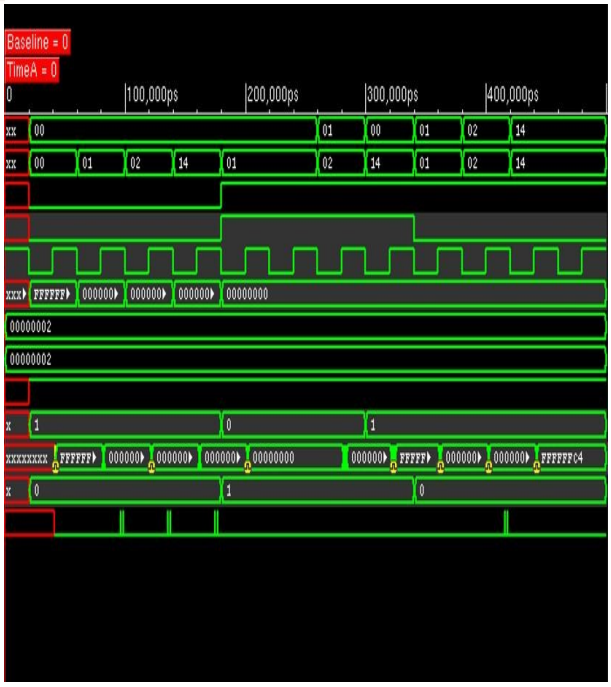
Compiling source file "gscl45nm.v"
Compiling source file "tb_cpu.v"
Compiling source file "cpu.vh"
Highest level modules:
AOI21X1
BUFX4
CLKBUF1
CLKBUF2
CLKBUF3
DFFNEGX1
DFFSR
FAX1
HAX1
INVX2
INVX4
INVX8
LATCH
MUX2X1
NAND3X1
NOR3X1
OAI22X1
OR2X2
TBUFX1
stimulus


"gscl45nm.v", 299: Timing violation in stimulus.proj.\a/l3/rc30/qout_reg
    $setup( negedge D:35999, posedge CLK:36000,  0.09 : 9 );

L30 "tb_cpu.v": $finish at simulation time 50100
0 simulation events (use +profile or +listcounts option to count) + 201694 accel
erated events + 345566 timing check events
CPU time: 0.1 secs to compile + 0.1 secs to link + 0.2 secs in simulation
```



(3) cpu_CSA.v

```
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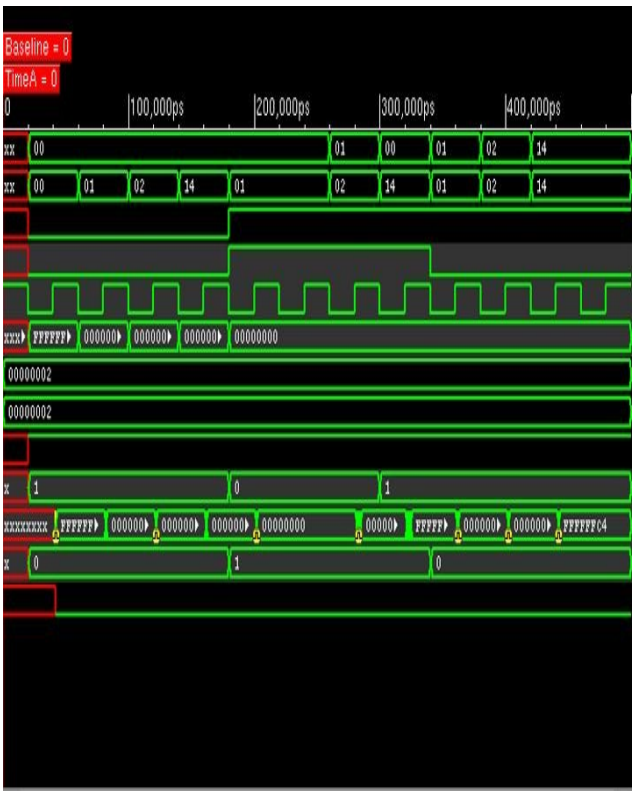
talkv@cadence.com

Compiling source file "gscl45nm.v"
Compiling source file "tb_cpu.v"
Compiling source file "cpu.vh"
Highest level modules:
AOI21X1
BUFX4
CLKBUF1
CLKBUF2
CLKBUF3
DFFNEGX1
DFFSR
FAX1
HAX1
INVX2
INVX4
INVX8
LATCH
MUX2X1
NOR3X1
OAI22X1
OR2X2
TBUFX1
stimulus


"gscl45nm.v", 299: Timing violation in stimulus.proj.\a/l3/rc30/qout_reg
    $setup( negedge D:35999, posedge CLK:36000,  0.09 : 9 );

L30 "tb_cpu.v": $finish at simulation time 50100
0 simulation events (use +profile or +listcounts option to count) + 203407 accel
erated events + 345558 timing check events
CPU time: 0.1 secs to compile + 0.1 secs to link + 0.2 secs in simulation
```



(4) cpu_CSeA

```
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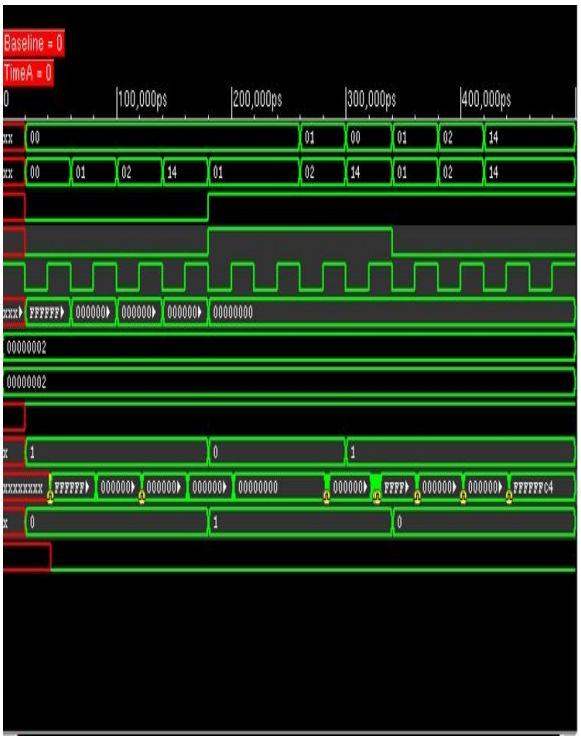
Compiling source file "gscl45nm.v"
Compiling source file "tb_cpu.v"
Compiling source file "cpu.vh"
Highest level modules:
AOI21X1
BUFX4
CLKBUF1
CLKBUF2
CLKBUF3
DFFNEGX1
DFFSR
FAX1
HAX1
INVX2
INVX4
INVX8
LATCH
MUX2X1
NAND3X1
NOR3X1
OAI22X1
OR2X2
TBUFX1
stimulus


"gscl45nm.v", 299: Timing violation in stimulus.proj.\a/l3/rc30/qout_reg
    $setup( negedge D:35999, posedge CLK:36000,  0.09 : 9 );

L30 "tb_cpu.v": $finish at simulation time 50100
0 simulation events (use +profile or +listcounts option to count) + 207669 accel
erated events + 345638 timing check events
CPU time: 0.1 secs to compile + 0.1 secs to link + 0.1 secs in simulation
```



4) Summarize timing.rep.5.final. What is the maximum clock frequency this circuit can run

(1) cpu_CLA.v

```
     | m0pd/bb/me1/qout_reg/Q          |   v   | B[1]                          | DFFPOSX1 | 0.249 |
0.581 |   18.502 |
     | mb/ram/mer30/m0/m31/U3/D        |   ^   | n13                           | AOI22X1  | 0.015 |
10.751 |   28.672 |
```

$$\frac{1}{clock_{\min}} = f_{\max} \qquad \frac{1}{D-Q} = f_{\max} \qquad \frac{1}{28.672-18.502} = 0.098328\,Hz$$

(2) cpu_CRA.v

```
     | mb/ram/mer15/m0/m30/U3/D        |   ^   | n993                          | AOI22X1  | 0.030 |
10.709 |   28.167 |
     | m0pd/bb/me2/qout_reg/Q          |   v   | B[2]                          | DFFPOSX1 | 0.244 |
0.607 |   18.065 |
```

$$\frac{1}{clock_{\min}} = f_{\max} \qquad \frac{1}{D-Q} = f_{\max} \qquad \frac{1}{28.167-18.065} = 0.09899\,Hz$$

(3) cpu_CSA.v

```
     | m0pd/bb/mel/qout_reg/Q          |   v   | B[1]                          | DFFPOSX1 | 0.216 |
0.525 |   18.844 |
     | mb/ram/mer11/m0/m31/U3/D        |   ^   | n1017                         | AOI22X1  | 0.017 |
10.827 |   29.146 |
```

$$\frac{1}{clock_{\min}} = f_{\max} \qquad \frac{1}{D-Q} = f_{\max} \qquad \frac{1}{29.146-18.844} = 0.097069\,Hz$$

(4) cpu_CSeA.v

```
     | m0pd/bb/mel/qout_reg/Q          |   v   | B[1]                          | DFFPOSX1 | 0.251 |
0.564 |   18.709 |
     | mb/ram/mer18/m0/m31/U3/D        |   ^   | n1028                         | AOI22X1  | 0.020 |
10.874 |   29.019 |
```

$$\frac{1}{clock_{\min}} = f_{\max} \qquad \frac{1}{D-Q} = f_{\max} \qquad \frac{1}{29.019-18.709} = 0.096993\,Hz$$

5) Provide the display screenshot or the text output of the post-P&R simulation and the screenshot from simvision

(1) cpu_CLA.v

```
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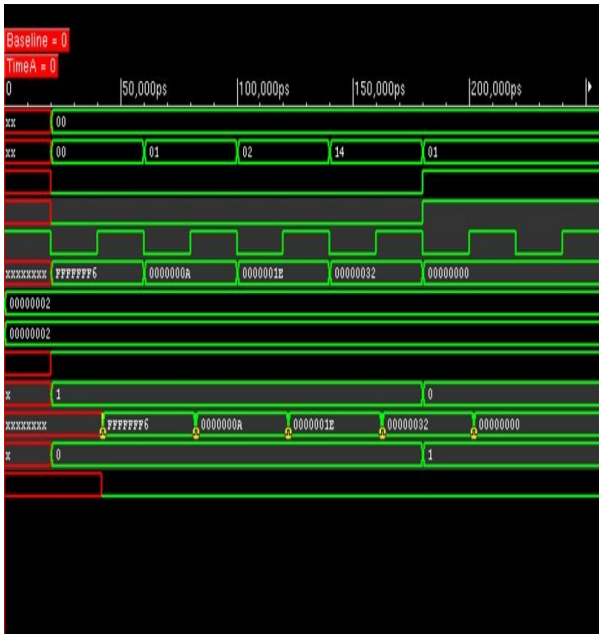
Compiling source file "gscl45nm.v"
Compiling source file "tb_cpu.v"
Compiling source file "final.v"
Highest level modules:
BUFX4
CLKBUF1
CLKBUF2
CLKBUF3
DFFNEGX1
DFFSR
FAX1
HAX1
INVX2
LATCH
MUX2X1
NAND3X1
NOR3X1
OAI22X1
OR2X2
TBUFX1
stimulus


"gscl45nm.v", 299: Timing violation in stimulus.proj.\a/l3/rc30/qout_reg
    $setup( negedge D:36017, posedge CLK:36018,  0.09 : 9 );

L30 "tb_cpu.v": $finish at simulation time 50100
0 simulation events (use +profile or +listcounts option to count) + 203917 accel
erated events + 345566 timing check events
CPU time: 0.1 secs to compile + 0.1 secs to link + 0.2 secs in simulation
```



(2) cpu_CRA.v

```
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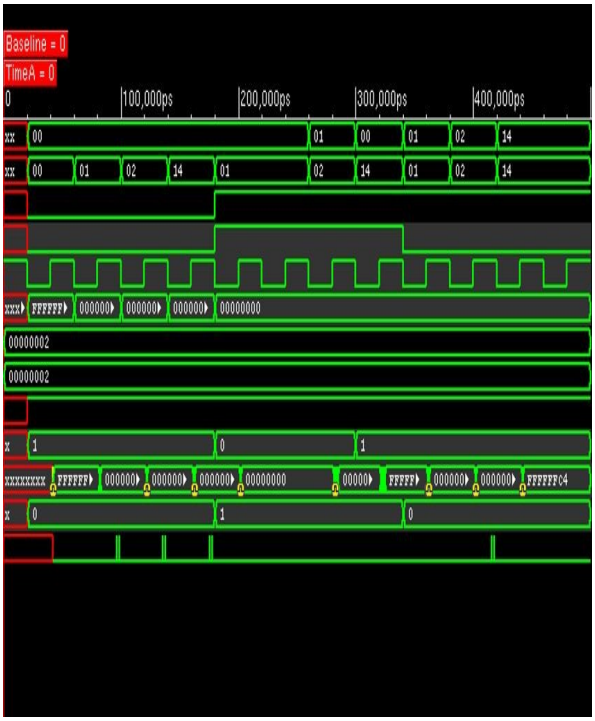
talkv@cadence.com

Compiling source file "gscl45nm.v"
Compiling source file "tb_cpu.v"
Compiling source file "final.v"
Highest level modules:
AOI21X1
BUFX4
CLKBUF1
CLKBUF2
CLKBUF3
DFFNEGX1
DFFSR
FAX1
HAX1
INVX2
INVX4
LATCH
MUX2X1
NAND3X1
NOR3X1
OAI22X1
OR2X2
TBUFX1
stimulus


"gscl45nm.v", 299: Timing violation in stimulus.proj.\a/l3/rc30/qout_reg
    $setup( negedge D:36017, posedge CLK:36018,  0.09 : 9 );

L30 "tb_cpu.v": $finish at simulation time 50100
0 simulation events (use +profile or +listcounts option to count) + 205645 accel
erated events + 345566 timing check events
CPU time: 0.1 secs to compile + 0.1 secs to link + 0.2 secs in simulation
```



(3) cpu_CSA.v

```
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Rights at 48 CFR 52.227-19, as applicable.

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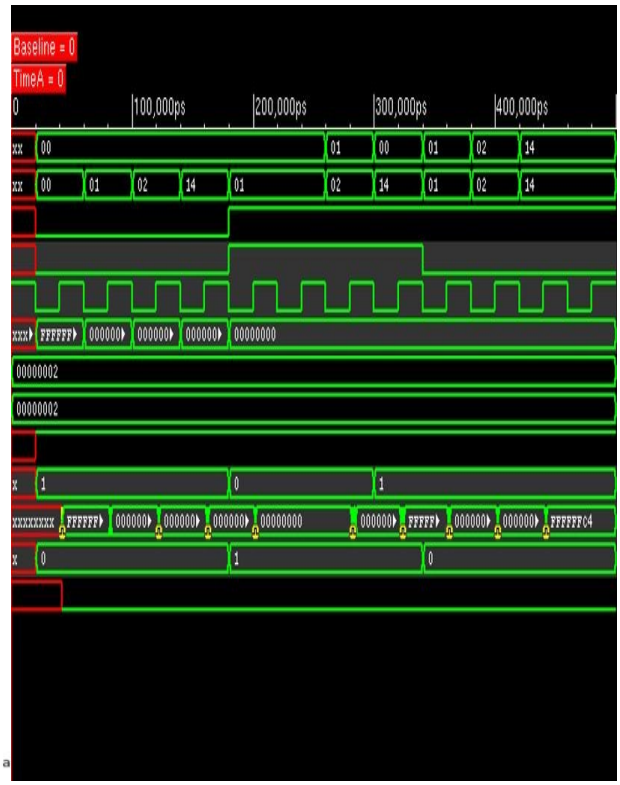
Compiling source file "gscl45nm.v"
Compiling source file "tb_cpu.v"
Compiling source file "final.v"
Highest level modules:
AOI21X1
BUFX4
CLKBUF1
CLKBUF2
CLKBUF3
DFFNEGX1
DFFSR
FAX1
HAX1
INVX2
LATCH
MUX2X1
NOR3X1
OAI22X1
OR2X2
TBUFX1
stimulus


"gscl45nm.v", 299: Timing violation in stimulus.proj.\a/l3/rc30/qout_reg
    $setup( negedge D:36017, posedge CLK:36018,  0.09 : 9 );

L30 "tb_cpu.v": $finish at simulation time 50100
0 simulation events (use +profile or +listcounts option to count) + 207877 a
```



(4) cpu_CSeA.v

```
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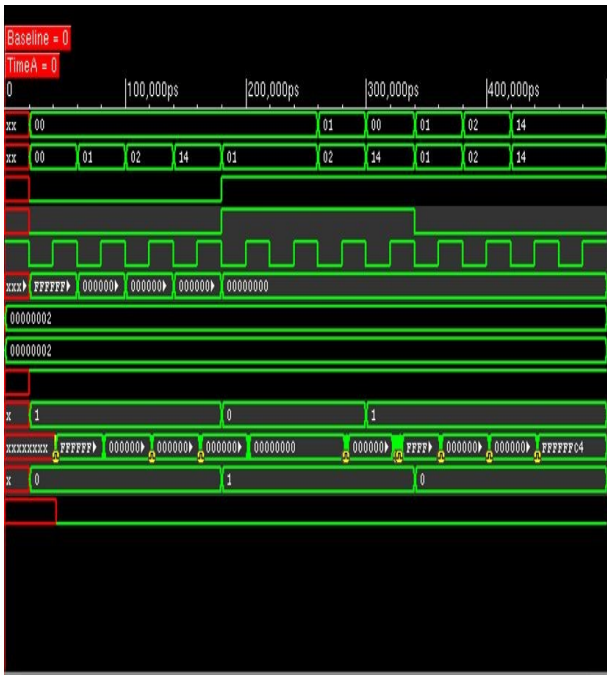
Compiling source file "gscl45nm.v"
Compiling source file "tb_cpu.v"
Compiling source file "final.v"
Highest level modules:
AOI21X1
BUFX4
CLKBUF1
CLKBUF2
CLKBUF3
DFFNEGX1
DFFSR
FAX1
HAX1
INVX2
INVX4
LATCH
MUX2X1
NAND3X1
NOR3X1
OAI22X1
OR2X2
TBUFX1
stimulus


"gscl45nm.v", 299: Timing violation in stimulus.proj.\a/l3/rc30/qout_reg
    $setup( negedge D:36017, posedge CLK:36018,  0.09 : 9 );

L30 "tb_cpu.v": $finish at simulation time 50100
0 simulation events (use +profile or +listcounts option to count) + 211984 accelerated
events + 345638 timing check events
CPU time: 0.1 secs to compile + 0.1 secs to link + 0.2 secs in simulation
```



6) Generate a new test bech file (tb_test.v) for the following instruction set

- See the attached file, “tb_test.v”

7) Provide the display screenshot and the text output of the RTL simulation and the screenshot from simvision for each cpu desgin (cpu_CRA.v, cpu_CLA.v, cpu_CSA.v, cpu_CSeA.v) with the new generated test bench (tb_test.v)

(1) cpu_CLA.v

```
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Compiling source file "tb_test.v"
Compiling source file "cpu_CLA.v"

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CLA.v", 636: CLA0(.s(s[15:0]), .a(a[15:0]),
          .b(b[15:0]), .c0(c0), .c16(c16), .p_16(p[0]), .
          g_16(g[0]))

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CLA.v", 615: CLA0(.s(s[3:0]), .a(a[3:0]), .
          b(b[3:0]), .c0(c0), .c4(c4), .g_4(g[0]), .p_4(p[
          0]))

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CLA.v", 616: CLA1(.s(s[7:4]), .a(a[7:4]), .
          b(b[7:4]), .c0(c4), .c4(c8), .g_4(g[1]), .p_4(p[
          1]))

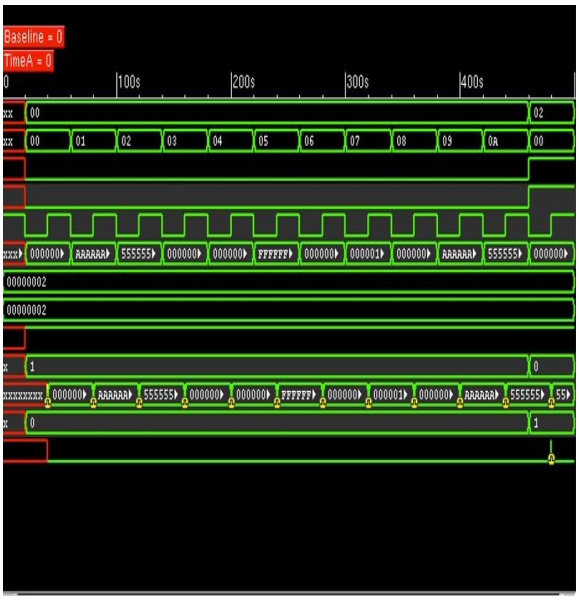
Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CLA.v", 617: CLA2(.s(s[11:8]), .a(a[11:8]),
          .b(b[11:8]), .c0(c8), .c4(c12), .g_4(g[2]), .p_4(
          p[2]))

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CLA.v", 615: CLA0(.s(s[3:0]), .a(a[3:0]), .
          b(b[3:0]), .c0(c0), .c4(c4), .g_4(g[0]), .p_4(p[
          0]))

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CLA.v", 616: CLA1(.s(s[7:4]), .a(a[7:4]), .
          b(b[7:4]), .c0(c4), .c4(c8), .g_4(g[1]), .p_4(p[
          1]))

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CLA.v", 617: CLA2(.s(s[11:8]), .a(a[11:8]),
          .b(b[11:8]), .c0(c8), .c4(c12), .g_4(g[2]), .p_4(
          p[2]))
Highest level modules:
stimulus

L30 "tb_test.v": $finish at simulation time 501
7 warnings
0 simulation events (use +profile or +listcounts option to count) + 14688 accele
rated events
CPU time: 0.0 secs to compile + 0.2 secs to link + 0.4 secs in simulation
```



(2) cpu_CRA.v

```
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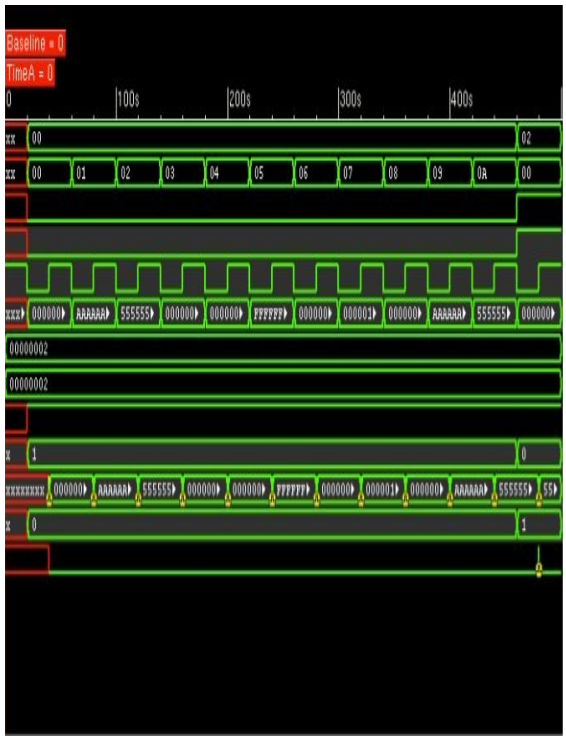
Compiling source file "tb_test.v"
Compiling source file "cpu_CRA.v"

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CRA.v", 557: cra0(.sum(sum[7:0]), .c_out(c7)
          , .a(a[7:0]), .b(b[7:0]), .c_in(c_in))

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CRA.v", 558: cra1(.sum(sum[15:8]), .c_out(
          c15), .a(a[15:8]), .b(b[15:8]), .c_in(c7))

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CRA.v", 559: cra2(.sum(sum[23:16]), .c_out(
          c23), .a(a[23:16]), .b(b[23:16]), .c_in(c15))
Highest level modules:
stimulus

L30 "tb_test.v": $finish at simulation time 501
3 warnings
0 simulation events (use +profile or +listcounts option to count) + 16246 accele
rated events
CPU time: 0.0 secs to compile + 0.1 secs to link + 0.4 secs in simulation
```



(3) cpu_CSA.v

```
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Compiling source file "tb_test.v"
Compiling source file "cpu_CSA.v"

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CSA.v", 598: cs0_15(.s(s[15:0]), .cout(c), .
          a(a[15:0]), .b(b[15:0]), .cin(cin))

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CSA.v", 582: cs0_3(.s(s[3:0]), .cout(c[0]),
          .a(a[3:0]), .b(b[3:0]), .cin(cin))

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CSA.v", 583: cs4_7(.s(s[7:4]), .cout(c[1]),
          .a(a[7:4]), .b(b[7:4]), .cin(c[0]))

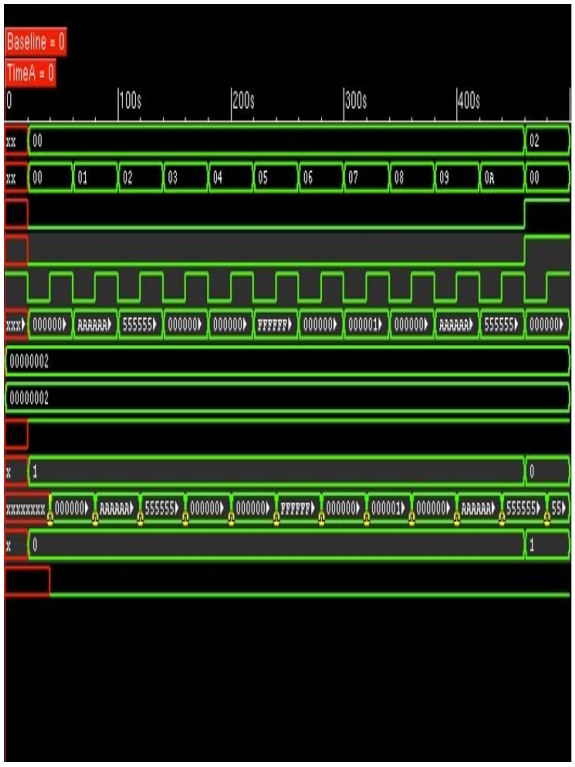
Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CSA.v", 584: cs8_11(.s(s[11:8]), .cout(c[2])
          , .a(a[11:8]), .b(b[11:8]), .cin(c[1]))

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CSA.v", 582: cs0_3(.s(s[3:0]), .cout(c[0]),
          .a(a[3:0]), .b(b[3:0]), .cin(cin))

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CSA.v", 583: cs4_7(.s(s[7:4]), .cout(c[1]),
          .a(a[7:4]), .b(b[7:4]), .cin(c[0]))

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CSA.v", 584: cs8_11(.s(s[11:8]), .cout(c[2])
          , .a(a[11:8]), .b(b[11:8]), .cin(c[1]))
Highest level modules:
stimulus

L30 "tb_test.v": $finish at simulation time 501
7 warnings
0 simulation events (use +profile or +listcounts option to count) + 16304 accele
rated events
CPU time: 0.0 secs to compile + 0.1 secs to link + 0.4 secs in simulation
```



(4) cpu_CSeA.v

```
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Compiling source file "tb_test.v"
Compiling source file "cpu_CSeA.v"

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CSeA.v", 606: csel(.s(s[15:0]), .cout(c), .
          a(a[15:0]), .b(b[15:0]), .cin(cin))

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CSeA.v", 591: c1(.s(s[3:0]), .cout(c[1]), .
          a(a[3:0]), .b(b[3:0]), .cin(cin))

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CSeA.v", 592: c2(.s(s[7:4]), .cout(c[2]), .
          a(a[7:4]), .b(b[7:4]), .cin(c[1]))

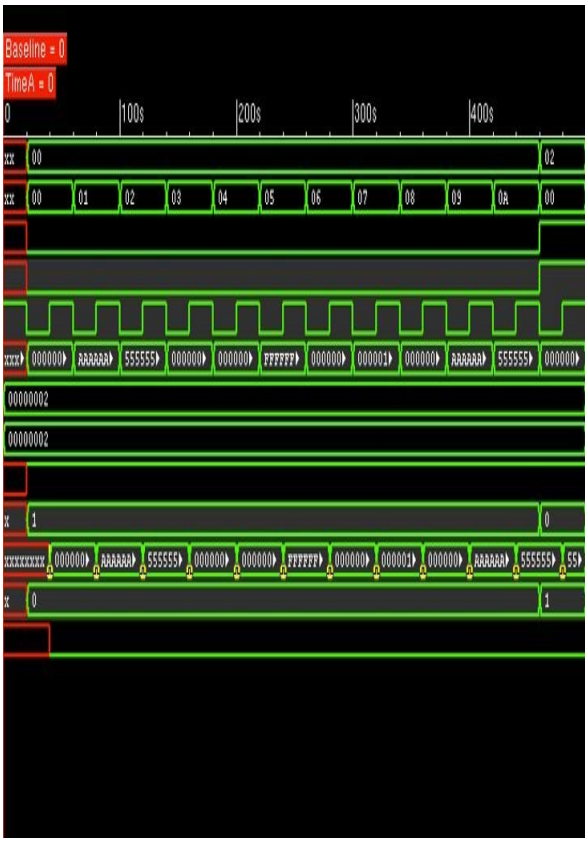
Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CSeA.v", 593: c3(.s(s[11:8]), .cout(c[3]), .
          a(a[11:8]), .b(b[11:8]), .cin(c[2]))

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CSeA.v", 591: c1(.s(s[3:0]), .cout(c[1]), .
          a(a[3:0]), .b(b[3:0]), .cin(cin))

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CSeA.v", 592: c2(.s(s[7:4]), .cout(c[2]), .
          a(a[7:4]), .b(b[7:4]), .cin(c[1]))

Warning!  Too few module port connections                    [Verilog-TFNPC]
          "cpu_CSeA.v", 593: c3(.s(s[11:8]), .cout(c[3]), .
          a(a[11:8]), .b(b[11:8]), .cin(c[2]))
Highest level modules:
stimulus

L30 "tb_test.v": $finish at simulation time 501
7 warnings
0 simulation events (use +profile or +listcounts option to count) + 17694 accele
rated events
CPU time: 0.0 secs to compile + 0.1 secs to link + 0.4 secs in simulation
```



8) Fill out the following performance comparison table after synthesis and analyze the results (explain the reasons of your comparison results)

		CLA(nS)	CRA(nS)	CSA(nS)	CSeA(nS)
Path Delay for Each Operation (Post-Synthesis Gate-Level Delay)	5555_5555 + 5	2.10	2.11	2.19	1.2
	AAAA_AAAA + 5555_5555	2.85	2.90	2.36	1.65
	0000_00C8 + 0000_012C	2.45	2.76	2.13	1.70
	5 + 0000_000A	2.69	2.59	2.18	1.69
	FFFF_FFFF - 0000_0001	2.68	2.4	2.24	2.07
	FFFF_FFFF + 0000_0001	2.55	2.32	2.28	1.85
	5555_5555 - 5	2.13	2.35	1.89	1.64
	AAAA_AAAB + 5555_5555	2.42	2.39	1.8	1.65

- As observed from above that more number of bits to be operated more delay will be there in path.
- CSeA take minimum path delay as it has less data to handle.
- CLA always takes less time to perform operation.

- CASE STUDY 2

1) Generate a new test bech file (tb_test_comp.v) for the following instruction set

- See the attached file, “tb_test_comp.v”

2) Provide the display screenshot or the text output of the RTL simulation and the screenshot from simvision with the test bench (tb_test_comp.v)

- See the attached file, “cpu_comp.v” which is modified for its right purpose.

```
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Compiling source file "tb_test_comp.v"
Compiling source file "cpu_comp.v"

Warning!  Too few module port connections                          [Verilog-TFNPC]
          "cpu_comp.v", 647: CLA0(.s(s[15:0]), .a(a[15:0])
          , .b(b[15:0]), .c0(c0), .c16(c16), .p_16(p[0]), .
          g_16(g[0]))

Warning!  Too few module port connections                          [Verilog-TFNPC]
          "cpu_comp.v", 626: CLA0(.s(s[3:0]), .a(a[3:0]), .
          b(b[3:0]), .c0(c0), .c4(c4), .g_4(g[0]), .p_4(p[
          0]))

Warning!  Too few module port connections                          [Verilog-TFNPC]
          "cpu_comp.v", 627: CLA1(.s(s[7:4]), .a(a[7:4]), .
          b(b[7:4]), .c0(c4), .c4(c8), .g_4(g[1]), .p_4(p[
          1]))

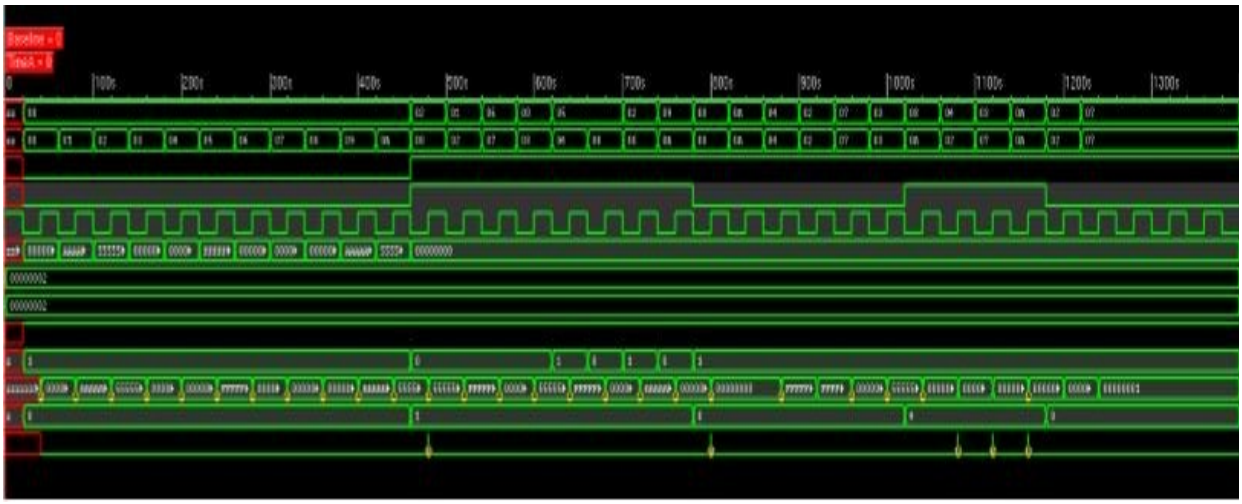
Warning!  Too few module port connections                          [Verilog-TFNPC]
          "cpu_comp.v", 628: CLA2(.s(s[11:8]), .a(a[11:8])
          , .b(b[11:8]), .c0(c8), .c4(c12), .g_4(g[2]), .
          p_4(p[2]))

Warning!  Too few module port connections                          [Verilog-TFNPC]
          "cpu_comp.v", 626: CLA0(.s(s[3:0]), .a(a[3:0]), .
          b(b[3:0]), .c0(c0), .c4(c4), .g_4(g[0]), .p_4(p[
          0]))

Warning!  Too few module port connections                          [Verilog-TFNPC]
          "cpu_comp.v", 627: CLA1(.s(s[7:4]), .a(a[7:4]), .
          b(b[7:4]), .c0(c4), .c4(c8), .g_4(g[1]), .p_4(p[
          1]))

Warning!  Too few module port connections                          [Verilog-TFNPC]
          "cpu_comp.v", 628: CLA2(.s(s[11:8]), .a(a[11:8])
          , .b(b[11:8]), .c0(c8), .c4(c12), .g_4(g[2]), .
          p_4(p[2]))
Highest level modules:
stimulus

Please check Select Lines!
L31 "tb_test_comp.v": $finish at simulation time 1401
7 warnings
0 simulation events (use +profile or +listcounts option to count) + 131981 accelerated events
CPU time: 0.0 secs to compile + 0.1 secs to link + 0.7 secs in simulation
```



3) Synthesize the design and summarize cell.rep and timing.rep

```
  Updating timing information
Information: Updating design information... (UID-85)

  Beginning Mapping Optimizations  (Medium effort)  (Incremental)
  ---------------------------------

  Beginning Incremental Implementation Selection
  ----------------------------------------------

  Beginning Delay Optimization Phase
  ----------------------------------

   ELAPSED              WORST NEG TOTAL NEG  DESIGN
    TIME       AREA       SLACK     SLACK   RULE COST           ENDPOINT
  --------- --------- --------- --------- --------- --------------------------
    0:00:01   49385.8      0.00       0.0       3.0
    0:00:01   49385.8      0.00       0.0       3.0
    0:00:02   49385.8      0.00       0.0       3.0


  Beginning Design Rule Fixing  (max_capacitance)
  ------------------------------

   ELAPSED              WORST NEG TOTAL NEG  DESIGN
    TIME       AREA       SLACK     SLACK   RULE COST           ENDPOINT
  --------- --------- --------- --------- --------- --------------------------
    0:00:02   49385.8      0.00       0.0       3.0
Loading db file '/apps/FreePDK45/osu_soc/lib/files/gscl45nm.db'

  Optimization Complete
  ---------------------
Warning: Design 'cpu' contains 1 high-fanout nets. A fanout number of 1000 will be used for delay calcu
lations involving these nets. (TIM-134)
     Net 'clk': 1625 load(s), 1 driver(s)
1
check_design
1
#report_constraint -all_violators
set filename [format "%s%s"  $my_toplevel ".vh"]
cpu.vh
write -f verilog -output $filename
Writing verilog file '/home/ykim/ece429/project/CASE2/cpu.vh'.
1
set filename [format "%s%s"  $my_toplevel ".sdc"]
cpu.sdc
write_sdc $filename
1
#set filename [format "%s%s"  $my_toplevel ".db"]
#write -f db -hier -output $filename -xg_force_db
redirect timing.rep { report_timing }
redirect cell.rep { report_cell }
redirect power.rep { report_power }
quit

Thank you...
Elapsed Time = 1:32.26, CPU Time = 84.779
```

cell.rep

```
mmOpn/ops/m0/qout_reg      DFFPOSX1        gscl45nm          7.978100   n
mmOpn/ops/m1/qout_reg      DFFPOSX1        gscl45nm          7.978100   n
mmOpn/outs/m0/qout_reg     DFFPOSX1        gscl45nm          7.978100   n
mmOpn/outs/m1/qout_reg     DFFPOSX1        gscl45nm          7.978100   n
mmOpn/outs/m2/qout_reg     DFFPOSX1        gscl45nm          7.978100   n
o/tr/t0/b1                 TBUFX2          gscl45nm          3.754400   n
o/tr/t1/b1                 TBUFX2          gscl45nm          3.754400   n
o/tr/t2/b1                 TBUFX2          gscl45nm          3.754400   n
o/tr/t3/b1                 TBUFX2          gscl45nm          3.754400   n
o/tr/t4/b1                 TBUFX2          gscl45nm          3.754400   n
o/tr/t5/b1                 TBUFX2          gscl45nm          3.754400   n
o/tr/t6/b1                 TBUFX2          gscl45nm          3.754400   n
o/tr/t7/b1                 TBUFX2          gscl45nm          3.754400   n
o/tr/t8/b1                 TBUFX2          gscl45nm          3.754400   n
o/tr/t9/b1                 TBUFX2          gscl45nm          3.754400   n
o/tr/t10/b1                TBUFX2          gscl45nm          3.754400   n
o/tr/t11/b1                TBUFX2          gscl45nm          3.754400   n
o/tr/t12/b1                TBUFX2          gscl45nm          3.754400   n
o/tr/t13/b1                TBUFX2          gscl45nm          3.754400   n
o/tr/t14/b1                TBUFX2          gscl45nm          3.754400   n
o/tr/t15/b1                TBUFX2          gscl45nm          3.754400   n
o/tr/t16/b1                TBUFX2          gscl45nm          3.754400   n
o/tr/t17/b1                TBUFX2          gscl45nm          3.754400   n
o/tr/t18/b1                TBUFX2          gscl45nm          3.754400   n
o/tr/t19/b1                TBUFX2          gscl45nm          3.754400   n
o/tr/t20/b1                TBUFX2          gscl45nm          3.754400   n
o/tr/t21/b1                TBUFX2          gscl45nm          3.754400   n
o/tr/t22/b1                TBUFX2          gscl45nm          3.754400   n
o/tr/t23/b1                TBUFX2          gscl45nm          3.754400   n
o/tr/t24/b1                TBUFX2          gscl45nm          3.754400   n
o/tr/t25/b1                TBUFX2          gscl45nm          3.754400   n
o/tr/t26/b1                TBUFX2          gscl45nm          3.754400   n
o/tr/t27/b1                TBUFX2          gscl45nm          3.754400   n
o/tr/t28/b1                TBUFX2          gscl45nm          3.754400   n
o/tr/t29/b1                TBUFX2          gscl45nm          3.754400   n
o/tr/t30/b1                TBUFX2          gscl45nm          3.754400   n
o/tr/t31/b1                TBUFX2          gscl45nm          3.754400   n
wb/bd/me0/qout_reg         DFFPOSX1        gscl45nm          7.978100   n
wb/bd/me1/qout_reg         DFFPOSX1        gscl45nm          7.978100   n
wb/bd/me2/qout_reg         DFFPOSX1        gscl45nm          7.978100   n
wb/bd/me3/qout_reg         DFFPOSX1        gscl45nm          7.978100   n
wb/bd/me4/qout_reg         DFFPOSX1        gscl45nm          7.978100   n
------------------------------------------------------------------------------
Total 14678 cells                                          49385.845973
1
```

timing.rep

```
a/l3/f1615/U5/Y (XNOR2X1)                    0.06          4.67  r
a/l3/f1615/U2/Y (XOR2X1)                     0.07          4.74  r
a/l3/f1714/U5/Y (XNOR2X1)                    0.06          4.80  r
a/l3/f1714/U2/Y (XOR2X1)                     0.07          4.87  r
a/l3/f1813/U5/Y (XNOR2X1)                    0.06          4.93  r
a/l3/f1813/U2/Y (XOR2X1)                     0.07          5.01  r
a/l3/f1912/U5/Y (XNOR2X1)                    0.06          5.07  r
a/l3/f1912/U2/Y (XOR2X1)                     0.07          5.14  r
a/l3/f2011/U5/Y (XNOR2X1)                    0.06          5.20  r
a/l3/f2011/U2/Y (XOR2X1)                     0.07          5.27  r
a/l3/f2110/U5/Y (XNOR2X1)                    0.06          5.33  r
a/l3/f2110/U2/Y (XOR2X1)                     0.06          5.40  r
U1349/Y (XOR2X1)                             0.05          5.45  r
U1348/Y (XOR2X1)                             0.07          5.52  r
a/l3/f2308/U5/Y (XNOR2X1)                    0.06          5.58  r
a/l3/f2308/U2/Y (XOR2X1)                     0.07          5.65  r
a/l3/f247/U5/Y (XNOR2X1)                     0.06          5.71  r
a/l3/f247/U2/Y (XOR2X1)                      0.07          5.78  r
a/l3/f256/U5/Y (XNOR2X1)                     0.06          5.85  r
a/l3/f256/U2/Y (XOR2X1)                      0.07          5.92  r
a/l3/f265/U5/Y (XNOR2X1)                     0.06          5.98  r
a/l3/f265/U2/Y (XOR2X1)                      0.07          6.05  r
a/l3/f274/U5/Y (XNOR2X1)                     0.06          6.11  r
a/l3/f274/U2/Y (XOR2X1)                      0.07          6.18  r
a/l3/f283/U5/Y (XNOR2X1)                     0.06          6.25  r
a/l3/f283/U2/Y (XOR2X1)                      0.07          6.32  r
a/l3/f292/U5/Y (XNOR2X1)                     0.06          6.38  r
a/l3/f292/U2/Y (XOR2X1)                      0.05          6.43  f
U1784/Y (AND2X1)                             0.03          6.46  f
a/l3/rc31/qout_reg/D (DFFPOSX1)              0.00          6.46  f
data arrival time                                          6.46

clock clk (rise edge)                       33.00         33.00
clock network delay (ideal)                  0.00         33.00
a/l3/rc31/qout_reg/CLK (DFFPOSX1)            0.00         33.00  r
library setup time                          -0.06         32.94
data required time                                        32.94
-----------------------------------------------------------------
data required time                                        32.94
data arrival time                                         -6.46
-----------------------------------------------------------------
slack (MET)                                               26.48
```

4) Provide the display screenshot or the text output of the post-synthesis simulation and the screenshot from simvision

```
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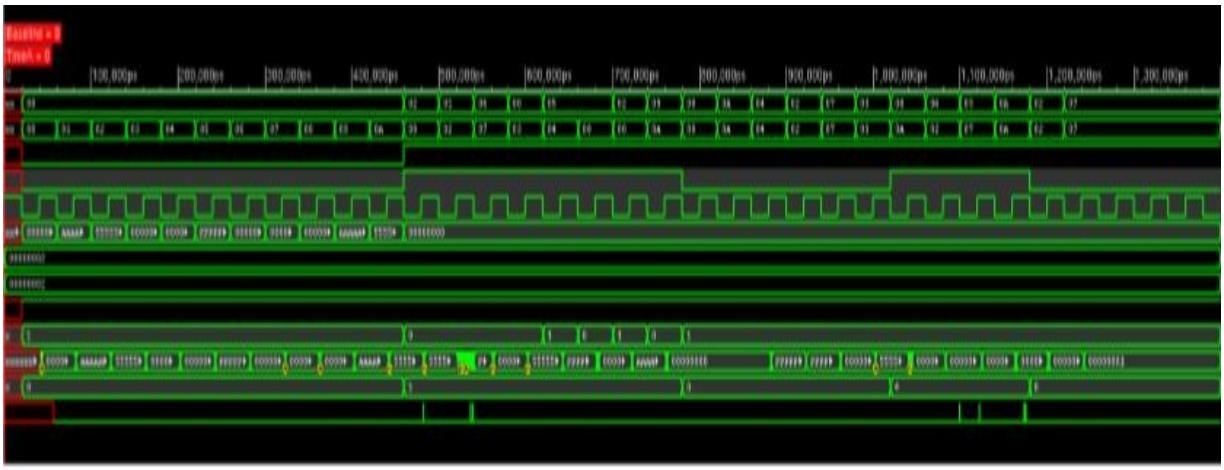
Compiling source file "gscl45nm.v"
Compiling source file "tb_test_comp.v"
Compiling source file "cpu.vh"
Highest level modules:
BUFX4
CLKBUF1
CLKBUF2
CLKBUF3
DFFNEGX1
DFFSR
FAX1
HAX1
INVX2
INVX4
INVX8
MUX2X1
OAI22X1
OR2X2
TBUFX1
stimulus

L31 "tb_test_comp.v": $finish at simulation time 148100
0 simulation events (use +profile or +listcounts option to count) + 799830 accel
erated events + 953312 timing check events
CPU time: 0.1 secs to compile + 0.1 secs to link + 0.4 secs in simulation
```



5) Summarize timing.rep.5.final. What is the maximum clock frequency this circuit can run

| a/l3/rc31/qout_reg/D | ^ | a/l3/c30[0] | DFFPOSX1 | 0.000 | 10.522 | 30.076 |
mOpd/bb/me2/qout_reg/Q | v | B[2] | DFFPOSX1 | 0.290 | 0.682 | 20.237 |

$$\frac{1}{clock_{\min}} = f_{\max} \qquad \frac{1}{D-Q} = f_{\max} \qquad \frac{1}{30.076-20.237} = 0.101636Hz$$

6) Provide the display screenshot or the text output of the post-P&R simulation and the screenshot from simvision

```
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Compiling source file "gscl45nm.v"
Compiling source file "tb_test_comp.v"
Compiling source file "final.v"
Highest level modules:
BUFX4
CLKBUF1
CLKBUF2
CLKBUF3
DFFNEGX1
DFFSR
FAX1
HAX1
INVX2
MUX2X1
OAI22X1
OR2X2
TBUFX1
stimulus

L31 "tb_test_comp.v": $finish at simulation time 140100
0 simulation events (use +profile or +listcounts option to count) + 810904 accel
erated events + 953312 timing check events
CPU time: 0.1 secs to compile + 0.1 secs to link + 0.4 secs in simulation
```