MUNEESHA KATHULA

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Summary:

Graduate student in Computer Engineering with strong foundation in computer architecture, digital system design, and ASIC verification. Proficient in C/C++, Python, Verilog/SystemVerilog, and experienced with front-end verification, performance modeling, and RTL-level hardware design. Skilled in working with pre- and post-silicon validation environments. Demonstrated ability to analyze and optimize hardware systems through academic research and real-world projects.

Education:

- **Master of Science., Computer Engineering** **August 2023 - Present**
  Illinois Institute of Technology, Chicago, IL **GPA: 3.70**
  Related Courses: Introduction to VLSI Design with Lab, High performance VLSI/IC Circuits, Hardware Acceleration Through Machine Learning, Analysis of Analog ICs, Object Oriented Programming Language and Machine Learning
- **Bachelor of Technology., Electronics and Communication Engineering** **June 2019 - May 2023**
  Sri Venkateswara College of Engineering, Tirupati, India **CGPA: 8.5**
  Related Courses: Digital Electronics and Logic Design, Computer Architecture and Organization, Electronic Devices and Circuits, Digital Design Through VHDL, Analog Circuits.

Technical Skills:

- **Programming Scripts:** Verilog, System Verilog, UVM, C, C++, Python, Perl, OOPS, VHDL, Linux Shell Scripting, TCL
- **EDA Tools:** Cadence Virtuoso Schematic Editor, Cadence Virtuoso Layout Suite, HSPICE Circuit Simulator
- **Application Tools:** Xilinx Vivado Suite (ISE Simulator), MATLAB, VS Code, Model Sim Altera, Git, Altium, KiCad
- **Software:** Windows, Linux, Virtual Box, Ubuntu, MS Office Suite, Excel, PowerPoint
- **Domains:** ASIC Design & Verification, Circuit Board Layout, Signal Integrity, Hardware Automation, Validation, RTL Coding
- **Professional skills:** Problem Solving, Debugging, Adaptability, Leadership, Time management, Teamwork, Critical Thinking

Work Experience:

Product Engineering Intern, Equibands Inc **September 2024 – Present**

- Lead the development and testing of a tremor detection device, improving accuracy by 15% and aiding in early diagnosis.
- Analyse patient data and fine-tune algorithms in matlab, increasing device sensitivity and reducing false positives by 10%.
- Enhanced lab debugging processes by implementing advanced test log analysis, reducing error identification time by 20%.

VLSI Design Intern, Verzeo **August 2022 - November 2022**

- Executed digital verification tasks using System Verilog and UVM methodology, ensuring 10% higher product reliability.
- Utilized Cadence and Synopsys tools for seamless RTL verification and DFT validation, reducing design cycle time.
- Executed simulations and resolved design issues, improving functionality and reducing design time by 15% while documenting processes for seamless project communication.

Projects:

FPGA-based Hardware Accelerator Design of KNN Machine Learning classifier (2024):

- Implemented FPGA-based hardware accelerators for matrix multiplication using AMD Vitis HLS, applying advanced optimization techniques like loop pipelining, loop unrolling, array partitioning to achieve 10x performance improvement.
- Synthesized a KNN classifier on PYNQ-Z2 FPGA, achieving over 90% accuracy with optimized BRAM, DSP, FF, and LUT utilization.
- Performed hardware synthesis, latency analysis and resource utilization tracking using Vivado Design Suite, generating synthesizable Verilog for FPGA Deployment.

FPGA-based Systolic Array Hardware Accelerator Design of VGG11 (2024)

- Developed an FPGA-based hardware accelerator for the VGG-11 model, achieving a 3x speedup in matrix multiplication performance compared to conventional methods by implementing a systolic array architecture.
- Optimized resource utilization under 100% and reduced latency by 25% through advanced techniques, including fixed-point arithmetic, tiling, and pragma-based optimizations on the PYNQ-Z2 FPGA platform.
- Explored over 10+ design configurations, evaluating the impact of processing element counts and tile sizes, resulting in a 15% improvement in computational efficiency and detailed analysis of design trade-offs.

Design Techniques to accelerate the convolutional layer of DNNs on FPGA (2024):

- Designed and implemented tiled convolution for the first layer of VGG-11, achieving baseline latency of 18.2 million cycles with Mean Squared Error (MSE) less than 5 across 1024 input tiles and 16 kernel groups.
- Optimized convolutional layer by exploring tile sizes and kernel groups, resulting in a latency reduction of over 40% and efficient FPGA resource utilization (BRAM, DSP, FF, LUT usage under 100%).
- Deployed fixed-point optimized convolution HLS IP on PYNQ-Z2 FPGA using Vitis, Vivado, PYNQ framework, demonstrating a 3x speed-up compared to baseline implementation with minimal quantization error.