Project Title: Design a 12-bit Custom RISC-V Microprocessor

ISA Design

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Introduction: Design a 12-bit Custom RISC-V Microprocessor.

Objectives: Our objective was to create a 12-bit ISA (Instruction Set Architecture) which can perform particular problems. Example: Arithmetic operations, branching, etc.

1. ***How many types of instructions?***
    - R-Type
    - I-Type
    - J-Type
2. ***Describe each of the formats***

    R-Type: R instructions are used when all the data values used by the instruction are located in the registers.

    In our case, the total number of bits is 12. We have split these bits into equal sized 4 parts, namely - Opcode, RS, RT, and RD(Write register).

Opcode	RS	RT	RD
3 bits	3 bits	3 bits	3 bits

    I-Type: I instructions consist of an opcode, a source register, a destination register and an immediate value.

Opcode	RS	RT	Immediate
3 bits	3 bits	3 bits	3 bits

J-type: J instruction consists of an opcode and a jump target.

Opcode	Jump Target
3 bits	9 bits

3. How many operands?

- R-type: 3 operands (RS, RT, and RD).
- I-type: 2 operands (RS, and RT).
- J-type: No operands.

4. How many operations?

- 8-operations. Those are
  - R-type(ADD, SUB)
  - I-type(MULi, DIVi, LW, SW, JMP, BEQ)

5. Types of operations?

- Arithmetic(ADD, SUB, MULi, DIVi)
- Memory(LW, SW)
- Branch(BEQ)
- Jump(JMP)