| Type | Mne-monic | Assembly Example | Machine Code | | | | | | | | Operation Summary | Detailed Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | OPR (Upper) | | | | OPA (Lower) | | | | | |
| Read RAM Character | **RDM** | rdm | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | ●PC+1→PCTEMP<br>●(RAM_CH)→ACC<br>●PCTEMP→PC | Reads the RAM main memory character selected by the DCL and SRC instructions and stores it in the ACC. The CY bit remains unchanged. |
| Read RAM Status Character 0 | **RD0** | rd0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | ●PC+1→PCTEMP<br>●(RAM_ST0)→ACC<br>●PCTEMP→PC | Reads RAM status character 0 selected by the DCL and SRC instructions and stores it in the ACC. The CY bit remains unchanged. |
| Read RAM Status Character 1 | **RD1** | rd1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | ●PC+1→PCTEMP<br>●(RAM_ST1)→ACC<br>●PCTEMP→PC | Reads RAM status character 1 selected by the DCL and SRC instructions and stores it in the ACC. The CY bit remains unchanged. |
| Read RAM Status Character 2 | **RD2** | rd2 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | ●PC+1→PCTEMP<br>●(RAM_ST2)→ACC<br>●PCTEMP→PC | Reads RAM status character 2 selected by the DCL and SRC instructions and stores it in the ACC. The CY bit remains unchanged. |
| Read RAM Status Character 3 | **RD3** | rd3 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | ●PC+1→PCTEMP<br>●(RAM_ST3)→ACC<br>●PCTEMP→PC | Reads RAM status character 3 selected by the DCL and SRC instructions and stores it in the ACC. The CY bit remains unchanged. |
| Read ROM Port | **RDR** | rdr | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | ●PC+1→PCTEMP<br>●(ROM_PORT_IN)→ACC<br>●PCTEMP→PC | Reads the ROM input port selected by the SRC instruction and stores it in the ACC. The CY bit remains unchanged.<br><br>Note: The ROM (4001) port is bidirectional. When reading from a port set to output, the signal level depends on the metal options specified when ordering the 4001 chip. |
| Write Accumulator into RAM Character | **WRM** | wrm | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | ●PC+1→PCTEMP<br>●ACC→(RAM_CH)<br>●PCTEMP→PC | Writes the contents of ACC to the RAM main memory character selected by the DCL and SRC instructions. The CY bit remains unchanged. |
| Write Accumulator into RAM Status Character 0 | **WR0** | wr0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | ●PC+1→PCTEMP<br>●ACC→(RAM_ST0)<br>●PCTEMP→PC | Writes the contents of ACC to RAM status character 0 selected by the DCL and SRC instructions. The CY bit remains unchanged. |
| Write Accumulator into RAM Status Character 1 | **WR1** | wr1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | ●PC+1→PCTEMP<br>●ACC→(RAM_ST1)<br>●PCTEMP→PC | Writes the contents of ACC to RAM status character 1 selected by the DCL and SRC instructions. The CY bit remains unchanged. |
| Write Accumulator into RAM Status Character 2 | **WR2** | wr2 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | ●PC+1→PCTEMP<br>●ACC→(RAM_ST2)<br>●PCTEMP→PC | Writes the contents of ACC to RAM status character 2 selected by the DCL and SRC instructions. The CY bit remains unchanged. |
| Write Accumulator into RAM Status Character 3 | **WR3** | wr3 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | ●PC+1→PCTEMP<br>●ACC→(RAM_ST3)<br>●PCTEMP→PC | Writes the contents of ACC to RAM status character 3 selected by the DCL and SRC instructions. The CY bit remains unchanged. |
| Write ROM Port | **WRR** | wrr | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | ●PC+1→PCTEMP<br>●ACC→(ROM_PORT_OUT)<br>●PCTEMP→PC | Writes the contents of ACC to the ROM output port selected by the SRC instruction. The CY bit remains unchanged.<br><br>Note: ROM (4001) ports are bidirectional. Writing to ports configured as input will have no effect. |
| Write Memory Port | **WMP** | wmp | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | ●PC+1→PCTEMP<br>●ACC→(RAM_PORT_OUT)<br>●PCTEMP→PC | Writes the contents of ACC to the RAM output port selected by the DCL and SRC instructions. The CY bit remains unchanged. |
| Add from Memory with Carry | **ADM** | adm | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | ●PC+1→PCTEMP<br>●ACC+(RAM_CH)+CY<br>→ACC,CY<br>●PCTEMP→PC | Reads the RAM main memory character selected by the DCL and SRC instructions, adds it to the ACC with carry. |
| Subtract from Memory with Borrow | **SBM** | sbm | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | ●PC+1→PCTEMP<br>●ACC+$\overline{(RAM\_CH)}+\overline{CY}$<br>→ACC,CY<br>●PCTEMP→PC | Reads the RAM main memory character selected by the DCL and SRC instructions, subtracts it from the ACC with borrow.<br><br>Note: If the CY value before the calculation is 0, subtraction proceeds without borrow. If CY is 1 before the calculation, subtraction is performed with borrow. After the operation: CY = 0 indicates a borrow occurred; CY = 1 indicates no borrow occurred. Be aware that the meaning of the CY bit is inverted after the calculation with respect to borrow. |
| Write Program RAM | **WPM** | wpm | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | Refer to the main text. | Special instructions for reading and writing program memory in systems where program memory is implemented in RAM. |