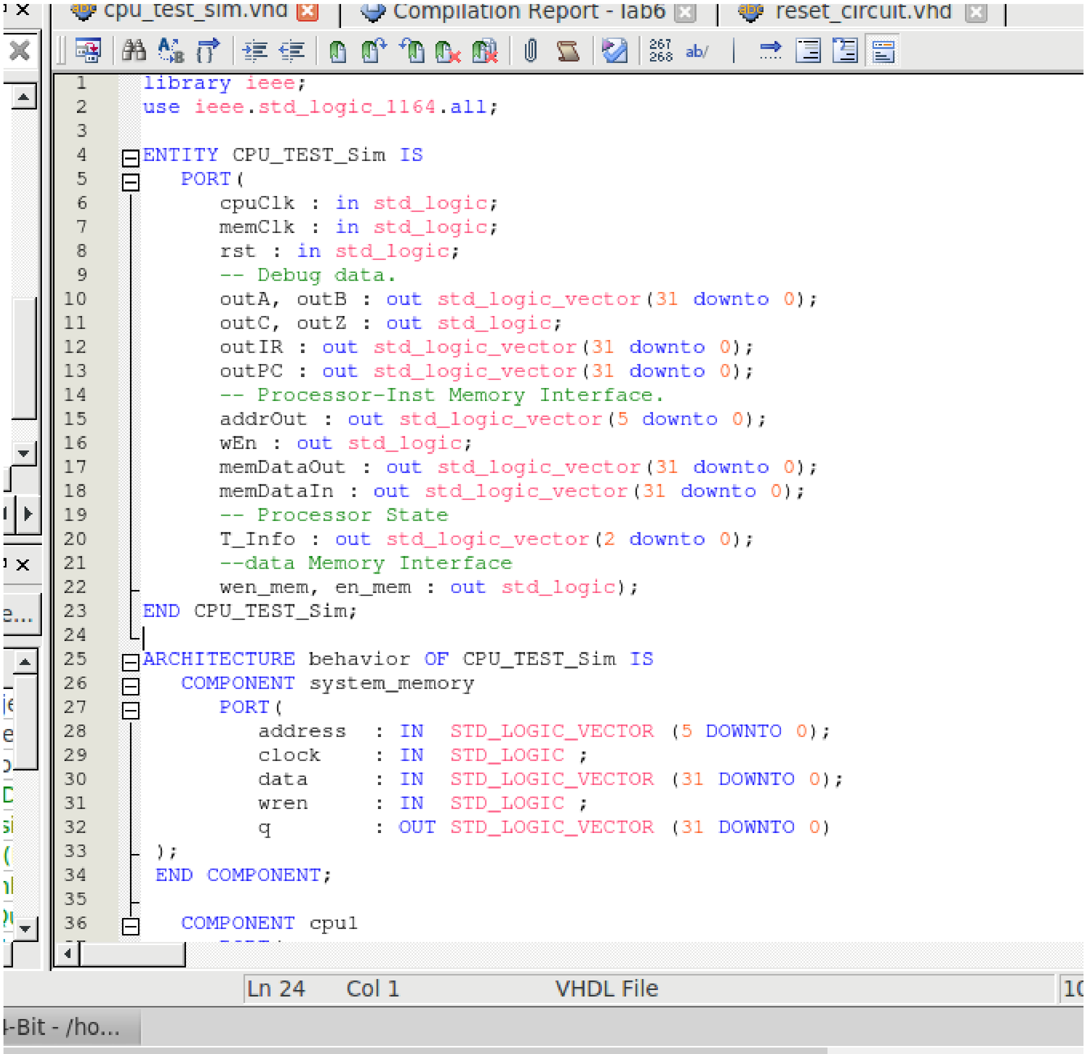
In this lab, we will combine data path and control from the previous labs with the reset circuit and form a complete CPU. We will use the complete CPU to perform the features described in the CPU specifics document.

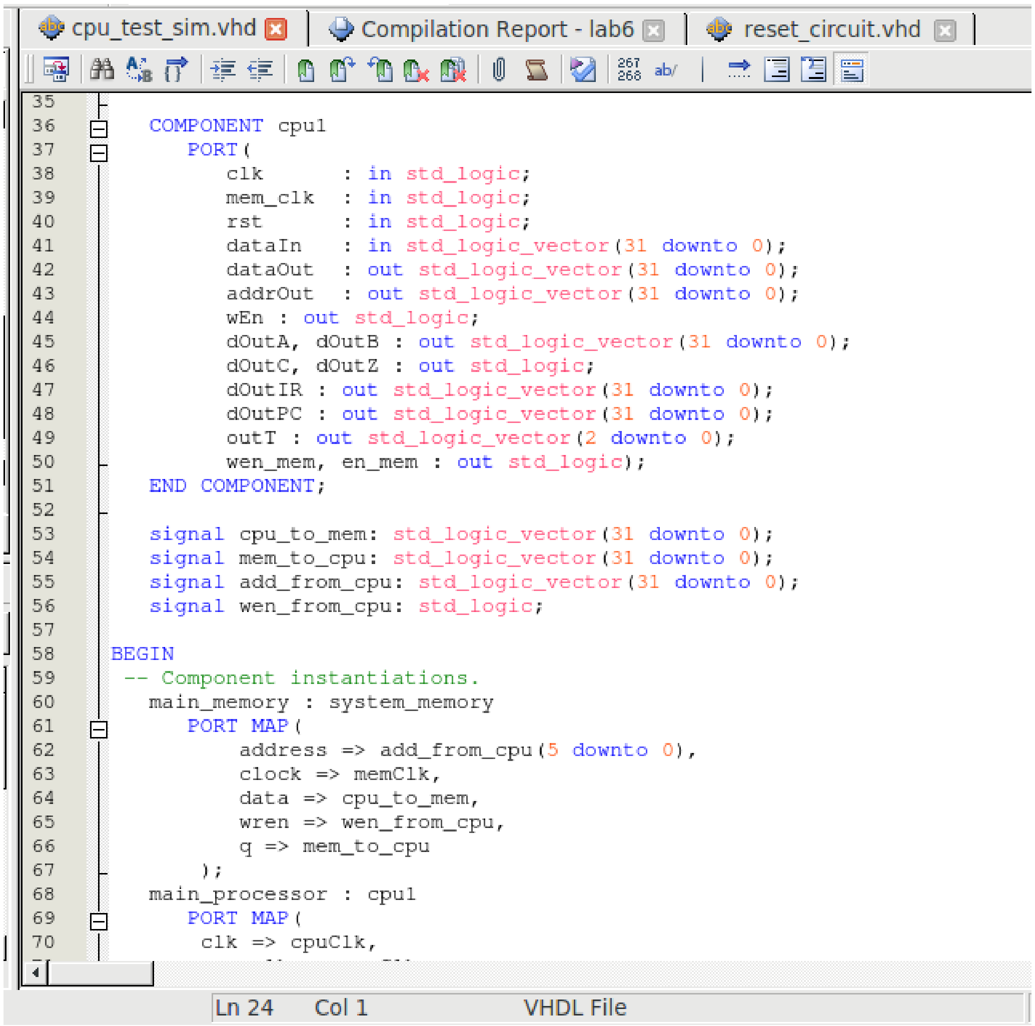


```vhdl
library ieee;
use ieee.std_logic_1164.all;

ENTITY CPU_TEST_Sim IS
   PORT(
      cpuClk : in std_logic;
      memClk : in std_logic;
      rst : in std_logic;
      -- Debug data.
      outA, outB : out std_logic_vector(31 downto 0);
      outC, outZ : out std_logic;
      outIR : out std_logic_vector(31 downto 0);
      outPC : out std_logic_vector(31 downto 0);
      -- Processor-Inst Memory Interface.
      addrOut : out std_logic_vector(5 downto 0);
      wEn : out std_logic;
      memDataOut : out std_logic_vector(31 downto 0);
      memDataIn : out std_logic_vector(31 downto 0);
      -- Processor State
      T_Info : out std_logic_vector(2 downto 0);
      --data Memory Interface
      wen_mem, en_mem : out std_logic);
END CPU_TEST_Sim;

ARCHITECTURE behavior OF CPU_TEST_Sim IS
   COMPONENT system_memory
      PORT(
         address  : IN  STD_LOGIC_VECTOR (5 DOWNTO 0);
         clock    : IN  STD_LOGIC ;
         data     : IN  STD_LOGIC_VECTOR (31 DOWNTO 0);
         wren     : IN  STD_LOGIC ;
         q        : OUT STD_LOGIC_VECTOR (31 DOWNTO 0)
 );
 END COMPONENT;

   COMPONENT cpu1
```

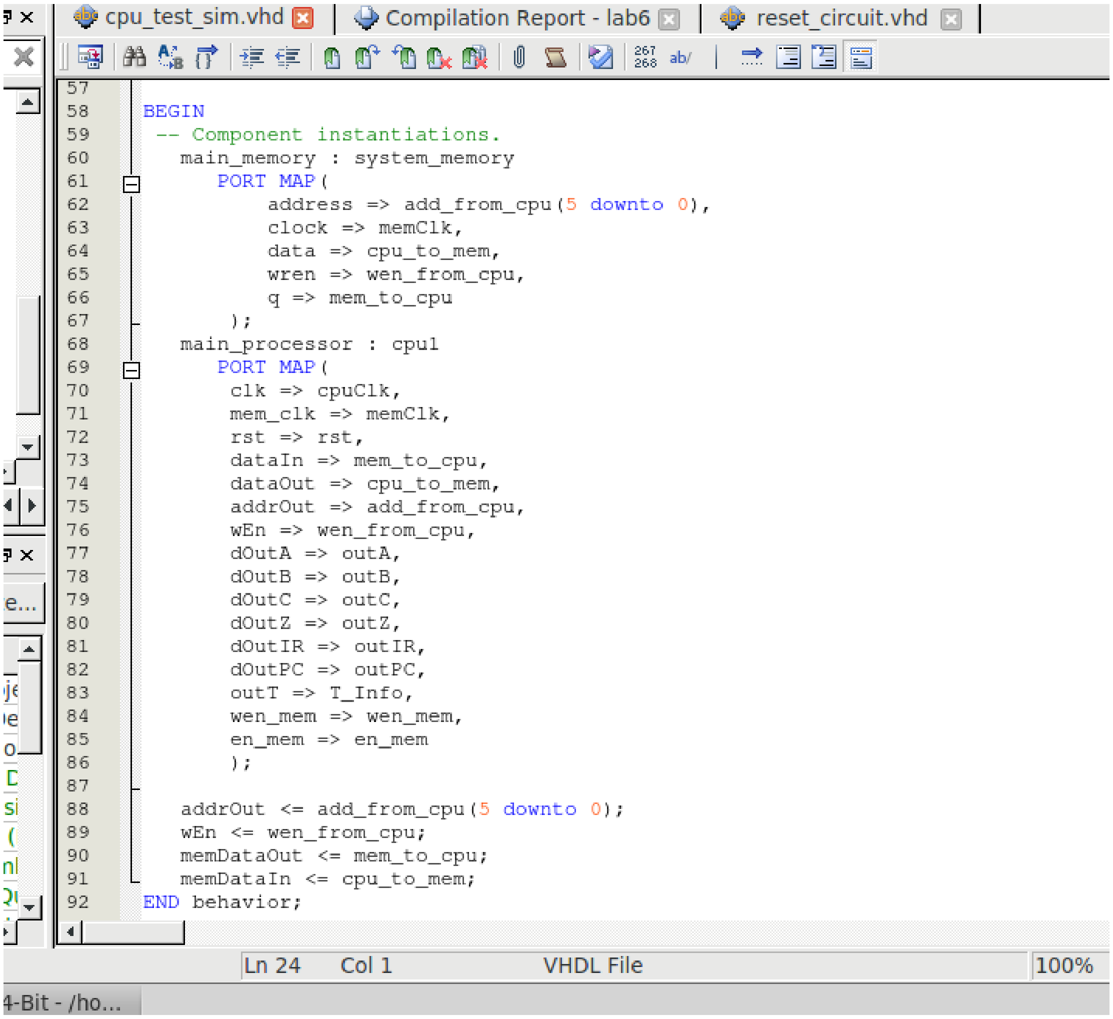


```vhdl

   COMPONENT cpul
      PORT(
         clk      : in std_logic;
         mem_clk  : in std_logic;
         rst      : in std_logic;
         dataIn   : in std_logic_vector(31 downto 0);
         dataOut  : out std_logic_vector(31 downto 0);
         addrOut  : out std_logic_vector(31 downto 0);
         wEn : out std_logic;
         dOutA, dOutB : out std_logic_vector(31 downto 0);
         dOutC, dOutZ : out std_logic;
         dOutIR : out std_logic_vector(31 downto 0);
         dOutPC : out std_logic_vector(31 downto 0);
         outT : out std_logic_vector(2 downto 0);
         wen_mem, en_mem : out std_logic);
   END COMPONENT;

   signal cpu_to_mem: std_logic_vector(31 downto 0);
   signal mem_to_cpu: std_logic_vector(31 downto 0);
   signal add_from_cpu: std_logic_vector(31 downto 0);
   signal wen_from_cpu: std_logic;

BEGIN
 -- Component instantiations.
   main_memory : system_memory
      PORT MAP(
          address => add_from_cpu(5 downto 0),
          clock => memClk,
          data => cpu_to_mem,
          wren => wen_from_cpu,
          q => mem_to_cpu
       );
   main_processor : cpul
      PORT MAP(
       clk => cpuClk,
```

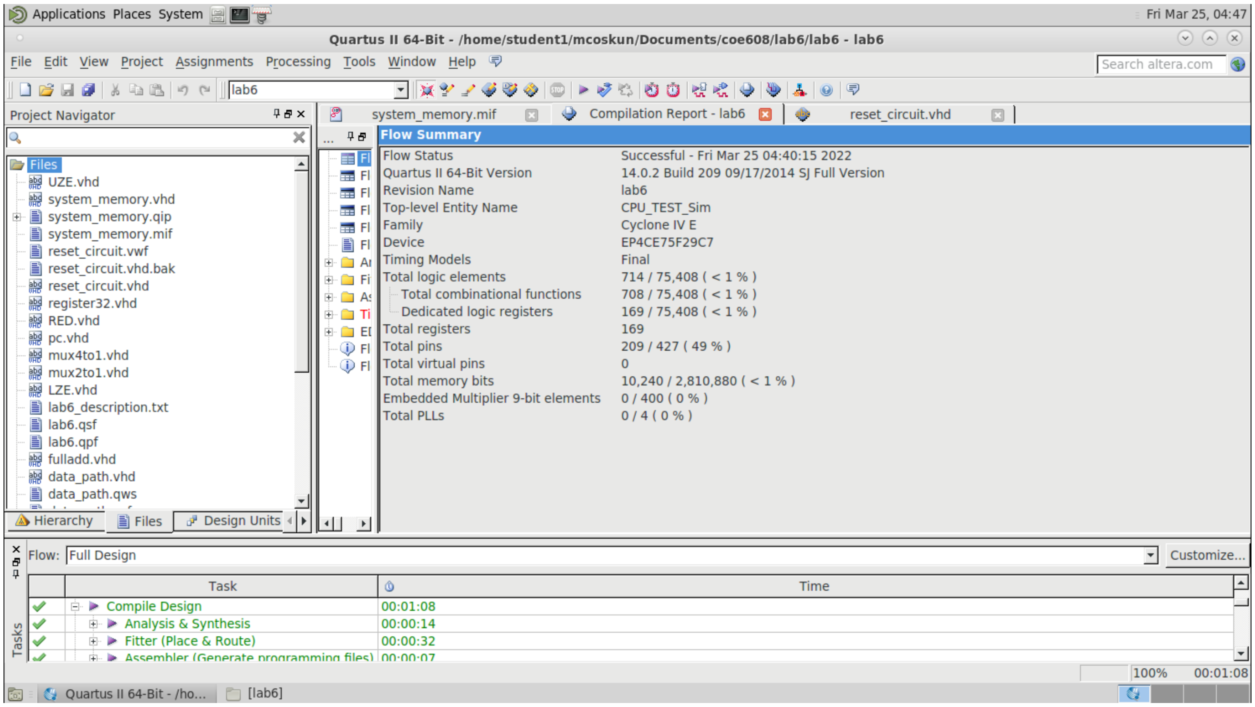


```vhdl

BEGIN
 -- Component instantiations.
   main_memory : system_memory
      PORT MAP(
          address => add_from_cpu(5 downto 0),
          clock => memClk,
          data => cpu_to_mem,
          wren => wen_from_cpu,
          q => mem_to_cpu
       );
   main_processor : cpu1
      PORT MAP(
       clk => cpuClk,
       mem_clk => memClk,
       rst => rst,
       dataIn => mem_to_cpu,
       dataOut => cpu_to_mem,
       addrOut => add_from_cpu,
       wEn => wen_from_cpu,
       dOutA => outA,
       dOutB => outB,
       dOutC => outC,
       dOutZ => outZ,
       dOutIR => outIR,
       dOutPC => outPC,
       outT => T_Info,
       wen_mem => wen_mem,
       en_mem => en_mem
       );

   addrOut <= add_from_cpu(5 downto 0);
   wEn <= wen_from_cpu;
   memDataOut <= mem_to_cpu;
   memDataIn <= cpu_to_mem;
END behavior;
```

CPU_TEST_Sim compiles successfully:

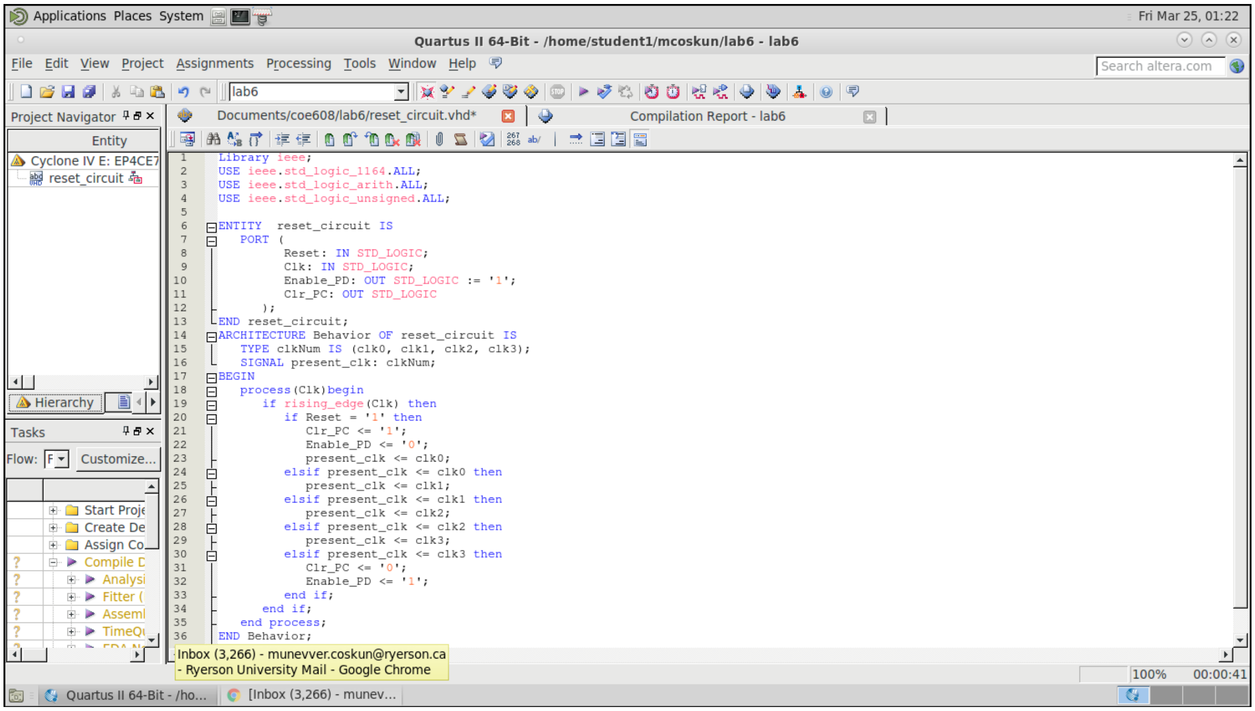


Flow Summary

Flow Status	Successful - Fri Mar 25 04:40:15 2022
Quartus II 64-Bit Version	14.0.2 Build 209 09/17/2014 SJ Full Version
Revision Name	lab6
Top-level Entity Name	CPU_TEST_Sim
Family	Cyclone IV E
Device	EP4CE75F29C7
Timing Models	Final
Total logic elements	714 / 75,408 (< 1 %)
Total combinational functions	708 / 75,408 (< 1 %)
Dedicated logic registers	169 / 75,408 (< 1 %)
Total registers	169
Total pins	209 / 427 (49 %)
Total virtual pins	0
Total memory bits	10,240 / 2,810,880 (< 1 %)
Embedded Multiplier 9-bit elements	0 / 400 (0 %)
Total PLLs	0 / 4 (0 %)

	Task	Time
✓	Compile Design	00:01:08
✓	Analysis & Synthesis	00:00:14
✓	Fitter (Place & Route)	00:00:32
✓	Assembler (Generate programming files)	00:00:07

Reset_circuit VHDL code:



Quartus II 64-Bit - /home/student1/mcoskun/lab6 - lab6

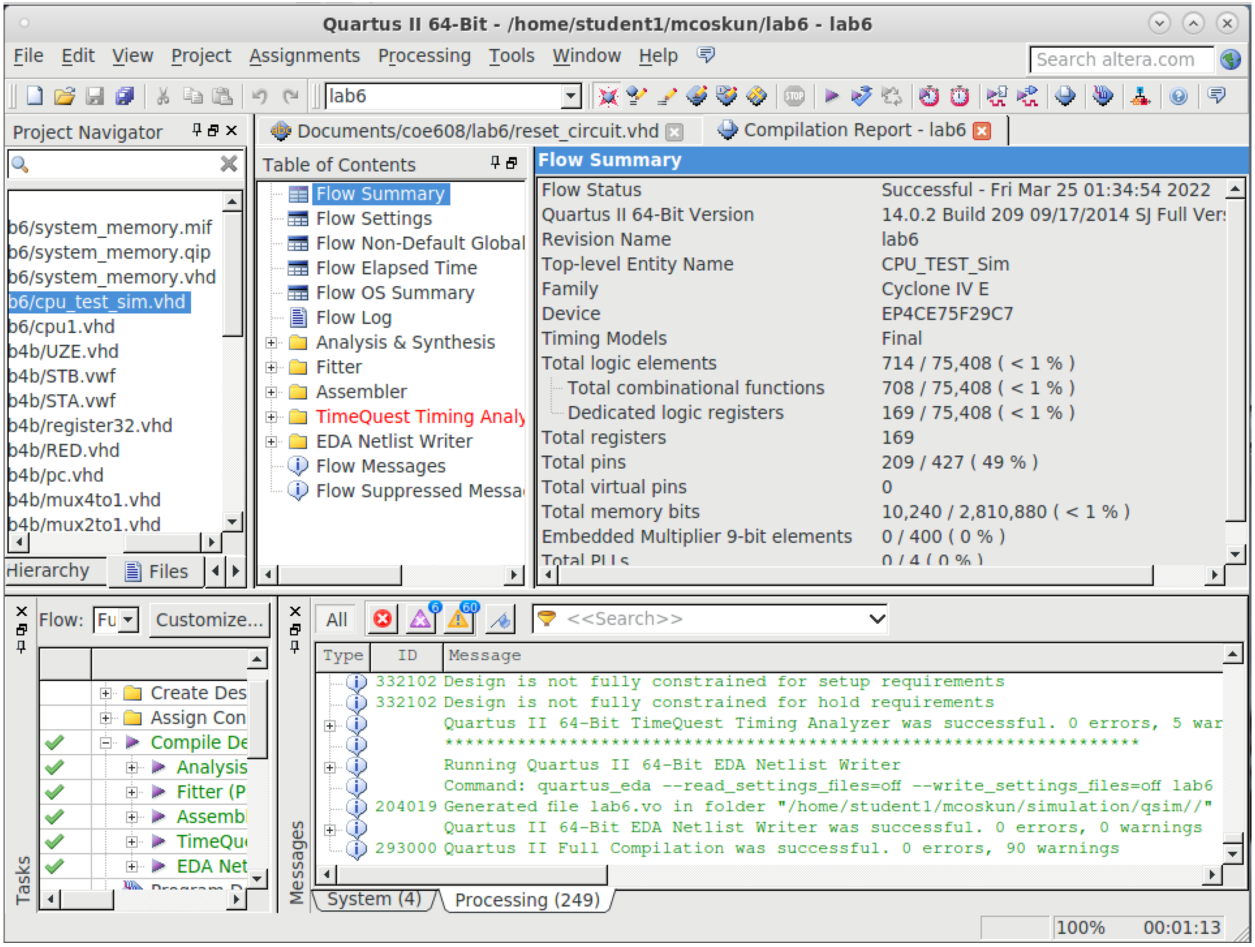
Documents/coe608/lab6/reset_circuit.vhd*

```vhdl
Library ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_arith.ALL;
USE ieee.std_logic_unsigned.ALL;

ENTITY  reset_circuit IS
   PORT (
         Reset: IN STD_LOGIC;
         Clk: IN STD_LOGIC;
         Enable_PD: OUT STD_LOGIC := '1';
         Clr_PC: OUT STD_LOGIC
      );
END reset_circuit;
ARCHITECTURE Behavior OF reset_circuit IS
   TYPE clkNum IS (clk0, clk1, clk2, clk3);
   SIGNAL present_clk: clkNum;
BEGIN
   process(Clk)begin
      if rising_edge(Clk) then
         if Reset = '1' then
            Clr_PC <= '1';
            Enable_PD <= '0';
            present_clk <= clk0;
         elsif present_clk <= clk0 then
            present_clk <= clk1;
         elsif present_clk <= clk1 then
            present_clk <= clk2;
         elsif present_clk <= clk2 then
            present_clk <= clk3;
         elsif present_clk <= clk3 then
            Clr_PC <= '0';
            Enable_PD <= '1';
         end if;
      end if;
   end process;
END Behavior;
```

Applications Places System
Fri Mar 25, 01:22
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
lab6
Project Navigator
Entity
Cyclone IV E: EP4CE7
reset_circuit
Hierarchy
Tasks
Flow: F
Customize...
Start Proje
Create De
Assign Co
Compile D
Analysi
Fitter (
Asseml
TimeQu
Compilation Report - lab6
Inbox (3,266) - munevver.coskun@ryerson.ca - Ryerson University Mail - Google Chrome
100%
00:00:41
Quartus II 64-Bit - /ho...
[Inbox (3,266) - munev...

We compile reset_circuit VHDL code successfully.



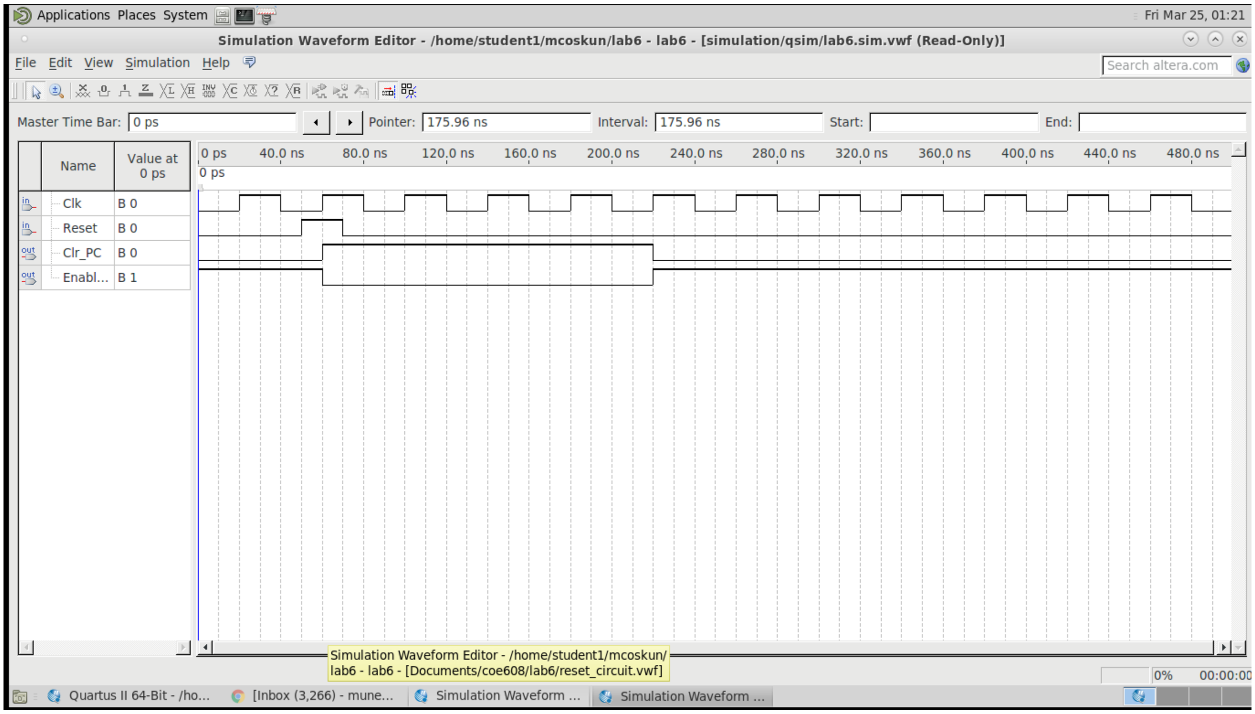
Quartus II 64-Bit - /home/student1/mcoskun/lab6 - lab6

Flow Summary

Flow Status	Successful - Fri Mar 25 01:34:54 2022
Quartus II 64-Bit Version	14.0.2 Build 209 09/17/2014 SJ Full Ver:
Revision Name	lab6
Top-level Entity Name	CPU_TEST_Sim
Family	Cyclone IV E
Device	EP4CE75F29C7
Timing Models	Final
Total logic elements	714 / 75,408 (< 1 %)
Total combinational functions	708 / 75,408 (< 1 %)
Dedicated logic registers	169 / 75,408 (< 1 %)
Total registers	169
Total pins	209 / 427 (49 %)
Total virtual pins	0
Total memory bits	10,240 / 2,810,880 (< 1 %)
Embedded Multiplier 9-bit elements	0 / 400 (0 %)
Total PLLs	0 / 4 (0 %)

```
Type  ID     Message
      332102 Design is not fully constrained for setup requirements
      332102 Design is not fully constrained for hold requirements
             Quartus II 64-Bit TimeQuest Timing Analyzer was successful. 0 errors, 5 war
             ***************************************************************
             Running Quartus II 64-Bit EDA Netlist Writer
             Command: quartus_eda --read_settings_files=off --write_settings_files=off lab6
      204019 Generated file lab6.vo in folder "/home/student1/mcoskun/simulation/qsim//"
             Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings
      293000 Quartus II Full Compilation was successful. 0 errors, 90 warnings
```

Waveform of reset_circuit



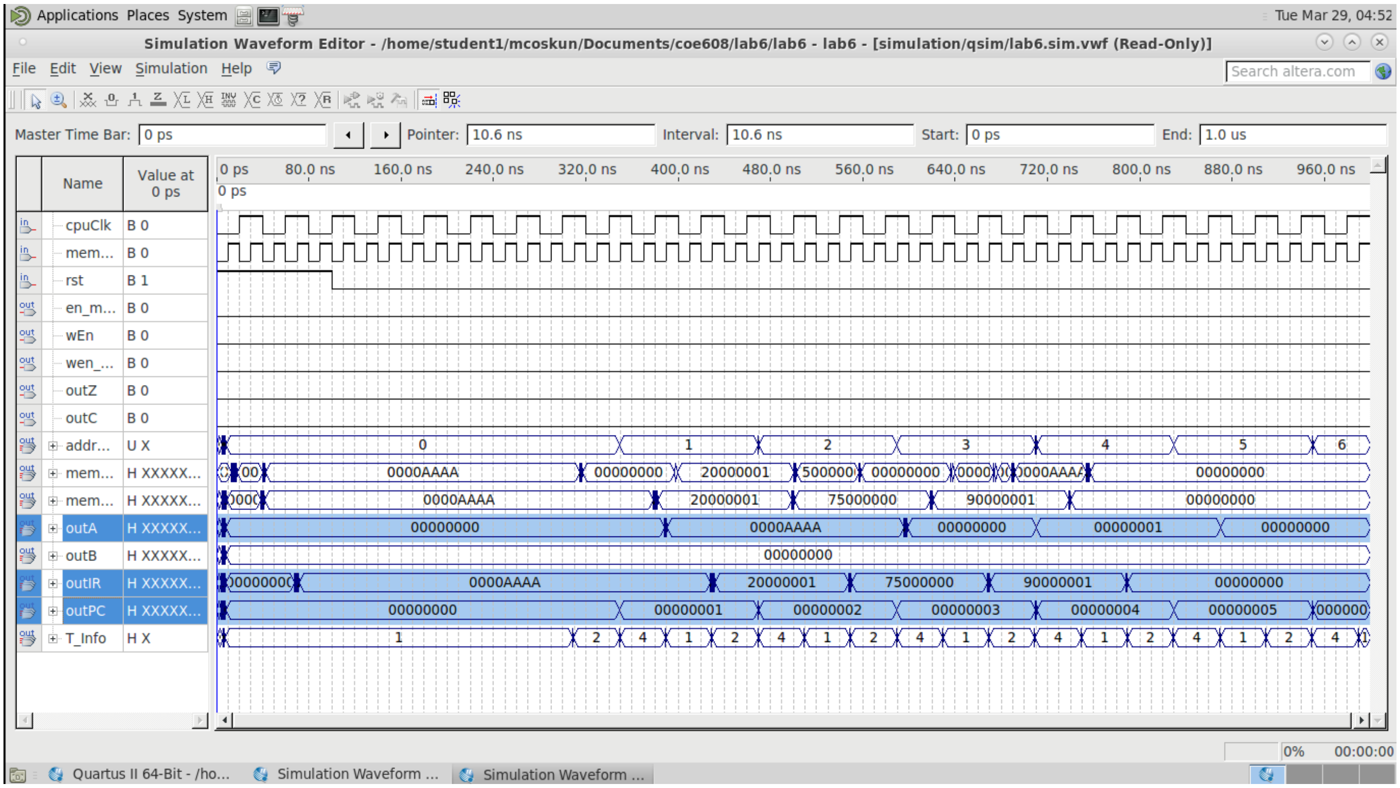
Simulation Waveform Editor - /home/student1/mcoskun/lab6 - lab6 - [simulation/qsim/lab6.sim.vwf (Read-Only)]

Master Time Bar: 0 ps
Pointer: 175.96 ns
Interval: 175.96 ns
Start:
End:

Simulation Waveform Editor - /home/student1/mcoskun/
lab6 - lab6 - [Documents/coe608/lab6/reset_circuit.vwf]

Timing waveforms for the rest of the lab manual as directed:

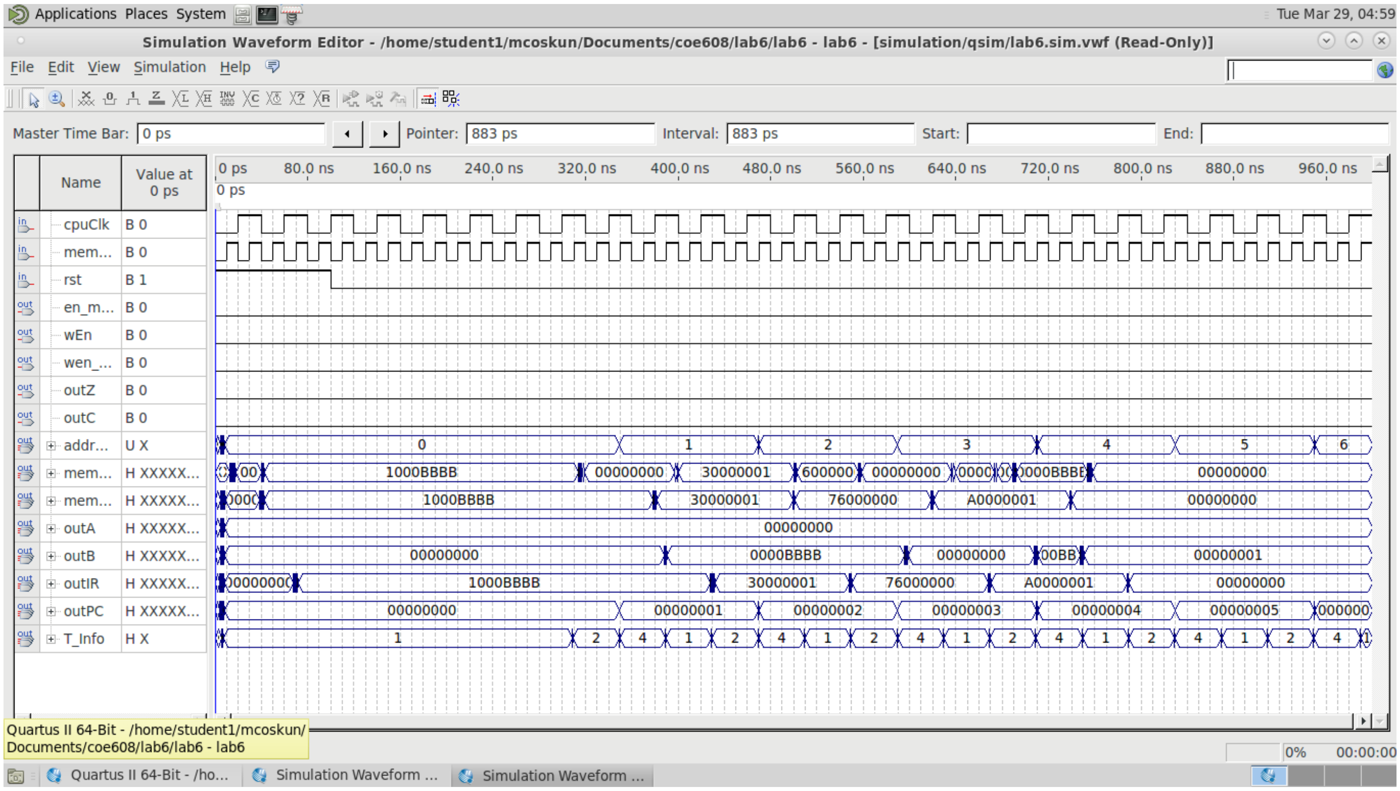
LDAI, STA, CLRA, LDA



Simulation Waveform Editor - /home/student1/mcoskun/Documents/coe608/lab6/lab6 - lab6 - [simulation/qsim/lab6.sim.vwf (Read-Only)]

Master Time Bar: 0 ps
Pointer: 10.6 ns
Interval: 10.6 ns
Start: 0 ps
End: 1.0 us

LDBI, STB, CLRB, LDB



Simulation Waveform Editor - /home/student1/mcoskun/Documents/coe608/lab6/lab6 - lab6 - [simulation/qsim/lab6.sim.vwf (Read-Only)]

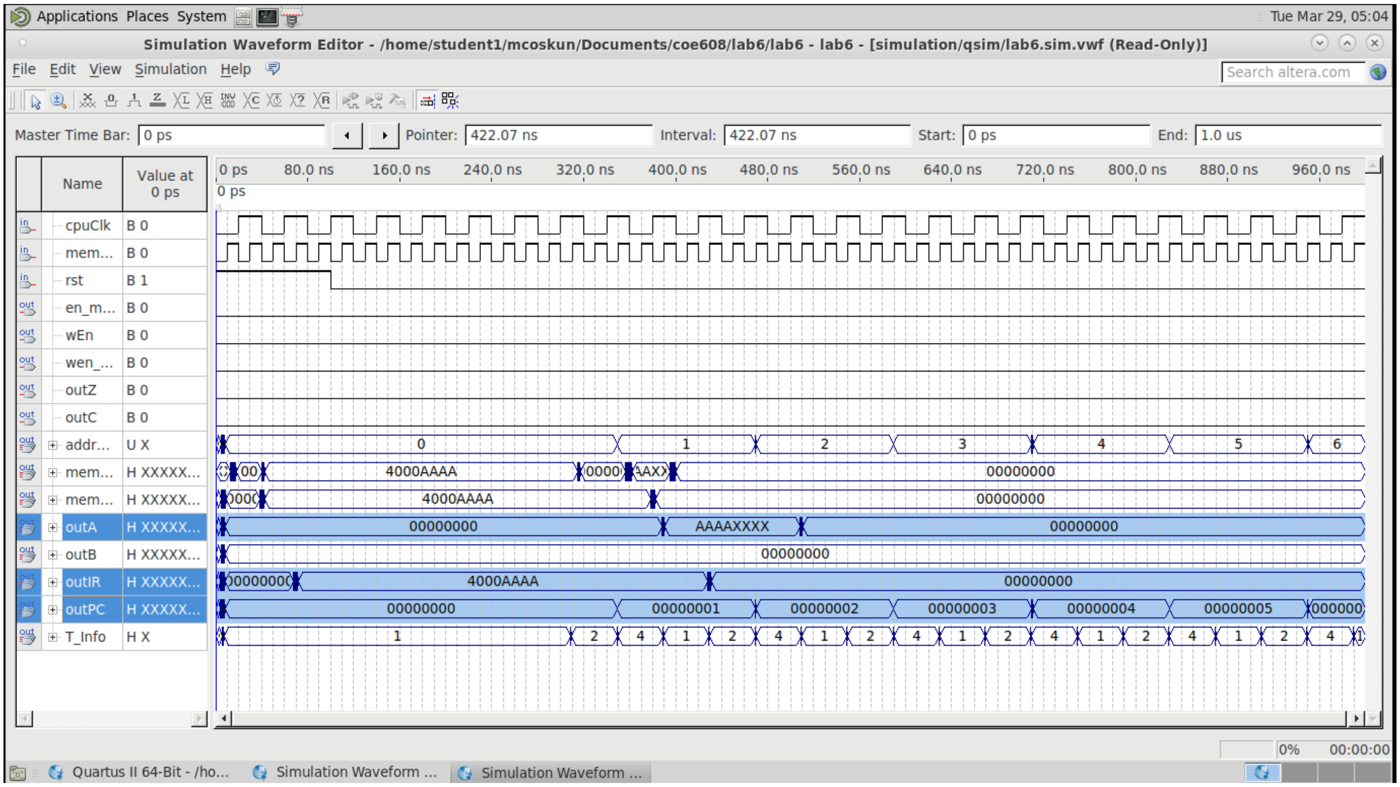
Master Time Bar: 0 ps Pointer: 883 ps Interval: 883 ps Start: End:

Name	Value at 0 ps
cpuClk	B 0
mem...	B 0
rst	B 1
en_m...	B 0
wEn	B 0
wen_...	B 0
outZ	B 0
outC	B 0
addr...	U X
mem...	H XXXXX...
mem...	H XXXXX...
outA	H XXXXX...
outB	H XXXXX...
outIR	H XXXXX...
outPC	H XXXXX...
T_Info	H X

Quartus II 64-Bit - /home/student1/mcoskun/ Documents/coe608/lab6/lab6 - lab6

Applications Places System
Tue Mar 29, 04:59
File Edit View Simulation Help
0 ps 80.0 ns 160.0 ns 240.0 ns 320.0 ns 400.0 ns 480.0 ns 560.0 ns 640.0 ns 720.0 ns 800.0 ns 880.0 ns 960.0 ns
0 ps
0 1 2 3 4 5 6
00 1000BBBB 00000000 30000001 600000 00000000 0000 0000BBBE 00000000
000 1000BBBB 30000001 76000000 A0000001 00000000
00000000
00000000 0000BBBB 00000000 00BB 00000001
0000000 1000BBBB 30000001 76000000 A0000001 00000000
00000000 00000001 00000002 00000003 00000004 00000005 000000
1 2 4 1 2 4 1 2 4 1 2 4 1 2 4 1 2 4
0% 00:00:00
Quartus II 64-Bit - /ho... Simulation Waveform ... Simulation Waveform ...

LUI



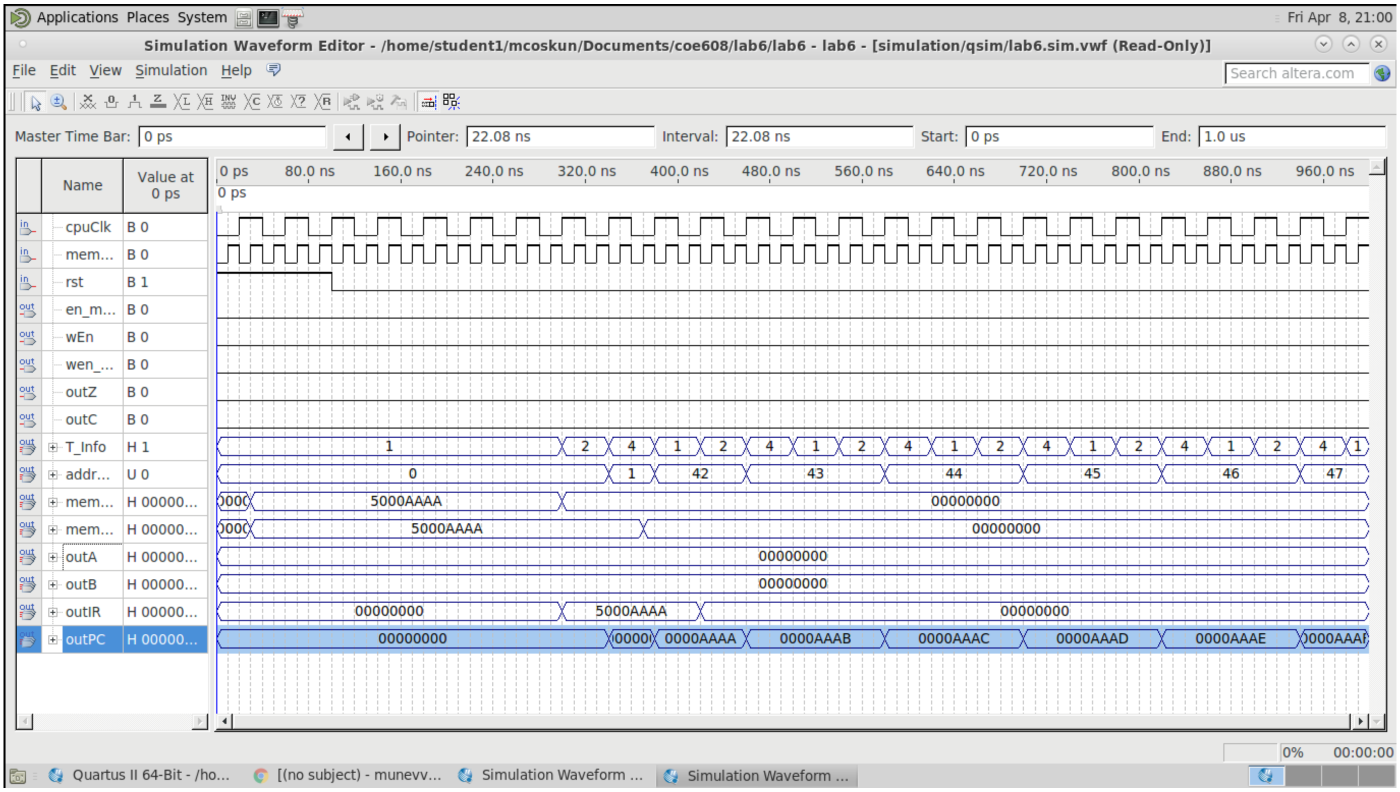
Simulation Waveform Editor - /home/student1/mcoskun/Documents/coe608/lab6/lab6 - lab6 - [simulation/qsim/lab6.sim.vwf (Read-Only)]

Master Time Bar: 0 ps Pointer: 422.07 ns Interval: 422.07 ns Start: 0 ps End: 1.0 us

Name	Value at 0 ps
cpuClk	B 0
mem...	B 0
rst	B 1
en_m...	B 0
wEn	B 0
wen_...	B 0
outZ	B 0
outC	B 0
addr...	U X
mem...	H XXXXX...
mem...	H XXXXX...
outA	H XXXXX...
outB	H XXXXX...
outIR	H XXXXX...
outPC	H XXXXX...
T_Info	H X

Applications Places System
Tue Mar 29, 05:04
File Edit View Simulation Help
Search altera.com
0 ps 80.0 ns 160.0 ns 240.0 ns 320.0 ns 400.0 ns 480.0 ns 560.0 ns 640.0 ns 720.0 ns 800.0 ns 880.0 ns 960.0 ns
0 ps
0 1 2 3 4 5 6
00 4000AAAA 0000 AAX 00000000
000 4000AAAA 00000000
00000000 AAAAXXXX 00000000
00000000
0000000 4000AAAA 00000000
00000000 00000001 00000002 00000003 00000004 00000005 000000
1 2 4 1 2 4 1 2 4 1 2 4 1 2 4 1 2 4
0% 00:00:00
Quartus II 64-Bit - /ho... Simulation Waveform ... Simulation Waveform ...

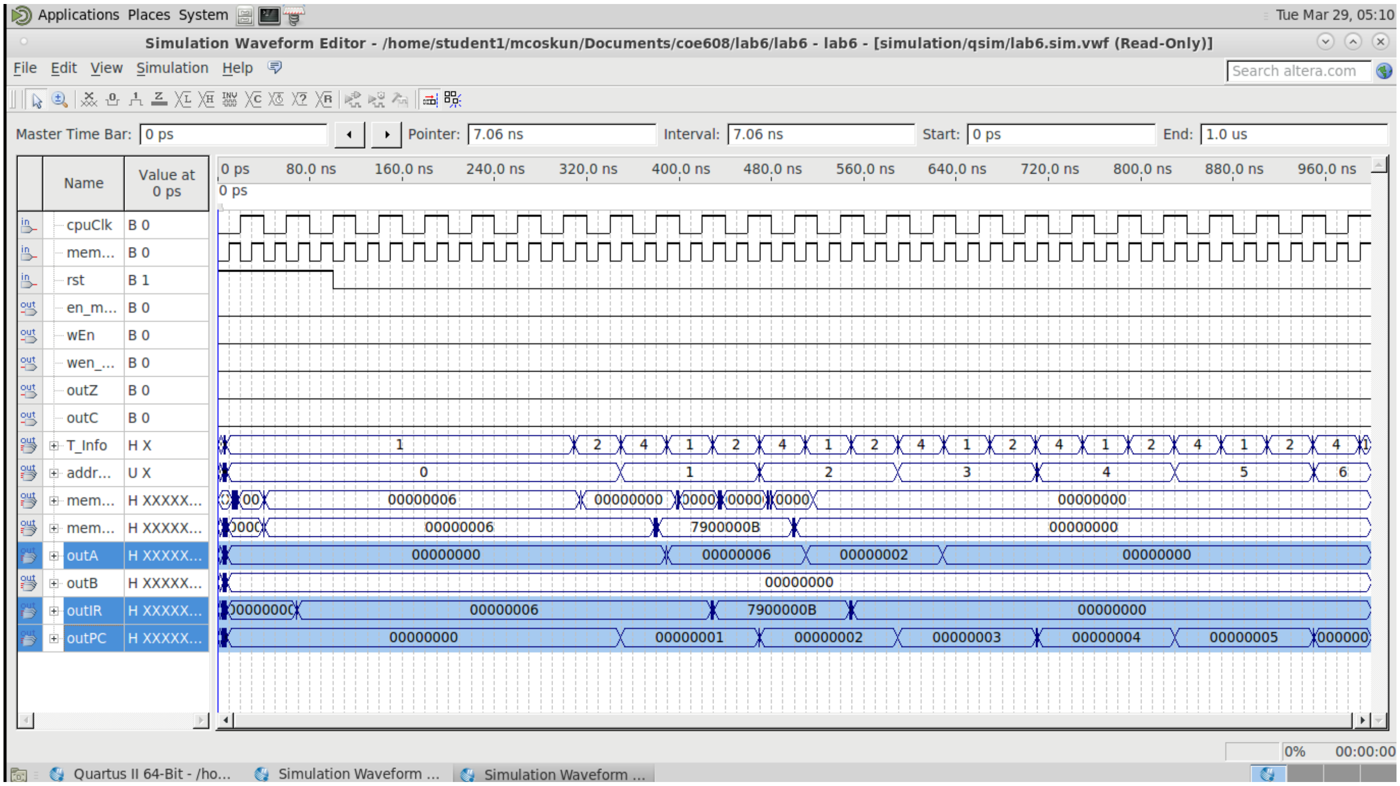
JMP


Applications Places System
Fri Apr 8, 21:00
File Edit View Simulation Help
Search altera.com
0 ps 80.0 ns 160.0 ns 240.0 ns 320.0 ns 400.0 ns 480.0 ns 560.0 ns 640.0 ns 720.0 ns 800.0 ns 880.0 ns 960.0 ns
Name
Value at 0 ps
cpuClk B 0
mem... B 0
rst B 1
en_m... B 0
wEn B 0
wen_... B 0
outZ B 0
outC B 0
T_Info H 1 — 1 2 4 1 2 4 1 2 4 1 2 4 1 2 4 1 2 4 1
addr... U 0 — 0 1 42 43 44 45 46 47
mem... H 00000... — 000 5000AAAA 00000000
mem... H 00000... — 000 5000AAAA 00000000
outA H 00000... — 00000000
outB H 00000... — 00000000
outIR H 00000... — 00000000 5000AAAA 00000000
outPC H 00000... — 00000000 0000 0000AAAA 0000AAAB 0000AAAC 0000AAAD 0000AAAE 000AAAF
0% 00:00:00
Quartus II 64-Bit - /ho...
[(no subject) - munevv...
Simulation Waveform ...
Simulation Waveform ...

Simulation Waveform Editor - /home/student1/mcoskun/Documents/coe608/lab6/lab6 - lab6 - [simulation/qsim/lab6.sim.vwf (Read-Only)]

Master Time Bar: 0 ps Pointer: 22.08 ns Interval: 22.08 ns Start: 0 ps End: 1.0 us

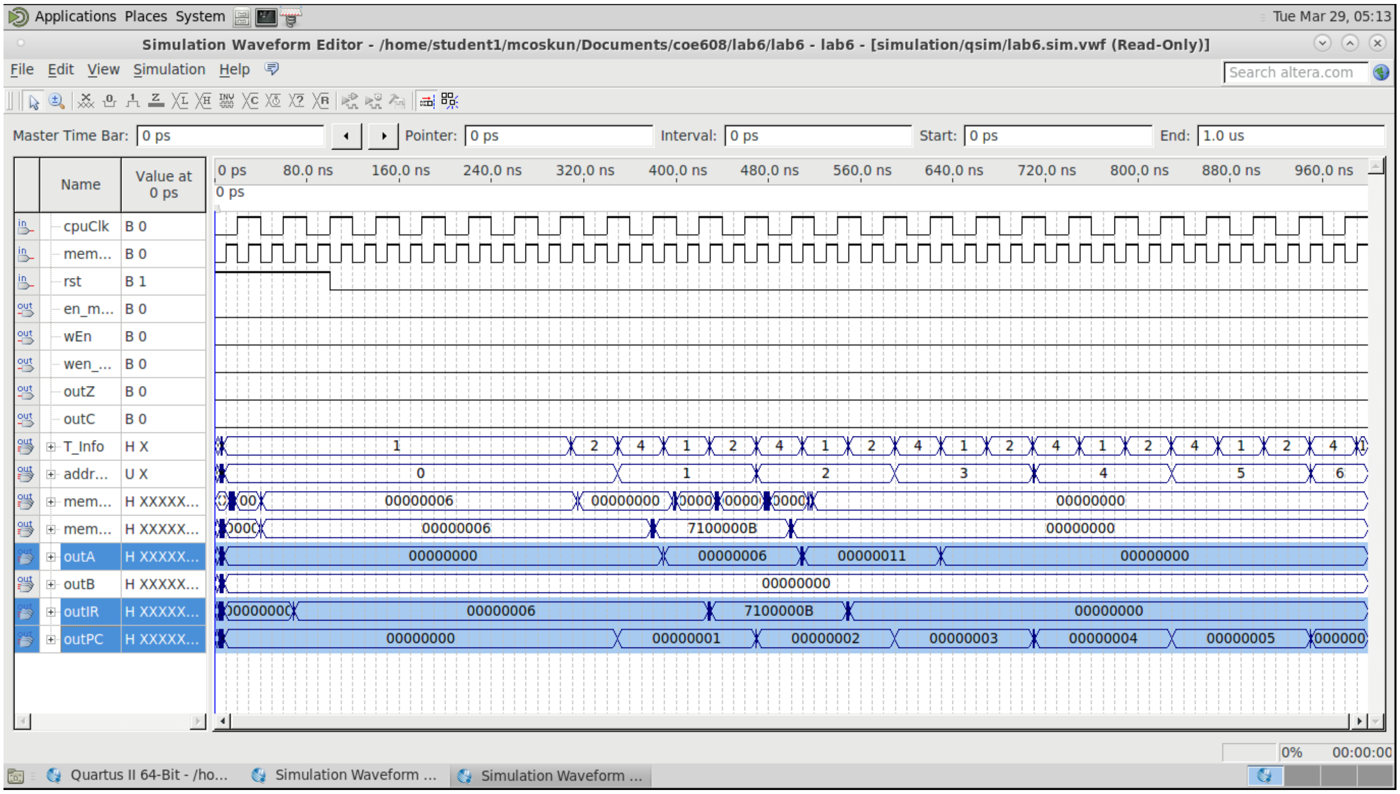
ANDI


Applications Places System
Tue Mar 29, 05:10
File Edit View Simulation Help
Search altera.com
0 ps 80.0 ns 160.0 ns 240.0 ns 320.0 ns 400.0 ns 480.0 ns 560.0 ns 640.0 ns 720.0 ns 800.0 ns 880.0 ns 960.0 ns
Name
Value at 0 ps
cpuClk B 0
mem... B 0
rst B 1
en_m... B 0
wEn B 0
wen_... B 0
outZ B 0
outC B 0
T_Info H X — 1 2 4 1 2 4 1 2 4 1 2 4 1 2 4 1 2 4
addr... U X — 0 1 2 3 4 5 6
mem... H XXXXX... — 00 00000006 00000000 0000 0000 0000 00000000
mem... H XXXXX... — 0000 00000006 7900000B 00000000
outA H XXXXX... — 00000000 00000006 00000002 00000000
outB H XXXXX... — 00000000
outIR H XXXXX... — 00000000 00000006 7900000B 00000000
outPC H XXXXX... — 00000000 00000001 00000002 00000003 00000004 00000005 000000
0% 00:00:00
Quartus II 64-Bit - /ho...
Simulation Waveform ...
Simulation Waveform ...

Simulation Waveform Editor - /home/student1/mcoskun/Documents/coe608/lab6/lab6 - lab6 - [simulation/qsim/lab6.sim.vwf (Read-Only)]

Master Time Bar: 0 ps Pointer: 7.06 ns Interval: 7.06 ns Start: 0 ps End: 1.0 us

ADDI

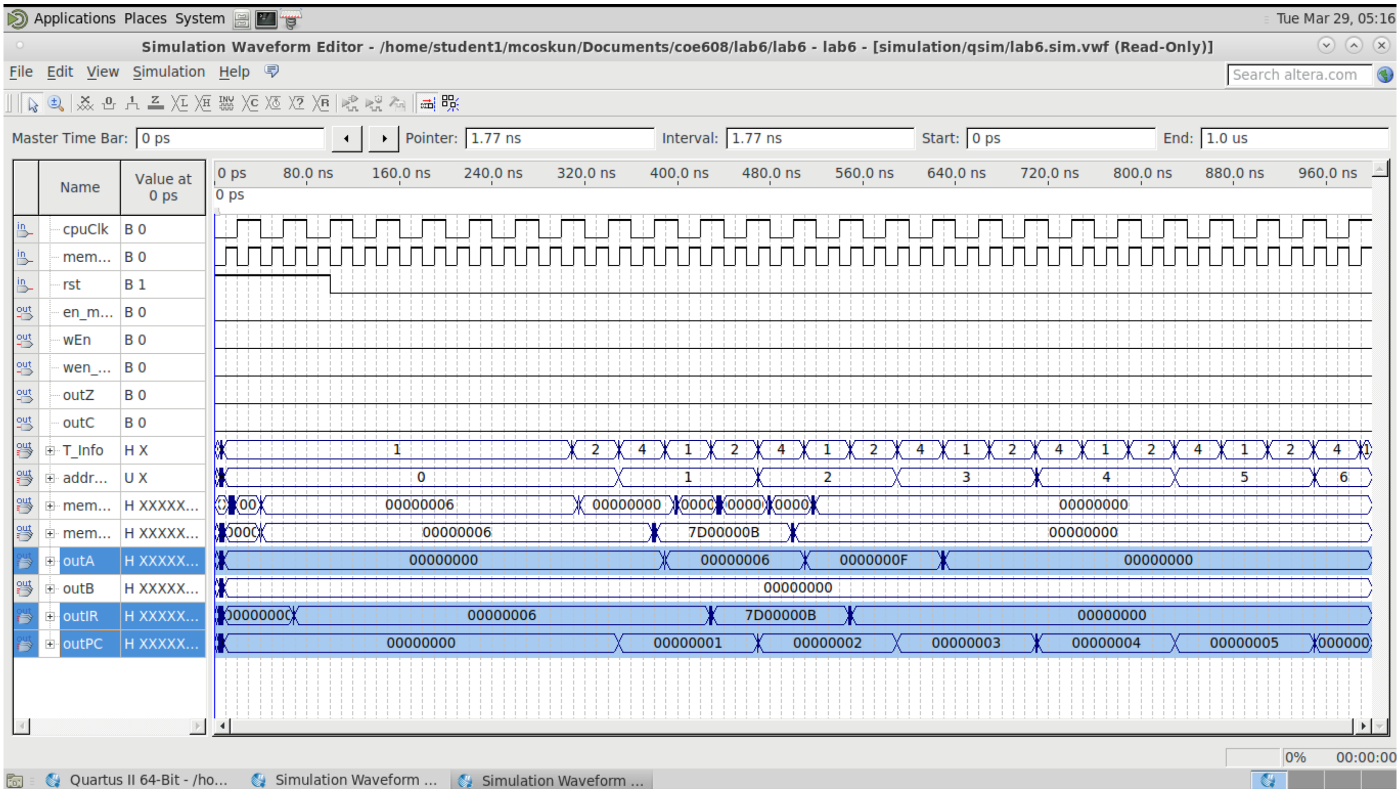


Simulation Waveform Editor - /home/student1/mcoskun/Documents/coe608/lab6/lab6 - lab6 - [simulation/qsim/lab6.sim.vwf (Read-Only)]

Master Time Bar: 0 ps Pointer: 0 ps Interval: 0 ps Start: 0 ps End: 1.0 us

Name	Value at 0 ps
cpuClk	B 0
mem...	B 0
rst	B 1
en_m...	B 0
wEn	B 0
wen_...	B 0
outZ	B 0
outC	B 0
T_Info	H X
addr...	U X
mem...	H XXXXX...
mem...	H XXXXX...
outA	H XXXXX...
outB	H XXXXX...
outIR	H XXXXX...
outPC	H XXXXX...

ORI



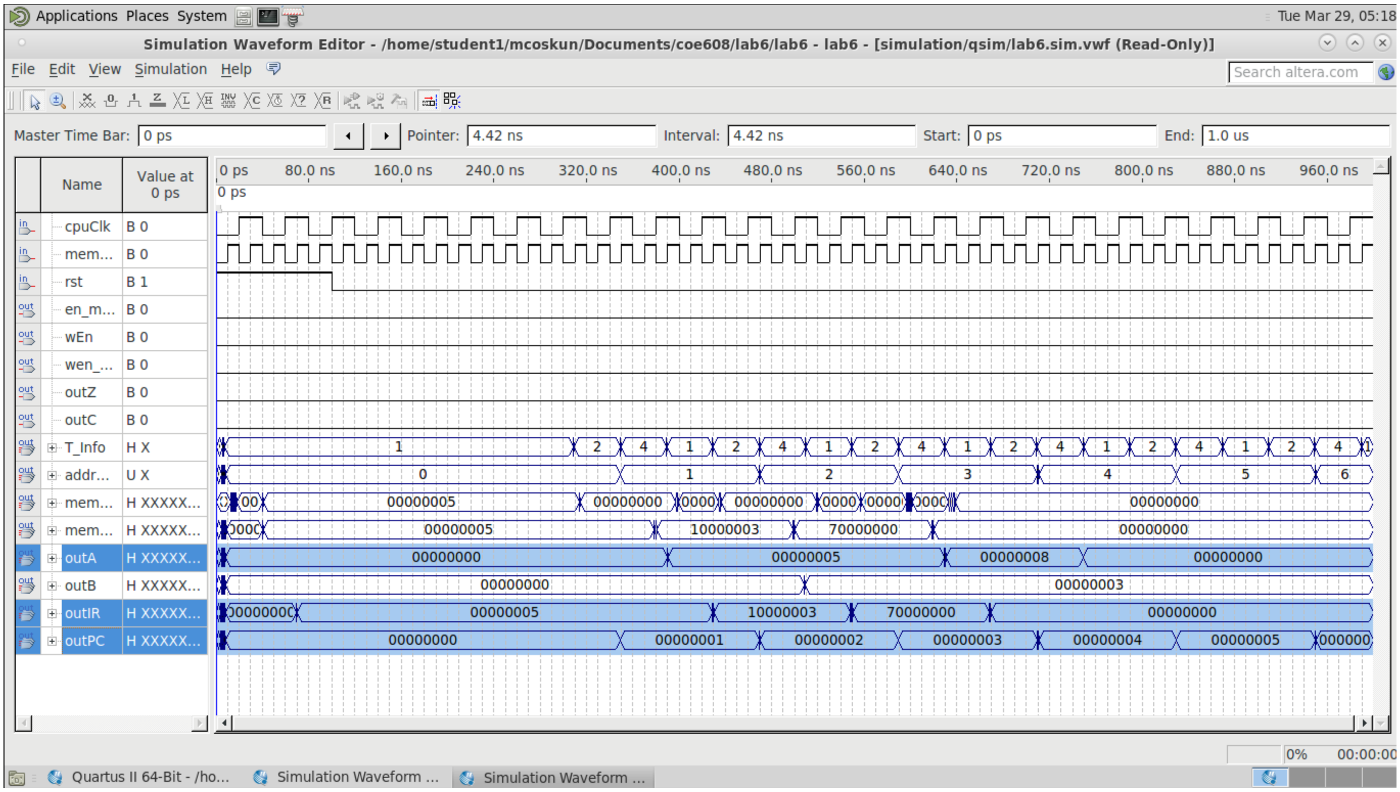
Simulation Waveform Editor - /home/student1/mcoskun/Documents/coe608/lab6/lab6 - lab6 - [simulation/qsim/lab6.sim.vwf (Read-Only)]

Master Time Bar: 0 ps Pointer: 1.77 ns Interval: 1.77 ns Start: 0 ps End: 1.0 us

Name	Value at 0 ps
cpuClk	B 0
mem...	B 0
rst	B 1
en_m...	B 0
wEn	B 0
wen_...	B 0
outZ	B 0
outC	B 0
T_Info	H X
addr...	U X
mem...	H XXXXX...
mem...	H XXXXX...
outA	H XXXXX...
outB	H XXXXX...
outIR	H XXXXX...
outPC	H XXXXX...

Applications Places System
Tue Mar 29, 05:16
File Edit View Simulation Help
Search altera.com
0 ps 80.0 ns 160.0 ns 240.0 ns 320.0 ns 400.0 ns 480.0 ns 560.0 ns 640.0 ns 720.0 ns 800.0 ns 880.0 ns 960.0 ns
1 2 4 1 2 4 1 2 4 1 2 4 1 2 4 1 2 4
0 1 2 3 4 5 6
00 00000006 00000000 0000 0000 0000 00000000
0000 00000006 7D00000B 00000000
00000000 00000006 0000000F 00000000
00000000
0000000 00000006 7D00000B 00000000
00000000 00000001 00000002 00000003 00000004 00000005 000000
0% 00:00:00
Quartus II 64-Bit - /ho...
Simulation Waveform ...
Simulation Waveform ...

ADD

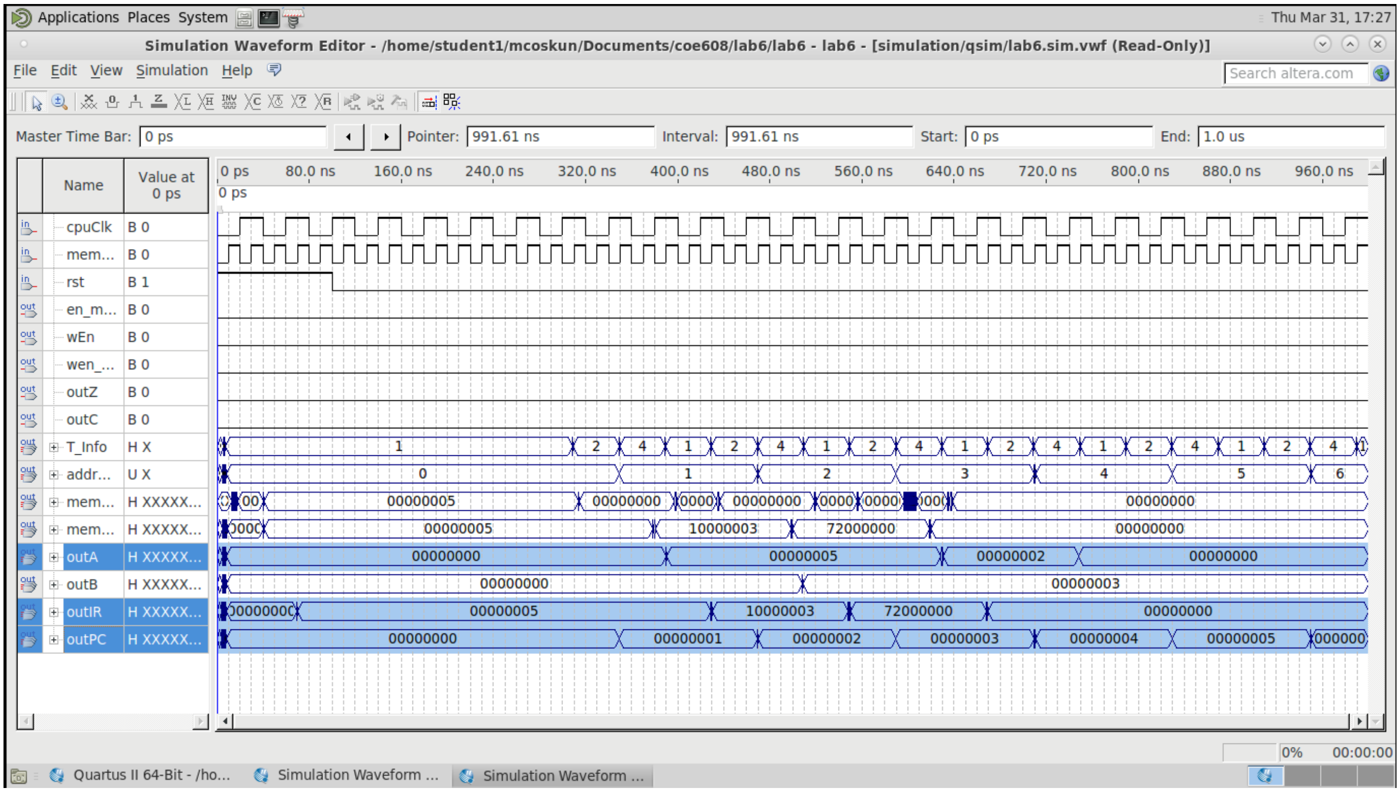

Applications Places System
Tue Mar 29, 05:18
File Edit View Simulation Help
Search altera.com
0 ps 80.0 ns 160.0 ns 240.0 ns 320.0 ns 400.0 ns 480.0 ns 560.0 ns 640.0 ns 720.0 ns 800.0 ns 880.0 ns 960.0 ns
1 2 4 1 2 4 1 2 4 1 2 4 1 2 4 1 2 4 1
0 1 2 3 4 5 6
00000005 00000000 0000 00000000 0000 0000 000C 00000000
0000 00000005 10000003 70000000 00000000
00000000 00000005 00000008 00000000
00000000 00000003
0000000C 00000005 10000003 70000000 00000000
00000000 00000001 00000002 00000003 00000004 00000005 000000
0% 00:00:00
Quartus II 64-Bit - /ho... Simulation Waveform ... Simulation Waveform ...

Simulation Waveform Editor - /home/student1/mcoskun/Documents/coe608/lab6/lab6 - lab6 - [simulation/qsim/lab6.sim.vwf (Read-Only)]

Master Time Bar: 0 ps Pointer: 4.42 ns Interval: 4.42 ns Start: 0 ps End: 1.0 us

Name	Value at 0 ps
cpuClk	B 0
mem...	B 0
rst	B 1
en_m...	B 0
wEn	B 0
wen_...	B 0
outZ	B 0
outC	B 0
T_Info	H X
addr...	U X
mem...	H XXXXX...
mem...	H XXXXX...
outA	H XXXXX...
outB	H XXXXX...
outIR	H XXXXX...
outPC	H XXXXX...

SUB

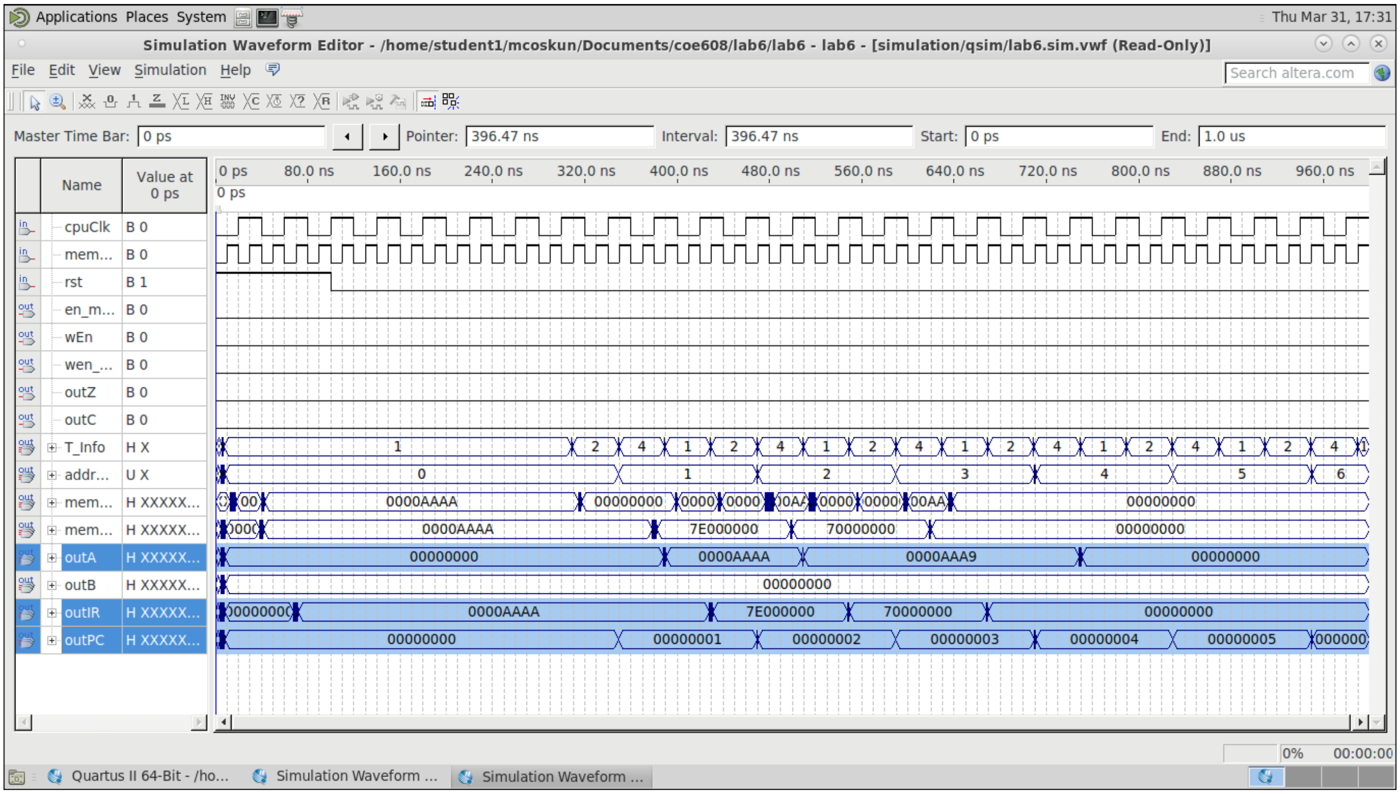

Applications Places System
Thu Mar 31, 17:27
File Edit View Simulation Help
Search altera.com
0 ps 80.0 ns 160.0 ns 240.0 ns 320.0 ns 400.0 ns 480.0 ns 560.0 ns 640.0 ns 720.0 ns 800.0 ns 880.0 ns 960.0 ns
1 2 4 1 2 4 1 2 4 1 2 4 1 2 4 1 2 4 1
0 1 2 3 4 5 6
00000005 00000000 0000 00000000 0000 0000 000 00000000
000C 00000005 10000003 72000000 00000000
00000000 00000005 00000002 00000000
00000000 00000003
0000000C 00000005 10000003 72000000 00000000
00000000 00000001 00000002 00000003 00000004 00000005 000000
0% 00:00:00
Quartus II 64-Bit - /ho... Simulation Waveform ... Simulation Waveform ...

Simulation Waveform Editor - /home/student1/mcoskun/Documents/coe608/lab6/lab6 - lab6 - [simulation/qsim/lab6.sim.vwf (Read-Only)]

Master Time Bar: 0 ps Pointer: 991.61 ns Interval: 991.61 ns Start: 0 ps End: 1.0 us

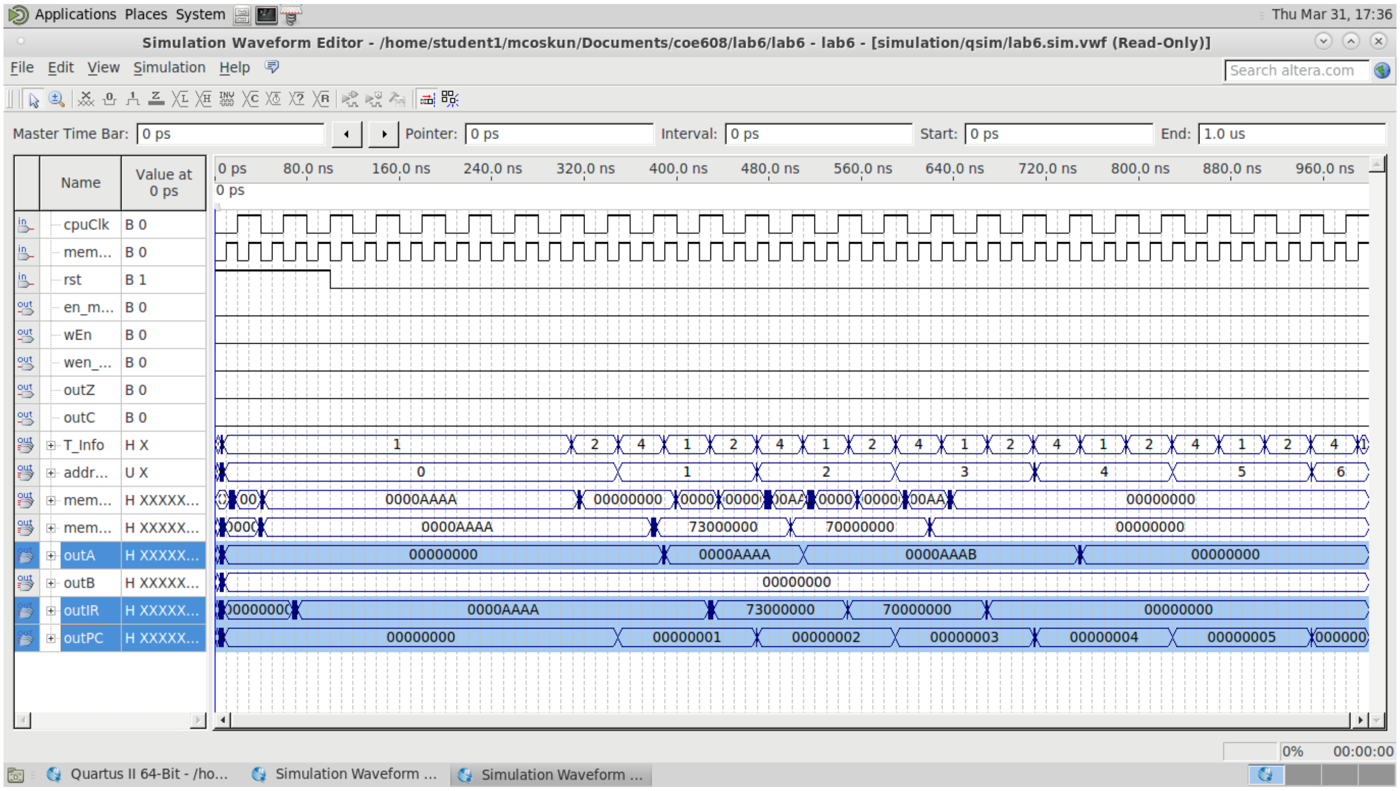
Name	Value at 0 ps
cpuClk	B 0
mem...	B 0
rst	B 1
en_m...	B 0
wEn	B 0
wen_...	B 0
outZ	B 0
outC	B 0
T_Info	H X
addr...	U X
mem...	H XXXXX...
mem...	H XXXXX...
outA	H XXXXX...
outB	H XXXXX...
outIR	H XXXXX...
outPC	H XXXXX...

DECA


Applications Places System
Thu Mar 31, 17:31
Simulation Waveform Editor - /home/student1/mcoskun/Documents/coe608/lab6/lab6 - lab6 - [simulation/qsim/lab6.sim.vwf (Read-Only)]
File Edit View Simulation Help
Search altera.com
Name
Value at 0 ps
0 ps 80.0 ns 160.0 ns 240.0 ns 320.0 ns 400.0 ns 480.0 ns 560.0 ns 640.0 ns 720.0 ns 800.0 ns 880.0 ns 960.0 ns
cpuClk B 0
mem... B 0
rst B 1
en_m... B 0
wEn B 0
wen_... B 0
outZ B 0
outC B 0
T_Info H X 1 2 4 1 2 4 1 2 4 1 2 4 1 2 4 1 2 4
addr... U X 0 1 2 3 4 5 6
mem... H XXXXX... 00 0000AAAA 00000000 0000 0000 00AA 0000 0000 00AA 00000000
mem... H XXXXX... 000C 0000AAAA 7E000000 70000000 00000000
outA H XXXXX... 00000000 0000AAAA 0000AAA9 00000000
outB H XXXXX... 00000000
outIR H XXXXX... 0000000C 0000AAAA 7E000000 70000000 00000000
outPC H XXXXX... 00000000 00000001 00000002 00000003 00000004 00000005 000000
0% 00:00:00
Quartus II 64-Bit - /ho... Simulation Waveform ... Simulation Waveform ...

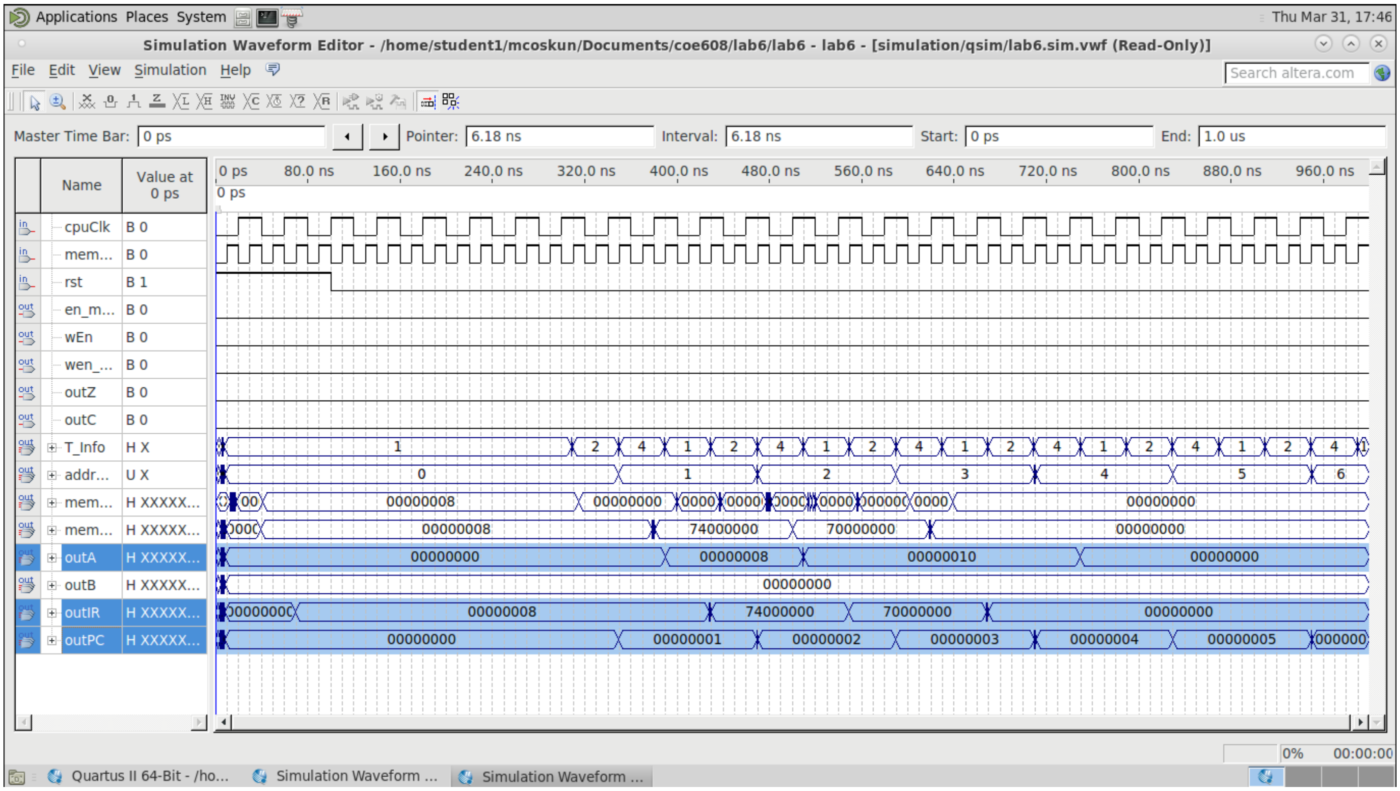
Master Time Bar: 0 ps
Pointer: 396.47 ns
Interval: 396.47 ns
Start: 0 ps
End: 1.0 us

INCA


Applications Places System
Thu Mar 31, 17:36
Simulation Waveform Editor - /home/student1/mcoskun/Documents/coe608/lab6/lab6 - lab6 - [simulation/qsim/lab6.sim.vwf (Read-Only)]
File Edit View Simulation Help
Search altera.com
Name
Value at 0 ps
0 ps 80.0 ns 160.0 ns 240.0 ns 320.0 ns 400.0 ns 480.0 ns 560.0 ns 640.0 ns 720.0 ns 800.0 ns 880.0 ns 960.0 ns
cpuClk B 0
mem... B 0
rst B 1
en_m... B 0
wEn B 0
wen_... B 0
outZ B 0
outC B 0
T_Info H X 1 2 4 1 2 4 1 2 4 1 2 4 1 2 4 1 2 4
addr... U X 0 1 2 3 4 5 6
mem... H XXXXX... 00 0000AAAA 00000000 0000 0000 00AA 0000 0000 00AA 00000000
mem... H XXXXX... 000C 0000AAAA 73000000 70000000 00000000
outA H XXXXX... 00000000 0000AAAA 0000AAAB 00000000
outB H XXXXX... 00000000
outIR H XXXXX... 0000000C 0000AAAA 73000000 70000000 00000000
outPC H XXXXX... 00000000 00000001 00000002 00000003 00000004 00000005 000000
0% 00:00:00
Quartus II 64-Bit - /ho... Simulation Waveform ... Simulation Waveform ...

Master Time Bar: 0 ps
Pointer: 0 ps
Interval: 0 ps
Start: 0 ps
End: 1.0 us

ROL

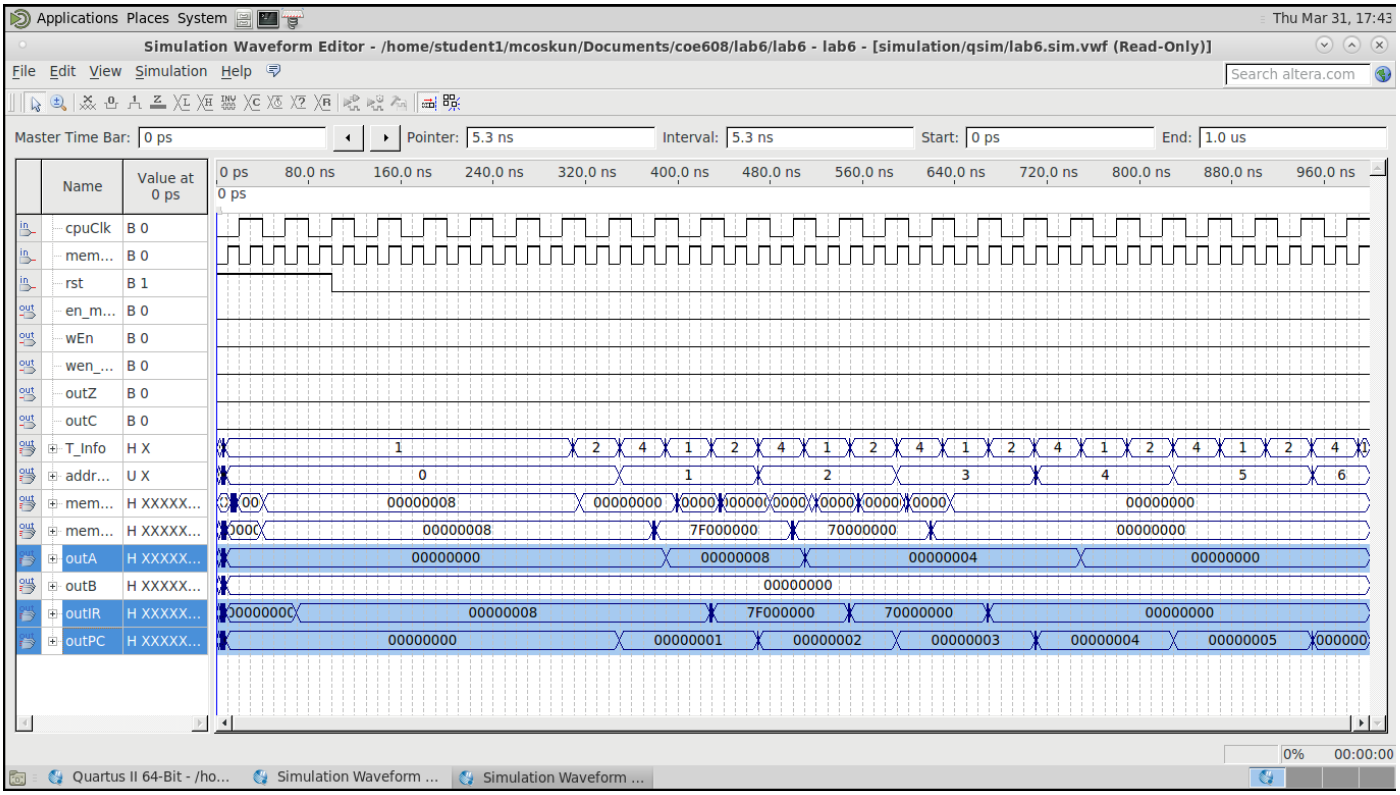

Applications Places System
Thu Mar 31, 17:46
File Edit View Simulation Help
Search altera.com
0 ps 80.0 ns 160.0 ns 240.0 ns 320.0 ns 400.0 ns 480.0 ns 560.0 ns 640.0 ns 720.0 ns 800.0 ns 880.0 ns 960.0 ns
T_Info: 1 2 4 1 2 4 1 2 4 1 2 4 1 2 4 1 2 4
addr: 0 1 2 3 4 5 6
mem: 00 00000008 00000000 0000 0000 000C 0000 00000 0000 00000000
mem: 000C 00000008 74000000 70000000 00000000
outA: 00000000 00000008 00000010 00000000
outB: 00000000
outIR: 0000000C 00000008 74000000 70000000 00000000
outPC: 00000000 00000001 00000002 00000003 00000004 00000005 000000
0% 00:00:00
Quartus II 64-Bit - /ho...
Simulation Waveform ...
Simulation Waveform ...

Simulation Waveform Editor - /home/student1/mcoskun/Documents/coe608/lab6/lab6 - lab6 - [simulation/qsim/lab6.sim.vwf (Read-Only)]

Master Time Bar: 0 ps Pointer: 6.18 ns Interval: 6.18 ns Start: 0 ps End: 1.0 us

Name	Value at 0 ps
cpuClk	B 0
mem...	B 0
rst	B 1
en_m...	B 0
wEn	B 0
wen_...	B 0
outZ	B 0
outC	B 0
T_Info	H X
addr...	U X
mem...	H XXXXX...
mem...	H XXXXX...
outA	H XXXXX...
outB	H XXXXX...
outIR	H XXXXX...
outPC	H XXXXX...

ROR

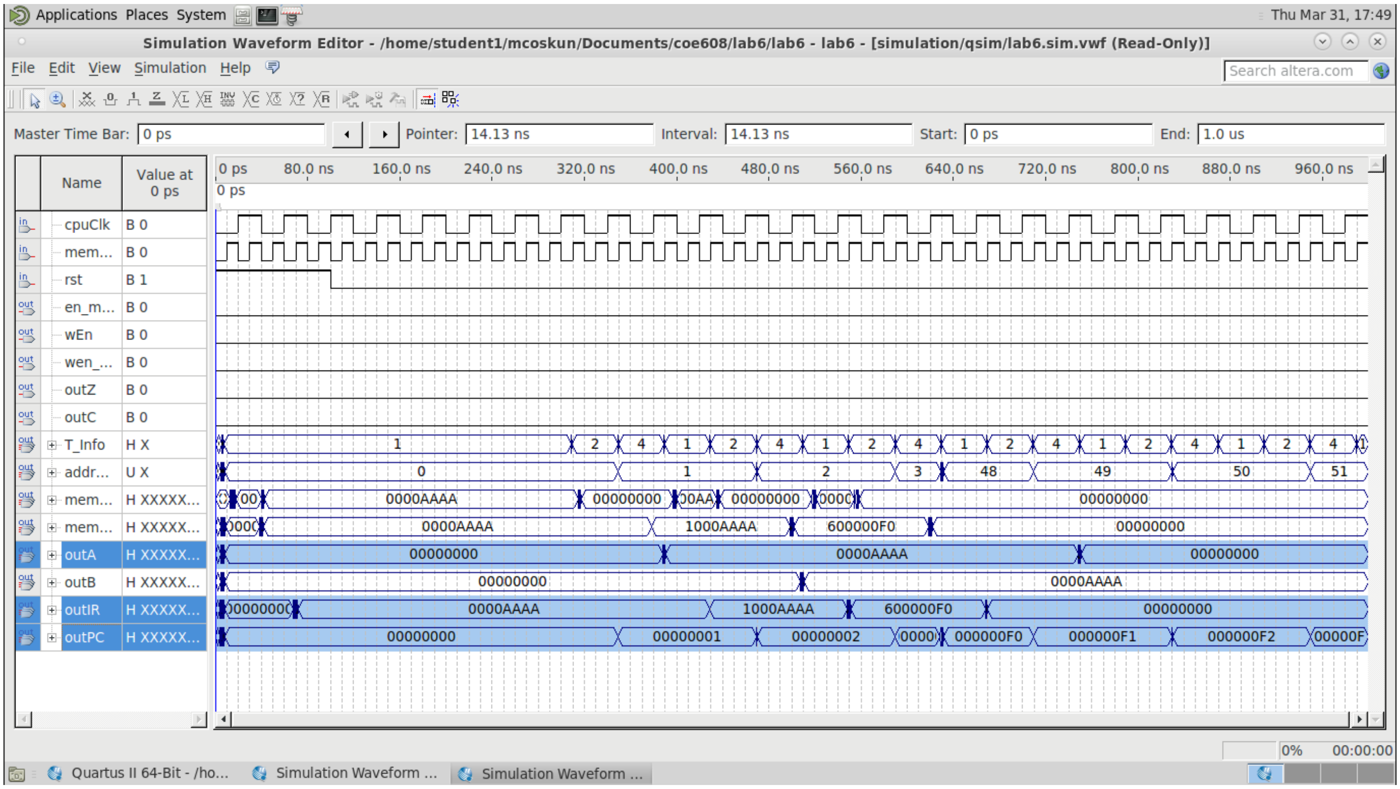

Applications Places System
Thu Mar 31, 17:43
File Edit View Simulation Help
Search altera.com
0 ps 80.0 ns 160.0 ns 240.0 ns 320.0 ns 400.0 ns 480.0 ns 560.0 ns 640.0 ns 720.0 ns 800.0 ns 880.0 ns 960.0 ns
T_Info: 1 2 4 1 2 4 1 2 4 1 2 4 1 2 4 1 2 4
addr: 0 1 2 3 4 5 6
mem: 00 00000008 00000000 0000 00000 0000 0000 0000 0000 00000000
mem: 000C 00000008 7F000000 70000000 00000000
outA: 00000000 00000008 00000004 00000000
outB: 00000000
outIR: 0000000C 00000008 7F000000 70000000 00000000
outPC: 00000000 00000001 00000002 00000003 00000004 00000005 000000
0% 00:00:00
Quartus II 64-Bit - /ho...
Simulation Waveform ...
Simulation Waveform ...

Simulation Waveform Editor - /home/student1/mcoskun/Documents/coe608/lab6/lab6 - lab6 - [simulation/qsim/lab6.sim.vwf (Read-Only)]

Master Time Bar: 0 ps Pointer: 5.3 ns Interval: 5.3 ns Start: 0 ps End: 1.0 us

Name	Value at 0 ps
cpuClk	B 0
mem...	B 0
rst	B 1
en_m...	B 0
wEn	B 0
wen_...	B 0
outZ	B 0
outC	B 0
T_Info	H X
addr...	U X
mem...	H XXXXX...
mem...	H XXXXX...
outA	H XXXXX...
outB	H XXXXX...
outIR	H XXXXX...
outPC	H XXXXX...

BEQ



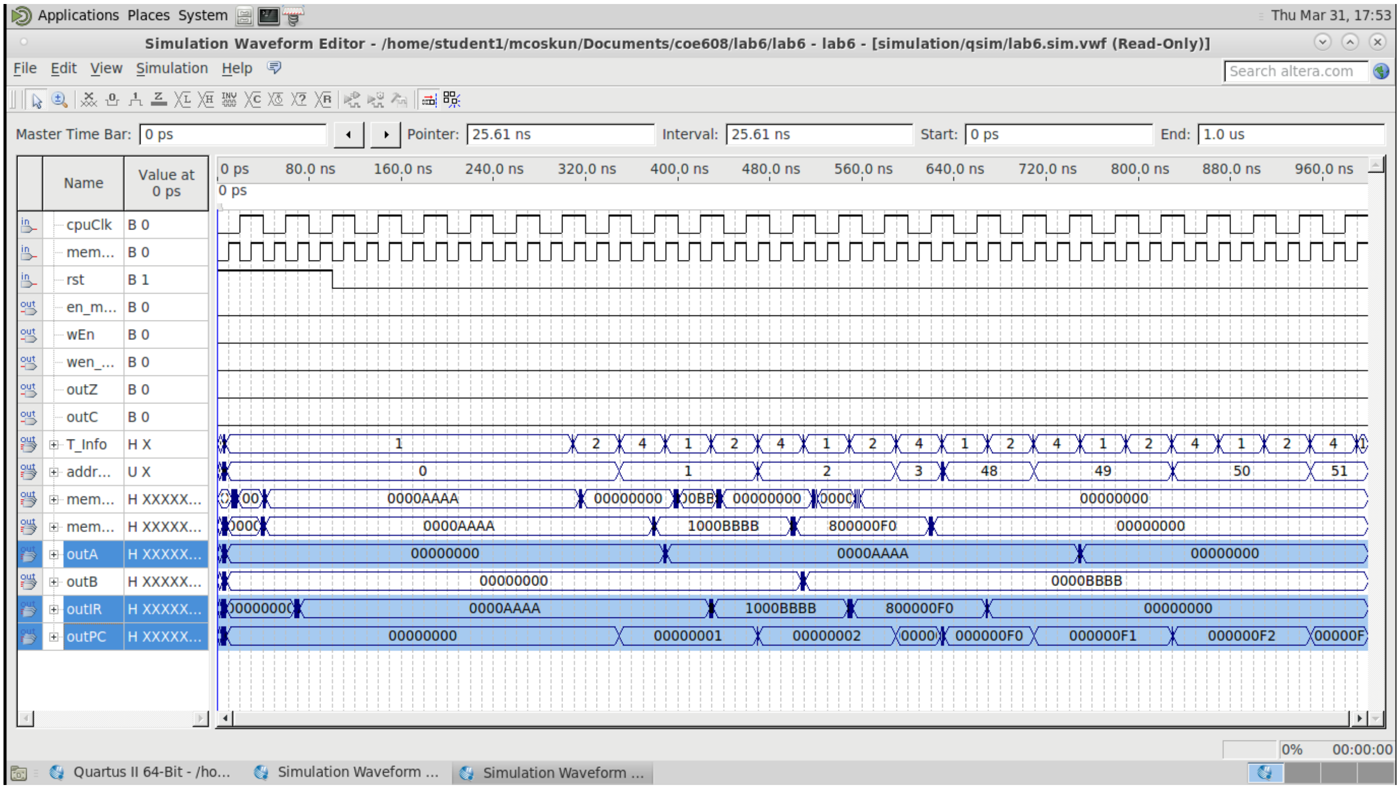
Applications Places System
Thu Mar 31, 17:49
File Edit View Simulation Help
Search altera.com
0 ps 80.0 ns 160.0 ns 240.0 ns 320.0 ns 400.0 ns 480.0 ns 560.0 ns 640.0 ns 720.0 ns 800.0 ns 880.0 ns 960.0 ns
1 2 4 1 2 4 1 2 4 1 2 4 1 2 4 1 2 4
0 1 2 3 48 49 50 51
00 0000AAAA 00000000 00AA 00000000 0000 00000000
0000AAAA 1000AAAA 600000F0 00000000
00000000 0000AAAA 00000000
00000000 0000AAAA
0000AAAA 1000AAAA 600000F0 00000000
00000000 00000001 00000002 000000F0 000000F1 000000F2
0% 00:00:00
Quartus II 64-Bit - /ho...
Simulation Waveform ...
Simulation Waveform ...

Simulation Waveform Editor - /home/student1/mcoskun/Documents/coe608/lab6/lab6 - lab6 - [simulation/qsim/lab6.sim.vwf (Read-Only)]

Master Time Bar: 0 ps Pointer: 14.13 ns Interval: 14.13 ns Start: 0 ps End: 1.0 us

Name	Value at 0 ps
cpuClk	B 0
mem...	B 0
rst	B 1
en_m...	B 0
wEn	B 0
wen_...	B 0
outZ	B 0
outC	B 0
T_Info	H X
addr...	U X
mem...	H XXXXX...
mem...	H XXXXX...
outA	H XXXXX...
outB	H XXXXX...
outIR	H XXXXX...
outPC	H XXXXX...

BNE



Applications Places System
Thu Mar 31, 17:53
File Edit View Simulation Help
Search altera.com
0 ps 80.0 ns 160.0 ns 240.0 ns 320.0 ns 400.0 ns 480.0 ns 560.0 ns 640.0 ns 720.0 ns 800.0 ns 880.0 ns 960.0 ns
1 2 4 1 2 4 1 2 4 1 2 4 1 2 4 1 2 4
0 1 2 3 48 49 50 51
00 0000AAAA 00000000 00BB 00000000 0000 00000000
0000AAAA 1000BBBB 800000F0 00000000
00000000 0000AAAA 00000000
00000000 0000BBBB
0000AAAA 1000BBBB 800000F0 00000000
00000000 00000001 00000002 000000F0 000000F1 000000F2
0% 00:00:00
Quartus II 64-Bit - /ho...
Simulation Waveform ...
Simulation Waveform ...

Simulation Waveform Editor - /home/student1/mcoskun/Documents/coe608/lab6/lab6 - lab6 - [simulation/qsim/lab6.sim.vwf (Read-Only)]

Master Time Bar: 0 ps Pointer: 25.61 ns Interval: 25.61 ns Start: 0 ps End: 1.0 us

Name	Value at 0 ps
cpuClk	B 0
mem...	B 0
rst	B 1
en_m...	B 0
wEn	B 0
wen_...	B 0
outZ	B 0
outC	B 0
T_Info	H X
addr...	U X
mem...	H XXXXX...
mem...	H XXXXX...
outA	H XXXXX...
outB	H XXXXX...
outIR	H XXXXX...
outPC	H XXXXX...