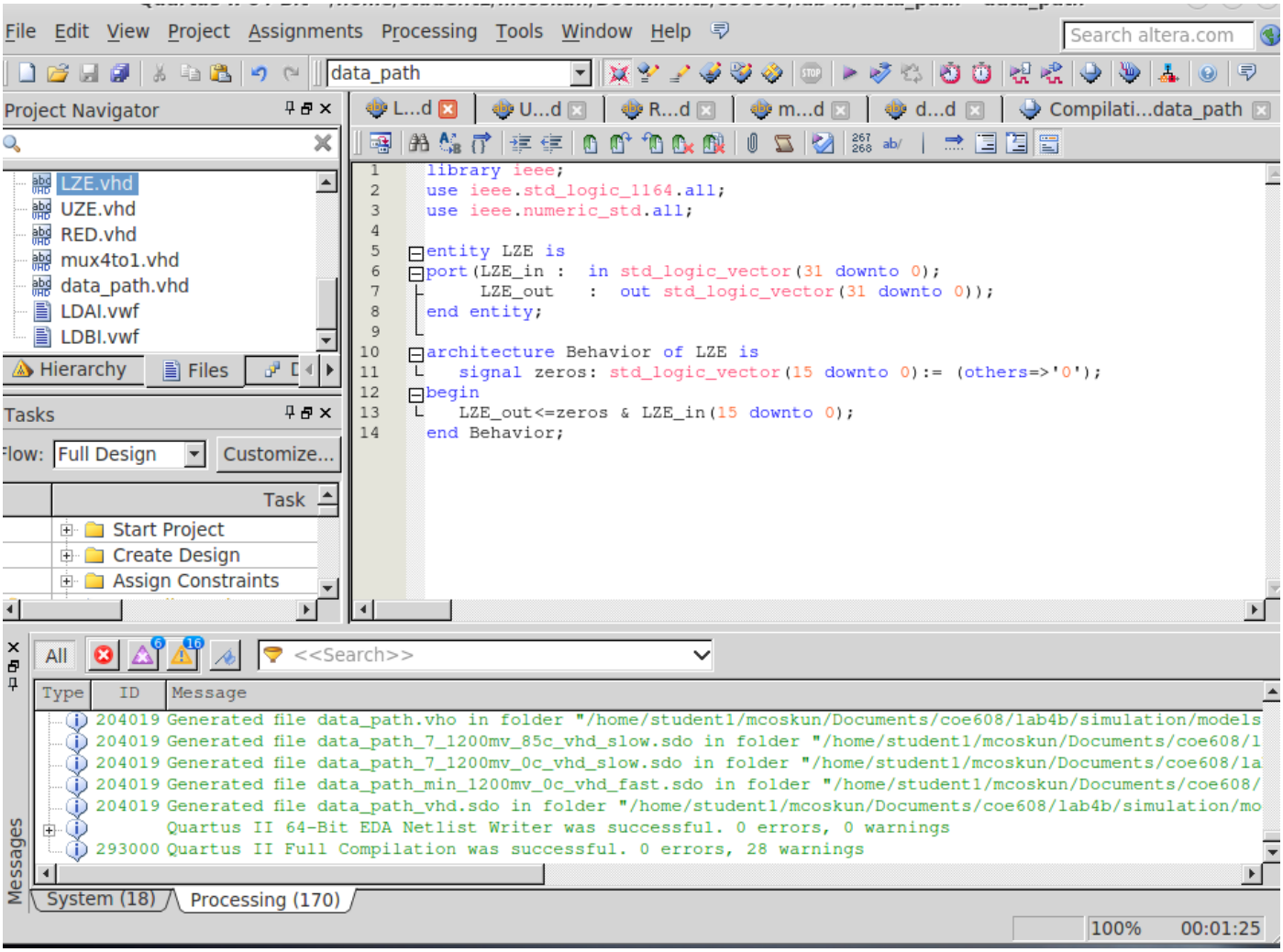
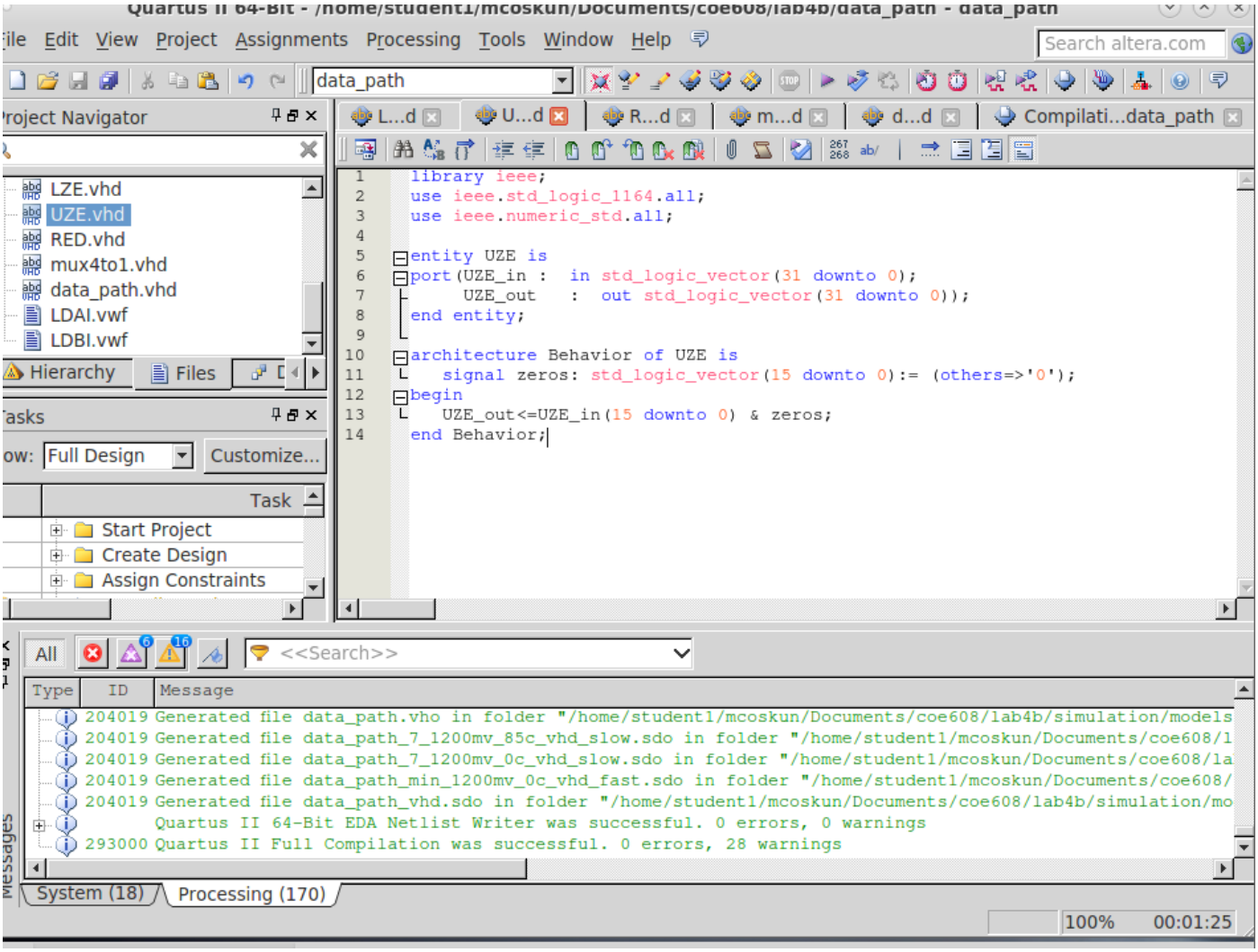
In this lab, we will be interconnecting the components (PC, Registers, data memory and ALU, reducer, extender etc.) required to create the CPU's data-path. Most of the components were created in the previous labs and their names are listed below. You can can find the screenshots of the VHDL codes of the rest of the necessary components for building and testing the data-path.

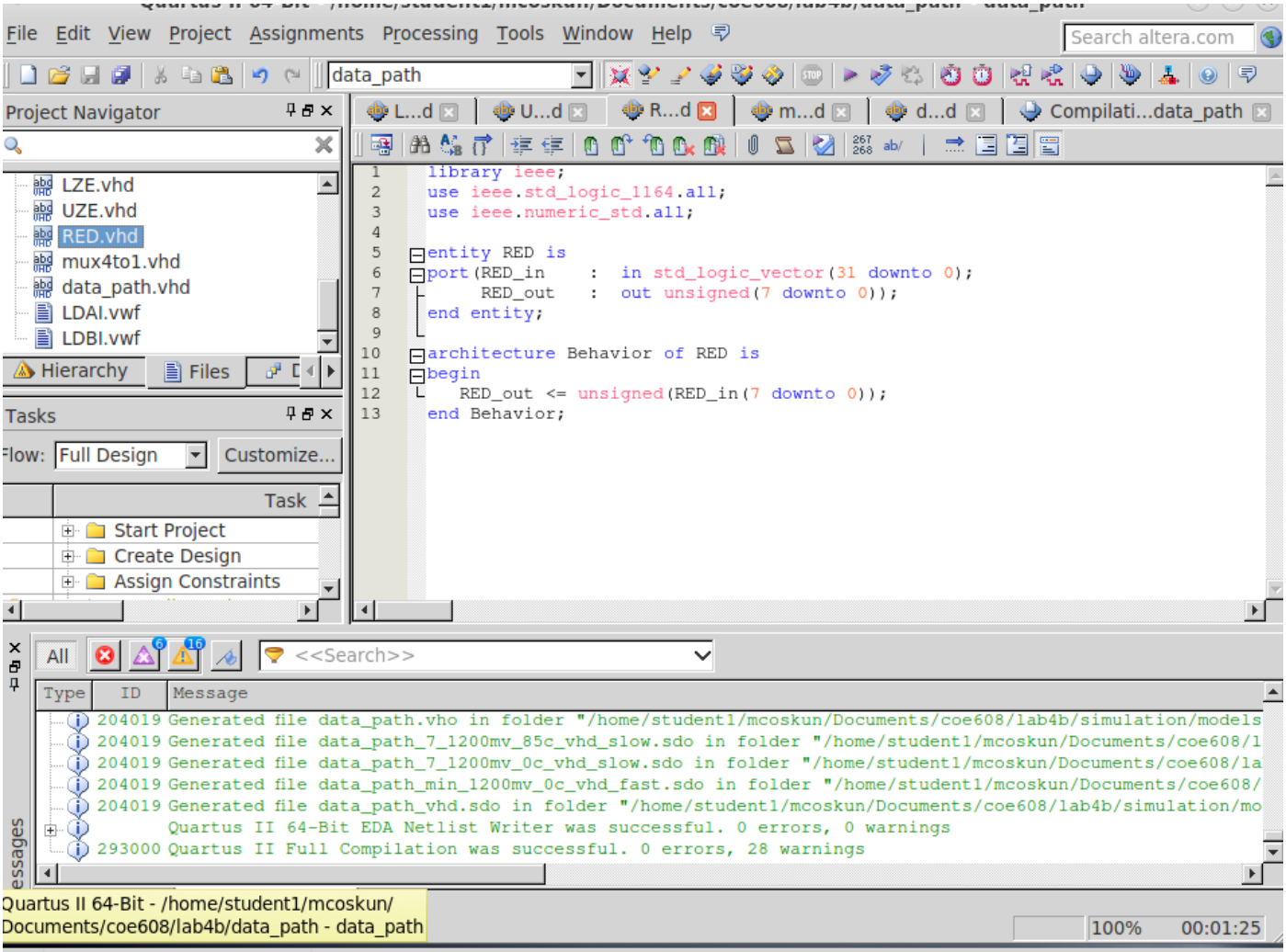
The VHDL code of LZE can be seen below.



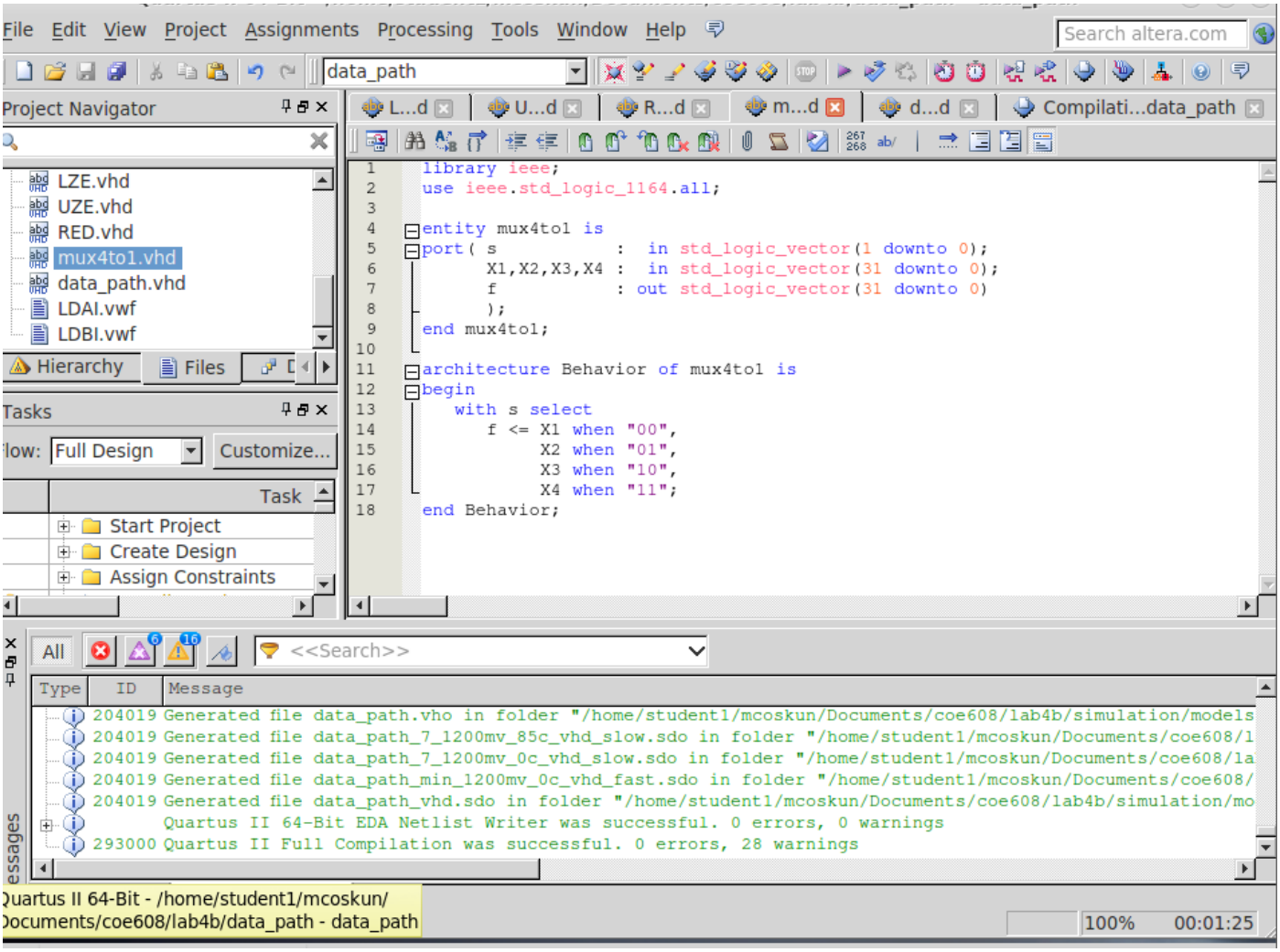
The VHDL code of UZE can be seen below.



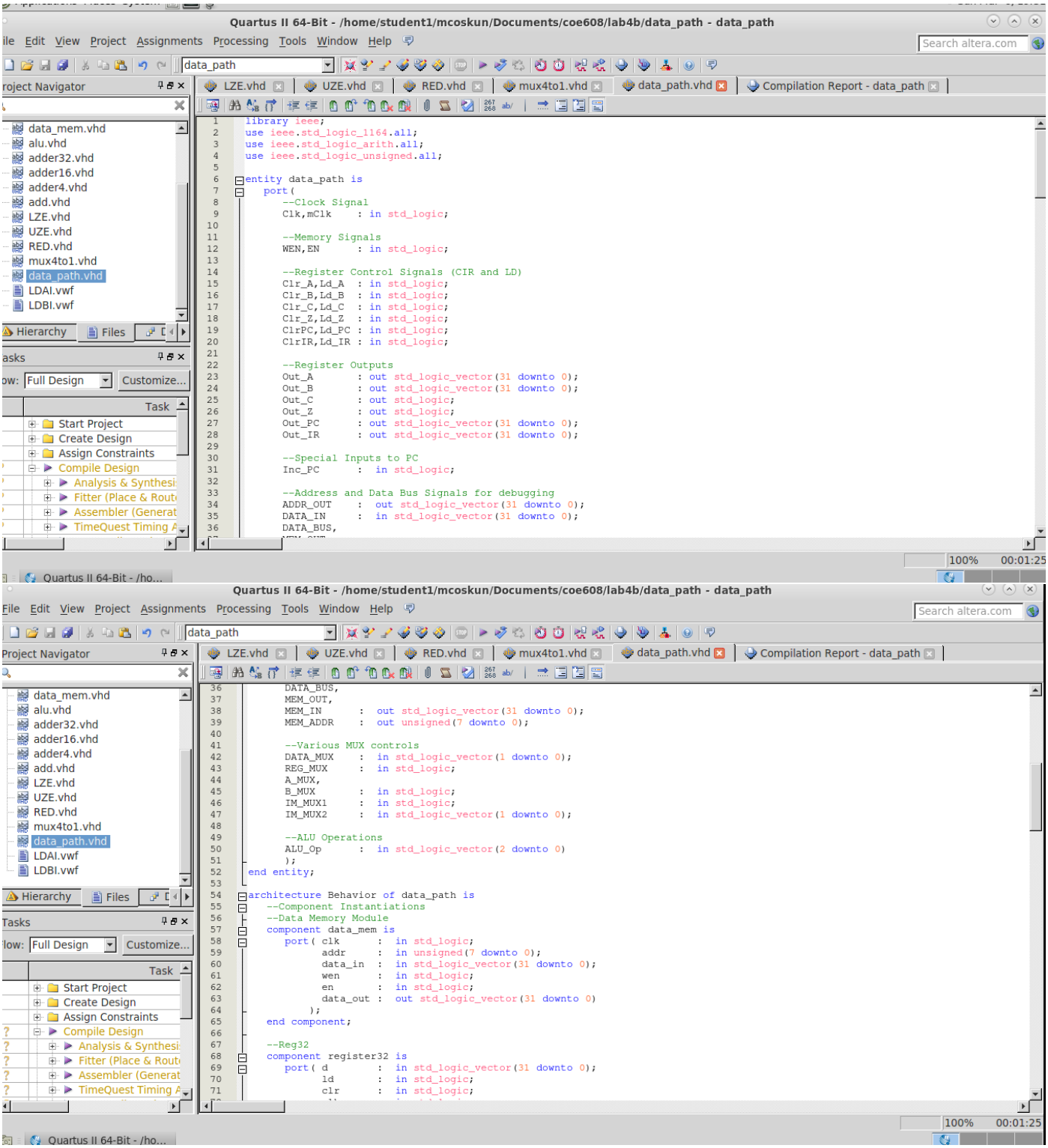
The VHDL code of RED can be seen below.



The VHDL code of mux4to1 can be seen below.



The VHDL code of data_path can be seen below.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adder16.vhd
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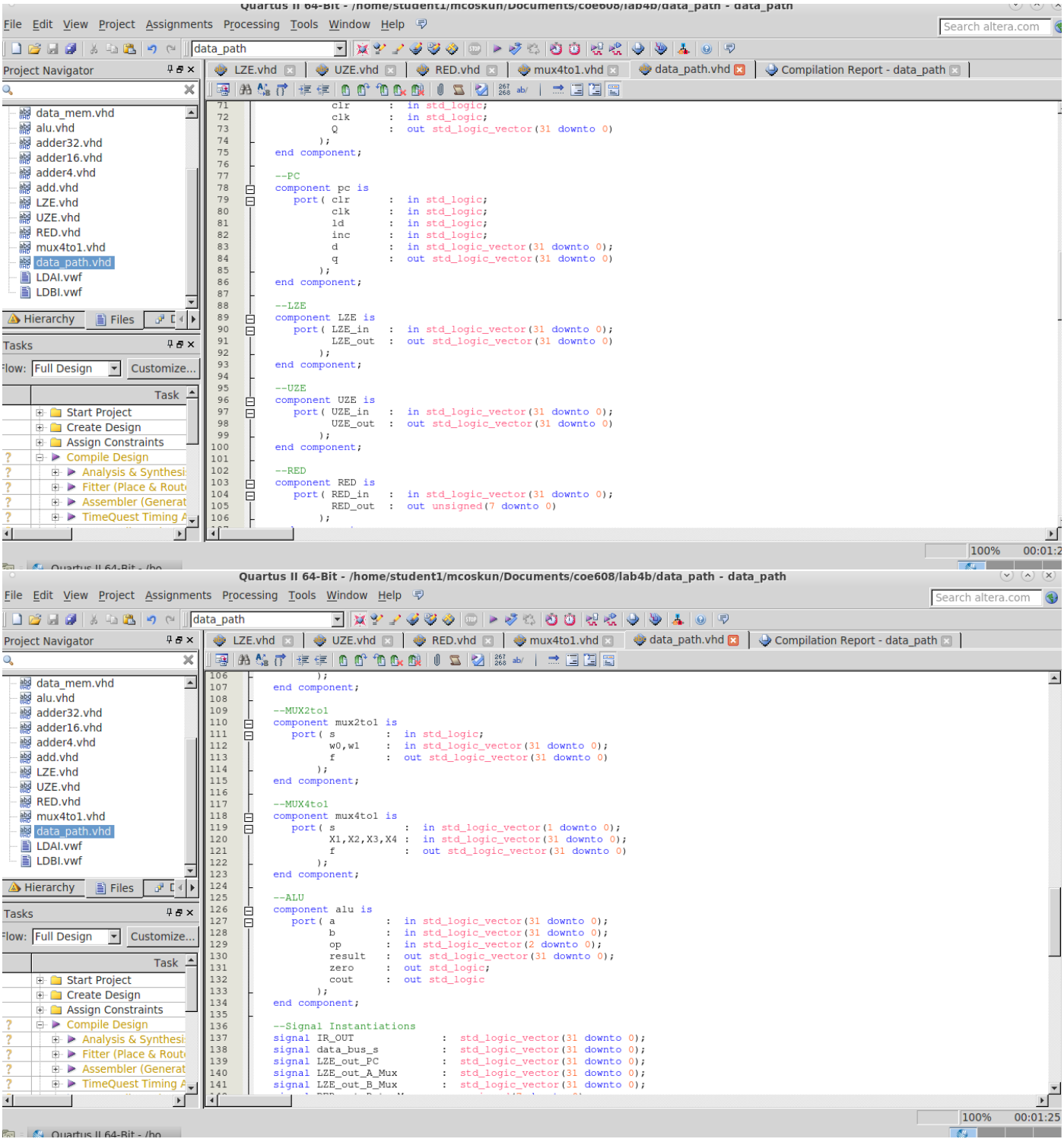
TimeQuest Timing A
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;
entity data_path is
port(
--Clock Signal
Clk,mClk : in std_logic;
--Memory Signals
WEN,EN : in std_logic;
--Register Control Signals (CIR and LD)
Clr_A,Ld_A : in std_logic;
Clr_B,Ld_B : in std_logic;
Clr_C,Ld_C : in std_logic;
Clr_Z,Ld_Z : in std_logic;
ClrPC,Ld_PC : in std_logic;
ClrIR,Ld_IR : in std_logic;
--Register Outputs
Out_A : out std_logic_vector(31 downto 0);
Out_B : out std_logic_vector(31 downto 0);
Out_C : out std_logic;
Out_Z : out std_logic;
Out_PC : out std_logic_vector(31 downto 0);
Out_IR : out std_logic_vector(31 downto 0);
--Special Inputs to PC
Inc_PC : in std_logic;
--Address and Data Bus Signals for debugging
ADDR_OUT : out std_logic_vector(31 downto 0);
DATA_IN : in std_logic_vector(31 downto 0);
DATA_BUS,
MEM_OUT,
MEM_IN : out std_logic_vector(31 downto 0);
MEM_ADDR : out unsigned(7 downto 0);
--Various MUX controls
DATA_MUX : in std_logic_vector(1 downto 0);
REG_MUX : in std_logic;
A_MUX,
B_MUX : in std_logic;
IM_MUX1 : in std_logic;
IM_MUX2 : in std_logic_vector(1 downto 0);
--ALU Operations
ALU_Op : in std_logic_vector(2 downto 0)
);
end entity;
architecture Behavior of data_path is
--Component Instantiations
--Data Memory Module
component data_mem is
port(clk : in std_logic;
addr : in unsigned(7 downto 0);
data_in : in std_logic_vector(31 downto 0);
wen : in std_logic;
en : in std_logic;
data_out : out std_logic_vector(31 downto 0)
);
end component;
--Reg32
component register32 is
port(d : in std_logic_vector(31 downto 0);
ld : in std_logic;
clr : in std_logic;
100%
00:01:25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71 clr : in std_logic;
72 clk : in std_logic;
73 Q : out std_logic_vector(31 downto 0)
74);
75 end component;
76
77 --PC
78 component pc is
79 port(clr : in std_logic;
80 clk : in std_logic;
81 ld : in std_logic;
82 inc : in std_logic;
83 d : in std_logic_vector(31 downto 0);
84 q : out std_logic_vector(31 downto 0)
85);
86 end component;
87
88 --LZE
89 component LZE is
90 port(LZE_in : in std_logic_vector(31 downto 0);
91 LZE_out : out std_logic_vector(31 downto 0)
92);
93 end component;
94
95 --UZE
96 component UZE is
97 port(UZE_in : in std_logic_vector(31 downto 0);
98 UZE_out : out std_logic_vector(31 downto 0)
99);
100 end component;
101
102 --RED
103 component RED is
104 port(RED_in : in std_logic_vector(31 downto 0);
105 RED_out : out unsigned(7 downto 0)
106);
100%
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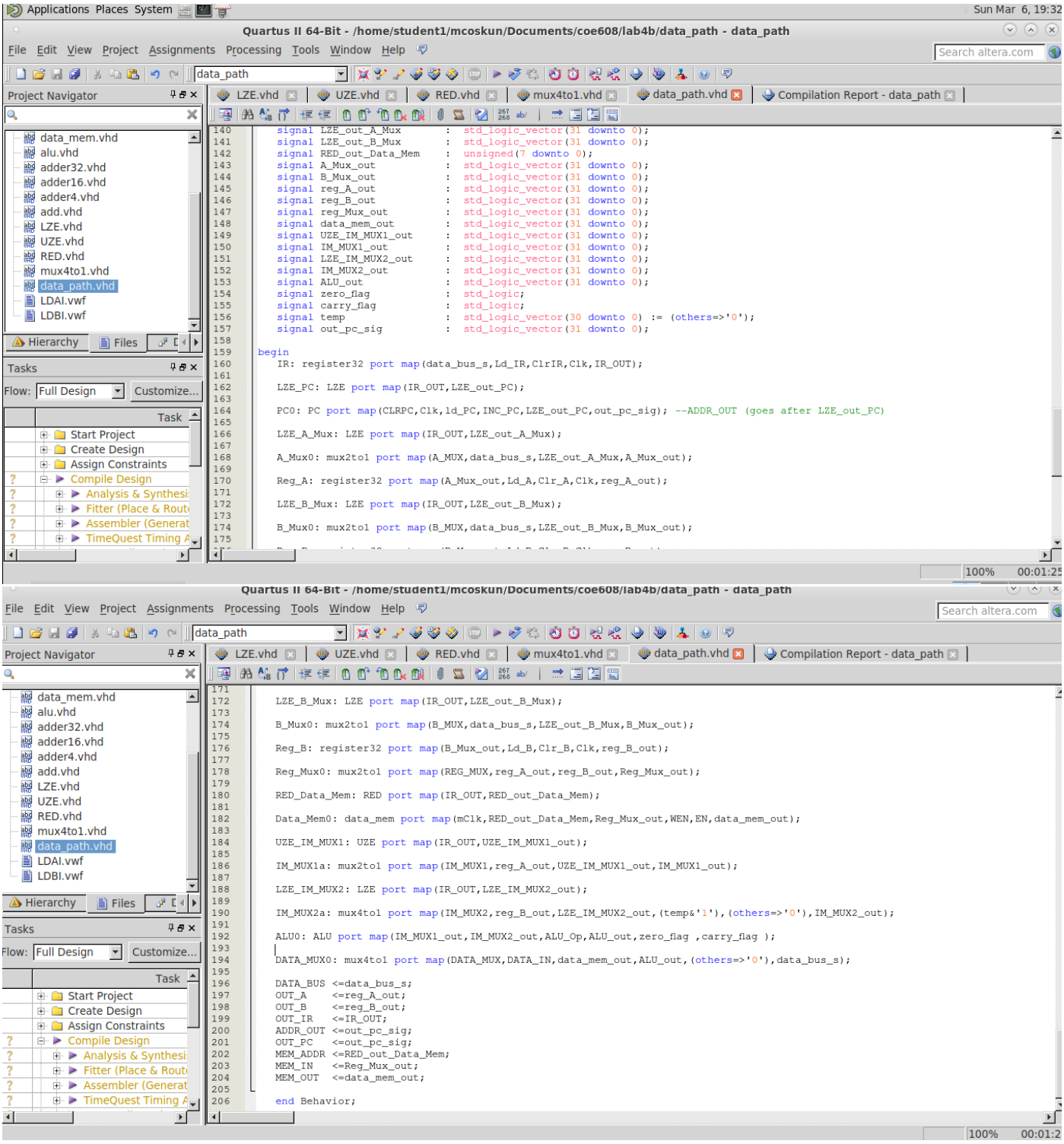
Assembler (Generat
TimeQuest Timing A
106);
107 end component;
108
109 --MUX2to1
110 component mux2to1 is
111 port(s : in std_logic;
112 w0,w1 : in std_logic_vector(31 downto 0);
113 f : out std_logic_vector(31 downto 0)
114);
115 end component;
116
117 --MUX4to1
118 component mux4to1 is
119 port(s : in std_logic_vector(1 downto 0);
120 X1,X2,X3,X4 : in std_logic_vector(31 downto 0);
121 f : out std_logic_vector(31 downto 0)
122);
123 end component;
124
125 --ALU
126 component alu is
127 port(a : in std_logic_vector(31 downto 0);
128 b : in std_logic_vector(31 downto 0);
129 op : in std_logic_vector(2 downto 0);
130 result : out std_logic_vector(31 downto 0);
131 zero : out std_logic;
132 cout : out std_logic
133);
134 end component;
135
136 --Signal Instantiations
137 signal IR_OUT : std_logic_vector(31 downto 0);
138 signal data_bus_s : std_logic_vector(31 downto 0);
139 signal LZE_out_PC : std_logic_vector(31 downto 0);
140 signal LZE_out_A_Mux : std_logic_vector(31 downto 0);
141 signal LZE_out_B_Mux : std_logic_vector(31 downto 0);
100%
00:01:25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adder16.vhd
adder4.vhd
add.vhd
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UZE.vhd
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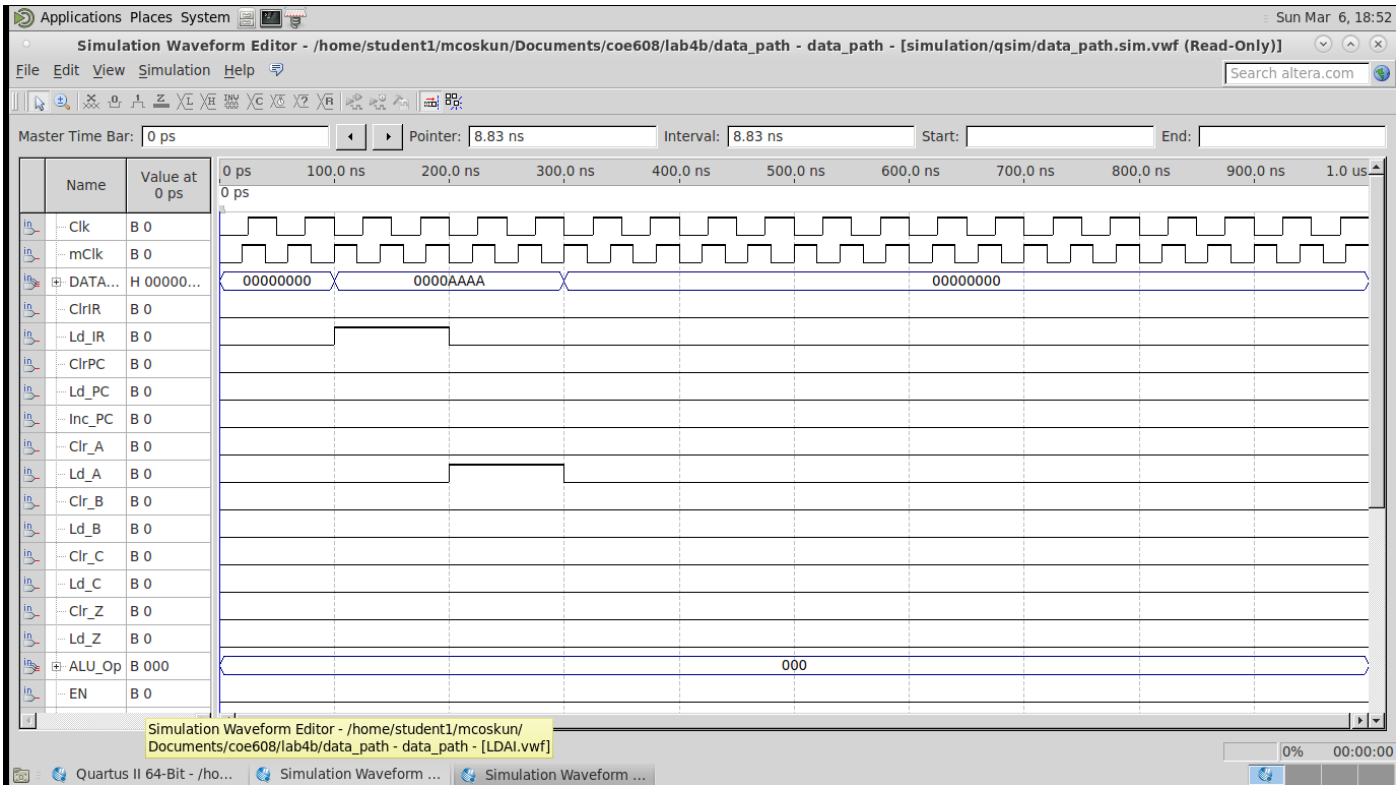
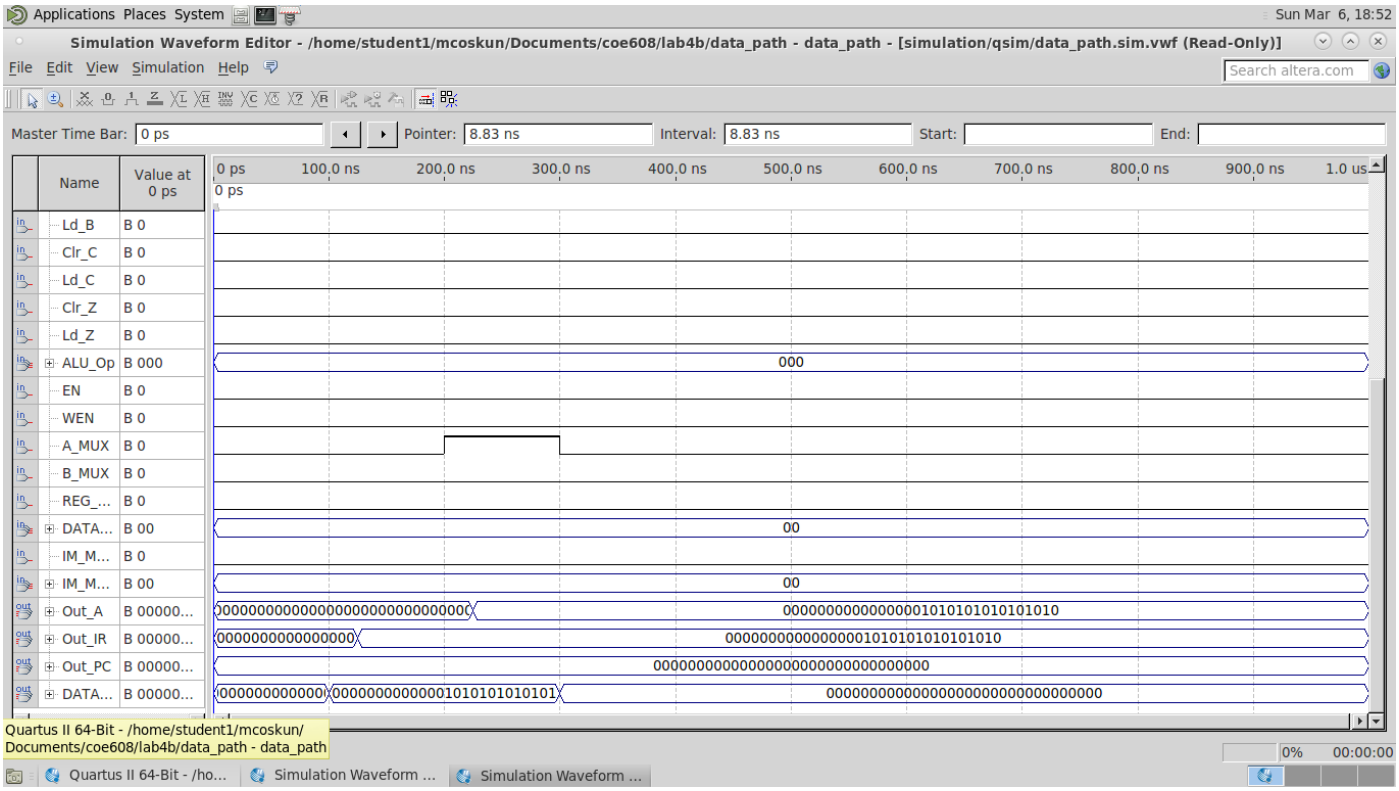
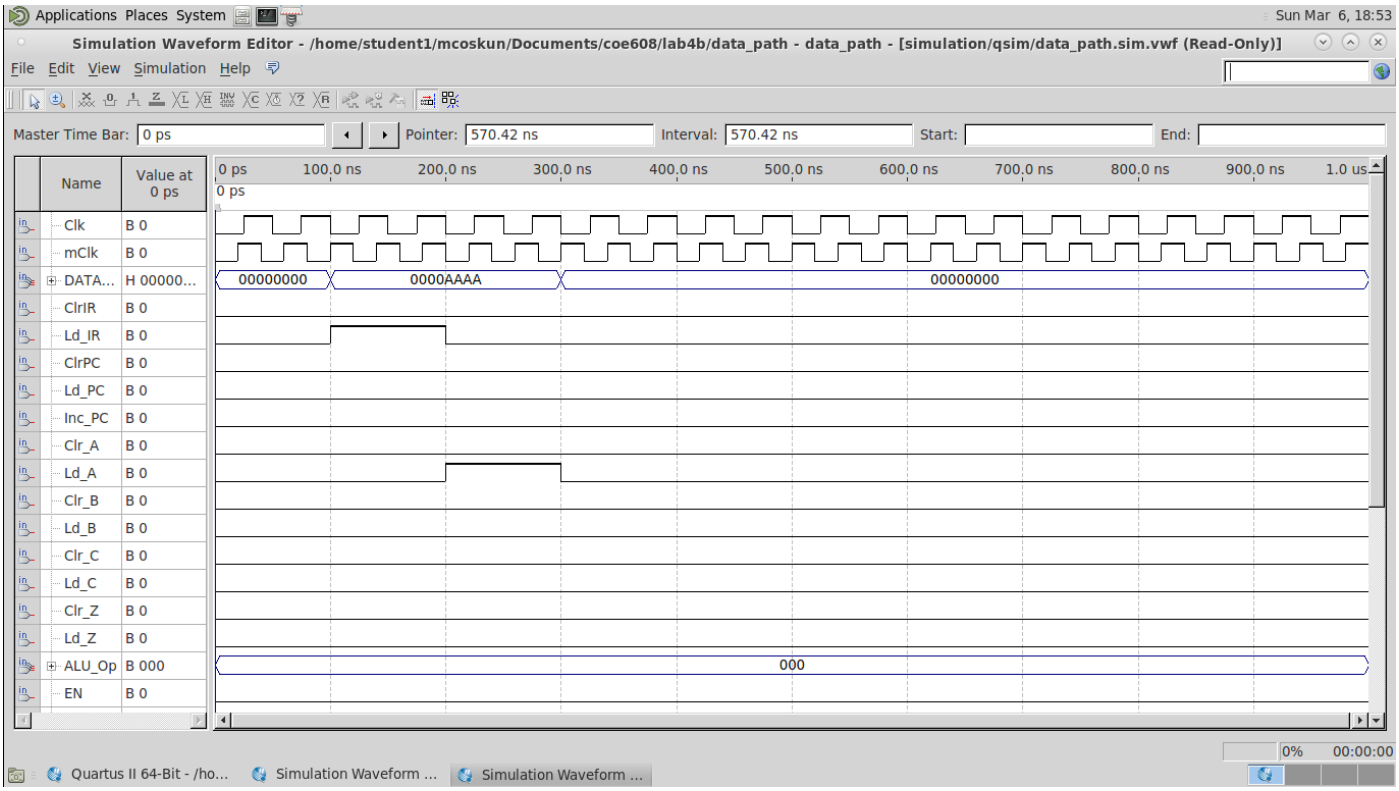
mux4to1.vhd
data_path.vhd
Compilation Report - data_path
140 signal LZE_out_A_Mux : std_logic_vector(31 downto 0);
141 signal LZE_out_B_Mux : std_logic_vector(31 downto 0);
142 signal RED_out_Data_Mem : unsigned(7 downto 0);
143 signal A_Mux_out : std_logic_vector(31 downto 0);
144 signal B_Mux_out : std_logic_vector(31 downto 0);
145 signal reg_A_out : std_logic_vector(31 downto 0);
146 signal reg_B_out : std_logic_vector(31 downto 0);
147 signal reg_Mux_out : std_logic_vector(31 downto 0);
148 signal data_mem_out : std_logic_vector(31 downto 0);
149 signal UZE_IM_MUX1_out : std_logic_vector(31 downto 0);
150 signal IM_MUX1_out : std_logic_vector(31 downto 0);
151 signal LZE_IM_MUX2_out : std_logic_vector(31 downto 0);
152 signal IM_MUX2_out : std_logic_vector(31 downto 0);
153 signal ALU_out : std_logic_vector(31 downto 0);
154 signal zero_flag : std_logic;
155 signal carry_flag : std_logic;
156 signal temp : std_logic_vector(30 downto 0) := (others=>'0');
157 signal out_pc_sig : std_logic_vector(31 downto 0);
158
159 begin
160 IR: register32 port map(data_bus_s,Ld_IR,ClrIR,Clk,IR_OUT);
161
162 LZE_PC: LZE port map(IR_OUT,LZE_out_PC);
163
164 PC0: PC port map(CLRPC,Clk,ld_PC,INC_PC,LZE_out_PC,out_pc_sig); --ADDR_OUT (goes after LZE_out_PC)
165
166 LZE_A_Mux: LZE port map(IR_OUT,LZE_out_A_Mux);
167
168 A_Mux0: mux2to1 port map(A_MUX,data_bus_s,LZE_out_A_Mux,A_Mux_out);
169
170 Reg_A: register32 port map(A_Mux_out,Ld_A,Clr_A,Clk,reg_A_out);
171
172 LZE_B_Mux: LZE port map(IR_OUT,LZE_out_B_Mux);
173
174 B_Mux0: mux2to1 port map(B_MUX,data_bus_s,LZE_out_B_Mux,B_Mux_out);
175
100%
00:01:25
Quartus II 64-Bit - /home/student1/mcoskun/Documents/coe608/lab4b/data_path - data_path
171
172 LZE_B_Mux: LZE port map(IR_OUT,LZE_out_B_Mux);
173
174 B_Mux0: mux2to1 port map(B_MUX,data_bus_s,LZE_out_B_Mux,B_Mux_out);
175
176 Reg_B: register32 port map(B_Mux_out,Ld_B,Clr_B,Clk,reg_B_out);
177
178 Reg_Mux0: mux2to1 port map(REG_MUX,reg_A_out,reg_B_out,Reg_Mux_out);
179
180 RED_Data_Mem: RED port map(IR_OUT,RED_out_Data_Mem);
181
182 Data_Mem0: data_mem port map(mClk,RED_out_Data_Mem,Reg_Mux_out,WEN,EN,data_mem_out);
183
184 UZE_IM_MUX1: UZE port map(IR_OUT,UZE_IM_MUX1_out);
185
186 IM_MUX1a: mux2to1 port map(IM_MUX1,reg_A_out,UZE_IM_MUX1_out,IM_MUX1_out);
187
188 LZE_IM_MUX2: LZE port map(IR_OUT,LZE_IM_MUX2_out);
189
190 IM_MUX2a: mux4to1 port map(IM_MUX2,reg_B_out,LZE_IM_MUX2_out,(temp&'1'),(others=>'0'),IM_MUX2_out);
191
192 ALU0: ALU port map(IM_MUX1_out,IM_MUX2_out,ALU_Op,ALU_out,zero_flag ,carry_flag);
193
194 DATA_MUX0: mux4to1 port map(DATA_MUX,DATA_IN,data_mem_out,ALU_out,(others=>'0'),data_bus_s);
195
196 DATA_BUS <=data_bus_s;
197 OUT_A <=reg_A_out;
198 OUT_B <=reg_B_out;
199 OUT_IR <=IR_OUT;
200 ADDR_OUT <=out_pc_sig;
201 OUT_PC <=out_pc_sig;
202 MEM_ADDR <=RED_out_Data_Mem;
203 MEM_IN <=Reg_Mux_out;
204 MEM_OUT <=data_mem_out;
205
206 end Behavior;
100%
00:01:2

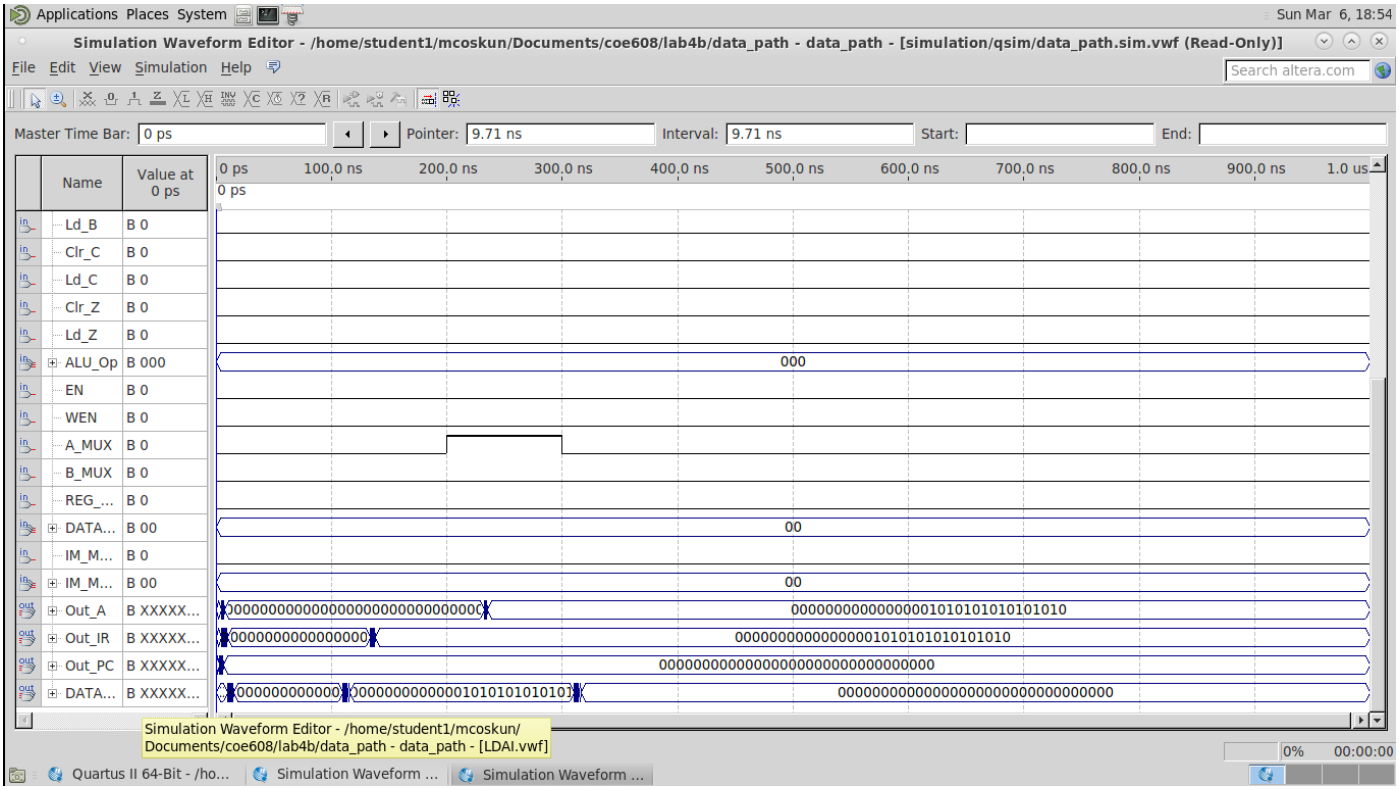
After compiling successfully, the waveform of the unit (LDAI) created following the lab manual is displayed below (function waveform).



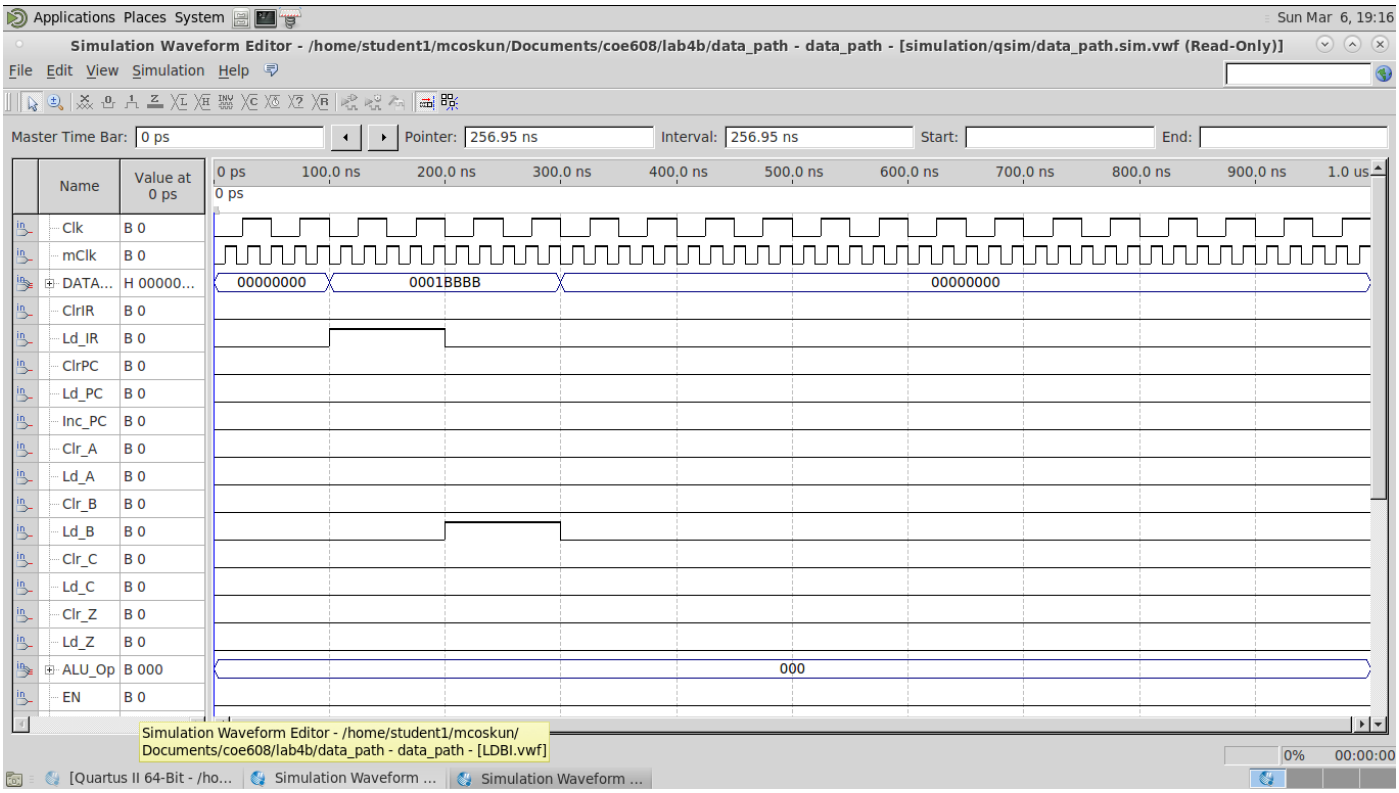


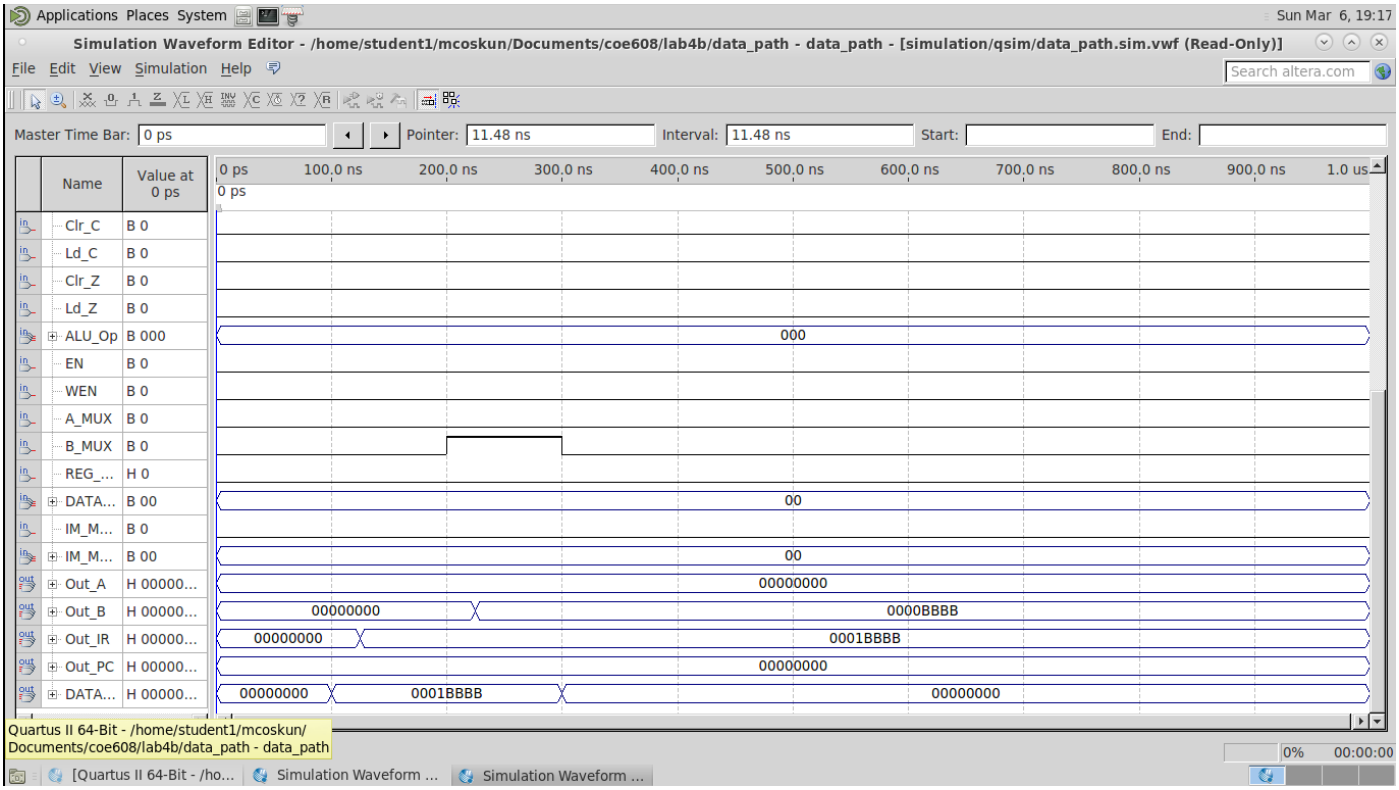
After compiling successfully, the waveform of the unit (LDAI) created following the lab manual is displayed below (timing waveform).



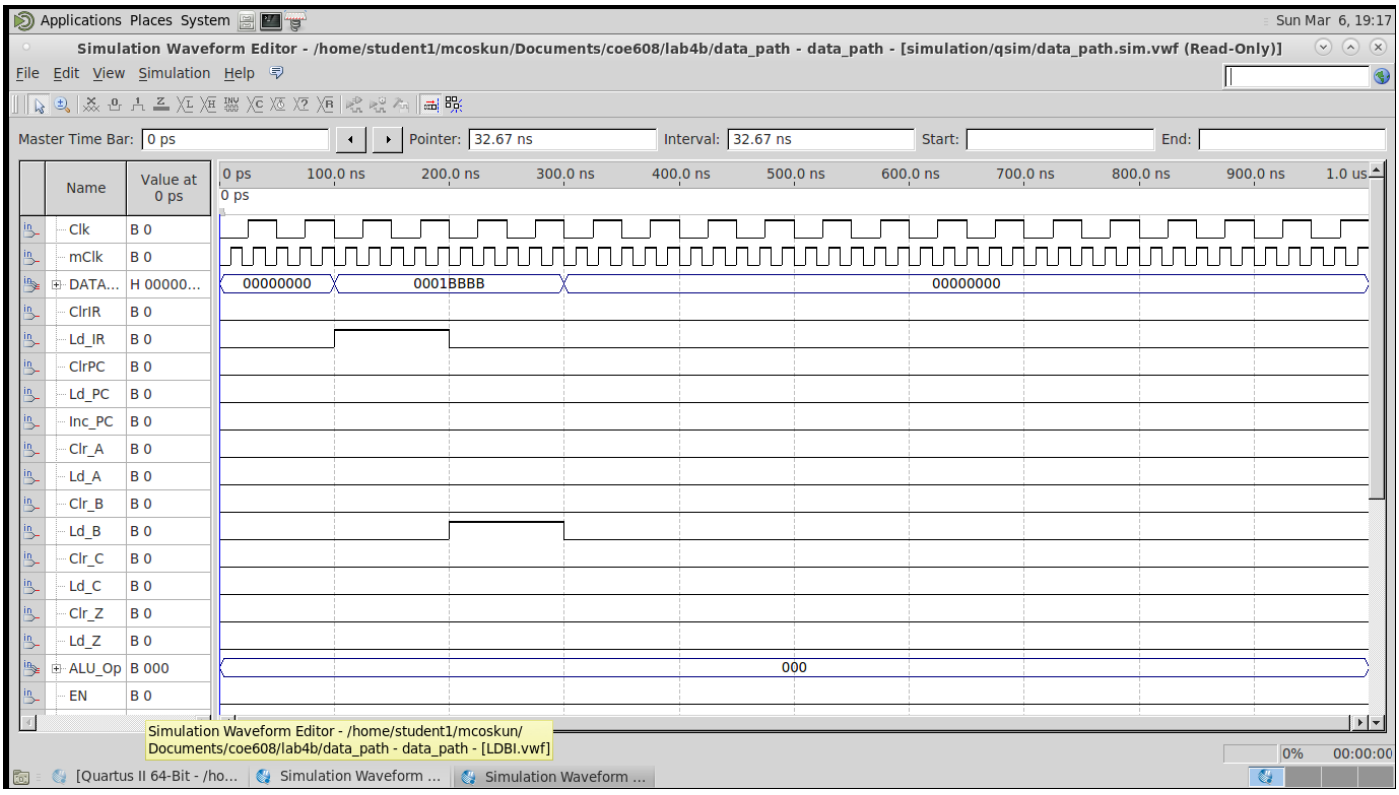


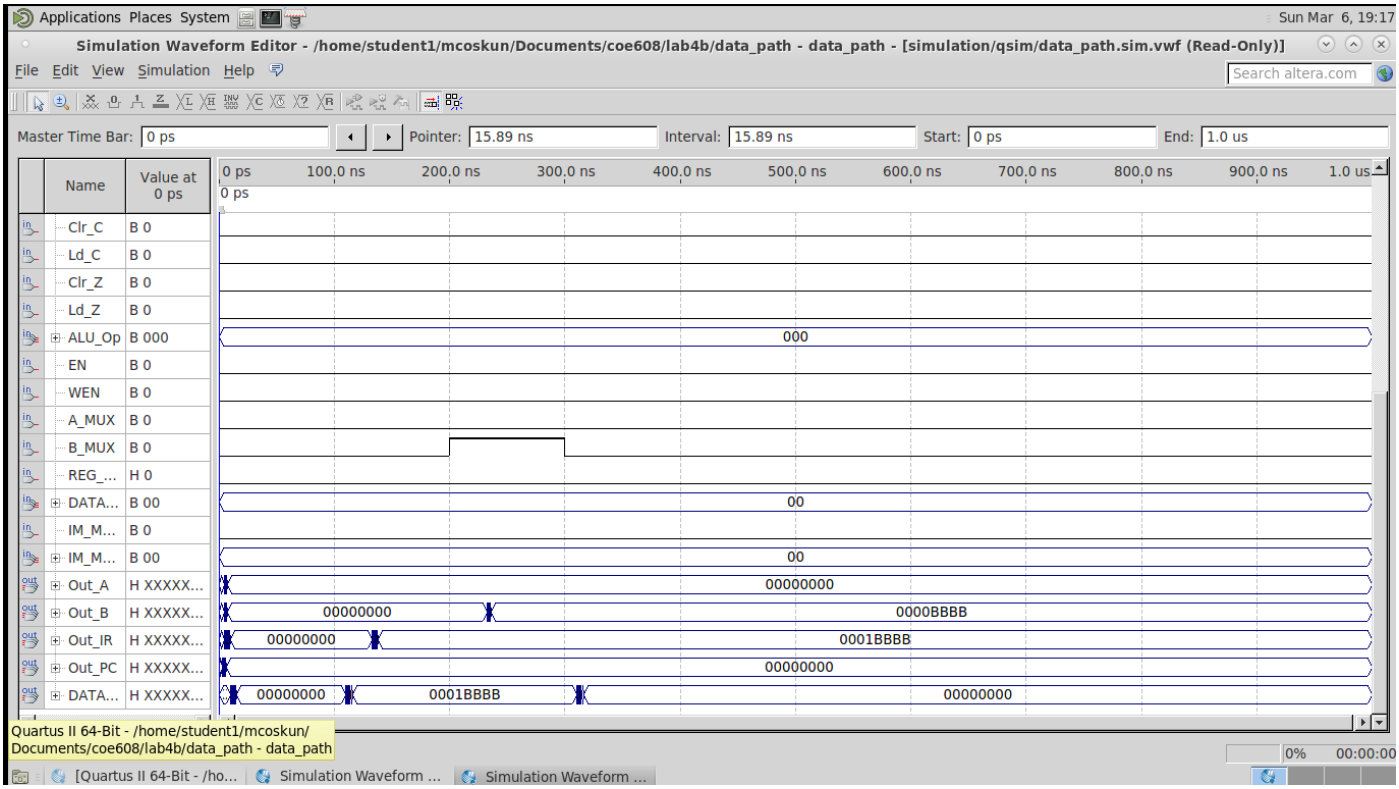
After compiling successfully, the waveform of the unit (LDBI) created following the lab manual is displayed below (function waveform).





After compiling successfully, the waveform of the unit (LDAI) created following the lab manual is displayed below (timing waveform).





Using “Table1: Supported Instructions and their Format” provided in the lab manual CPU_Specification1, the rest of the instructions has been applied and the table below has been filled accordingly.

Student Name: __Munevver Coskun__ Student#:__500923319__ Section: __06_

INST	**CLR_IR LD_IR**	**LD_PC INC_PC**	**CLR_A LD_A**	**CLR_B LD_B**	**CLR_C LD_C**	**CLR_Z LD_Z**	**ALU OP**	**EN WEN**	**A/B MUX**	**REG MUX**	**Data MUX**	**IM_MUX1 IM_MUX2**
LDA	0/0	0/0	0/1	0/0	0/0	0/0	XXX	1/0	0/X	X	01	X
LDB	0/0	0/0	0/0	0/1	0/0	0/0	XXX	1/0	X/0	X	01	X
STA	0/0	0/0	0/0	0/0	0/0	0/0	XXX	1/1	X	0	X	X
STB	0/0	0/0	0/0	0/0	0/0	0/0	XXX	1/1	X	1	X	X
JMP	0/0	1/0	0/0	0/0	0/0	0/0	XXX	X	X	X	X	X
LDAI	0/0	0/0	0/1	0/0	0/0	0/0	XXX	X	1/X	X	X	X
LDBI	0/0	0/0	0/0	0/1	0/0	0/0	XXX	X	X/1	X	X	X

LUI	0/0	0/0	0/1	1/0	0/0	0/0	001	X	0/X	X	10	1/X
ANDI	0/0	0/0	0/1	0/0	0/1	0/1	000	X	0/X	X	10	0/01
DECA	0/0	0/0	0/1	0/0	0/1	0/1	110	X	0/X	X	10	0/10
ADD	0/0	0/0	0/1	0/0	0/1	0/1	010	X	0/X	X	10	0/00
SUB	0/0	0/0	0/1	0/0	0/1	0/1	110	X	0/X	X	10	0/00
INCA	0/0	0/0	0/1	0/0	0/1	0/1	010	X	0/X	X	10	0/10
AND	0/0	0/0	0/1	0/0	0/1	0/1	000	X	0/X	X	10	0/00
ADDI	0/0	0/0	0/1	0/0	0/1	0/1	010	X	0/X	X	10	0/01
ORI	0/0	0/0	0/1	0/0	0/1	0/1	001	X	0/X	X	10	0/01
ROL	0/0	0/0	0/1	0/0	0/1	0/1	100	X	0/X	X	10	0/X
ROR	0/0	0/0	0/1	0/0	0/1	0/1	101	X	0/X	X	10	0/X
CLRA	0/0	0/0	1/0	0/0	0/0	0/0	XXX	X	X	X	X	X
CLRB	0/0	0/0	0/0	1/0	0/0	0/0	XXX	X	X	X	X	X
CLRC	0/0	0/0	0/0	0/0	1/0	0/0	XXX	X	X	X	X	X
CLRZ	0/0	0/0	0/0	0/0	0/0	1/0	XXX	X	X	X	X	X
PC <= PC+4	0/0	1/1	0/0	0/0	0/0	0/0	XXX	X	X	X	X	X
IR <= M[INST]	0/1	0/0	0/0	0/0	0/0	0/0	XXX	X	X	X	00	X
PC <= IR[15..0]	0/0	1/0	0/0	0/0	0/0	0/0	XXX	X	X	X	X	X

Table 1: Data-Path Control Signals

Questions:

1.It implements INCA by setting the values of the inputs of the components to the values of INCA. Using the given Table (Table1: Supported Instructions and their Format) for instructions of INCA, ADDI, LDBI, and LDA operations.

2.Means Max frequency at which the circuit can operate without any hazards or glitches. We find the average of fall and rise values in the compilation report and 1/ the average gives us frequency.

3. Average of fall and rise values of DATA BUS []. The answer is: 24.5255