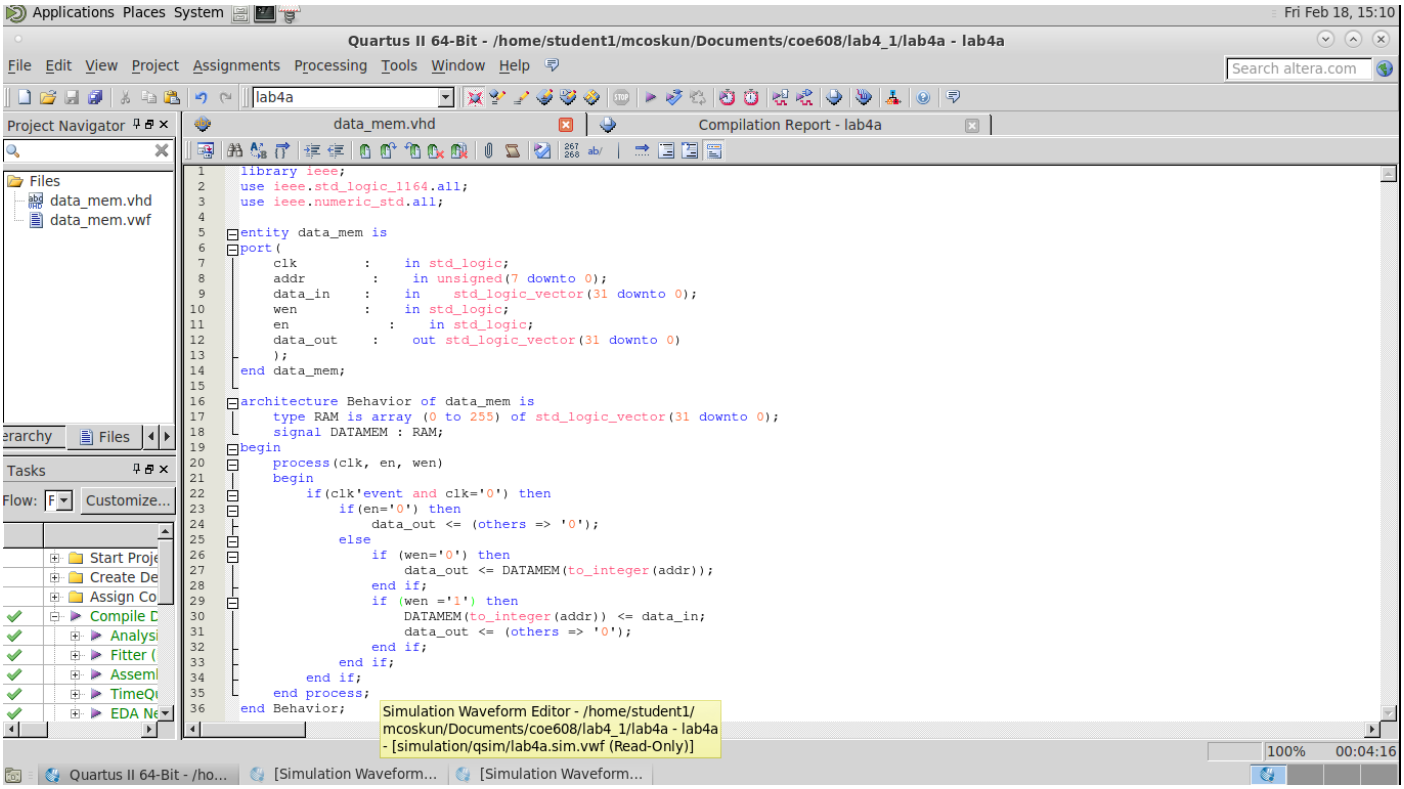
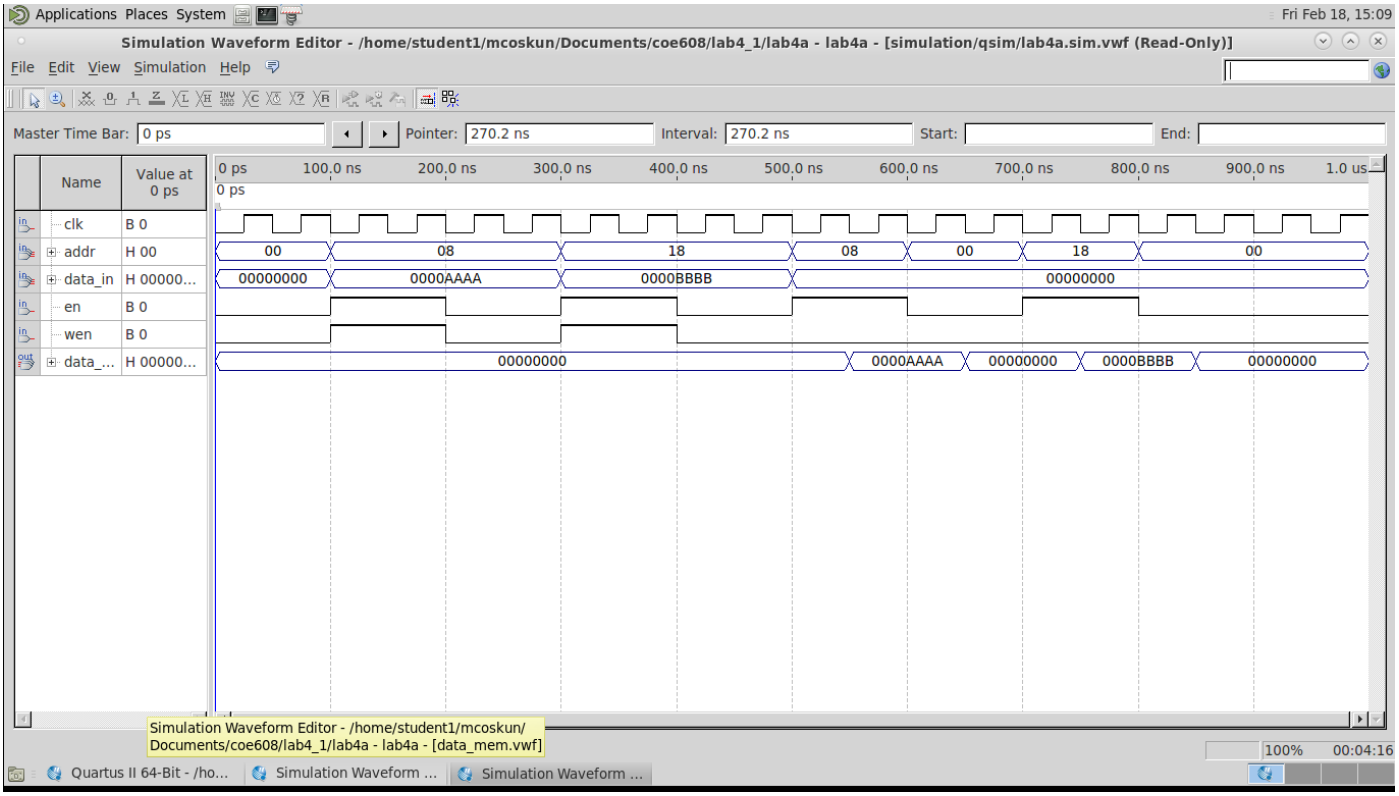
In this lab, we will be implementing a simple memory unit that can read and write within a clock cycle. The unit consists of 8 bit-address input (addr), 32 bit-data input and output (data_in and data_out), enable(en), write enable(wen), and clock(clk).

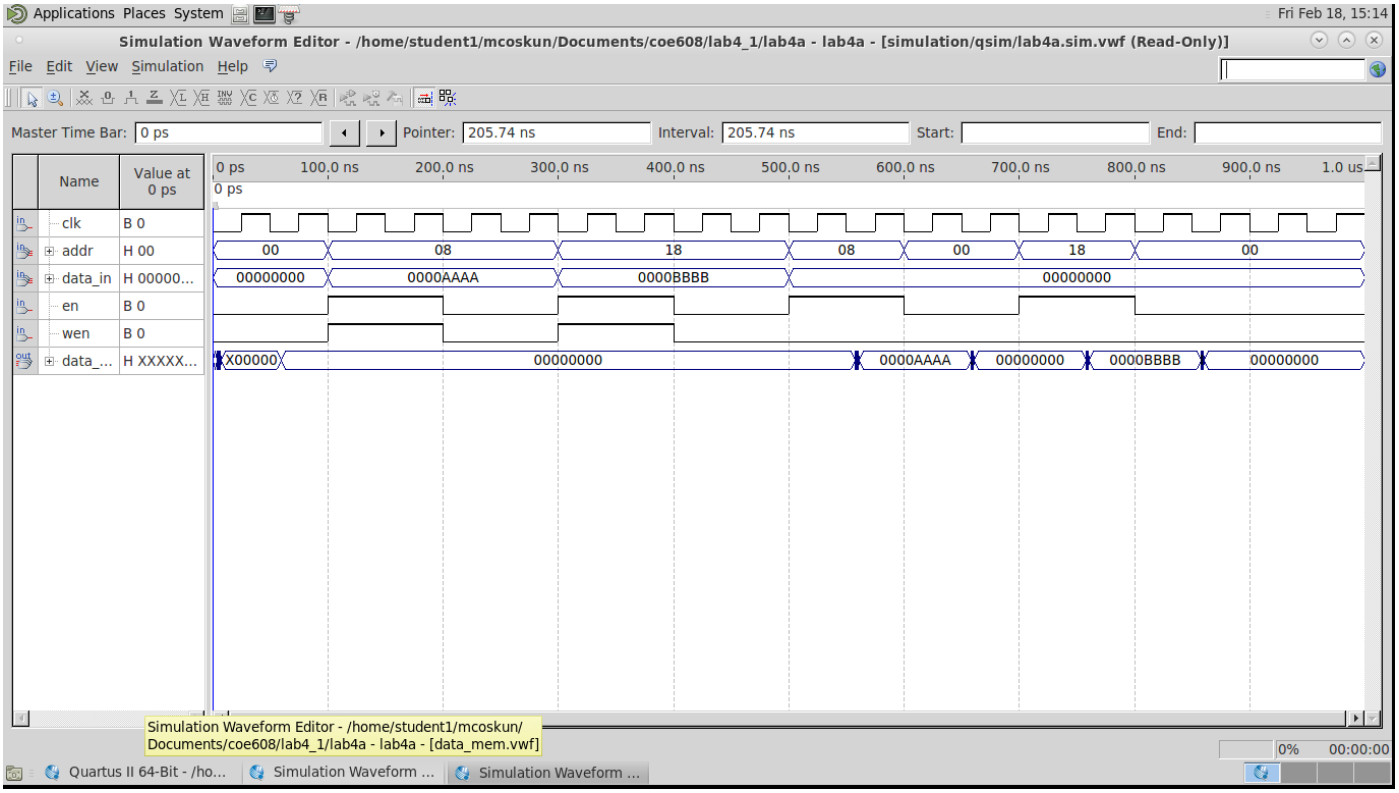
The VHDL code of the unit can be seen below.



After compiling successfully, the waveform of the unit created following the lab manual is displayed below (function waveform).



After compiling successfully, the waveform of the unit created following the lab manual is displayed below (timing waveform).



In order to find the worst-case delays for reads and writes of various inputs, we refer to the compilation report of lab4a, “TimeQuest Timing Analyzer>Multicorner Datasheet>Clock to Output Times” section. The average of data_out[*] Rise and Fall gives us an approximate for the worst-case scenario delays. In our case, it is 10.0065.