Sir Syed University of Engineering & Technology
Faculty of Computing & Applied Sciences
Department of Computer Science

Online End Semester Examinations (Fall 2020)

Course Title with Code	**CS-128 Digital Logic Design**	**Program**	BS(CS)
Instructor	**Chandanlal**	**Semester**	2nd
Start date & Time	November 14, 2020 at 10:30 AM	**Submission Deadline**	November 14, 2020 at 03:30 PM
Maximum Marks	**50**		

IMPORTANT INSTRUCTIONS:

Read the following Instructions carefully:

- Attempt All Questions on MS-Word. Font theme and size must be Times New Roman and 12 points respectively. Use line spacing 1.5. Convert file to PDF format before submitting.
- You may provide answers HANDWRITTEN. The scanned solution must be submitted in PDF file format (Use any suitable Mobile Application for Scanning)
- For Diagrams, you can use paper and share a clear visible snapshot in the same Answer Sheet.
- Arrange questions and their subsequent parts in sequence.
- Make sure that your answers are not plagiarized or copied from any other sources. In case of plagiarism, **ZERO** marks will be awarded.
- Provide relevant, original and conceptual answers, as this exam aims to test your ability to examine, explain, modify or develop concepts discussed during the course.
- Recheck your answer before the submission on **VLE** to correct any content or language related errors.
- You must upload your answers via the VLE platform ONLY.

You must follow general guideline for students before online examination and during online examination which had already been shared by email and WhatsApp.

This paper has a total of 03 pages including this title page

Sir Syed University of Engineering & Technology
Faculty of Computing & Applied Sciences
Department of Computer Science

Note:

- **Attach the scanned copy of University Student Card (both sides) with answer script**
- **Students must meet their submission deadline as there is no re-take or re-attempt after the deadline.**
- **Assume decimal number Z = (Your roll number + N), Where N = 128 (If roll number is from 1 to 100), N = 54 (If roll number is from 101 to 200), N = 14 (If roll number is greater than 200)**
- **Convert Z into eight bits binary equivalent for future utilization**

Q.1. (10)

(a) Apply the conversion rules on Z, and convert it into binary & hexadecimal numbers and vice versa.

(b) Find the 2's complement of Z and then with proper steps show it into floating point format.

Q.2. (10)

(a) Find standard SOP and POS equations of the following truth table. By using Boolean laws simplify both expressions. Where output X is equal to Z ,for 000 input condition(A,B,C) X is LSB of Z and put remaining values of Z in the output column accordingly till the MSB of Z for 111.

INPUTS			OUTPUT
A	**B**	**C**	**X**
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

(b) Draw the K-map for the above truth table and write down both Boolean expressions by grouping of ones and zeros separately. Which expression should be implemented and why? Also draw the logic diagram of that expression.

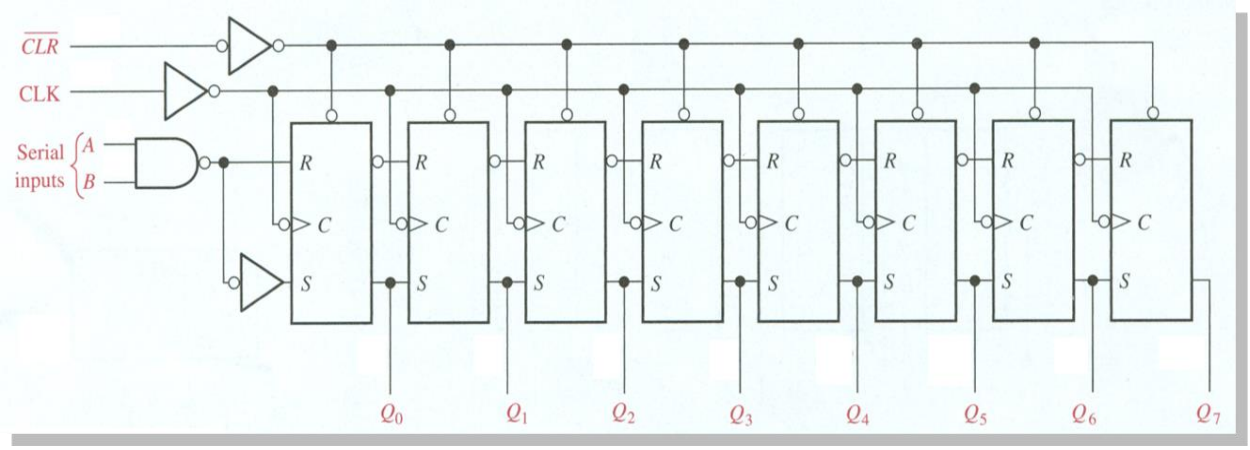
Sir Syed University of Engineering & Technology
Faculty of Computing & Applied Sciences
Department of Computer Science

Q.3. (10)

Separate the eight bits binary value of Z into two groups, each of four bits. Draw the circuit diagram with full adders to show the addition of these two numbers. Also draw and explain the circuit diagram of multiplexer used to multiplex the result of the adder.

Q.4. (10)

Remember positive edge triggered J K flip flop to draw the wave forms of clock, J, K and Q when J = Z and K is High. Also with the help of 8 bits serial-in parallel-out register as shown in the following diagram, show how the value of Z is loaded in the register. Initially register is clear.



Q.5. (10)

The register in Q4 requires 8 pulses to store the value of Z. Draw the circuit of asynchronous or synchronous counter used to count the pulses required for Z and then it should reset in next coming pulse. Show the counting procedure with the help of wave forms and binary numbers.