SIR SYED UNIVERSITY OF ENGINEERING & TECHNOLOGY
COMPUTER SCIENCE & INFORMATION TECHNOLOGY DEPARTMENT

SPRING 2021

MICROPROCESSOR & ASSEMBLY LANGUAGE (CS-330)

ASSIGNMENT # 01 SOLUTION

Semester: 5th — Batch: 2019
Due Date: 17th March, 2021 — Max Marks: 10

Instruction:

- Attempt all questions in a sequence.

1- Answer the following questions:

(a) How many nibbles are 16 bits?
Answer: 4 nibbles

(b) How many bytes are 32 bits?
Answer: 4 bytes

(c) If a word is defined as 16 bits, how many words is a 64-bit data item?
Answer: 4 words

(d) If a computer has a 32-bit data bus. What is the largest number that can be carried into the CPU at a time?
Answer: 4,294,967,295

(e) Regarding address bus, data bus and control bus, which is unidirectional and which is bidirectional?
Answer: Data Bus (Bidirectional), Address bus and Control bus (Unidirectional)

(f) Which section of CPU is responsible for performing addition?
Answer: ALU is responsible for all arithmetic and logical calculations.

2- Add the following hex values.

(a) 2CH + 3FH
Answer: 6BH

(b) F34H + 5D6H
Answer: 150AH

(c) 20000H + 12FFH
Answer: 2112FFH

(d) FFFFH + 2222H
Answer: 12221H

3- Subtract the following hex values.

(a) 24FH – 129H

Answer: 126H

(b) FE9H – 5CCH

Answer: A1DH

(c) 2FFFFH – FFFFFH

Answer: -D0000H

(d) 9FF25 – 4DD99H

Answer: 5218CH

4- Which of the following instructions cannot be coded in 8086 Assembly language? Give reason why not, if any.

(a) MOV AX, 27

Answer: It is legal.

(b) MOV AL, 97F

Answer: It is illegal, because the data item is of 12 bits.

(c) MOV DS, 9BF2

Answer: It is illegal, because immediate addressing is not possible in segment register.

(d) MOV CX, 397

Answer: It is legal.

(e) MOV SI, 9516

Answer: It is legal.

(f) MOV CS, 3490

Answer: It is illegal, because immediate addressing is not possible in segment register.

(g) MOV DS, BX

Answer: It is legal.

(h) MOV BX, CS

Answer: It is legal.

(i) MOV CH, AX

Answer: It is illegal, because destination is small in size.

(j) MOV AX, 23FB9

Answer: It is illegal, because data item is too large.

(k) MOV CS, BH

Answer: It is illegal, because the register sizes do not match.

(l) MOV AX, DL

Answer: It is illegal, because operand sizes do not match.

5- If CS = 3499H and IP = 2500H, find:
   (a) The logical address
   Answer: CS:IP = 3499:2500
   (b) The physical address
   Answer: PA = (CS x 10H) + IP = 34990 + 2500 = 36E90H
   (c) The lower and upper ranges of code segment
   Answer: Lower range of CS = 34990H and Upper range of CS = 4498FH

6- If DS = 1298H and offset is 3FB9H, find:
   (a) The physical address
   Answer: PA = (DS x 10H) + offset = 12980 + 3FB9 = 16939H
   (b) The logical address of the data being fetched
   Answer: 1298:3FB9
   (c) The lower and upper range addresses of the data segment
   Answer: Lower range of DS = 12980H and Upper range of CS = 2297FH

7- If an instruction that needs to be fetched is in physical memory location 389F2H and CS = 2700H, does the code segment range include it or not? If not, what value should be assigned to CS if the IP must equal 1282?
   Answer: No, because the upper range of this code segment is 36FFFH, CS should be 3777H for the given physical memory location 389F2H, if the IP is 1282H.

8- If SS = 2000H and SP = 4578H, find:
   (a) The physical address
   Answer: PA = (SS x 10H) + SP = 20000 + 4578 = 24578H
   (b) The logical address
   Answer: SS:SP = 2000:4578
   (c) The lower range of stack segment
   Answer: Lower range of SS = 20000H
   (d) The upper range of stack segment
   Answer: Upper range of SS = 2FFFFH

9- The following registers are used as offsets. Assuming that the default segment is used to get the logical address, give the segment register associated with each offset.
   (a) BP *Answer:* SS
   (b) DI *Answer:* DS or ES
   (c) SI *Answer:* DS or ES
   (d) IP *Answer:* CS
   (e) SP *Answer:* SS
   (f) BX *Answer:* DS or ES

10- Find the status of all conditional flags for the following operations:

(a) MOV AH, 9FH
ADD AH, 61H
Answer: CF = 1, PF = 1, AF = 1, ZF = 1, SF = 0, OF = 0

(b) MOV BL, 23H
ADD BL, 97H
Answer: CF = 0, PF = 0, AF = 0, ZF = 0, SF = 1, OF = 0

(c) MOV DX, 10FFH
ADD DX,1
Answer: CF = 0, PF = 1, AF = 1, ZF = 0, SF = 0, OF = 0

11- Assume that the registers have the following values (all in hex) and that CS = 1000, DS = 2000, SS = 3000, SI = 4000, DI = 5000, BX = 6080, BP = 7000, AX = 25FF, CX = 8791 and DX = 1299. Calculate the physical address of the memory where the operand is stored and the contents of the memory locations in each of the following addressing examples:

(a) MOV [SI], AL
Answer: PA = (DS x 10H) + SI = 20000 + 4000 = 24000H (FF)

(b) MOV [SI+BX+8], AH
Answer: PA = (DS x 10H) + SI + BX + 8 = 20000 + 4000 + 6080 + 8 = 2A088H (25)

(c) MOV [BX], AX
Answer: PA = (DS x 10H) + BX = 20000 + 6080 = 26080 (FF) and 26081 (25)

(d) MOV [DI+6], BX
Answer: PA = (DS x 10H) + DI + 6 = 20000 + 5000 + 6 = 25006 (80) and 25007 (60)

(e) MOV [3600], AX
Answer: PA = (DS x 10H) + 3600 = 20000 + 3600 = 23600 (FF) and 23601 (25)

(f) MOV [BP]+200, AX
Answer: PA = (SS x 10H) + BP +200 = 30000 + 7000 + 200 = 37200 (FF) and 37201 (25)

12- Give the addressing mode for each of the following commands:

(a) MOV AX, DS
Answer: Register addressing mode

(b) MOV CX, [3000]
Answer: Direct addressing mode

(c) MOV [BP]+6, AL
Answer: Based relative addressing mode

(d) MOV BX, 5678H
Answer: Immediate addressing mode

(e) MOV AL, [BX]

Answer: Register Indirect addressing mode

(f) MOV [DI], BX

Answer: Register indirect addressing mode

(g) MOV DX, [BX][DI]+200

Answer: Based Indexed relative addressing mode

(h) MOV [2348], DX

Answer: Direct addressing mode

(i) MOV [BX+SI+50], AH

Answer: Based Indexed relative addressing mode

(j) MOV [SI+60], AL

Answer: Indexed relative addressing mode