

SCSR1013 DIGITAL LOGIC

MODULE 3: LOGIC GATES

FACULTY OF COMPUTING



Module 3: Overview

NOT Gate (Inverter)

AND Gate

OR Gate

NAND Gate

NOR Gate

Exclusive-OR (XOR) Gate

Exclusive-NOR (XNOR) Gate



- For each gates, we will emphasize on the following:
 - Characteristics
 - ii. Symbols
 - iii. Operator
 - iv. Boolean expression
 - v. Truth Table
 - vi. Timing Diagram

Outline

two logic values either 0 or 1.

- NOT Gate (Inverter)
- AND Gate
- OR Gate
- NAND Gate
- NOR Gate
- Exclusive-OR (XOR) Gate
- Exclusive-NOR (XNOR) Gate

Basic building block

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Universal gate using 2 of the basic gates



NOT Gate

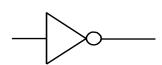
NOT Gate (Inverter)

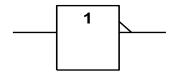
Characteristics

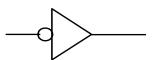
Performs inversion or complementation

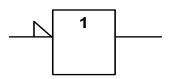
- Changes a logic level to the opposite
- 0(LOW) → 1(HIGH); 1 → 0

Symbols:









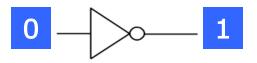
(a) Distinctive shape symbols with negation indicators

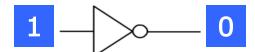
(b) Rectangular outline symbols with polarity indicators

Example:

"Output will be 0 if the input is 1"

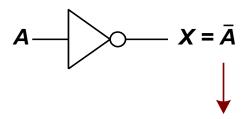
"Output will be 1 if the input is 0"







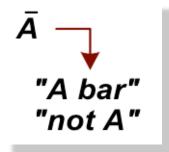
- Operator
 - NOT Gate is represented by overbar
- Logic expression



X is the complement of A

X is the inverse of A

X is NOT A

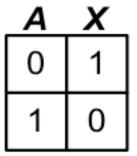


$$X = \bar{A}$$
 or $X = A'$

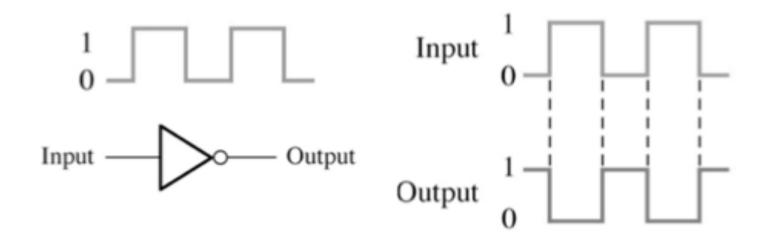
OUTPUT is the complement of INPUT
OUTPUT is the inverse of INPUT
OUTPUT is NOT INPUT



Truth table



Timing diagrams





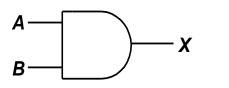
AND Gate

wwi

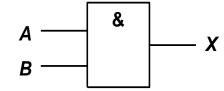
Characteristics

- Performs 'logical multiplication'
 - If all of the input are HIGH, then the output is HIGH.
 - If any of the input are LOW, then the output is LOW.
 - AND gate must at least have two (2) INPUTs, and must always have 1 (one) OUTPUT. The AND gate can have more than two INPUTs

Symbols



(a) Distinctive shape



(b) Rectangular outline with the AND (&) qualifying symbol



Operator

$$0.0 = 0$$

$$0.1 = 0$$

$$1.0 = 0$$

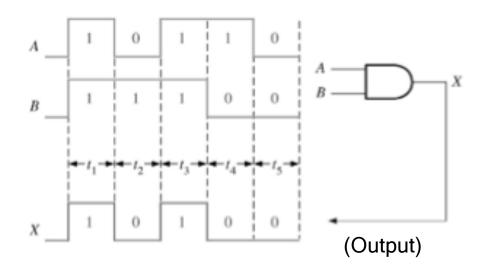
Logic operation

$$X = A \bullet B$$

Truth table

A B	$X = A \cdot B$
0 0	0
0 1	0
1 0	0
1 1	1

• Timing Diagram





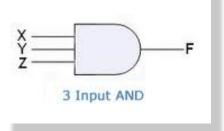


Exercise 3.1:

- (a) Develop the truth table for a 3-input AND gate.
- (b) Determine the total number of possible input combinations for a 4-input AND gate.

Solution:

(a) Possible input combinations = $2^3 = 8$



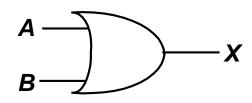
(b) Possible input combinations $= 2^4 = 16$

INPUTS			OUTPUT
Α	В	С	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

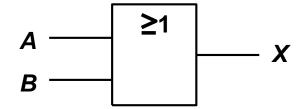
(Output 1 when all inputs 1)



- Performs 'logical addition'
 - If any of the input are HIGH, then the output is HIGH.
 - If <u>all</u> of the input are LOW, then the output is LOW
- Symbols used:



(a) Distinctive shape



(b) Rectangular outline with the OR (≥1) qualifying symbol



Operator

OR operator can be represented by a plus sign "+"

OR gate performs Boolean addition

Boolean addition follows the basic rules as follows:

$$0 + 0 = 0$$

$$0 + 1 = 1$$

$$1 + 0 = 1$$

$$1 + 1 = 1$$

Logical Expression

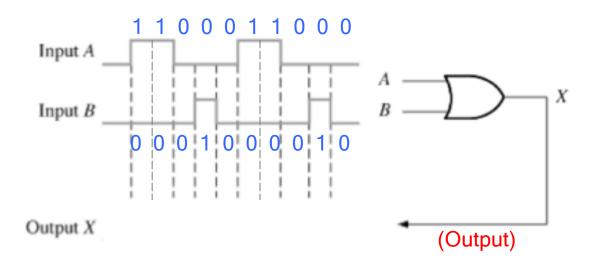
$$X = A + B$$



Truth Table

A B X = A + B 0 0 0 1 1 1 0 1 1

Timing Diagram (DIY)



Exercise 3.2:

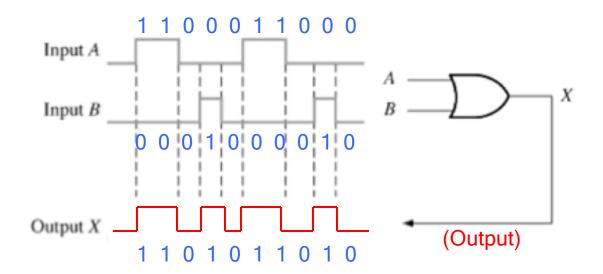
Draw the output waveform.



Truth Table

A B X = A + B 0 0 0 1 1 1 0 1 1

Timing Diagram (DIY)





Extera

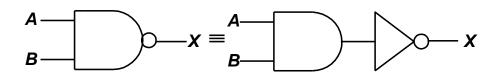
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Self-Test:

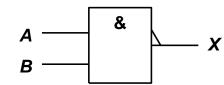
- a) Input of a NOT gate is A. If A is LOW, the output is HIGH
- b) If all inputs of an AND gate are LOW, then the output is LOW
- c) If any input of an OR gate is LOW, then the output is HIGH
- d) If A = HIGH, B = LOW, is the logical operation $X = A \bullet B = A + B$ true? NO
- e) From d), what we can do to get X = HIGH ? Invert B
- f) Rewrite the new logical operation from e): $X = A \cdot \overline{B} = A + \overline{B}$



- NAND → NOT-AND ⇒ combines the AND gate and an inverter
- Used as a universal gate
 - Combinations of NAND gates can be used to perform AND, OR and inverter operations
 - If <u>all or any</u> of the input are <u>LOW</u>, then the output is <u>HIGH</u>.
 - If <u>all</u> of the input are HIGH, then the output is LOW
- Symbol used:



(a) Distinctive shape: 2 input NAND gate and its NOT/AND equivalent



(b) Rectangular outline: 2 input NAND gate with polarity indicator



Operator

NAND operator can be represented by a dot with an overbar symbol

$$\overline{0.0} = \overline{0} = 1$$

$$\overline{0.1} = \overline{0} = 1$$

$$\overline{1.0} = \overline{0} = 1$$

$$\overline{1.1} = \overline{1} = 0$$

Logical Expression

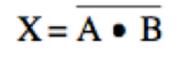
$$X = \overline{A \bullet B}$$

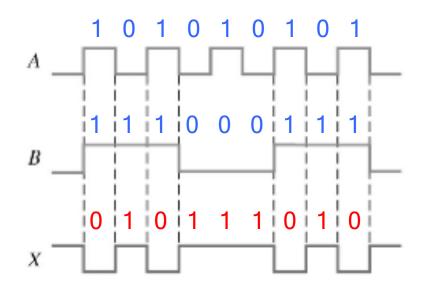
Truth Table

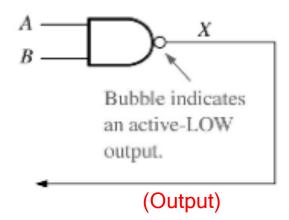
INPUTS		ОИТРИТ	
Α	В	AB	\rightarrow $\overline{AB} = X$
0	0	0	$\overline{0.0} = \overline{0} = 1$
0	1	0	$\overline{0.1} = \overline{0} = 1$
1	0	0	$\overline{1.0} = \overline{0} = 1$
1	1	1	$\overline{1.1} = \overline{1} = 0$



Timing Diagram (DIY)





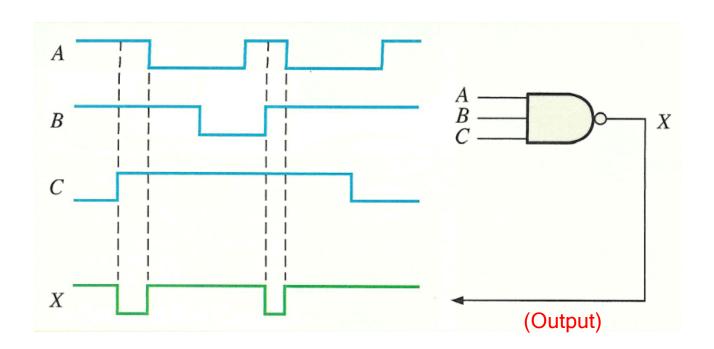






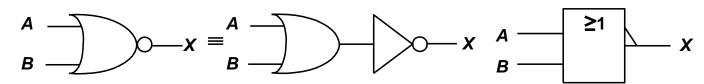
Exercise 3.3:

Show the output waveform for the 3-input NAND gate below with its proper time relationship to the inputs.





- NOR → NOT-OR ⇒combines the OR gate and an inverter
- Used as a universal gate
 - Combinations of NOR gates can be used to perform AND, OR and inverter operations
 - If <u>all or any</u> of the input are HIGH, then the output is LOW.
 - If <u>all</u> of the input are <u>LOW</u>, then the output is <u>HIGH</u>
- Symbol used:



(a) Distinctive shape: 2 input NOR gate and its NOT/OR equivalent

(b) Rectangular outline with the OR (≥1) qualifying symbol



Operator

NOR operator can be represented by a plus with an overbar symbols

$$\overline{0+0} = \overline{0} = 1$$

$$\overline{0+1} = \overline{1} = 0$$

$$\overline{1+0} = \overline{1} = 0$$

$$\overline{1+1} = \overline{1} = 0$$

Logical Expression

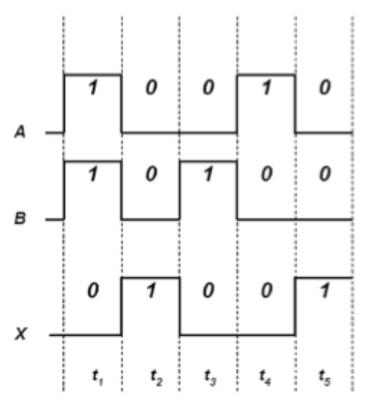
$$X = \overline{A + B}$$

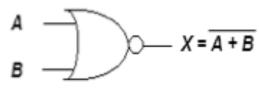
Truth Table

INPUTS		OUTPUT		
	Α	В	A + B	$\rightarrow \overline{A+B}=X$
_	0	0	0	$\overline{0+0} = \overline{0} = 1$
	0	1	1	$\overline{0+1} = \overline{1} = 0$
	1	0	1	$\overline{1+0} = \overline{1} = 0$
	1	1	1	$\overline{1+1} = \overline{1} = 0$



Timing Diagram (DIY)



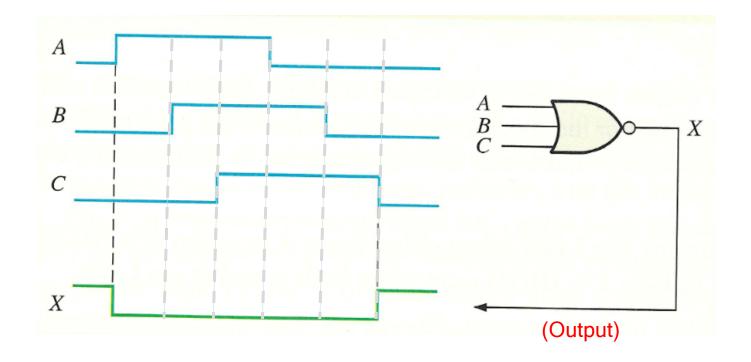






Exercise 3.4:

Show the output waveform for the 3-input NOR gate below with its proper time relationship to the inputs.



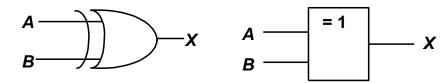
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XOR Gate

Characteristics

- Combines basic logic circuits of AND, OR and Inverter.
- Has only 2 inputs
- Used as a universal gate
 - Can be connected to form an adder that allows a computer to do perform addition, subtraction, multiplication and division in ALU (Arithmetic and Logic Unit).
 - If <u>both</u> of the input are at the <u>same logic level</u>, then the output is LOW.
 - If <u>both</u> of the input are at <u>opposite logic levels</u>, then the output is HIGH

Symbol



- (a) Distinctive shape
- (b) Rectangular outline



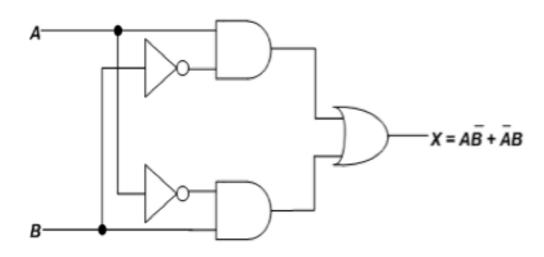
Operator

XOR operator can be represented by a \oplus symbol

Logical Expression

$$X = A \oplus B$$

= $AB + AB$



XOR is a combination of 2 AND gates, 1 OR gate, and 2 NOT gates (inverter)

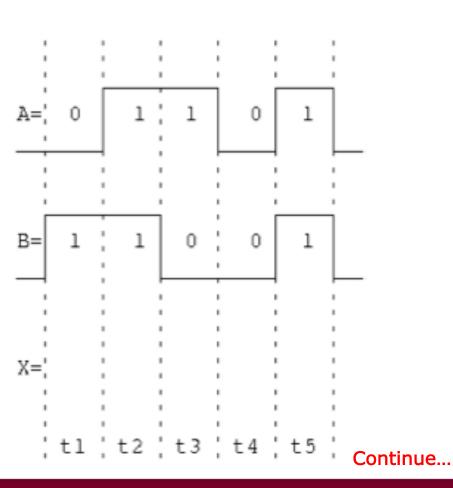


Truth Table

Α	В	X	$=AB+\overline{A}B$
0	0	0	•
0	1	1	
1	0	1	
1	1	0	
	0	0 0 0 1	0 0 0 0 1 1 1 0 1

X-OR truth table

Timing Diagram (DIY)

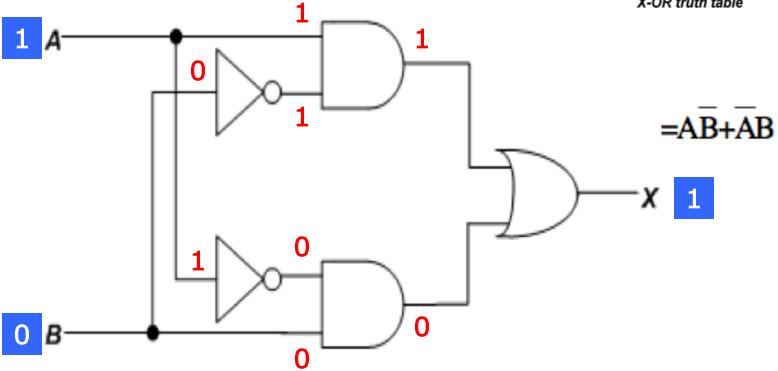




Truth Table

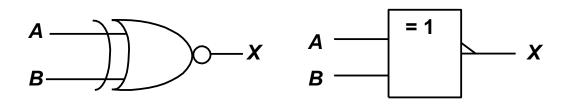
Α	В	X
0	0	0
0	1	1
1	0	1
1	1	0

X-OR truth table





- Has only 2 inputs, but output of XNOR is the opposite of XOR
 - If <u>both</u> of the input are at the <u>same logic level</u>, then the output is HIGH.
 - If both of the input are at opposite logic levels, then the output is LOW.
- Symbol used:



(a) Distinctive shape

(b) Rectangular outline



Operator

XNOR operator can be represented by a ⊙ symbol

Logical Expression

$$X = A \odot B$$

$$= \overline{A \oplus B}$$

$$= A\overline{B} + \overline{A}B$$

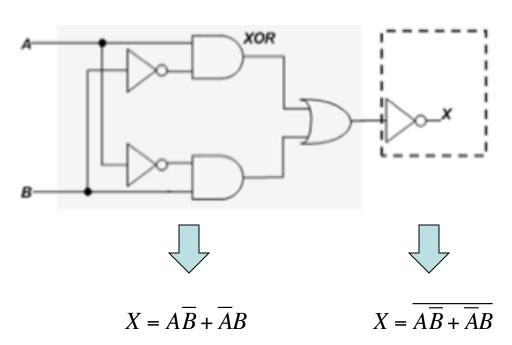
$$= AB + \overline{A}B$$



XNOR Implementation

- There are two ways in implementing XNOR Gate:
 - The first implementation by complementing (inverting)
 XOR circuit

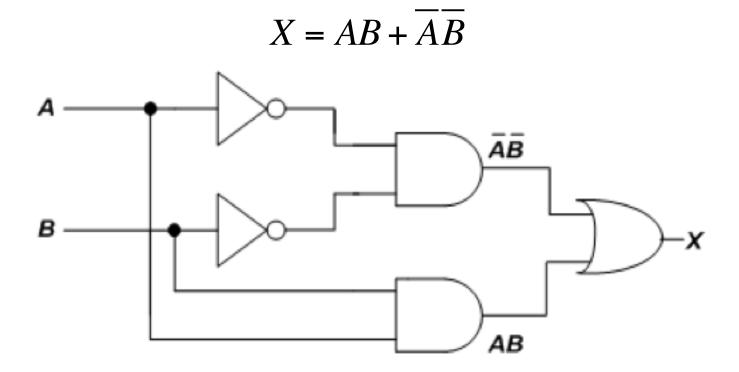
1





Second implementation is by directly implementing the following expression:

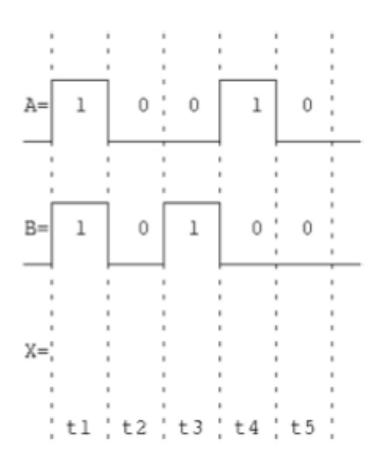
2





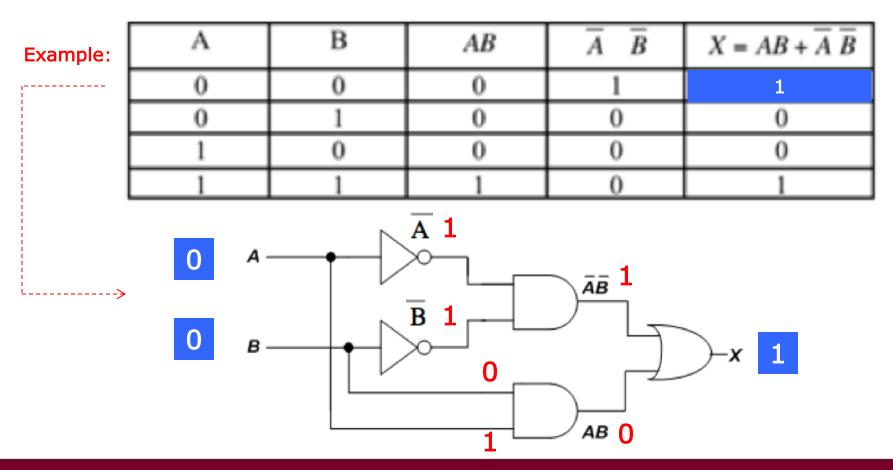
Truth Table

Timing Diagram (DIY)





The characteristic of the above circuit can be proven by the following truth table







Exercise 3.5:

Determine the output waveforms for the XOR gate and XNOR gate, given the input waveforms, A and B.

