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Project Digital Logic

Network Packet Transmission Monitoring System

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2024/2025-1

FACULTY OF COMPUTING

This project is to implement knowledge gained from this course by simulating the real case outside classroom.

Strategies used:

- Group self explore
- Creative problem solution and design
- Good idea solution, presentation, reporting & demo session

Requirement for Conducting Project

- Form a group consists of max 4 students
- Understand the case study
- Design the circuit. Show the details design in Project Report
- Prepare Project Report
  - Show the details design in Project Report
- Prepare project slide presentation and present the project
  - Convert the project report to presentation format
  - Each member's should take part in presentation
  - Offline video recording
- Demo the circuit (show and test the result)
  - Offline video recording
- Submit in e-learning
  - Project Report
  - Presentation Slide
  - Video recording (use youtube to publish (private link))- share the link
  - Complete Deeds Circuit

Due Date:

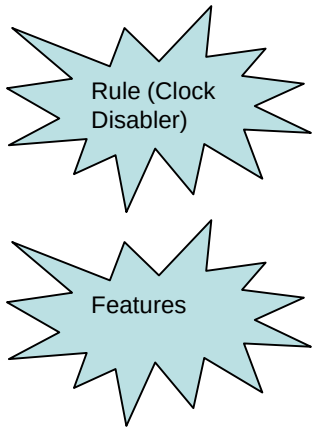
Study week or
3 days after final date
Discuss with your lecturer
(To be advise later)

Case study Scenario

- A group of computer in Lab 1 are connected to a group of computer in Lab 2 via one cable.
- We want to transmit a number of packet data (define from user) from one source of computer in Lab 1 to another destination computer in Lab 2.
- Refer Figure 1 and Figure 2.
- Design and simulate circuit to execute the packet transmission using Deeds. Consider the following components function in your circuit design
  - Connection computers from Lab 1 and lab 2
    - MUX and DEMUX
  - Count up counter Function
    - Asynchronous or Synchronous counter
    - JK/D/T flip-flop
  - Comparator Function
    - Comparator Module/XOR/XNOR
  - Clock Enabler Function
    - AND gate/NAND gate
  - Monitoring Packet transfer Function
    - Mux/Demux/Decoder/Basic gate (or other suitable method)
  - Display Controller (Fun Concept) Function
    - Use Demux (to alternate Vcc Input to the Display Component)
  - Monitoring Fault Detection (advanced - optional)
    - Mux/Demux/Decoder/Basic gate (or other suitable method)

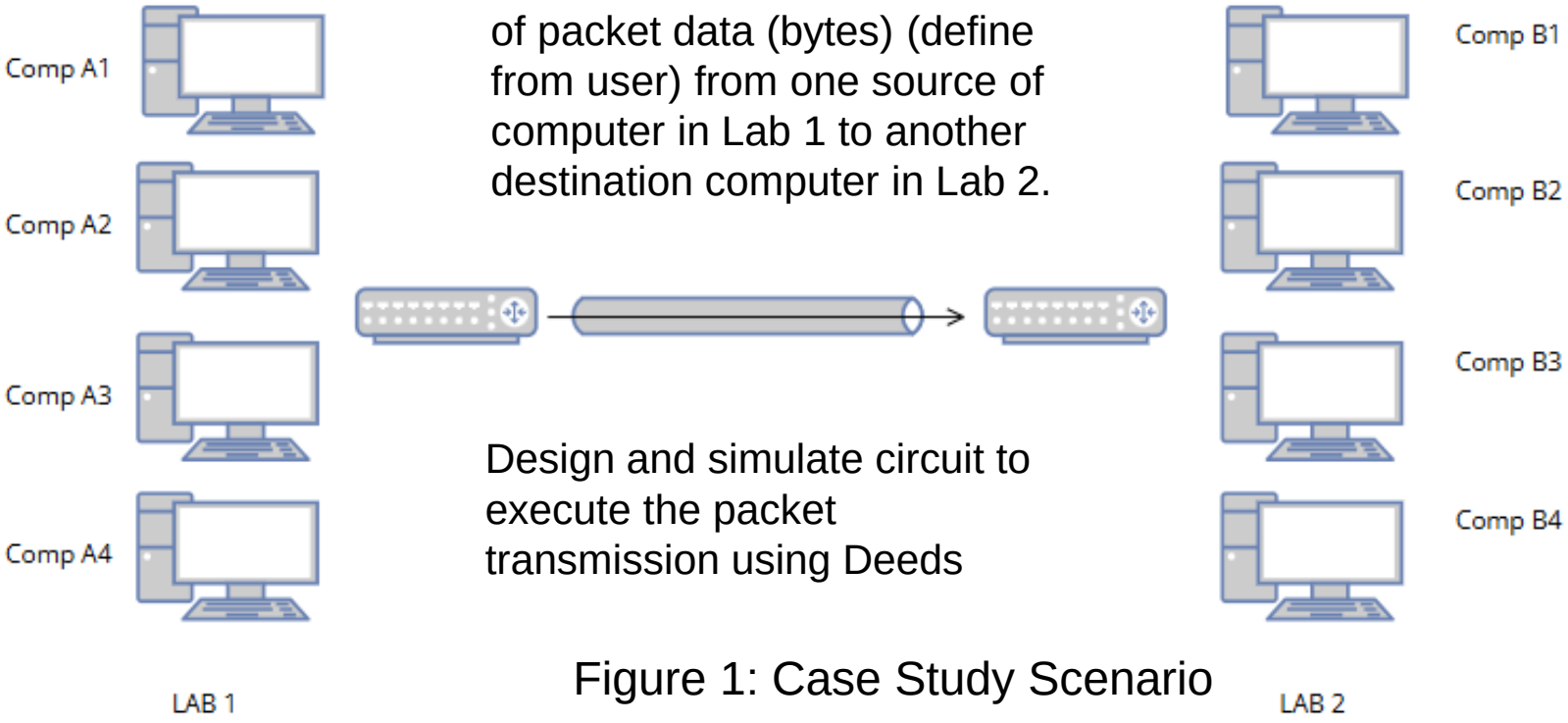
Basic

Advance



Network Packet Transmission Monitoring System

We want to transmit a number of packet data (bytes) (define from user) from one source of computer in Lab 1 to another destination computer in Lab 2.



Design and simulate circuit to execute the packet transmission using Deeds

Figure 1: Case Study Scenario

Understand Design & Operational Work: Basic and Advance

Basic Components and Connection

Basic Operational Design

Advance Features:

- More rule for clock enabler, such as:
  - set correct Password
  - set Full Duplex mode
  - others
- Monitor other extra status
- Fun Display Info
- Others

Component Design: Mux, Demux, Basic Gate, Flip-flops, Comparator, Decoder (depend on ideas/creativities)

Basic Operation:

1. Power On the Computer
2. Change Counter to Synchronous Mode and Reset the counter
3. Fulfill the Clock Enabler Condition
   - Power_ON
   - set Source Comp A (Lab A) and Destination Comp B (Lab B)
   - set Max packet (byte) transfer
   - simulate data to be transferred (e.g. by activating clock)
   - set start/ready button
   - activate clock edge by edge (by using push button)

   (check the condition (rule) in the circuit design to enable the counter)

4. Run simulation byte transfer by showing each clock change (use push button)

5. Monitor dashboard to check status transfer
   - Power_ON (OK)
   - Counter (OK)

Architecture of Network Packet Transmission Monitoring System

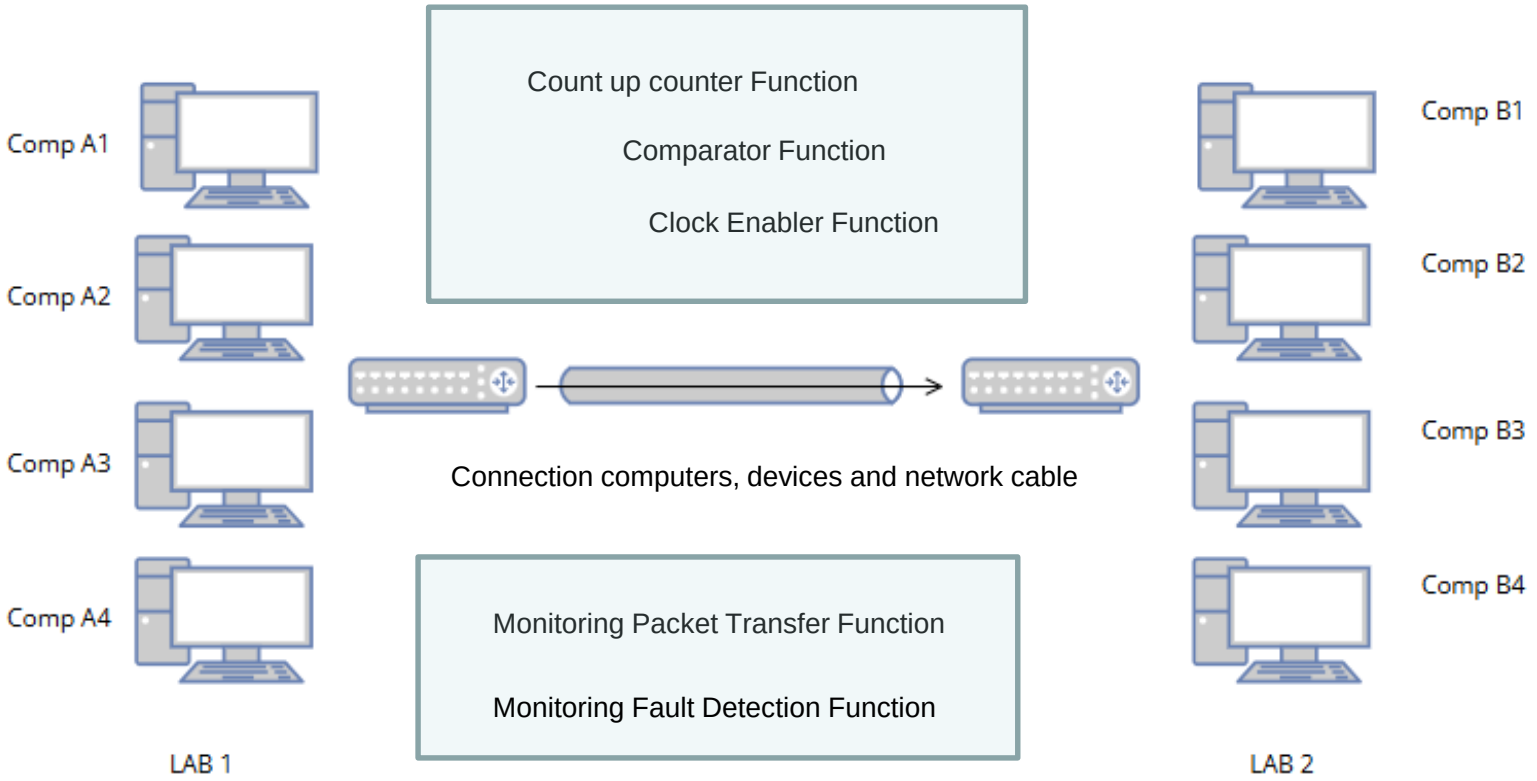


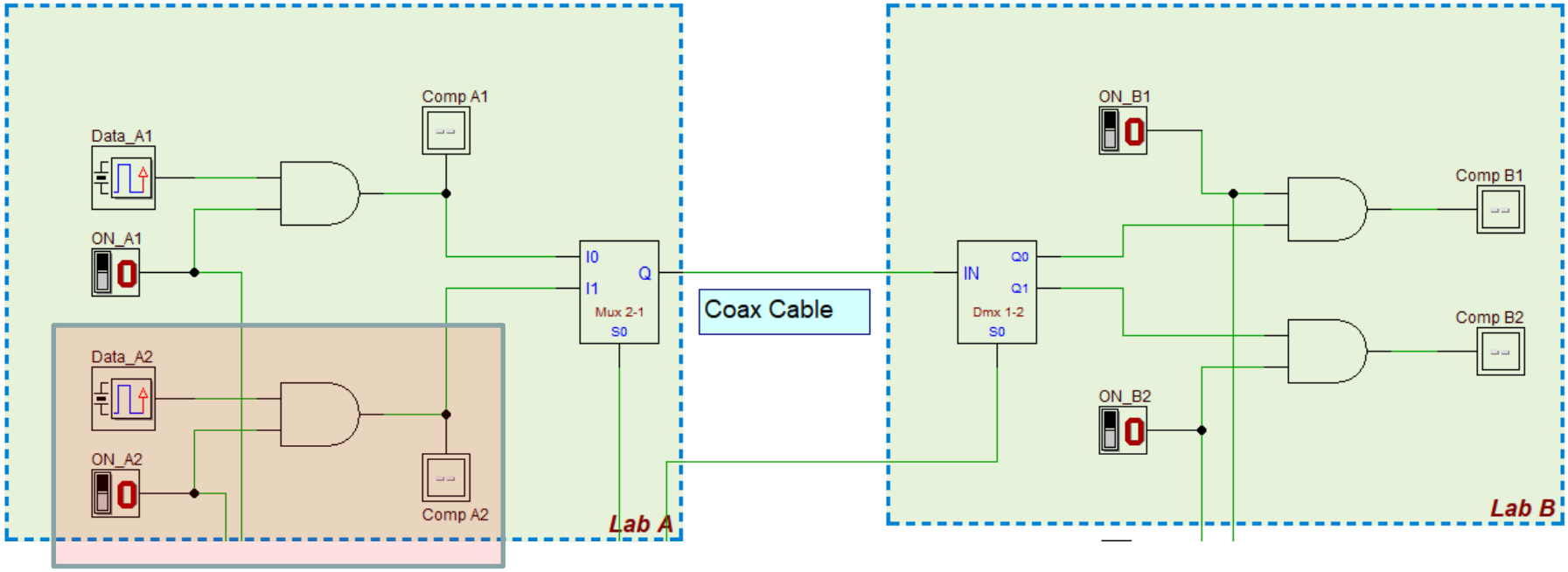
Figure 2: Simple Architecture

Connection Computers, Device and Cable (Hardware connection)

- Define number of computers in Lab 1 and Lab 2
  - E.g 4 or 8 Computers in each Lab
- Use 1 cable connection from Lab 1 to lab 2
- Select appropriate Mux (Lab 1)
- Select appropriate Demux (Lab 2)

Example: Use MUX (2x1) and DEMUX (1X2)

How to Connect?



Model Computer (Data Generator and Power ON)

Figure 3: Hardware Connection

Example circuit: Use your own design requirement

Count up Counter Function Design

- Define max number of packet to be transfer from one source of computer to another destination computer
- Based on Max number of Byte (Packet), design a count up counter to monitor the packet increment transfer
- Design the synchronous counter using JK, D, T Flip-flops

Circuit Controller : Eg. 8 Packet (Byte) Counter

- **Core components** (Basic design)

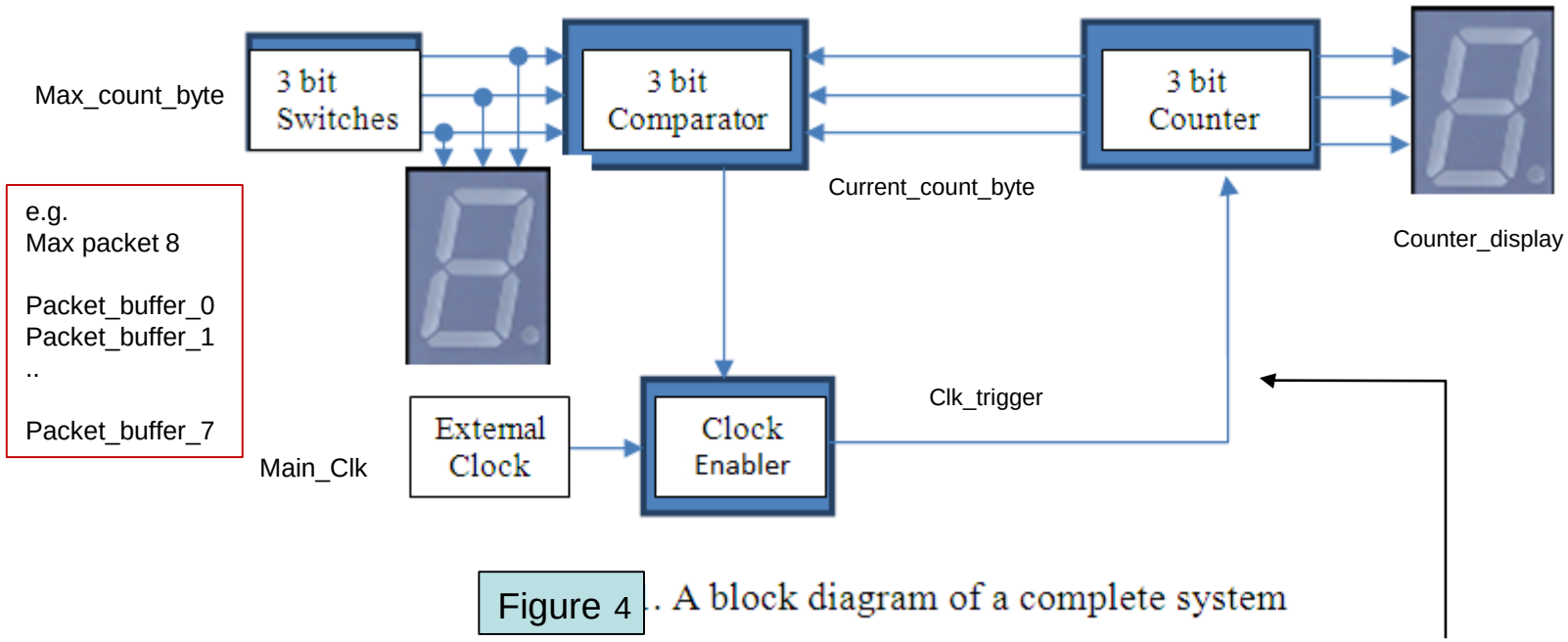


Figure 4. A block diagram of a complete system

Clock Enabler (Pattern Detector)

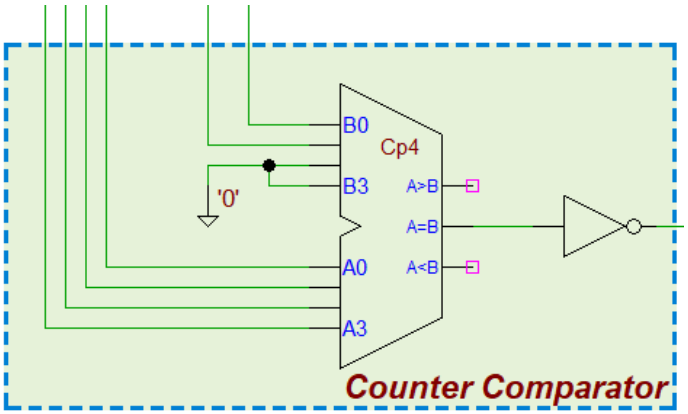
Rule_to_EnableClk

When counter NOT EQUAL Input Switch
Clock is Active
When counter EQUAL Input Switch
Clock is NOT Active

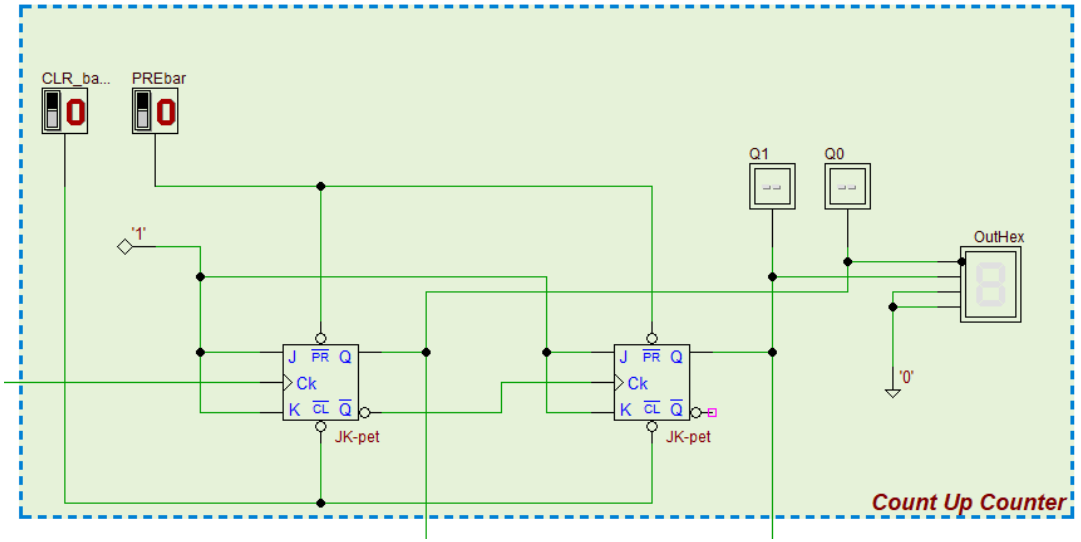
Example circuit: Basic Components (Counter)

Max Packet In

Counter In (Q1Q0) – 2 bit example



Example circuit of 2 bit counter



2 bit count up AC counter

Figure 5

Comparator Function Design

- Comparator will compare
  - Max packet number to be transmitted by computer source, with
  - Current count packet in the counter
- Rule
  - If packet number count by the counter is NOT equal max packet number, continue counting, ELSE stop counting packet
- Other rules are also required to design clock enabler to enable the count up counter is working
- Comparator also is used to design password detector to increase security features for the system

You can use:
. - inequality (XOR) or equality (XNOR)

OR
- comparator

Clock Enabler Function Design

- Clock enabler will control counter operation
- Use either AND or NAND gate (output active HIGH or LOW)
- Input of gate AND or NAND gate.
  - Basic rule clock enabler
  - Advance rule clock enabler
- Example:
  - Use AND gate to design Clock Enabler to enable the clock counter:
  - Input as the following (e.g. advance rule):
    - Power ON (computers that in used)
    - Comparator counter (Comparator Condition: max byte with counter output)
    - Comparator output (Security (password))
    - Transmission Mode (Full_Duplex)
  - Use your own design requirement
- Output clock enabler
  - If clock enabler is true than counter will count the packet (byte) transmission, else the counter will stop counting

Rule_to_Enable_Clk

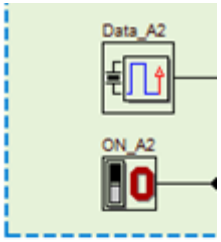
1. Power On Computers
2. Fulfill the Clock Enabler Condition
   - PowerON
   - set source and Destination
   - set max byte transfer
   - set ReadyTRX
   - set start button
   - activate clock by using push button

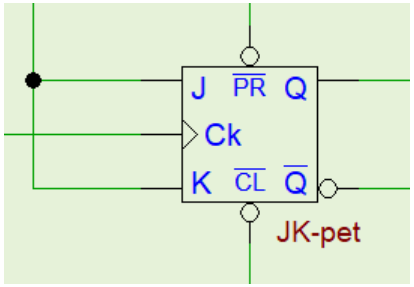
   (check the condition (rule) in the cicuit design to enable the counter)

3. Run simulation byte transfer by showing each clock change (use push button)

Clock Enabler
(Pattern Detector)

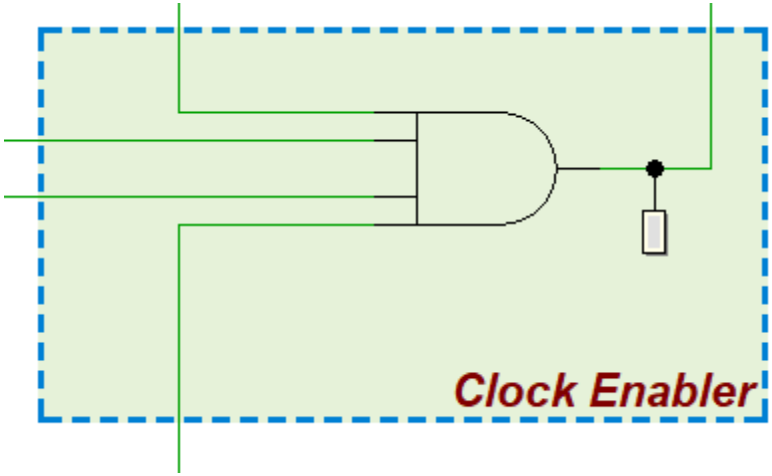
Example circuit: Clock Enabler





Output of Clock Enabler will trigger the counter to operate (count up)

Rule: Input that will enable the clock of counter



You can use either AND gate or NAND gate
- Look at the counter clock either active LOW or active HIGH

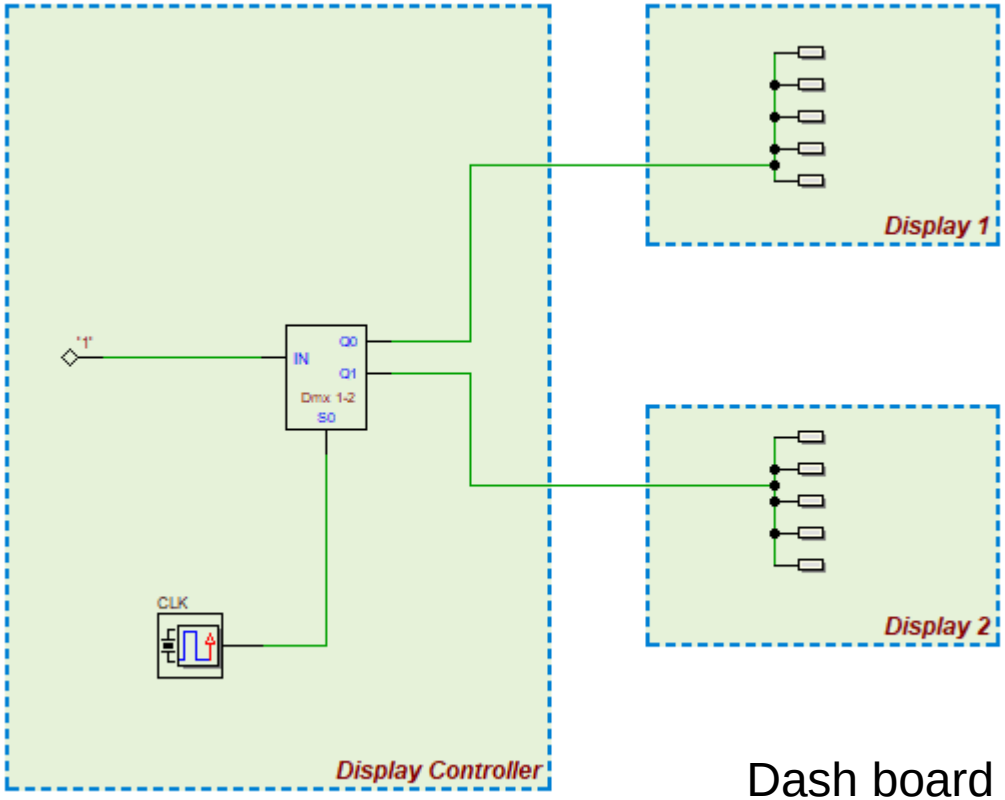
Figure 6

Monitoring Packet Transfer Function Design

- To monitor status output.
- Example (advance feature):
  - Power ON (computer)
  - Mode Data Transmission OK (Full Duplex)
  - Completed packet transmission (Counter OK)
  - Security Module OK (Password)
  - Etc
- Use Decoder/basic gate (or other method)

Basic Monitor dashboard to check status transfer
- Power_ON (OK)
- Counter (OK)

Example circuit: Basic Dashboard



Dash board - Display

Figure 6

Use suitable MSI (Decoder) Function

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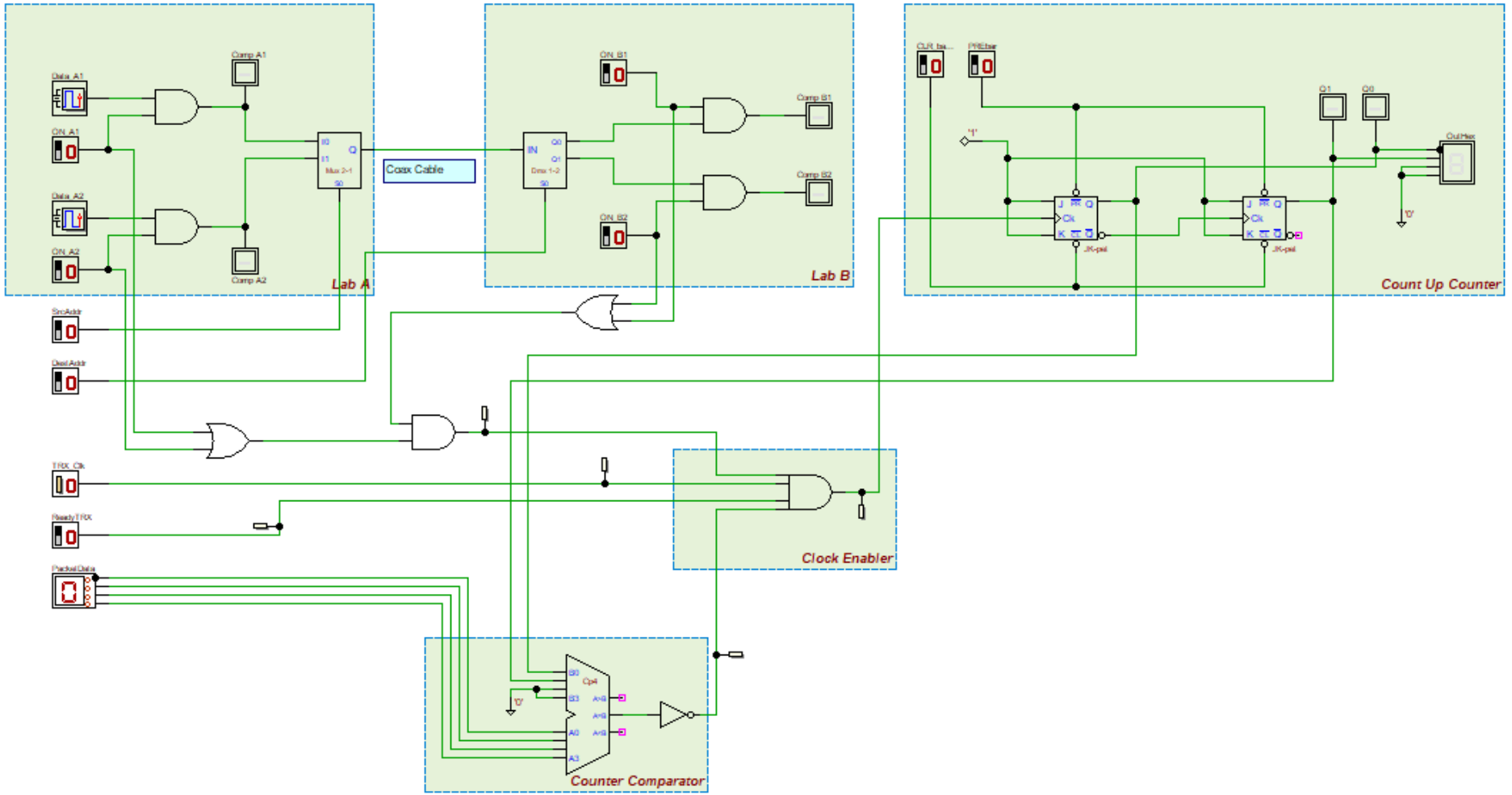
Complete Circuit (Basic Function)



Provide user manual in your circuit design

Example:

Use your own design

Instruction Manual

Circuit Design By Dr Mohd Foad for SECR1013/SCSR1013 2024-2025-01

Component Design Uses: Basic Gate, Flip-flops, Mux, Demux, Decoder, Comparator

User Manual:

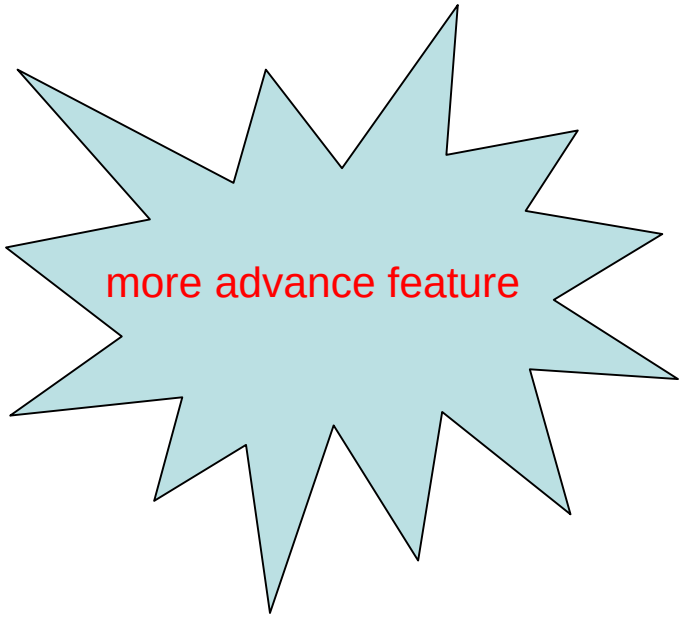
1. Power On Computers
2. Fulfill the Clock Enabler Condition
   - PowerON
   - set source and Destination
   - set max byte transfer
   - set ReadyTRX
   - set start button
   - activate clock by using push button

   (check the condition (rule) in the cicuit design to enable the counter)

3. Run simulation byte transfer by showing each clock change (use push button)

Monitoring Fault Detection Function Design (more advance feature) - optional

- To monitor if any fault or error occurs, system will generate error code.
- Base on error code, system will alert type of error.
- Example of error type:
  - Power_fault (not working)
  - Counter _fault (not working)
  - Comparator_fault (not working)
  - Clock_Enabler_fault (not working)
  - Mux_fault (not working)
  - Demux_fault (not working)
- Use Decoder/Gate



Variation of Group project

- Different layout of connection component hardware
  - Up to 8 computers each lab
- Different size packets
  - 8 packets
  - 16 packets
- Different counter design
  - Synchronous counter
    - JK flip-flop
    - D flip-flop
    - T flip-flop
- Different clock enabler design
  - Different rules
  - Use your own design rules

Report Format

Format

- Times New Roman 12 font
- 1.5 spacing
- Turn on MS Word spell and grammar checker

What should be in the report?

- TITLE PAGE
- DEDICATION & ACKNOWLEDGEMENT
- TABLE OF CONTENTS
- REPORT CONTENT
- REFERENCES
- APPENDICES

Under Appendices

- list of tasks distribution among members of group
- Photo(s) of your group working together
- And others supporting materials that will strengthen the explanation of your project.

PROJECT REPORT CONTENT

- You may use the lab manual as guidance and inspiration. Don't forget to cite the manual.

1) The background
2) The Problem
3) Suggested Solution (must Include the block diagram and explain)
4) The Requirement
5) System Implementation (must include DEEDS drawing and explain)
6) Conclusion and Reflection
   - Summarizes the whole project. Write your reflections.
   - Describe your achievements, strength and weaknesses.
   - Propose future work to improve your design

Option Design

Group	Option
1	Comp (5), 4 bit Counter, JK flip-flop
2	Comp (5), 4 bit Counter, T flip-flop
3	Comp (5), 4 bit Counter, D flip-flop
4	Comp (6), 4 bit Counter, JK flip-flop
5	Comp (6), 4 bit Counter, T flip-flop
6	Comp (6), 4 bit Counter, D flip-flop
7	Comp (6), 3 bit Counter, T flip-flop
8	Comp (6), 3 bit Counter, D flip-flop

Project Timeline

Date	Activity
1	Briefing & group setup
2	Work on Part 1 (refer Figure 4) and discuss enhancement with lecturer
3	Receive approval/comments for improvement
4	Submit Part 1 .pbs
5	Work on project
6	Project report develop/improve (discuss with lecturer)
7	Submit Project .pbs, Project Report, Presentation/Demo Video

- * All e-learning deadline at 11:00pm

- GOOD LUCK !!!!