Paper – I: COMPUTER ARCHITECTURE

Time: 3 Hours   **M. Marks: 75**

Instructions for the Paper Setters:-
Eight questions of equal marks (Specified in the syllabus) are to be set, two in each of the four Sections (A-D). Questions may be subdivided into parts (not exceeding four). Candidates are required to attempt five questions, selecting at least one question from each Section. The fifth question may be attempted from any Section.

Section A
Information Representation: Register Transfer Language, Various Registers, Implementing Common Bus Using Multiplexers: Logical; Arithmetic & Shift Micro – operations.
Basic Computer Design   Instruction Codes, Computer Instructions, Timing Signals, Instruction Cycle, Design of a Basic Computer.

Section B
CPU Design General Register Organization, Stack Organized CPU, Instruction Formats, Addressing Modes, Program Control, Hardwired & Microprogrammed (Wilhe's Design) Control Unit, RISC and CISC Characteristics.
Section C
Memory Organization   Memory Hierarchy, Designs & Concepts of Main Memory, Auxiliary Memory, Associative Memory, Cache and Virtual Memory.

Section D
I/O Organization I/O Interface, Modes of Transfer, Program Interrupt, DMA & I/O Processor.
Pipeline & Vector Processing   Introduction to Parallel Processing and Pipelining, SISD, SIMD & MISD, MIMD Machines.

References:
Computer System Architecture: M.M. Mano (PHI)
Computer Architecture: J.P. Hayes.
Computer Architecture: Patterson & Hemessy.