Exam. Code : 107203
Subject Code : 1789

Bachelor of Computer Application (BCA)

3rd Semester

COMPUTER ARCHITECTURE

Paper—I

Time Allowed—3 Hours] [Maximum Marks—75

Note :— (1) The candidates are required to attempt **five** questions, selecting at least **one** question from each Section. The **fifth** question may be attempted from any Section.

(2) All questions carry **15** marks each.

(3) The students can use only non-programmable non-storage type calculator.

SECTION—A

1. (a) Explain implementing Common Bus with Multiplexers using Logical, Arithmetic and Shift micro operations. 7.5

(b) Draw the block diagram of dual 4 to 1 line multiplexers and explain its operation by means of a functional table. 7.5

2. (a) Draw and explain the flowchart of floating point addition process. 7.5

(b) State the Non-restoring division technique. 7.5

SECTION—B

3. (a) Explain the different addressing modes in detail. An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor registers R1 contains the number 200. Evaluate the effective address for the different addressing modes. 7.5

(b) A relative mode branch type of instruction is stored in memory at an address equivalent to decimal 750. The branch is made to an address equivalent to decimal 500.

(i) What should be the value of the relative address field of the instruction (in decimal) ? Determine the relative address value in binary using 12 bits. (Why must the number be in 2's complement ?)

(ii) Determine the binary value in PC after the fetch phase and calculate the binary value 500. Then show that the binary value in PC plus the relative address calculated in part (a) is equal to the binary value of 500. 7.5

4. (a) What is microprocessor ? Is it possible to design a microprocessor without a micro-programmed ? Also discuss the classification of microprocessor in detail. 7.5

(b) Explain Stack Organization in detail. 7.5

SECTION—C

5. (a) What do you mean by virtual memory ? Discuss how paging helps in implementing virtual memory. 7.5

(b) Explain the cache memory and its accessing methods in detail. And how these methods are used to improve cache performance. How many total bits are required for a direct mapped cache with 16 KB of data and 4 word blocks, assuming a 32 bit address ? 7.5

6. What is Memory Interleaving ? Explain the addressing of multiple module memory system. 15

SECTION—D

7. Explain with the block diagram the DMA transfer in a computer system. 15

8. Explain how the instruction pipeline works. What are the various situations where an instruction pipeline can stall? What can be its resolution ? In certain scientific computations it is necessary to perform the arithmetic operation $(A_i + B_i)(C_i + D_i)$ with a stream of numbers. Specify a pipeline configuration to carry out this task. List the contents of all registers in the pipeline for i = 1 through 6. 15