ECE 165 – Homework #5

Due: 5/20/2025 @ 6:00PM

Problem 1.

You are synthesizing a chip composed of random logic with an average activity factor of 0.1. You are using a standard cell process with an average switching capacitance of 300 pF/mm^2. Estimate the dynamic power consumption of your chip if it has an area of 5x5 mm^2 and runs at 400 MHz at V_{DD} = 0.9V.

Problem 2.

Use Boolean algebra to prove that $S = ABC + \overline{C_{out}}(A + B + C) = A \oplus B \oplus C$.

Problem 3.

What is the worst-case input of an n-bit ripple-carry adder? Why is it not '111...11 + 111…11'?

Problem 4.

One important building block of arithmetic logic is the full adder. You will need to analyze this circuit carefully as it is a critical block. The full adder takes three inputs, A, B, and carry in, and computes two outputs, S and carry out.

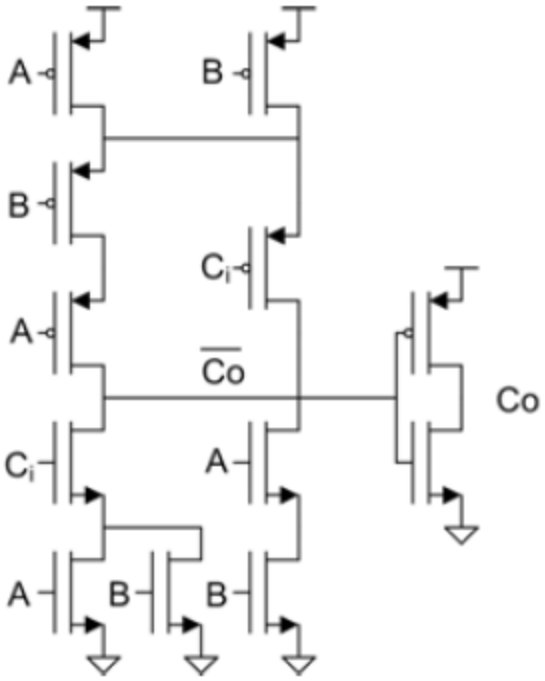
a) Consider implementing the full adder using combinational gates with fan-in of two or three. Draw a circuit (logic) schematic for the two functions above.

b) Calculate the delay from Ci to Co if H = 1.

c) Calculate the delay from Ci to S if H = 2. Which is slower?

d) The carry circuit is particularly important to speed. A fast carry circuit is shown below. Determine the appropriate sizing for the transistors in this circuit.

e) Calculate the conditions for the slowest low-to-high and high-to-low transitions. Give expressions for the worst case t_{pLH} and t_{pHL} at node $\overline{C_0}$.



Problem 4 d,e