UNIVERSITY OF RUHUNA

Faculty of Engineering

EE5260 – Hardware Description Languages

Take Home Assignment 01

Q1 Ripple Counter

A ripple counter is a cascaded arrangement of flip-flops where the output of one flip-flop drives the clock input of the following flip-flop. The number of flip-flops in the cascade depends on the number of different logic states it goes through before repeating the sequence, known as the modulus of the counter. An n-bit ripple counter can count up to 2^n states and is also called a MOD n counter. It is named a ripple counter because the clock pulse ripples through the flip-flops.
A counter can be an up counter that counts upwards, a down counter that counts downwards, or both (up and down) depending on the input control.

Tasks

a) Define the states of a 3-bit ripple counter.
b) Sketch the state diagram of the 3-bit up-down ripple counter.
c) Design a Verilog module for the 3-bit up-down ripple counter.
d) Write a test bench to verify the design and attach the simulated output graphs.

Q2 Multiplexer

A multiplexer is a combinational circuit that has a maximum of 2^n data inputs, n selection lines, and a single output line. One of these data inputs will be connected to the output based on the values of the selection lines. Since there are n selection lines, there are 2^n possible combinations of zeros and ones. Each combination will select only one data input.

Tasks

a) Write a Verilog module to implement a 4-to-1 multiplexer.
b) Design a Verilog module for an 8-to-1 multiplexer using two 4-to-1 multiplexers from part a) and one 2-to-1 multiplexer.
   (Hint: The inputs should be fed from the 4-to-1 multiplexers, and the final output should be obtained through the 2-to-1 multiplexer.)
c) Write a test bench to verify the design of the 8-to-1 multiplexer.
d) Attach the simulated output graphs.