UNIVERSITY OF RUHUNA

Faculty of Engineering

EE5260/ EE6205 – Hardware Description Languages

Take Home Assignment 02

- For this assignment, take the last digit of your index number multiplied by 10 as P (e.g.: for EG/20XX/1234, P = 40*10 = 40). Use P = 50 if your last digit is 0.
- All the Verilog files and screenshots of testbench output sequences should be included in your submission.

Task01:

1. Create a Verilog module called 'IC7490' to imitate **only the BCD counting functionality** of DM7490A integrated circuit using **behavior modeling**. Use the given IC datasheet as reference. (Read and understand the datasheet carefully since the IC offers multiple counting modes). Ignore the Reset/Count Function table/ four reset pins and include single reset pin which reset the count back to 0.
2. Create a test bench called 'IC7490TB' to simulates the counting function of the above module in BCD counting mode. The testbench output should display the BCD Count Sequence table given in the datasheet.

Task02:

1. Create a Verilog module called 'Decoder' which accepts four-bit BCD signals and decode them for a seven-segment display (seven outputs; ignore the decimal point). Use either gate level or behavior modeling.
2. Create a Verilog module called 'IC4017' to imitate functionality of CD4017 integrated circuit using **behavior modeling**. (You can use the module given in the lectures as well.)

Task03:

1. Create a Verilog module called 'Counter' which can count from 0 up to P and display the count using two 7 segment displays. Use the modules created above. Create 'CounterTB' to supply clock signal and get the outputs. Simulate the testbench and capture output waveforms.