Analysis of Charge-Shared Matchline Sensing Schemes and Current Race Scheme in High-Speed Ternary Content Addressable Memory (TCAM)

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***Abstract*—Due to emerging of hi-speed communication larger TCAMs with higher speed is needed. A comparative analysis of different Matchline sensing schemes in high speed Ternary content addressable memory (TCAM) is presented in this paper. With the conventional current race scheme, two different methods of charge sharing matchline sensing schemes are being analyzed. The power is distributed along the matchline by dividing it and sharing charge. This two charge shared schemes also improve search time and voltage margin. Simulations are performed using 180nm 1.8V CMOS logic in HSPICE.**

Keywords—*content-addressable memory; charge sharing; energy consumption; search time; sensing scheme; current race, voltage margin*

I. INTRODUCTION

CONTENT-ADDRESSABLE memory (CAM) is a high speed memory which allows an input search data to be searched in entire memory and return the address of the data in a single clock cycle [1]. For its impeccable search speed, it is widely used in network router where high speed data forwarding is necessary [2]. An ordinary binary CAM can perform searching operation but Ternary Content Addressable Memory (TCAM) has the advantage of having don't care bits which makes the search operation more efficient specially while longest-prefix-match searches in routing tables[3]–[4]. Due to the rapid growth of data transfers the word sizes are getting larger which in turns reduces the search time because of larger matchline capacitances and also increased amount of matchline sensing amplifiers between the matchlines are increasing the power consumption to greater extent. Therefore, low-energy high-performance designs are needed, that improve the search speed of TCAMs without increasing their power consumption. Several methods [5]–[8] have been developed to reduce the power consumption in TCAMs. However in all those methods power in the matchline is distributed uniformly independent of match or mismatch.

In this paper, we divide the matchline into segments in two different ways rather distribute charge uniformly so that the charge can be shared by the matchlines from segments and then we compare performance with traditional current race scheme.

II. TCAM BASICS

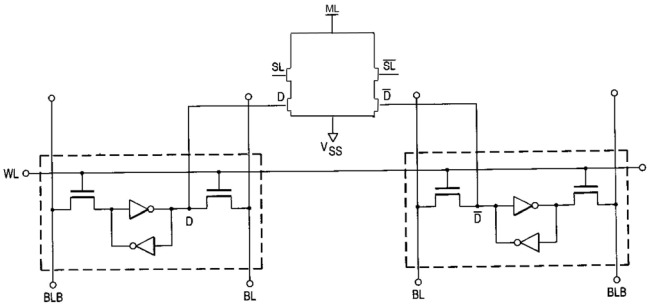

Fig. 1. TCAM cell

A typical TCAM cell consists of two SRAMs, where the data are stored and read while comparing with the searched data. The core cells may be different depending on number of transistors and performance priorities. Typically, core cells available are 9-T, 10-T and 16-T structures [9]. The matchline structures can be of different variants. [4]. The READ and WRITE operation are carried out using the Bit Lines (BLs) and Word Lines (WL). The data to be searched are supplied to the Search Lines (SLs) and the data word is connected to the Match Line (ML). Therefore, when there is a match, the Match line (ML) goes HIGH. Otherwise, the ML is pulled down to the ground. The HIGH is sensed by the Match Line Sensing Amplifiers (MLSAs). The MLSAs can be different according to the scheme chosen for the operation. For our simulation purpose we have used 10-T NAND type structure.

III. CURRENT-RACE SCHEME

Current Race (CR) Scheme is one of the most used match line sensing schemes. It was introduced to reduce the amount of power used by Match - Line (ML). It is used to get better performance over the usual pre-charge high scheme. This

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scheme is considered as a separate class of sensing scheme, nowadays. CR is used widely since it is a pre-charge low scheme. It pre-discharges all the MLs to low, not the other way around, e.g. charging them to high. All the MLs are charged to high while MLs are being evaluated. We use NOR cells, and for that, when there is match, the matched MLs are charged up quickly to high voltage, and when there is a mismatch, the mismatched MLs have low voltage as there is no discharging paths. Fig. 2 shows the CR scheme.

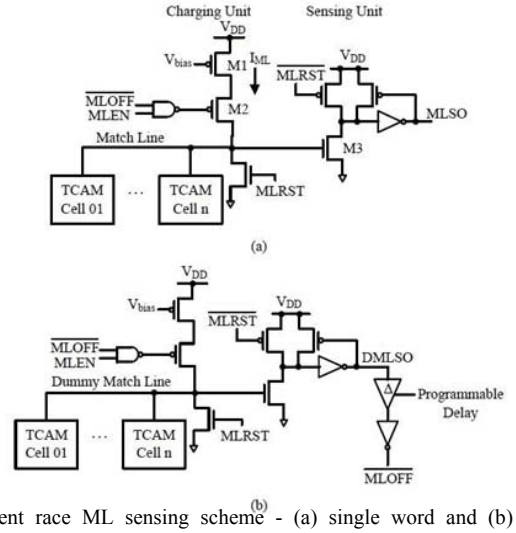

Fig. 2.Current race ML sensing scheme - (a) single word and (b) using dummy (replica) word

Match-Line Sensing Amplifiers (MLSA) have two units: the charging unit and the sensing unit. We set any voltage of ML (V_{ML}) and outputs (MLSOs and DMLSO) by using MLRST. Then the transistor M2 is turned on by enabling MLEN signal which causes I_{ML} current flowing. The Match-Line capacitance (C_{ML}) starts charging. If the word matches, then the ML gets charged up to the threshold voltage of M3 transistor which makes it turn on. Thus, MLSO becomes high. Otherwise If the word miss matches then M3 remains off and MLSO remains null. The dummy word never miss matches and so MLSA always gives high output. MLOFF turns off the M2 transistors in all words. DMLSO signal is created by delaying and inverting MLOFF. By turning off the M2 transistors in all word segments, unnecessary charging is stopped and so power consumption of the MLs remains low. The dummy word also minimizes the effects of process variations since it is situated close to the usual words and process variations are same as those words. When the dummy word finds the match, the programmable delay DMLSO confirms that all the MLs can get sufficient amount of time to get charged up until it reaches threshold voltage of M3 transistors. V_{bias} controls I_{ML} that controls the speed and also energy consumption of detection process. Parasitic capacitance (C_{ML}) of MLs depends on data stored and also search data. As different cells have different stored data so C_{ML} will vary from ML to ML.As bits to be searched are same along a column, C_{ML} is same for all MLs in a search. This ensures precise matching between MLs and reduces sensing error which is caused by variation of capacitance.

IV. Charge Shared Match Line Sensing Scheme with 2 Blocks (four segmentation)

In this technique the ML is divided into 4 segments. It precharges two segments (segment 1 & 4) to V_{DD} while in operation. Signal CS is kept low so that the charge is not shared. In the 2nd phase, SLs are provided with search data, so, CS gates are made open. If the two segments in a block fully matches, it keeps its voltage; otherwise mismatch causes the ML voltages to discharge to ground. The match sensor block combines the result of two blocks and give away the final match result. The main advantage is that the voltage remaining in the previous cycle has the opportunity to be reused in this technique. Therefore, it reduces power dissipation while retaining its speed.

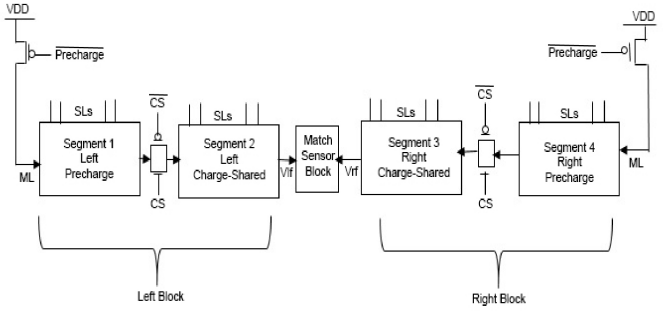

Fig. 3. Charge shared ML sensing proposed scheme.

V. Charge Shared Matchline Sensing Scheme with Selective Precharge and Replica Control

In this scheme two ML segments are used, where ML segment 1 is greater than ML segment 2. All the MLs and MLSA outputs discharge to the ground before starting the search operation. After starting the search operation the MLEN signal starts charging and match with the search keys.

If only there is a match, ML segment 1 enables the sensing unit to produce high MLSO1. So the second segment can get charged up by sharing charge from transistor M1 by the pass transistor M2. Segment 2 is then compared with the remaining portion of search keys. If there is a match, then output logic will be high and in case there is mismatch the output voltage will gets low.

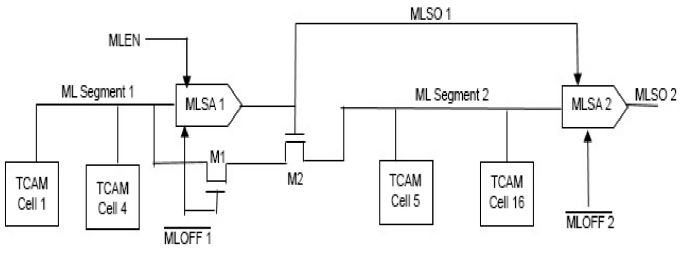

Fig. 4. ML sensing scheme using charge sharing one word of TCAM array.

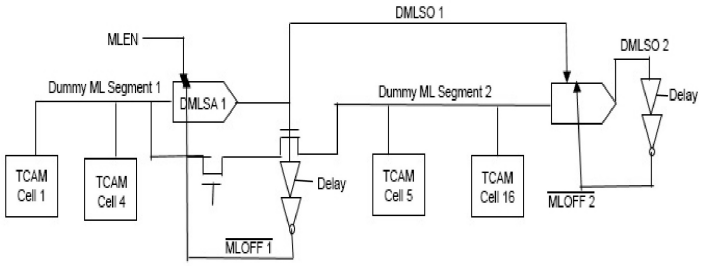

Fig. 5. ML sensing method using charge shared between dummy words

In case of dummy words, they are always matched due to local masking. When DMLSO1 becomes high as they are matched, the charging of 1st segments are stopped by MLOFF1 .This makes the charge sharing between the two segments stop.
This scheme is actually a combination of charge sharing and current race techniques using selective precharge.

VI. SIMULATION RESULTS AND ANALYSIS

The simulation presented here are done each with 32 bit 16x16 array of TCAM and the graphs were viewed in COSMO-SCOPE. Our main objective was to visualize the search time that is the delay between the initializing signal (Precharge or Matchline reset signal) and output of matchline sensing amplifier. We also gained voltage margin (difference in 1bit mismatching maximum voltage and crossing of matchline result with matched matchline voltage) for comparing overall performance.

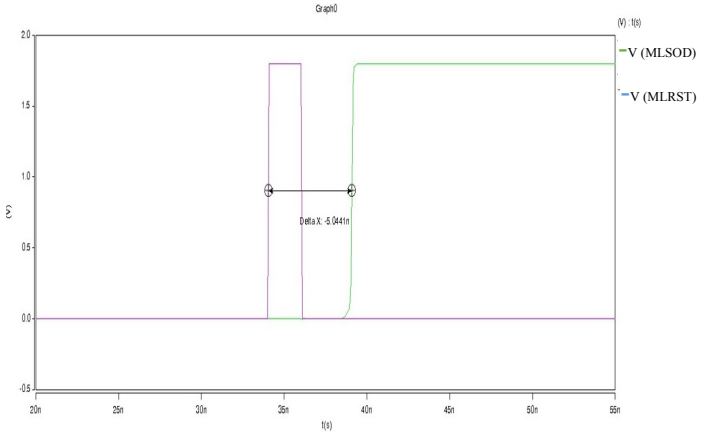

Fig. 6. Search time for current race scheme.

Fig. 6 shows the search time for current race scheme where we view the difference (5.0441 ns) between the initial MLRST signal and final output DMLSO signal. In case of voltage margin (Fig.6) we find the difference between maximum voltage of the matchline V_{ML}=0.030595V and crossing (V=1.095V) of output matchline voltage (DMLSO) with the mismatched voltage. Therefore the voltage margin is (1.095-0.030595) =1.64405V

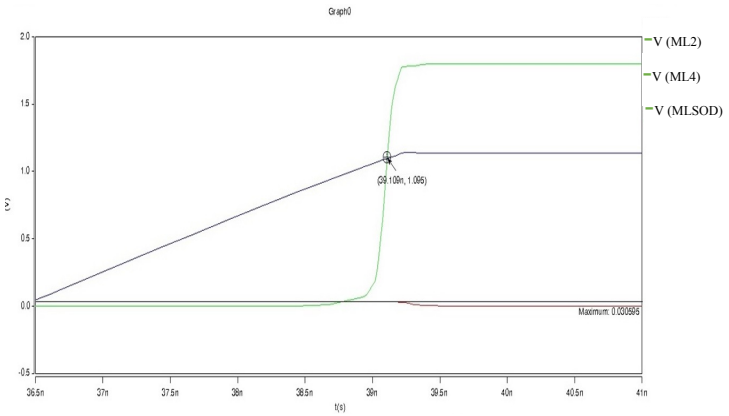

Fig. 7. Voltage margin for current race scheme.

For charge shared match line sensing scheme with 4 segments (Fig.7) search time is difference between precharge (PREB) signal and final match result.

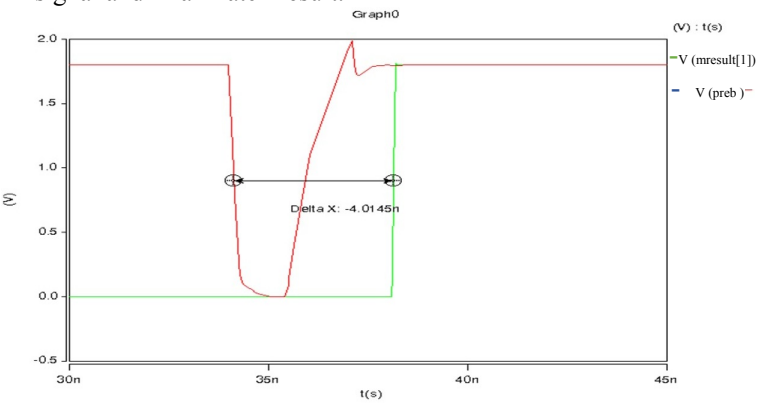

Fig. 8. Search time for charge shared matchline sensing scheme with 4 segmentation.

For measuring voltage margin we have considered two cases depending on mismatch occurring in different blocks. Fig.8 shows voltage margin for mismatch in left block while Fig.9 depicts mismatch in right block. In both cases we measured the difference between maximum voltage and crossing of final output with mismatched ML voltage. For mismatch in left block voltage margin (0.25157 V) is lesser than voltage margin (0.76002 V) due to mismatch in right block because of ML capacitance.

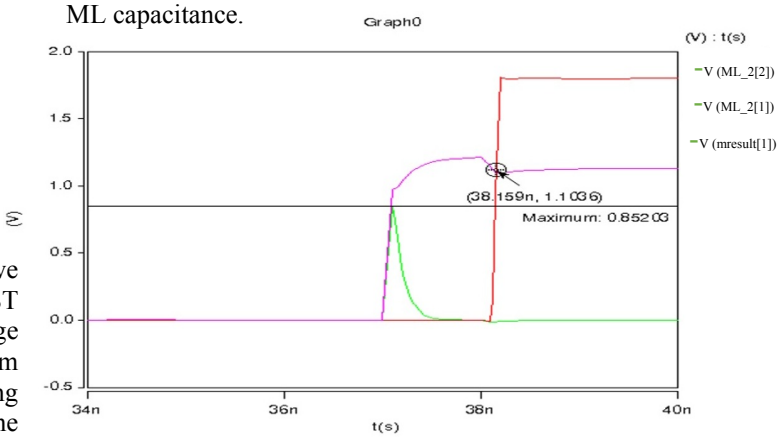

Fig. 9. Voltage margin for charge shared matchline sensing scheme with 4 segmentation (mismatch in left block).

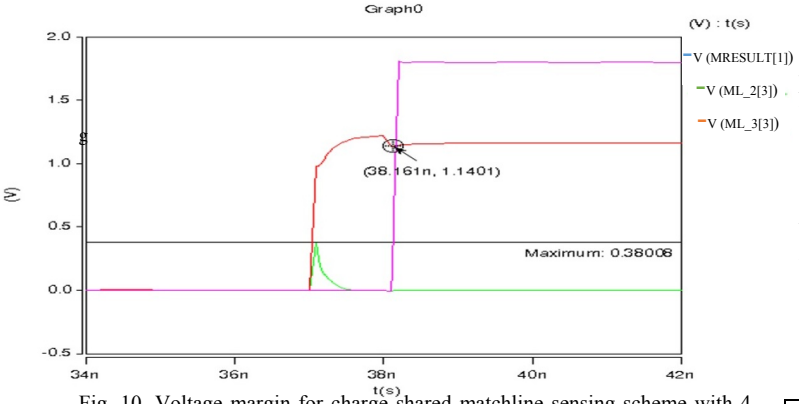

Fig. 10. Voltage margin for charge shared matchline sensing scheme with 4 segmentation (mismatch in left block).

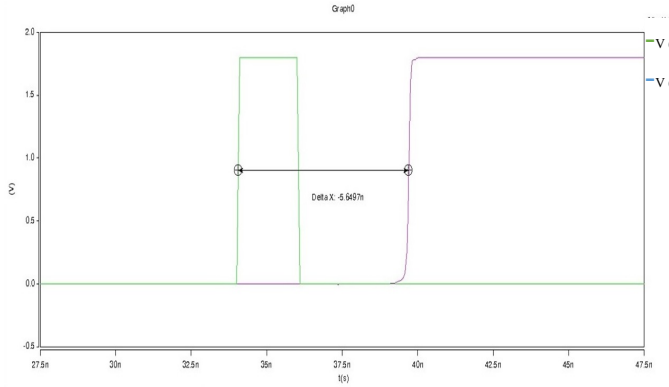

Fig. 11. Search time for charge shared matchline sensing scheme with selective precharge and replica control.

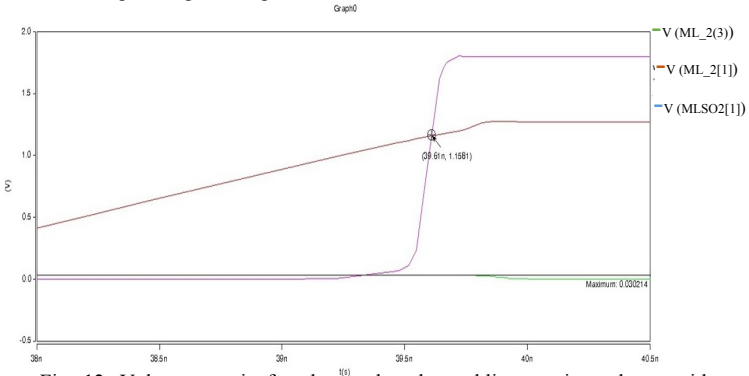

Fig. 12. Voltage margin for charge shared matchline sensing scheme with selective precharge and replica control (mismatch in 1st segment) .

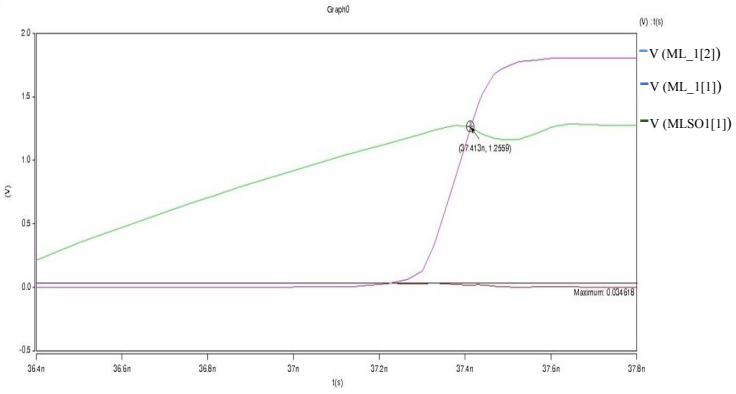

Fig. 13. Voltage margin for charge shared matchline sensing scheme with selective precharge and replica control(mismatch in 2nd segment)

For measuring voltage margin we considered similar cases as previous scheme. If there is mismatch in 1st segment, voltage margin nothing but the difference between maximum voltage of matched ML and crossing of matchline sensing amplifier's output with mismatched ML (Fig.11). In case of mismatch in 2nd segment (Fig.12) voltage margin is calculated same as before but the matchline sensing amplifier will be different in this case

TABLE I
PERFORMANCE COMPARISON OF DIFFERENT MATCHLINE SENSING SCHEMES FROM SIMULATION RESULTS

Current Race Matchline Sensing Scheme		**Charged Shared Matchline Sensing Scheme**			
Search time	5.0441	***Segmentation into 2 Blocks (4 Segments)***		***Selective Precharge and Replica Control***	
		4.0145		5.6497	
Voltage margin	1.064405	***Mismatch in Left Block***	***Mismatch in Right Block***	***Mismatch in 1st Segment***	***Mismatch in 2nd Segment***
		0.25157	0.76002	1.127786	1.2212

VII. CONCLUSION

The matchline (ML) consumes most of the power while searching. To decrease the amount of power consumption, we have segmented the ML in two different ways. The main advantage of Charge shared matchline sensing scheme with 4 segments is that it divides the ML in 4 parts. So any charge remaining in most recent search can be reused to save power and also as we see the search time is considerably low than other schemes. While in charge shared method with selective precharge and Replica control scheme the performance is degraded to some extent from segmented schemes but it reduces power consumption to a great extent [10].

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