



SPECIFICATION

1 (229)

DMIF-L99GP-C130

May 18th, 2012

V1.00

DMIF-L99GP-C130

DISPLAY MODULE INTERFACE SPECIFICATION

For 360 (H) x RGB x 640 (V) Resolution OLED with DSI

Owner: Jani Penttila

Status: V1.0

Document ID: N/A

Version History

Version	Date	Handled by	Comments
V 1.00	18052012	Jani Penttila	

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SPECIFICATION

2 (229)

DMIF-L99GP-C130

V1.00

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CHANGE HISTORY

ABBREVIATIONS

↑	Rising edge active
ABC	Automatic Brightness Control
A/D	Analog to Digital Converter
ASIC	Application Specific Integrated Circuit
BL	Backlight Light
CMOS	Complementary Metal Oxide Semiconductor
CSX	Chip Select, active low
D/CX	Data/Command, Command is active low
DIN	Data In, display side
DOUT	Data Out, display side
DSI	Display Serial Interface, MIPI
DSI-1M	DSI with one data and one clock lane differential pairs, MeSSI Replacement
DSI-2M	DSI with two data and one clock lane differential pairs, MeSSI Replacement
DSI-3M	DSI with three data and one clock lane differential pairs, MeSSI Replacement
DSI-4M	DSI with four data and one clock lane differential pairs, MeSSI Replacement
DSI-1V	DSI with one data and one clock lane differential pairs, ViSSI Replacement
DSI-2V	DSI with two data and one clock lane differential pairs, ViSSI Replacement
DSI-3V	DSI with three data and one clock lane differential pairs, ViSSI Replacement
DSI-4V	DSI with four data and one clock lane differential pairs, ViSSI Replacement
High-Z	High Impedance
H-Sync	Horizontal Synchronization
HS-0	Lane pair is in the High Speed mode, Negative lane is higher potential than Positive line
HS-1	Lane pair is in the High Speed mode, Positive lane is higher potential than Negative line
HS-RX	High Speed – Receiver, Differential, MIPI DSI
HS-TX	High Speed – Transmitter, Differential, MIPI DSI
HW	Hardware
I/O	Input/Output
LSB	Least Significant Bit
LP-00	Lane pair is in the Low Power mode, Positive and Negative lanes are in low potential
LP-01	Lane pair is in the Low Power mode, Positive lane is low potential and Negative lane is high potential
LP-10	Lane pair is in the Low Power mode, Positive lane is high potential and Negative lane is low potential
LP-11	Lane pair is in the Low Power mode, Positive and Negative lanes are in high potential
LP-CD	Low Power – Contention-Detector, Single End, MIPI DSI
LP-RX	Low Power – Receiver, Single End, MIPI DSI
LP-TX	Low Power – Transmitter, Single End, MIPI DSI
LPDT	Low Power Data Transmission
MCU	Micro Controller Unit
MeSSI-8	Medium Speed Screen Interface, 8 lines (Intel 80 compatible)
MeSSI-16	Medium Speed Screen Interface, 16 lines (Intel 80 compatible)
MIPI	Mobile Industry Processor Interface
MSB	Most Significant Bit

PWM	Pulse Width Modulation
RESX	Reset, active low
RDX	Read, the display starts to control D[15...0] or D[7...0] lines when there is a falling edge of the RDX and the host reads D[15...0] or D[7...0] lines when there is a rising edge of the RDX
RL	Relative Luminance
SW	Software
SCNN	DSI-CLK (Clock lane differential pair): Slave – Clock – Not Applicable – Not Applicable, Clock Only, Escape Mode (Ultra Low Power Mode (ULPS))
SFEN	DSI-D1/2/3 (The second/third/fourth data lane differential pair, D1/D2/D3): Slave – Forward Only – Events (Triggers and ULPS Only) – Not Applicable, Unidirectional High-Speed to the Display Module, Forward Escape Mode Only, No LPDT
SFAA	DSI-D0 (The first data lane differential pair, D0): Slave – Forward Only – All – All, Unidirectional High-Speed to the Display Module, Bi-Directional Escape Mode, Bi-Directional LPDT
Ta	Ambient Temperature
TBD	To Be Defined
WRX	Write, The host starts to control D[15...0] or D[7...0] lines when there is a falling edge of the WRX and the display reads D[15...0] or D[7...0] lines when there is a rising edge of WRX
VDDI	Power supply for logic
VPNL	Power Supply for Display Panel
V-Sync	Vertical Synchronization
VSS	Ground

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1 Introduction

This document describes one of display interfaces, which Nokia is using for display modules and how it is implemented for DMIF-L99GP-C130.

This document is also a guideline for Nokia's display designers, Nokia's software designers, Nokia's ASIC designers and display module suppliers when they want to know how MIPI DSI (Mobile Industry Processor Interface – Display Serial Interface) is working in the DMIF-L99GP-C130.

This document gives definition of the display interface as follows:

- Electrical specification
- Timing specification
- Protocol specification
- Command set
- (General) functional description of the display module

2 Features

- Display resolution: [360xRGB](H) x 640(V)
- Logic power supply: 1.65 to 1.95V
- Display Panel power supply: 2.3 to 4.8V
- Display Frame Memory (e.g. RAM) 360x24x640 bits
- MIPI DSI compatible interface, Note 4
 - 1 clock (SCNN) and 1 data (SFAA) lane pairs, DSI-1M
 - Maximum Speed: 500Mbps/Channel
- Number of colours on the display panel 8 or 16,777,216 colours/pixel.
- Number of colours supported by interface: 65,536 (via 16 bit/pixel to 24 bit/pixel converter) and 16,777,216 colours/pixel
- 1 preset gamma curve
- On module timing generator
- On module oscillator
- On module DC/DC converter
- On module colour characteristics
- On module checksums checking
- Temperature compensation on the display module
- Temperature range:- 30...+70 °C (to + 85 °C no damage),
- Factory default values (Contrast preset value, Module ID, Module version, etc.) are stored on the display module

Notes:

1. Reference Documents for DSI
 - a. MIPI Alliance Standard for D-PHY, Version 0.9
 - b. MIPI Alliance Standard for Display Serial Interface, Version 1.01 r11

3 Display Module Block Diagram (example)

Note: The display module supplier will enclose the actual block diagram.

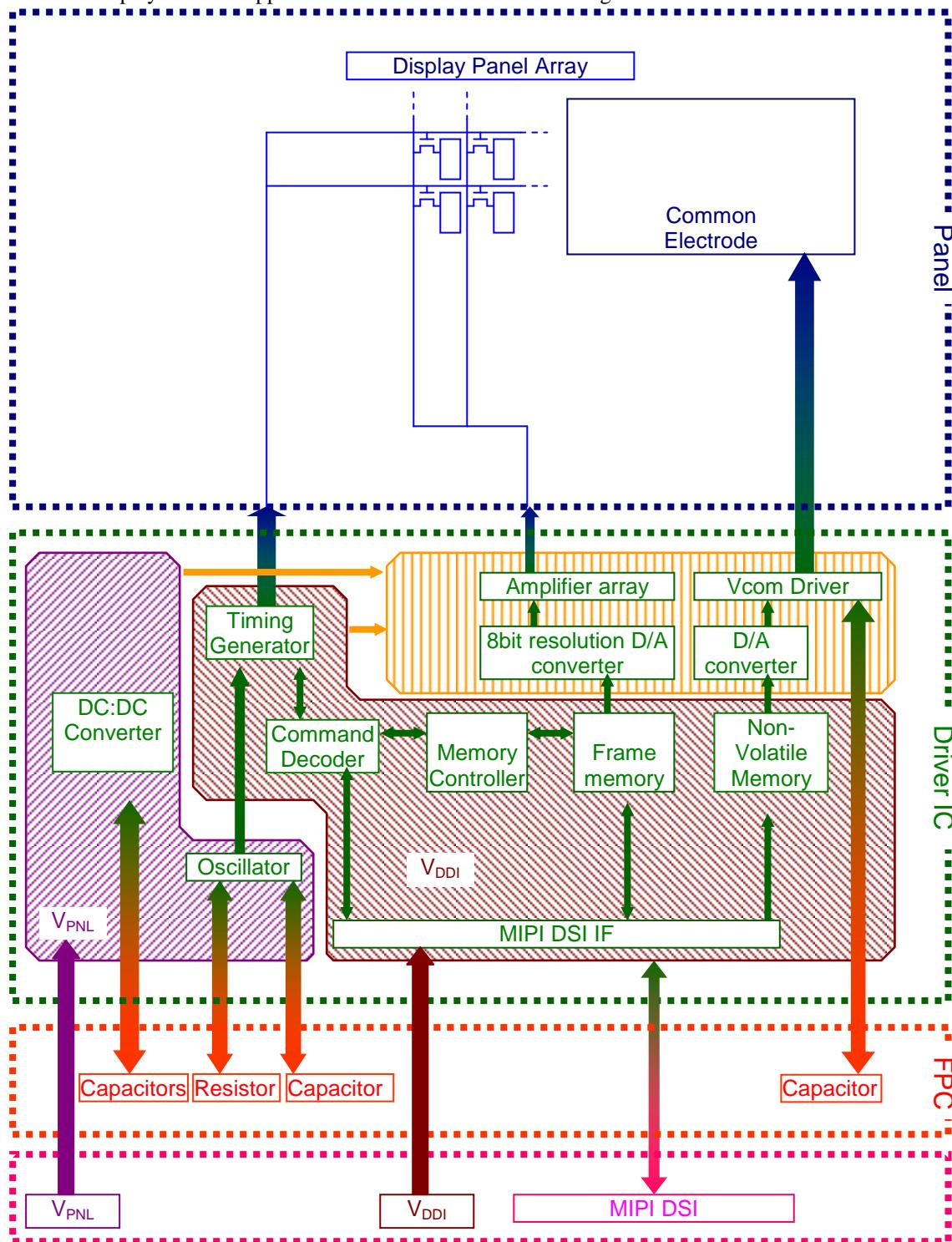


Figure 1: Display Module Block Diagram

4 Display Module Pin Configuration (example)

Note: The display supplier will enclose the actual display module pin configuration.

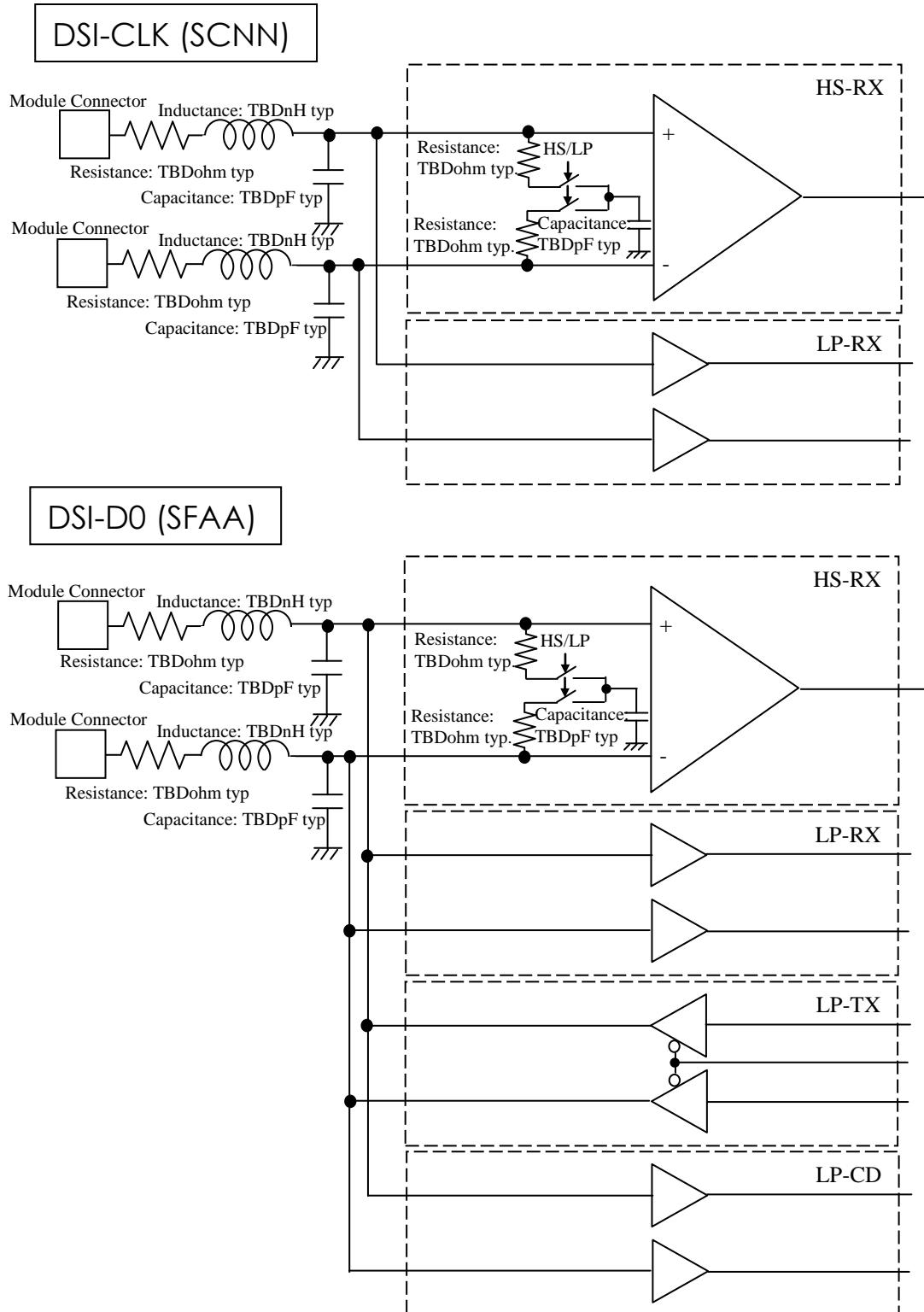


Figure 2: Display Module Pin Configuration 1/2

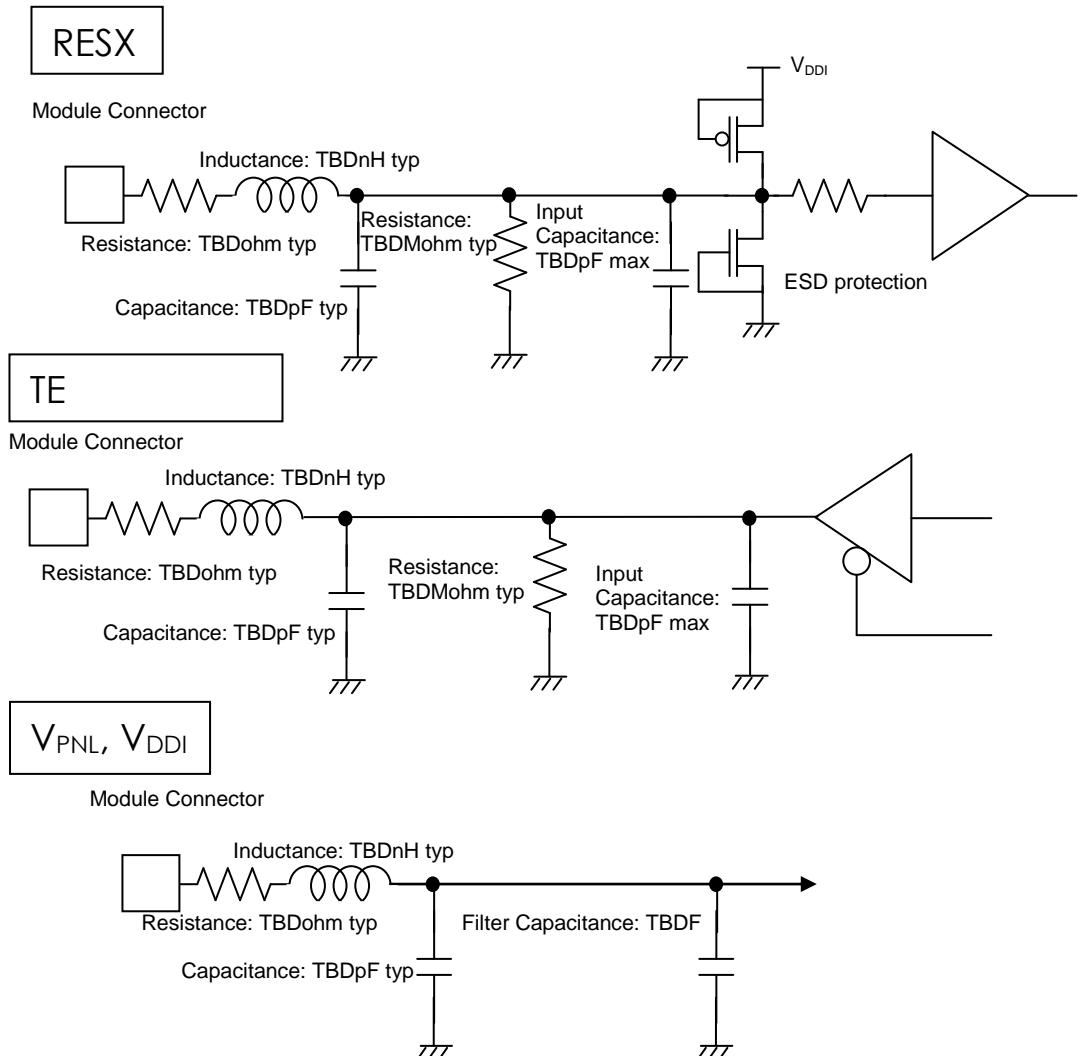


Figure 3: Display Module Pin Configuration 2/2

5 Display Module Pin Description

5.1 Power Supply Pins

Table 1: Power Supply

Symbol	Name	Description
V _{PNL}	Panel Power	Power Supply for Panel
V _{DDI}	Digital Power	Low voltage power supply for logic circuits
GND	Ground	GND

5.2 DSI Interface Logic

Table 2: DSI Interface Logic

Symbol	Name	Note	I/O	Description
DSI-CLK+	DSI Clock +	2	I	DSI Clock +, SCNN
DSI-CLK-	DSI Clock -	2	I	DSI Clock -, SCNN
DSI-D0+	DSI D0 +	2	I/O	DSI Data 0 +, SFAA
DSI-D0-	DSI D0 -	2	I/O	DSI Data 0 -, SFAA
RESX	Reset	1	I	Reset when low.
Vsel	Voltage selection for TE /Resx line	-	I	I/O voltage selection input When VSEL is high level, I/O voltage is typically 1.8V When VSEL is low level, I/O voltage is typically 1.2V
TE	Tearing Effect Output	-	O	Tearing Effect Output line to synchronise MCU to Frame writing, activated by S/W command. When this line is not activated, then pin is low.

Notes:

1. Pull-Up or Pull-Down resistors are not on the display module. They are on the MCU.
2. Connected to DSI

5.3 MCU and Display Module Interface Configurations

5.3.1 DSI with TE Line

The display module, which is using DSI and the TE line, is connected to the MCU as it is illustrated below.

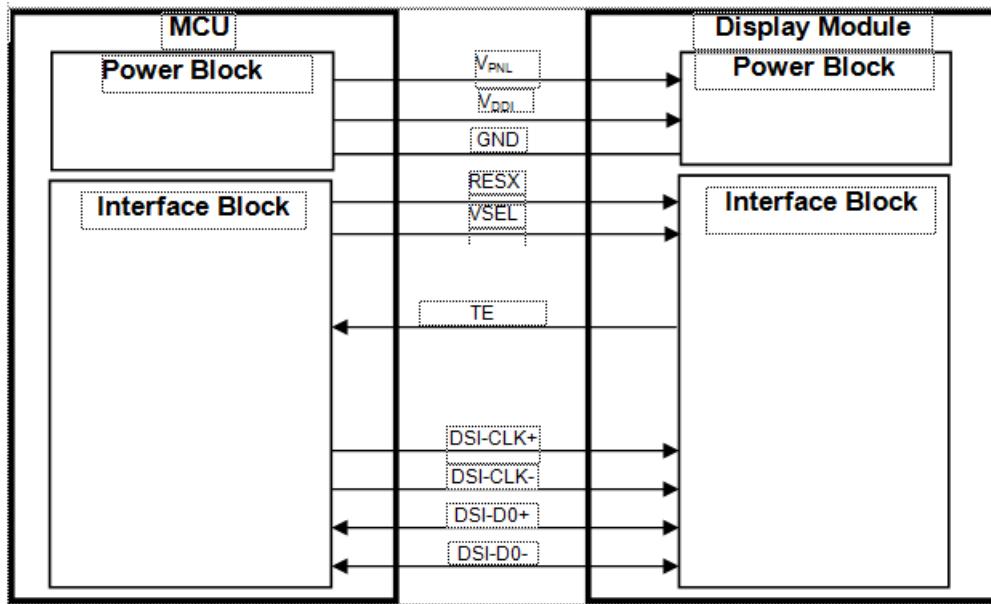


Figure 4: DSI with TE Line

Note: TE Line is enabled on the display module by the display module supplier e.g. a setting on EEPROM or separated pin on the display driver IC.

5.3.2 DSI without TE Line

The display module, which is using DSI without the TE line, is connected to the MCU as it is illustrated below.

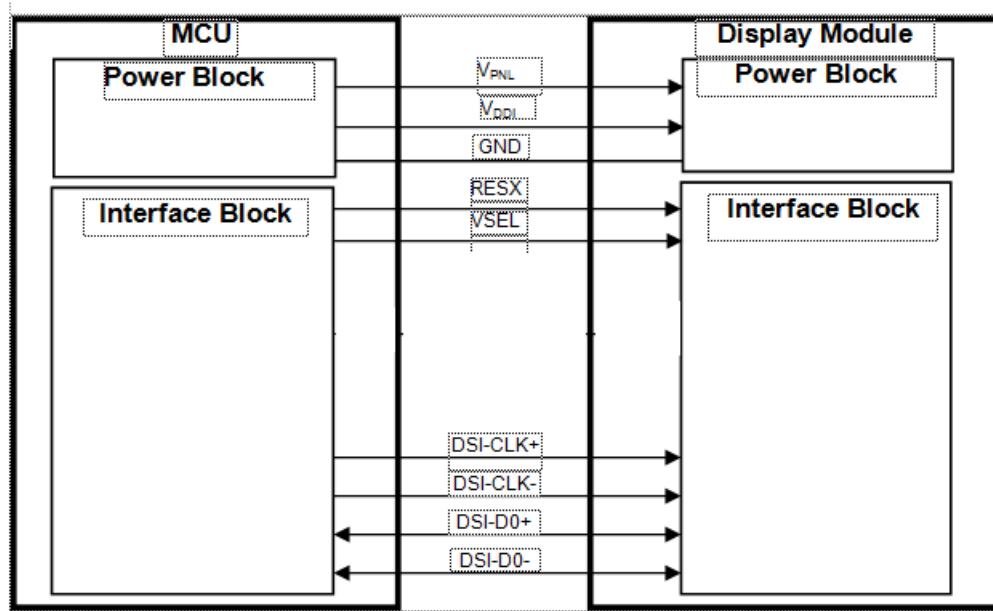


Figure 5: DSI without TE Line

Note: TE Line is disabled on the display module by the display module supplier e.g. a setting on EEPROM or separated pin on the display driver IC. This means that “9.2.25 Tearing Effect Line On (35h)” command cannot activate a separated TE line as it can do an implementation which is in chapter “5.3.1 DSI with TE Line”.

6 Display Module Electrical Characteristics

6.1 Absolute Maximum Ratings

Table 3: Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Panel Power Supply Voltage	V _{PNL}	-0.3 to +4.8V *3	V
Power Supply Voltage(Logic)	V _{DDI}	-0.3 to +2.5	V
Logic Signal Input Voltage	V _I	-0.3 to +2.5	V
Logic Signal Output Voltage	V _O	-0.3 to +2.5	V
Differential Input Voltage	DSI-CLK+, DSI-CLK-, DSI-Dn+, DSI-Dn-	-0.3 to +1.8	V

Notes:

1. Ta = -30 to 70 °C (to +85 °C no damage)
2. n = 0
3. Intermittent voltage max 5.4V allowed maximum 1.4seconds in V_{PNL} and display will not see permanent damage

6.2 DC Characteristics

DSI is using different state codes which are depending on DC voltage levels of the clock and data lanes. The meaning of the state codes are defined on the following table.

Table 4: DSI State Codes and DC Characteristics

State Code	Line DC Voltage Levels	
	CLK+ or Dn+ -line	CLK- or Dn- -line
HS-0	Low (HS)	High (HS)
HS-1	High (HS)	Low (HS)
LP-00	Low (LP)	Low (LP)
LP-01	Low (LP)	High (LP)
LP-10	High (LP)	Low (LP)
LP-11	High (LP)	High (LP)

Note: n = 0

DC levels of the LP-00, LP-01, LP-10 and LP-11 are defined on Table 7: DC Characteristics for DSI LP mode when LP-RX, LP-CD or LP-TX is mentioned on the condition column.

DC levels of the HS-0 and HS-0 are defined on Table 9: DC Characteristics for DSI HS mode. See also Figure 8: Differential Inputs Logical ‘0’s and ‘1’s, Threshold High/Low, Differential Voltage Range.

Table 5: DC Characteristics for Power Lines

Parameter	Symbol	Condition	Specification			unit
			min	typ	max	
Panel Power Supply Voltage	V_{PNL}	Panel Voltage	2.3	3.7	4.8	V
Power Supply Voltage(Logic)	V_{DDI}	I/O supply Voltage	1.65	1.8	1.95	V

Ta = -30 to 70 °C (to +85 °C no damage)

Table 6: Noise on Power Supply Lines

Parameter	Symbol	Condition	Max.	Unit
Panel Power Supply Voltage Noise	V_{PNL_NOISE}	Noise Range, 0 to 100MHz, Sinusoidal Wave	100	mV, peak-to-peak
		Noise Range, 0 to 30kHz, Pulse Wave with Duty Cycle (50%/50%)	500	mV, peak-to-peak
Power Supply Voltage(Logic) Noise	V_{DDI_NOISE}	Noise Range, 0 to 100MHz, Sinusoidal Wave	100	mV, peak-to-peak,

Notes:

1. Ta = -30 to 70 °C (to +85 °C no damage)
2. These values are not symmetric amplitude, which centre points are V_{DDI} or V_{PNL} . See examples as reference purposes, when V_{PNL_NOISE} and V_{DDI_NOISE} are maximums, below.

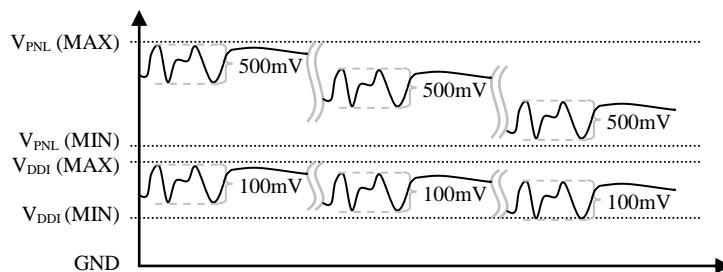
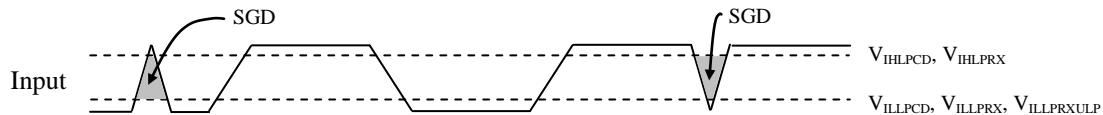
**Figure 6: Noise on Power Supply Lines**

Table 7: DC Characteristics for DSI LP mode

Parameter	Symbol	Condition	Specification			unit
			min	typ	max	
Logic High level input voltage	V _{IH}	Note 2	0.7V _{DDI}		V _{DDI}	V
Logic Low level input voltage	V _{IL}	Note 2	0.0		0.3V _{DDI}	V
Logic High level output voltage	V _{OH}	Note 3; I _{OUT} = -1mA	0.8V _{DDI}		V _{DDI}	V
Logic Low level output voltage	V _{OL}	Note 3; I _{OUT} = +1mA	0.0		0.2V _{DDI}	V
Logic High level input voltage	V _{IHLPCD}	LP-CD, Note 4	450		1350	mV
Logic Low level input voltage	V _{ILLPCD}	LP-CD, Note 4	0.0		200	mV
Logic High level input voltage	V _{IHLPRX}	LP-RX (CLK, D0), Note 4	880		1350	mV
Logic Low level input voltage	V _{ILLPRX}	LP-RX (CLK, D0), Note 4	0.0		550	mV
Logic Low level input voltage	V _{ILLPRXULP}	LP-RX (CLK ULP mode), Note 4	0.0		300	mV
Logic High level output voltage	V _{OHLPTX}	LP-TX (D0), Note 4	1.1		1.3	V
Logic Low level output voltage	V _{OLLPTX}	LP-TX (D0), Note 4	-50		50	mV
Logic High level input current	I _{IH}	Note 2, Note 4, LP-CD, LP-RX			10	uA
Logic Low level input current	I _{IL}	Note 2, Note 4, LP-CD, LP-RX	-10			uA

Notes:

1. Ta = -30 to 70 °C (to +85 °C no damage)
2. RESX
3. TE
4. DSI High Speed mode is off

**Figure 7: Spike/Glitch Rejection - DSI****Table 8: Spike/Glitch Rejection - DSI**

Signal	Symbol	Parameter	Min	Max	Unit
Input (DSI-CLK+/-, DSI-Dn+/-)	SGD	Input Pulse Rejection for DSI		300	Vps

Notes:

1. Peak Interference Amplitude max. 200mV and Interference Frequency min. 450MHz.
2. n = 0 and 1

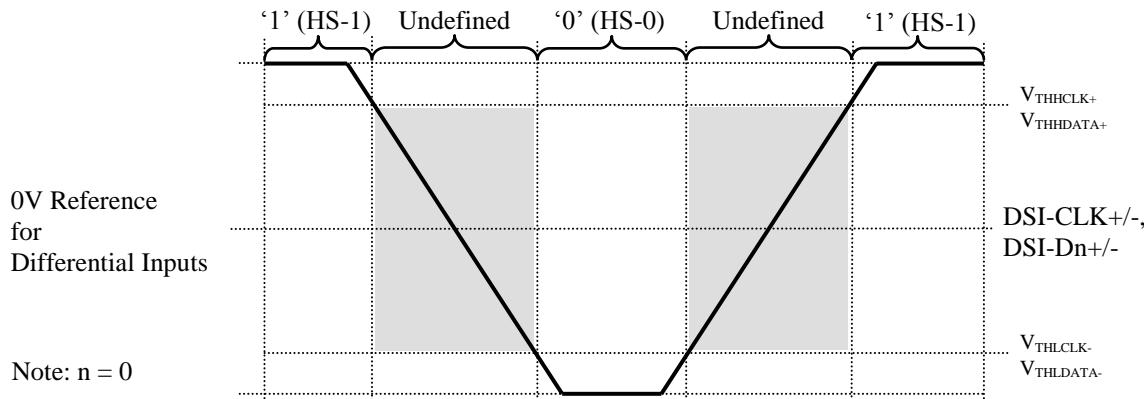
Table 9: DC Characteristics for DSI HS mode

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Input Common Mode Voltage for Clock	V_{CMCLK}	DSI-CLK+/-, Note 2 and 3	70		330	mV
Input Common Mode Voltage for Data	V_{CMDATA}	DSI-Dn+/-, Note 2, 3 and 5	70		330	mV
Common Mode Ripple for Clock Equal or Less than 450MHz	$V_{CMRCLKL450}$	DSI-CLK+/-, Note 4	-50		50	mV
Common Mode Ripple for Data Equal or Less than 450 MHz	$V_{CMRDATAL450}$	DSI-Dn+/-, Note 4 and 5	-50		50	mV
Common Mode Ripple for Clock More than 450MHz (peak sine wave)	$V_{CMRCLKM450}$	DSI-CLK+/-			100	mV
Common Mode Ripple for Data More than 450 MHz (peak sine wave)	$V_{CMRDATAM450}$	DSI-Dn+/-, Note 5			100	mV
Differential Input Low Level Threshold Voltage for Clock	$V_{THLCLK-}$	DSI-CLK+/-	-70			mV
Differential Input Low Level Threshold Voltage for Data	$V_{THLDATA-}$	DSI-Dn+/-, note 5	-70			mV
Differential Input High Level Threshold Voltage for Clock	$V_{THHCLK+}$	DSI-CLK+/-			70	mV
Differential Input High Level Threshold Voltage for Data	$V_{THHDATA+}$	DSI-Dn+/-, Note 5			70	mV
Single-ended Input Low Voltage	V_{ILHS}	DSI-CLK+/-, DSI-Dn+/-, Note 3 and 5	-40			mV
Single-ended Input High Voltage	V_{IHHS}	DSI-CLK+/-, DSI-Dn+/-, Note 3 and 5			460	mV
Differential Termination Resistor	R_{TERM}	DSI-CLK+/-, DSI-Dn+/-, Note 5	80	100	125	Ω
Single-Ended Threshold Voltage for Termination Enable	$V_{TERM-EN}$	DSI-CLK+/-, DSI-Dn+/-, Note 5			450	mV
Termination Capacitor	C_{TERM}	DSI-CLK+/-, DSI-Dn+/-, Note 5			14	pF

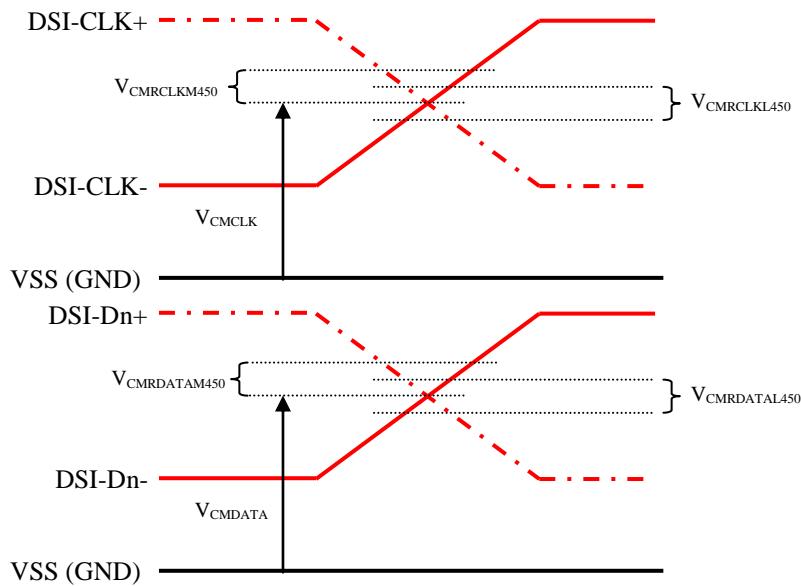
Notes:

1. $T_a = -30$ to 70 °C (to $+85$ °C no damage), $V_{DDI} = 1.65$ to 1.95 V, GND = 0V
2. Includes 50mV (-50mV to 50mV) ground difference
3. Without $V_{CMRCLKM450}/V_{CMRDATAM450}$
4. Without 50mV (-50mV to 50mV) ground difference
5. $n = 0$

The DSI receiver (HS mode) is understanding that there is logical ‘1’ (HS-1) when a differential voltage is more than $V_{THH(CLK+/DATA+)}$ and the DSI receiver (HS mode) is understanding that there is logical ‘0’ (HS-0) when a differential voltage is more than $V_{THL(CLK-/DATA-)}$. There is undefined state if the differential voltage is less than $V_{THH(CLK+/DATA+)}$ and less than $V_{THL(CLK-/DATA-)}$. A reference figure is below.

**Figure 8: Differential Inputs Logical ‘0’s and ‘1’s, Threshold High/Low, Differential Voltage Range**

May 18th, 2012



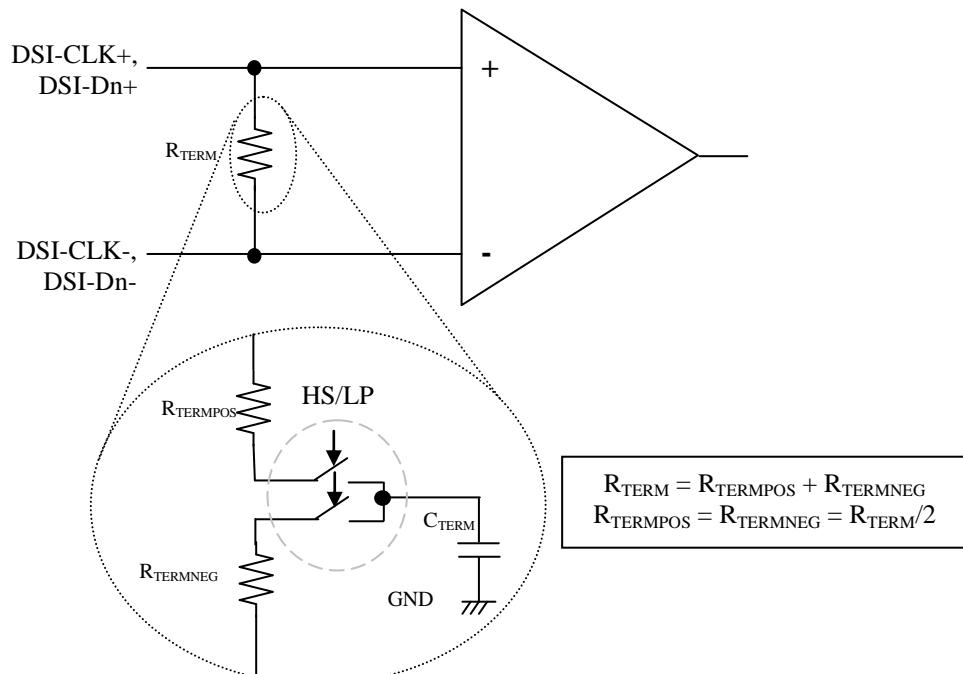
Note: n = 0

Figure 9: Common Mode Voltage on Clock and Data Channels

The termination resistor (R_{TERM}) of the differential DSI receiver can be driven two different states by the receiver:

- Low Power (LP) mode when the termination resistor is not connected between differential inputs (DSI-CLK+ <=> DSi-CLK- or DSi-D0+ <=> DSi-D0-)
- High Speed (HS) mode when the termination resistor is connected between differential inputs (DSI-CLK+ <=> DSi-CLK- or DSi-D0+ <=> DSi-D0-)

The termination switch (HS/LP), when the termination resistor is not connected, is illustrated below.



Note: n = 0

Figure 10: Differential Pair Termination Resistor on the Receiver Side

6.3 Power Consumption

Note: Power consumption table is included display module specification.

6.4 Measurement Point for DC Characteristics

Note: Measurement Point for DC Characteristics is illustrated below: -

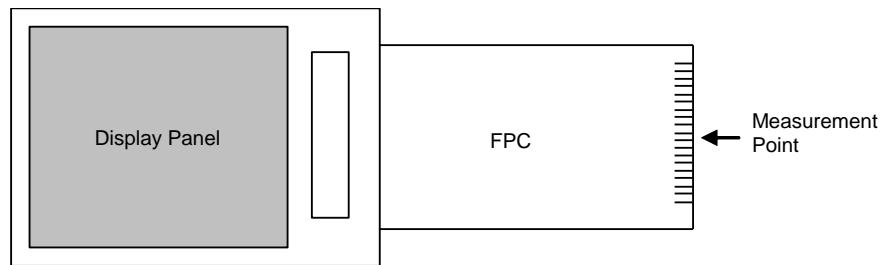


Figure 11: Measurement Point for DC Characteristics

7 Timing Characteristics

7.1 DSI

7.1.1 High Speed Mode

7.1.1.1 Clock Channel Timings

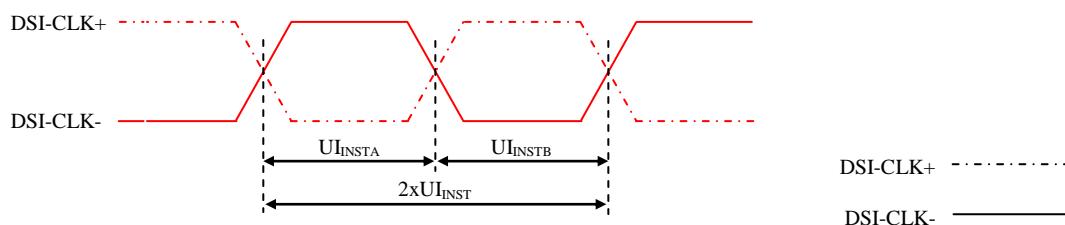


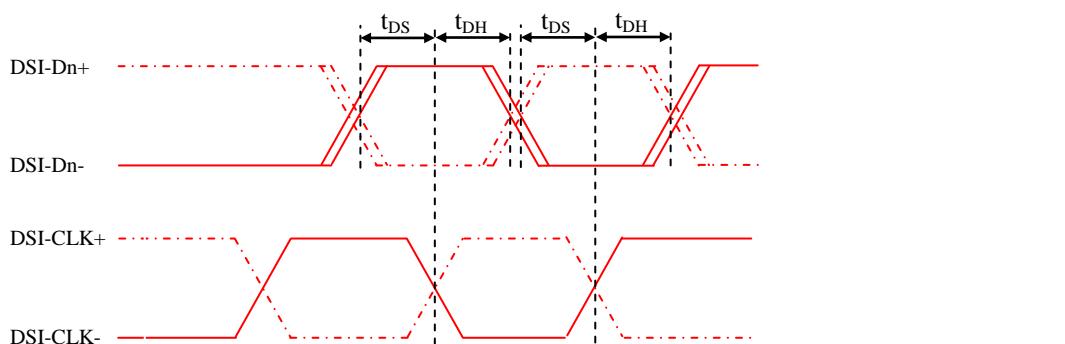
Figure 12: DSI Clock Channel Timings

Table 10: DSI Clock Channel Timings

Signal	Symbol	Parameter	Min	Max	Unit
DSI-CLK+/-	2xUI _{INST}	Double UI instantaneous	4	25	ns
DSI-CLK+/-	UI _{INSTA} , UI _{INSTB}	UI instantaneous Halfs	2	12.5	ns

Note: UI = UI_{INSTA} = UI_{INSTB}

7.1.1.2 Data to Clock Channel Timings



Note: n = 0

Figure 13: DSI Data to Clock Channel Timings

DSI-CLK+, DSI-Dn+ (dashed line)

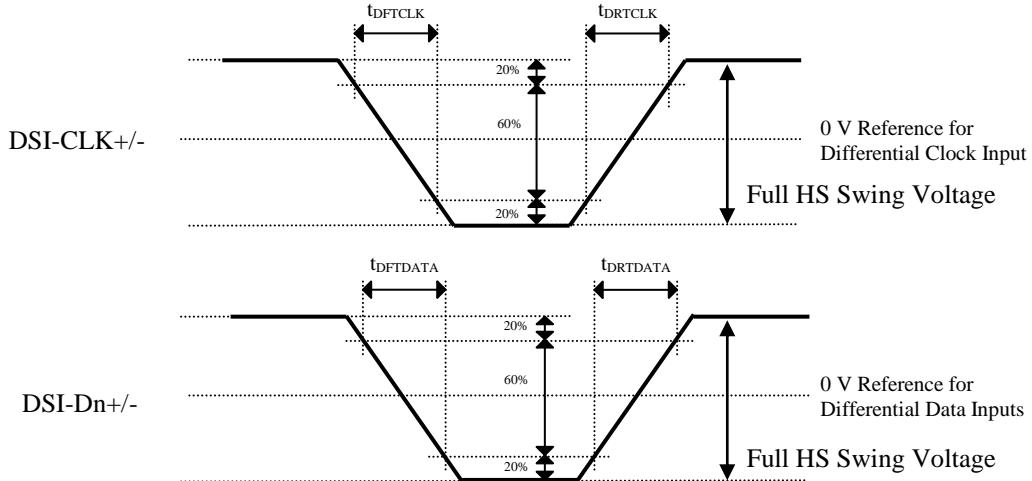
DSI-CLK-, DSI-Dn- (solid line)

Table 11: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max	Unit
DSI-Dn+/-	t _{DS}	Data to Clock Setup Time	0.15xUI	-	ps
DSI-Dn+/-	t _{DH}	Clock to Data Hold Time	0.15xUI	-	ps

Note: n = 0

7.1.1.3 Rise and Fall Timings



Note: n = 0

Figure 14: Rise and Fall Timings on Clock and Data Channels

Table 12: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Differential Rise Time for Clock	t_{DRTCLK}	DSI-CLK+/-				Note 2 ps
Differential Rise Time for Data	$t_{DRTDATA}$	DSI-Dn+/-				Note 2 ps
Differential Fall Time for Clock	t_{DFTCLK}	DSI-CLK+/-				Note 2 ps
Differential Fall Time for Data	$t_{DFTDATA}$	DSI-Dn+/-				Note 2 ps

Notes:

1. n = 0
2. The display module has to meet timing requirements, what are defined for the transmitter (MCU) on MIPI D-Phy standard

7.1.2 Low Power Mode

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) sequence below.

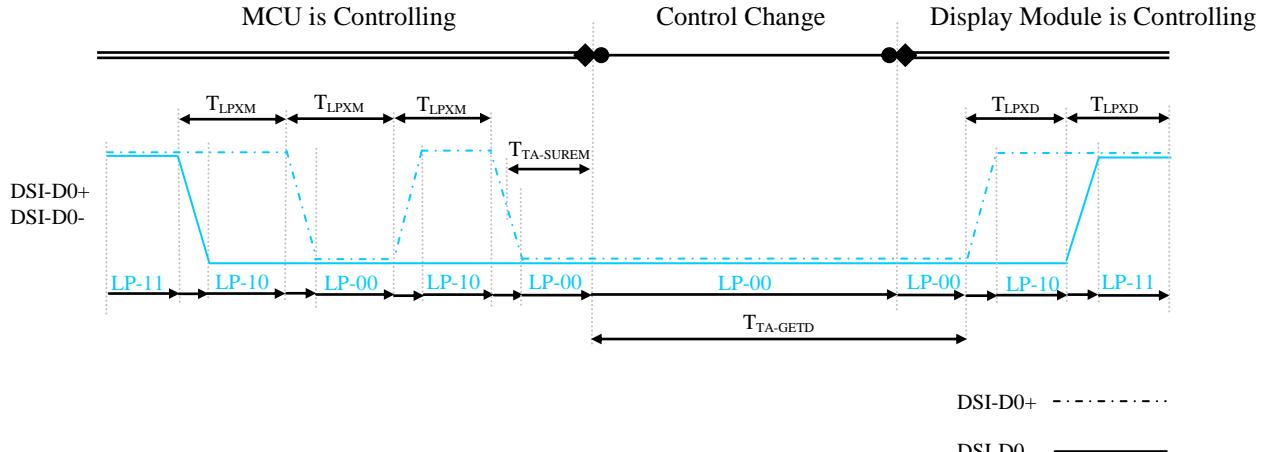


Figure 15: BTA from the MCU to the Display Module

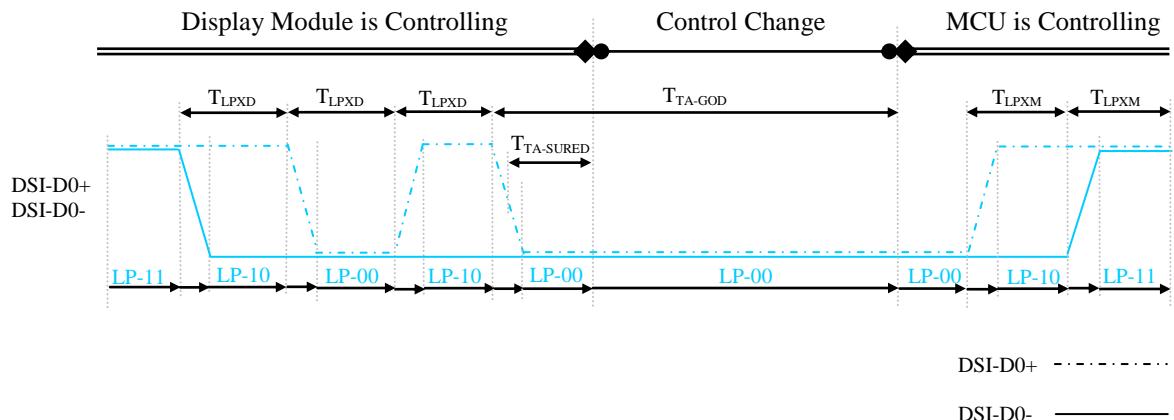


Figure 16: BTA from the Display Module to the MCU

Table 13: Low Power State Period Timings – Table A

Signal	Symbol	Description	Min	Max	Unit
Input (DSI-D0+/-)	T _{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU => Display Module	50	75	ns
Input (DSI-D0+/-)	T _{TA-SUREM}	Time-Out before the display module starts driving	T _{LPXM}	2xT _{LPXM}	ns
Output (DSI-D0+/-)	T _{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module => MCU	50	75	ns
Output (DSI-D0+/-)	T _{TA-SURED}	Time-Out before the MCU starts driving	T _{LPXD}	2xT _{LPXD}	ns

Table 14: Low Power State Period Timings – Table B

Signal	Symbol	Description	Time	Unit
Input (DSI-D0+/-)	T _{TA-GETD}	Time to drive LP-00 by Display Module	5xT _{LPXD}	ns
Output (DSI-D0+/-)	T _{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	4xT _{LPXM}	ns

The Bus Turnaround (BTA) sequence is described on chapter “8.1.2.3.4 Bus Turnaround (BTA)”.

7.1.3 DSI Data Bursts - High Speed Mode to/from Low Power Mode

7.1.3.1 Data Lanes from Low Power Mode to High Speed Mode

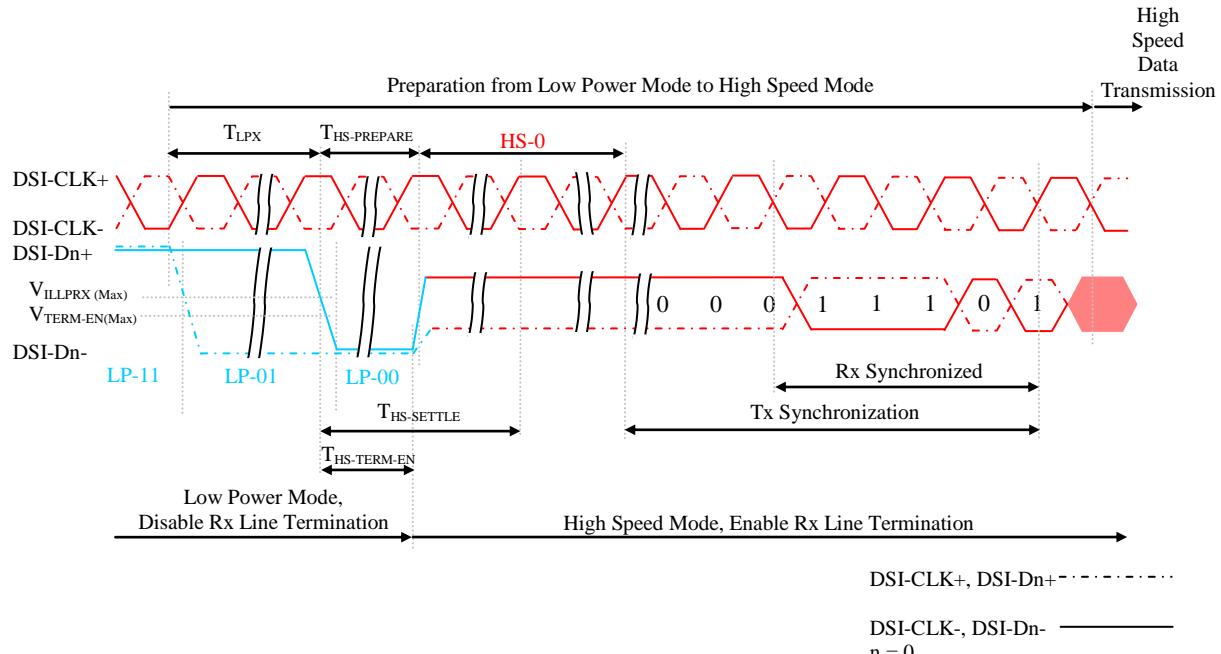


Figure 17: Data Lanes - Low Power Mode to High Speed Mode Timings

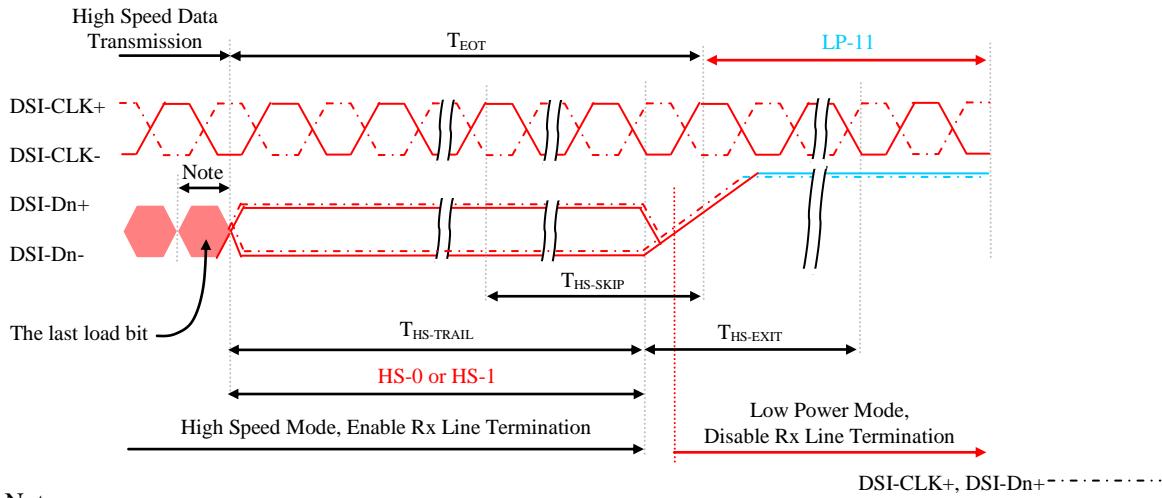
Table 15: Data Lanes - Low power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
Input (DSI-Dn+/-)	T_{LPX}	Length of any Low Power State Period	50	-	ns
Input (DSI-Dn+/-)	$T_{HS-PREPARE}$	Time to Drive LP-00 to prepare for HS Transmission	$40 + 4xUI$	$85 + 6xUI$	ns
Input (DSI-Dn+/-)	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when D_n crosses V_{ILMAX}	-	$35 + 4xUI$	ns

Notes:

1. See UI definition on Table 10: DSI Clock Channel Timings.
2. $n = 0$
3. The display module has to meet timing requirements, what are defined for the transmitter (MCU) on MIPI D-Phy standard

7.1.3.2 Data Lanes from High Speed Mode to Low Power Mode



Note:

If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.
If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

DSI-CLK+, DSi-Dn+ $\cdots \cdots \cdots$

DSI-CLK-, DSi-Dn- ---
 $n = 0$

Figure 18: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 16: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
Input (DSI-Dn+/-)	$T_{HS-SKIP}$	Time-Out at Display Module to Ignore Transition Period of EoT	40	$55+4xUI$	ns
Input (DSI-Dn+/-)	$T_{HS-EXIT}$	Time to Drive LP-11 after HS Burst	100	-	ns

Notes:

1. $n = 0$
2. The display module has to meet timing requirements, what are defined for the transmitter (MCU) on MIPI D-Phy standard

7.1.4 DSI Clock Bursts – High Speed Mode to/from Low Power Mode

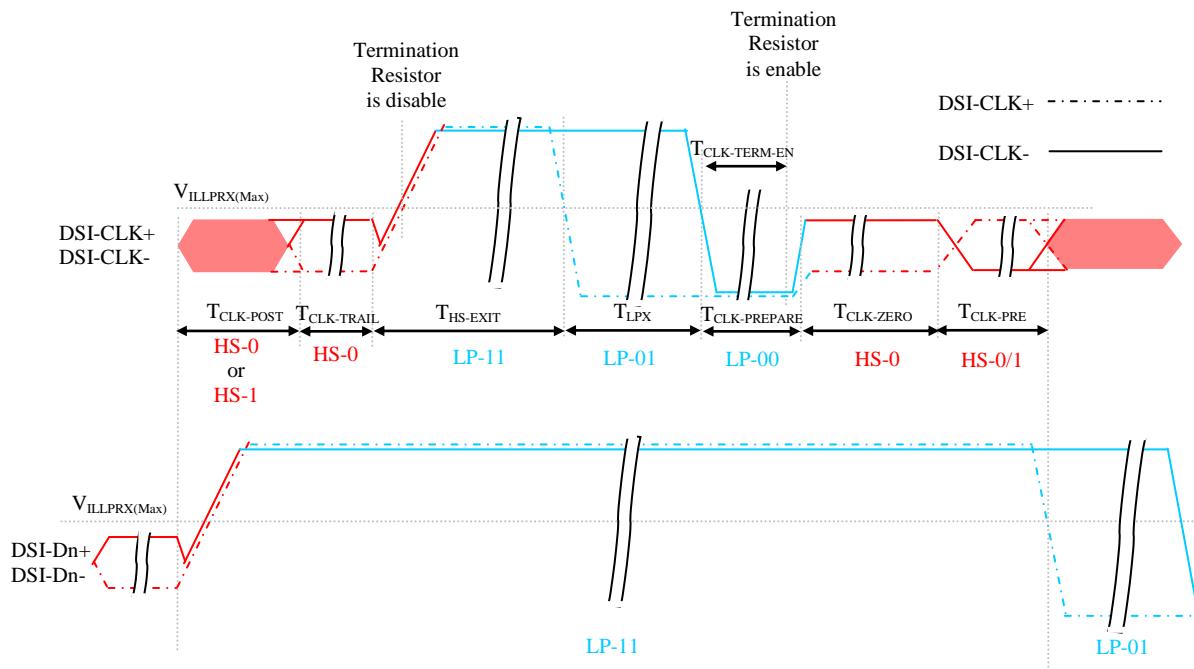


Figure 19: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 17: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
Input (DSI-CLK+/-)	$T_{\text{CLK-POST}}$	Time that the MCU shall continue sending HS clock after The last associated Data Lane has transitioned to LP mode	$60 + 52x\text{UI}$	-	ns
Input (DSI-CLK+/-)	$T_{\text{CLK-TRAIL}}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
Input (DSI-CLK+/-)	$T_{\text{HS-EXIT}}$	Time to drive LP-11 after HS burst	100	-	ns
Input (DSI-CLK+/-)	$T_{\text{CLK-PREPARE}}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
Input (DSI-CLK+/-)	$T_{\text{CLK-TERM-EN}}$	Time-out at Clock Lane Display Module to enable HS Termination	-	38	ns
Input (DSI-CLK+/-)	$T_{\text{CLK-PREPARE}} + T_{\text{CLK-ZERO}}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
Input (DSI-CLK+/-)	$T_{\text{CLK-PRE}}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	$8x\text{UI}$	-	ns

Note: See UI Definition on Table 10: DSI Clock Channel Timings

7.2 Measurement Point for Timing Characteristics

Note: Measurement Point for Timing Characteristics is illustrated below: -

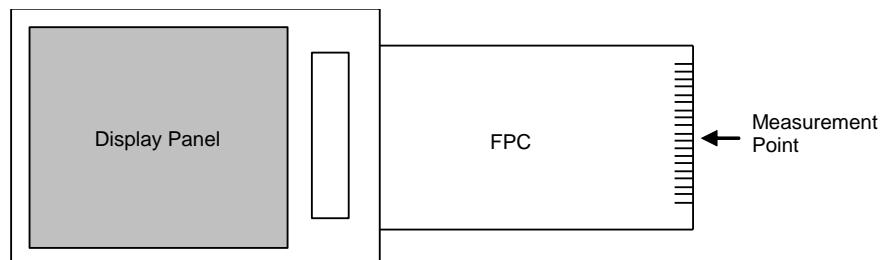


Figure 20: Measurement Point for Timing Characteristics

8 Functional Description

8.1 DSI Input

8.1.1 General Description

Communication sequences between the MCU and the display module are described on chapter “8.1.3.3 Communication Sequences”.

The communication can be separated 2 different levels between the MCU and the display module:

- Low level communication what is done on the interface level
- High level communication what is done on the packet level

8.1.2 Interface Level Communication

8.1.2.1 General

The display module uses data and clock lane differential pairs for DSI (DSI-1M). Both differential lane pairs can be driven Low Power (LP) or High Speed (HS) mode.

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode.

High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode.

There are used different modes and protocols in each mode when there is wanted to transfer information from the MCU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Table 18: High Speed and Low-Power Lane Pair State Codes

Lane Pair State Code	Line DC Voltage Levels		High Speed (HS) Burst Mode	Low-Power (LP)	
	Dn+ -line	Dn- -line		Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential-0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential-1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS-Request	Mark-0
LP-10	High (LP)	Low (LP)	Not Defined	LP-Request	Mark-1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Notes:

1. Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.
2. If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.
3. n = 0

8.1.2.2 DSI-CLK Lanes

DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM), Ultra Low Power Mode (ULPS) or High Speed Clock Mode (HSCM).

Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode (LPM) or Ultra Low Power Mode (ULPS).

Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM).

These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.

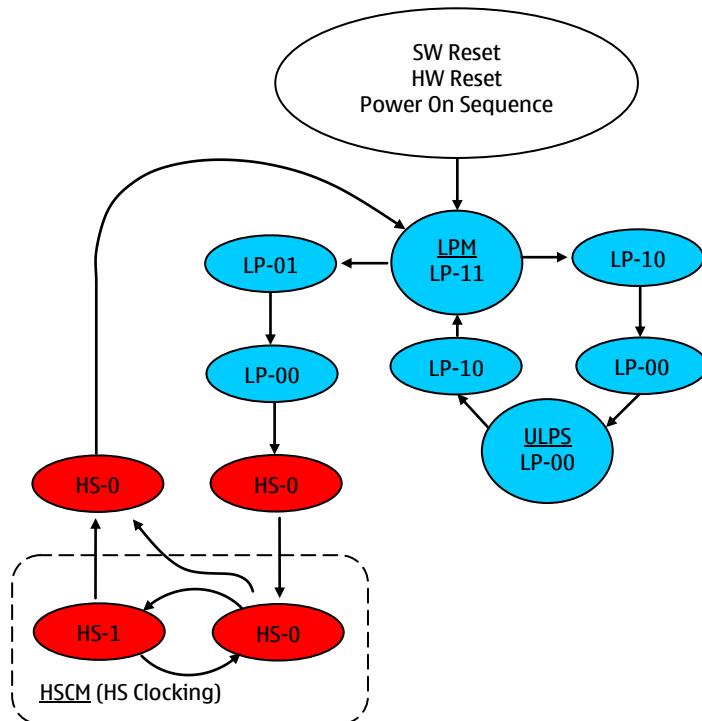


Figure 21: Clock Lanes Power Modes

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8.1.2.2.1 Low Power Mode (LPM)

DSI-CLK+/- lanes can be driven to the Low Power Mode (LPM), when DSI-CLK lanes are entering LP-11 State Code, in three different ways:

- 1) After SW Reset, HW Reset or Power On Sequence =>LP-11
- 2) After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPS, LP-00 State Code) =>LP-10 =>LP-11 (LPM). This sequence is illustrated below.

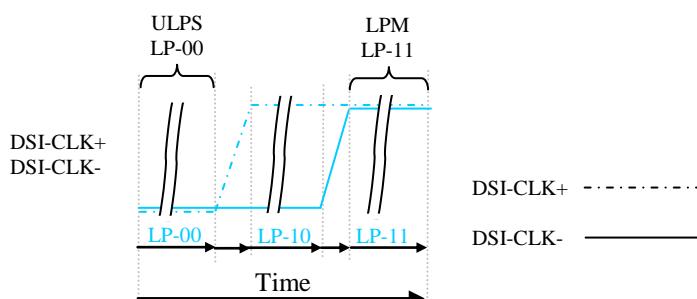


Figure 22: From ULPS to LPM

- 3) After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM). This sequence is illustrated below.

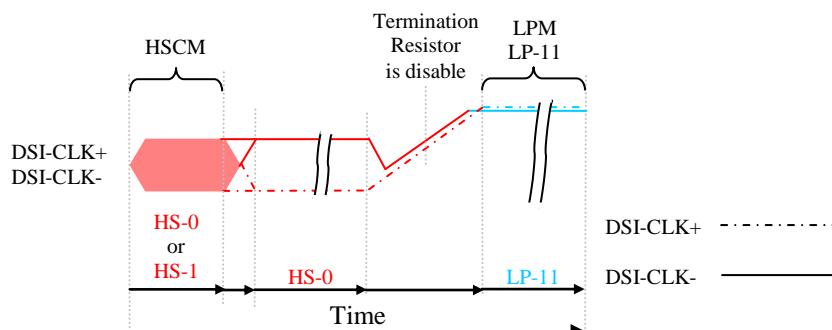


Figure 23: From High Speed Clock Mode (HSCM) to LPM

All three mode changes are illustrated a flow chart below.

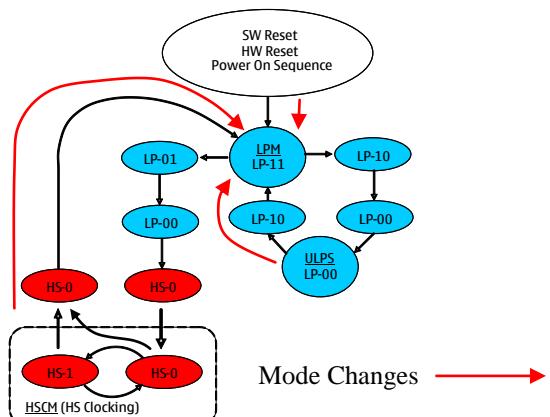


Figure 24: All Three Mode Changes to LPM on the Flow Chart

8.1.2.2.2 Ultra Low Power State (ULPS)

DSI-CLK+/- lanes can be driven to the Ultra Low power state (ULPS), when DSI-CLK lanes are entering LP-00 State Code.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-10 =>LP-00 (ULPS). This sequence is illustrated below.

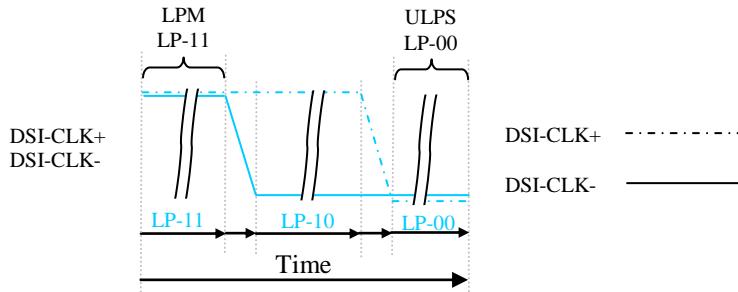


Figure 25: From LPM to ULPS

The mode change is also illustrated below.

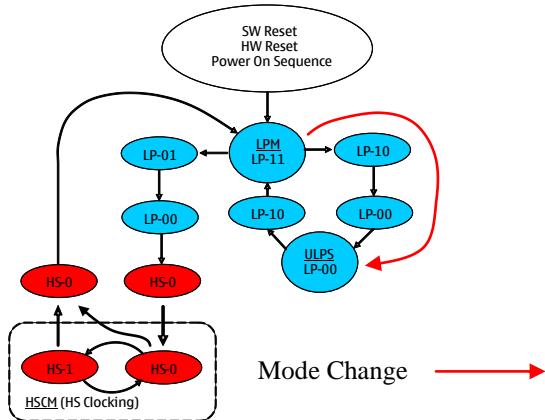


Figure 26: Mode Change from LPM to ULPS on the Flow Chart

8.1.2.2.3 High-Speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

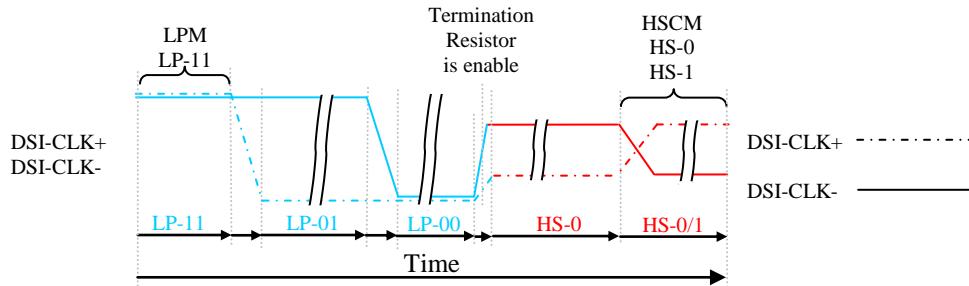


Figure 27: From LPM to HSCM

The mode change is also illustrated below.

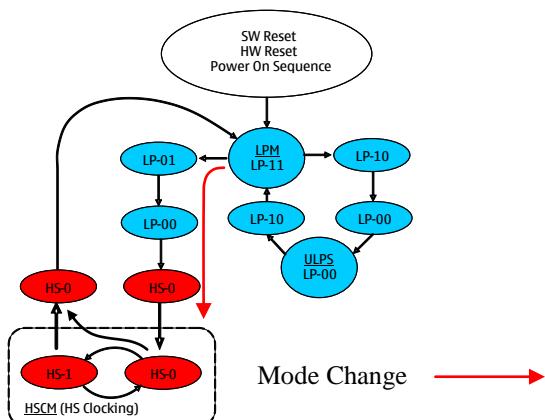


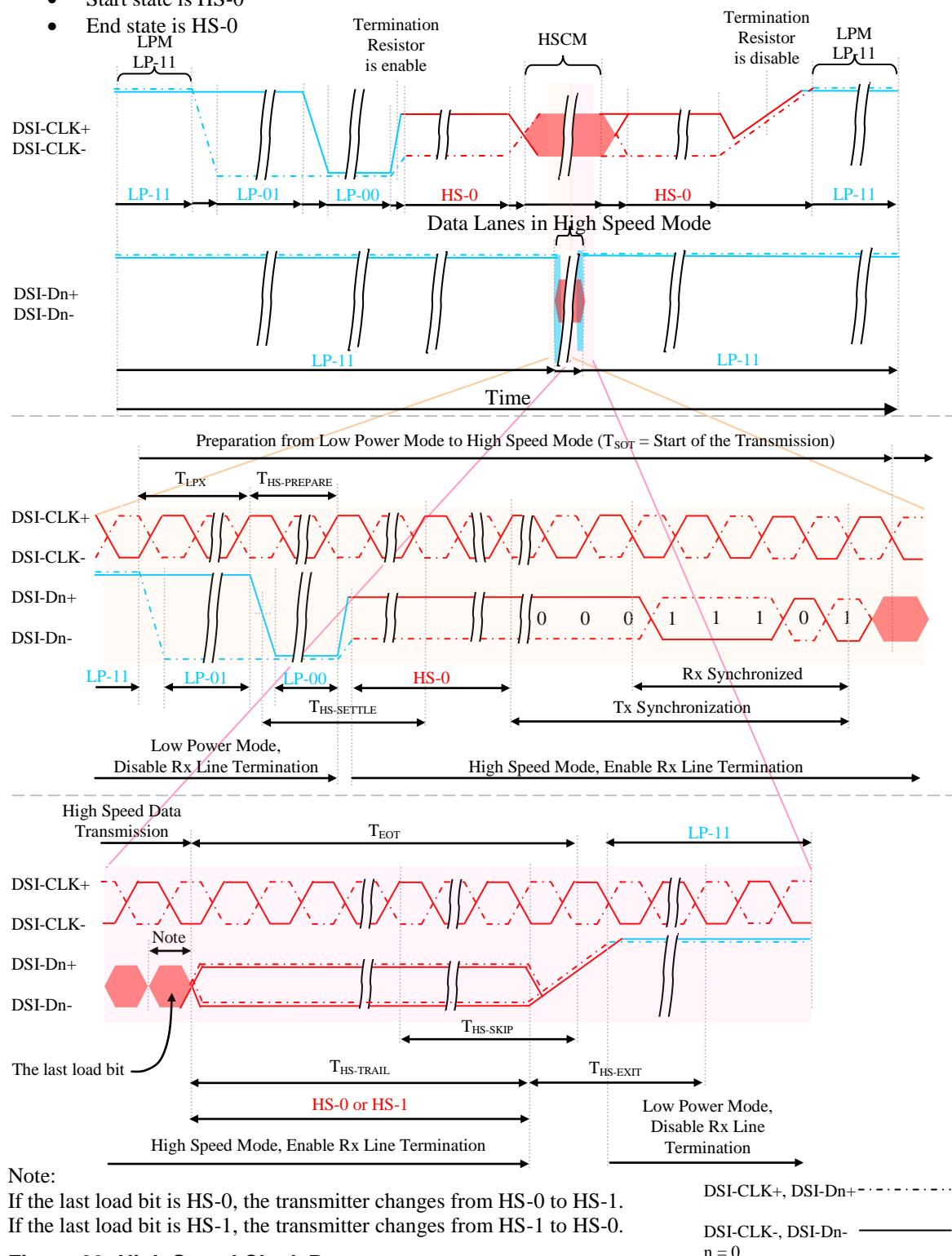
Figure 28: Mode Change from LPM to HSCM on the Flow Chart

May 18th, 2012

The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-D0+/- lanes. The high speed clock continues clocking after the high speed data sending has been stopped.

The burst of the high speed clock consists of:

- Even number of transitions
- Start state is HS-0
- End state is HS-0



Note:

If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

DSI-CLK+, DSI-Dn+
DSI-CLK-, DSI-Dn-
 $n = 0$

Figure 29: High Speed Clock Burst

8.1.2.3 DSI-D0 Data Lanes

8.1.2.3.1 General

DSI-D0+/- Data Lanes can be driven in different modes which are:

- Escape Mode (DSI-D0+/- data lanes are used)
- High-Speed Data Transmission (DSI-D0+/- data lanes are used)
- Bus Turnaround Request (DSI-D0+/- data lanes are used)

These modes and their entering codes are defined on the following table.

Table 19: Entering and Leaving Sequences

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode, Note 1	LP-11 => LP-10 => LP-00 => LP-01 => LP-00	LP-00 => LP-10 => LP-11 (Mark-1)
High-Speed Data Transmission, Note 2	LP-11 => LP-01 => LP-00 => HS-0	(HS-0 or HS-1) => LP-11
Bus Turnaround Request, Note 1, 3	LP-11 => LP-10 => LP-00 => LP-10 => LP-00	High-Z

Notes:

1. DSI-D0+/- data lanes are used.
2. DSI-D0+/- data lanes are used.
3. More information on chapter “8.1.2.3.4 Bus Turnaround ”.

8.1.2.3.2 Escape Modes

DSI-D0+/- data lanes can be used in different Escape Modes when data lanes are in Low Power (LP) mode.

These Escape Modes are used to:

- Send “Low-Power Data Transmission” (LPDT) e.g. from the MCU to the display module,
- Drive data lanes to “Ultra-Low Power State” (ULPS),
- Indicate “Remote Application Reset” (RAR), which is resetting the display module,
- Indicate “Tearing Effect” (TEE), which is used for a TE line event from the display module to the MCU,
- Indicate “Acknowledge” (ACK), which is used for a non-error event from the display module to the MCU.

The basic sequence of the Escape Mode is as follow

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Escape Command (EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit (DSI-D0+ = 1, DSI-D0- = 0) e.g. when DSI-D0- is changing from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this low-to-high-to-low transition for its internal clock.
- A load if it is needed
- Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11
- End: LP-11

This basic construction is illustrated below:

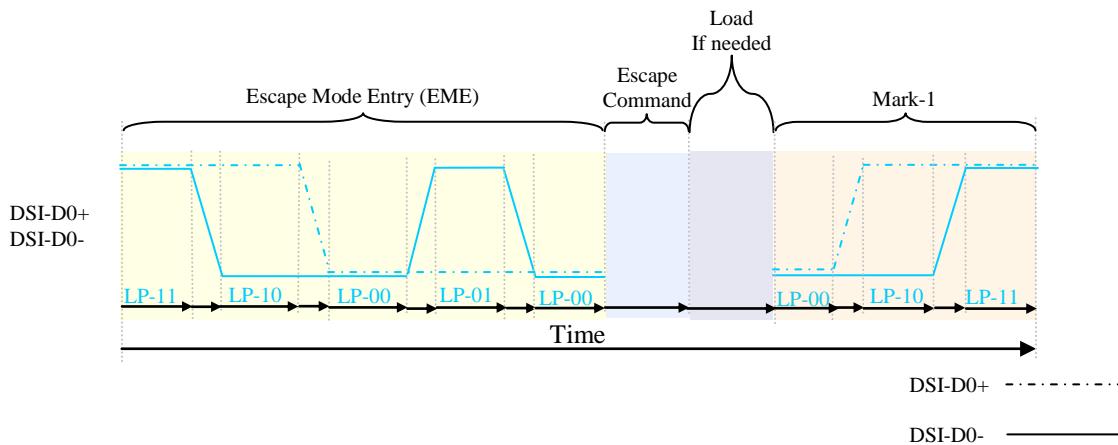


Figure 30: General Escape Mode Sequence

There are a total of eight Escape Commands (EC) divided into two types, Modes and Triggers, (see Table 20: Escape Commands).

An example of a Mode type Escape Command is ‘Ultra-Low Power Mode’ where the MCU instructs the display module to enter it’s Ultra-Low Power Mode.

An example of a Trigger type Escape Command is ‘Tearing Effect’. In this case the MCU has already instructed the display module to provide this trigger and is waiting for the response. The display module then sends a TE trigger (TEE) on the next V-sync event.

Escape commands are defined on the next table.

Table 20: Escape Commands

Escape Command	Command Type Mode/Trigger	Entry Command Pattern (First Bit => Last Bit Transmitted)	Dn	D0
Low-Power Data Transmission	Mode	1110 0001 _{bin}	-	X
Ultra-Low Power Mode	Mode	0001 1110 _{bin}	X	X
Undefined-1, Note 1	Mode	1001 1111 _{bin}	-	-
Undefined-2, Note 1	Mode	1101 1110 _{bin}	-	-
Remote Application Reset	Trigger	0110 0010 _{bin}	-	X
Tearing Effect	Trigger	0101 1101 _{bin}	-	X
Acknowledge	Trigger	0010 0001 _{bin}	-	X
Unknown-5, Note 1	Trigger	1010 0000 _{bin}	-	-

Notes:

1. This Escape command support has not been implemented on the display module.
2. n = 1
3. x = Supported
4. - = Not Supported

8.1.2.3.2.1 Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU.

The Low Power Data Transmission (LPDT) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)
- Load (Data):
 - One or more bytes (8 bit)
 - Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

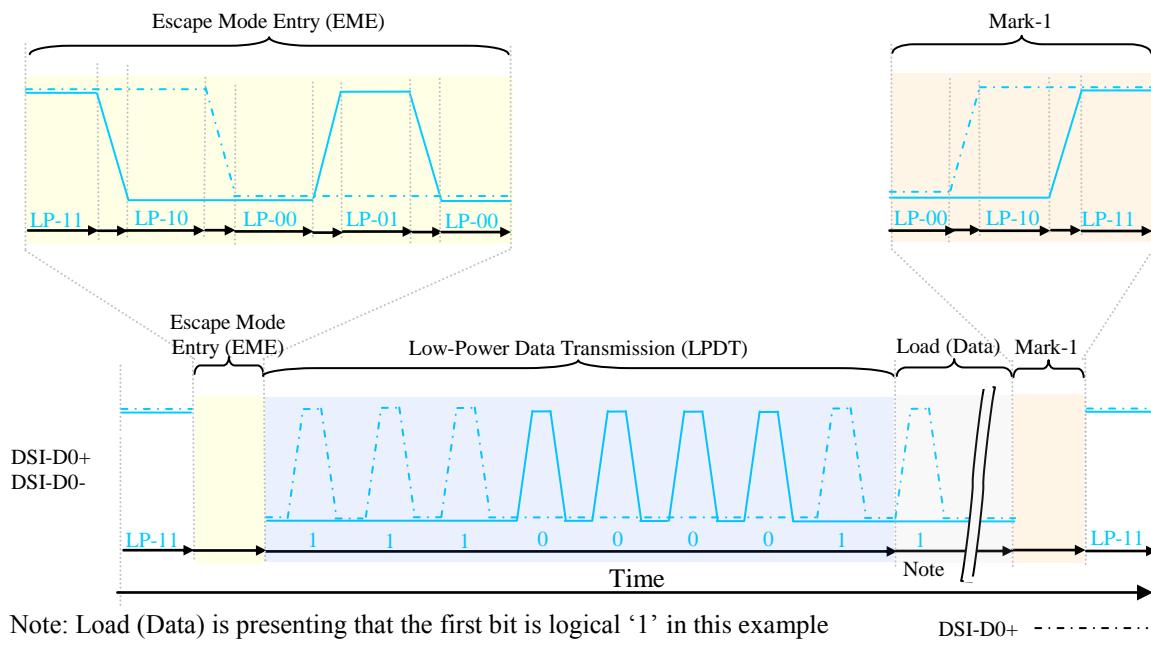


Figure 31: Low-Power Data Transmission (LPDT)

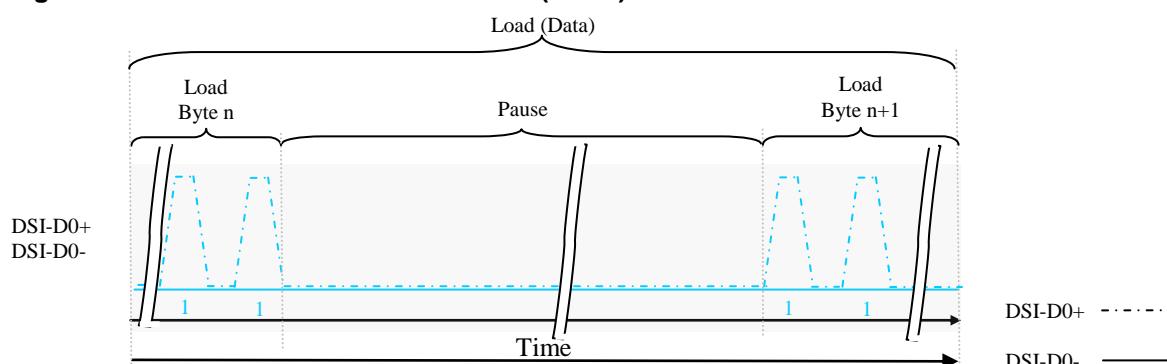


Figure 32: Pause (Example)

8.1.2.3.2.2 Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

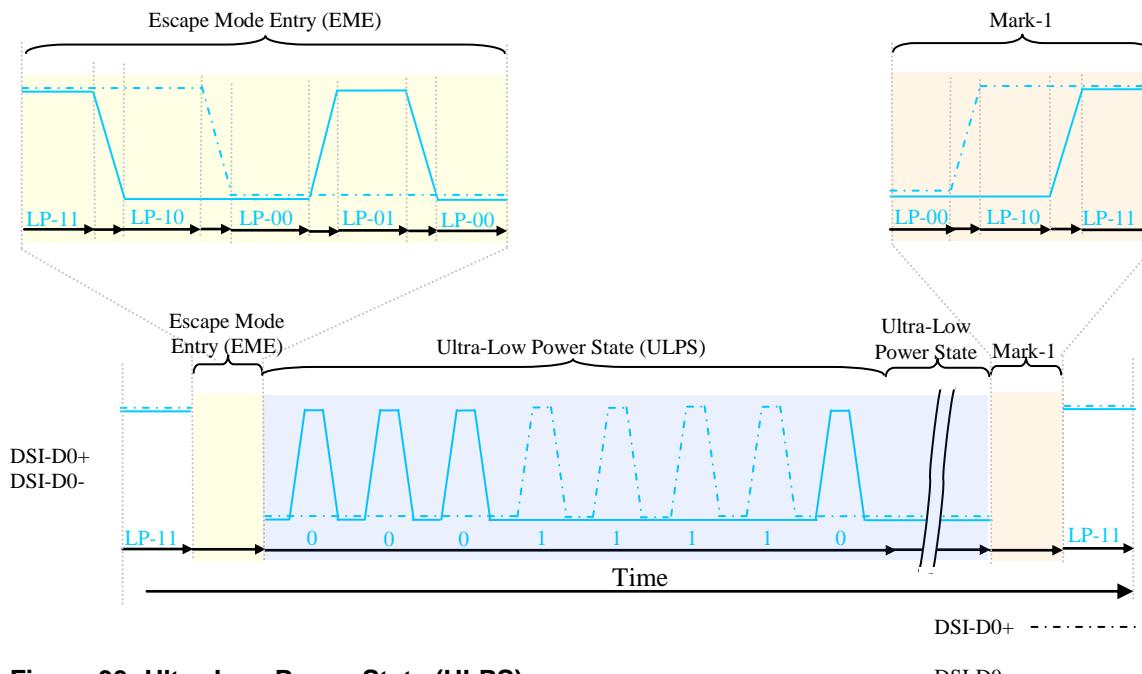


Figure 33: Ultra-Low Power State (ULPS)

8.1.2.3.2.3 Remote Application Reset (RAR)

The MCU can inform to the display module that it should be reseted in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode.

The Remote Application Reset (RAR) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

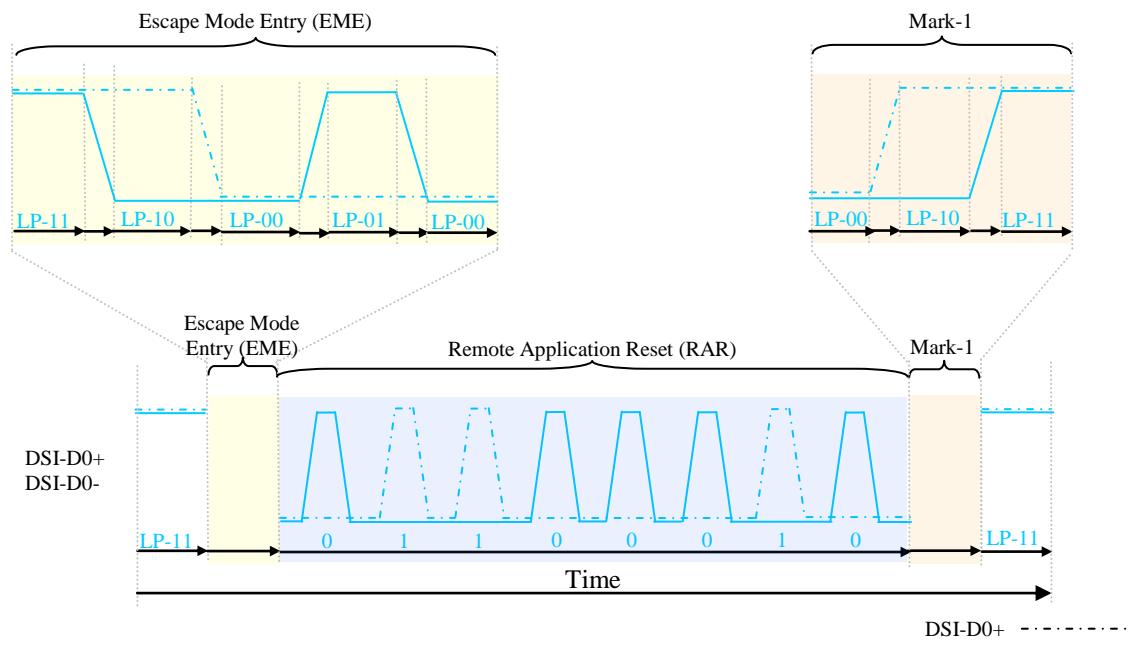


Figure 34: Remote Application Reset (RAR)

8.1.2.3.2.4 Tearing Effect (TEE)

The display module can inform to the MCU when a tearing effect event (New V-synch) has been happened on the display module by Tearing Effect (TEE).

The display module is sending the Tearing Effect (TEE) what is a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

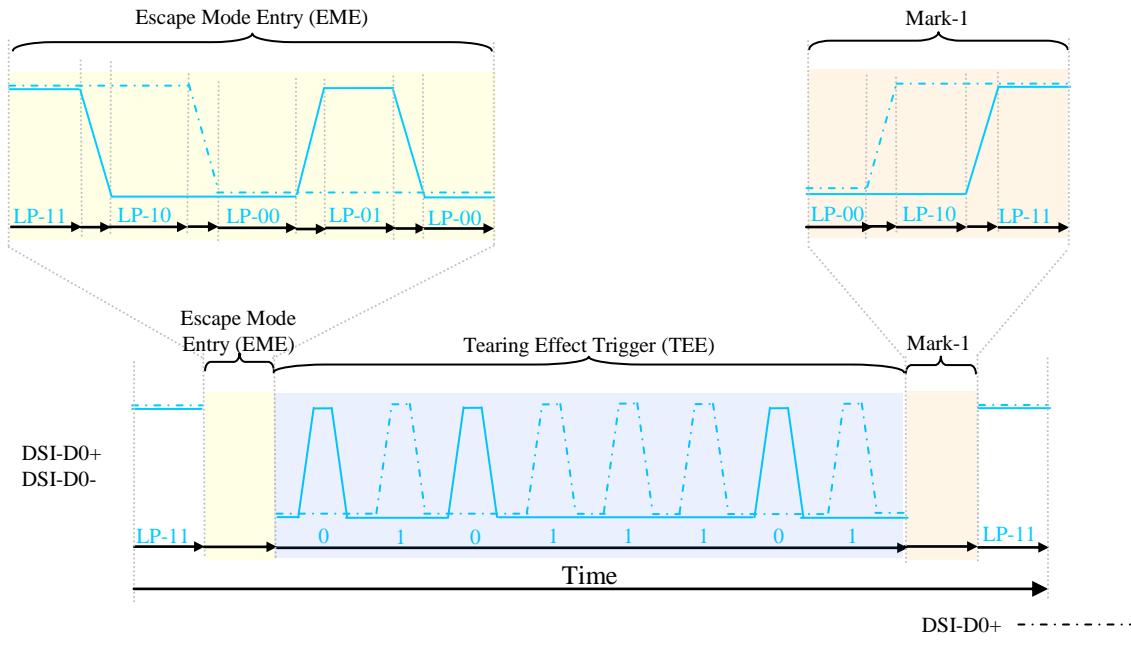


Figure 35: Tearing Effect (TEE)

8.1.2.3.2.5 Acknowledge (ACK)

The display module can inform to the MCU when no error has been recognized on it by Acknowledge (ACK).

The display module is sending the Acknowledge (ACK) what is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

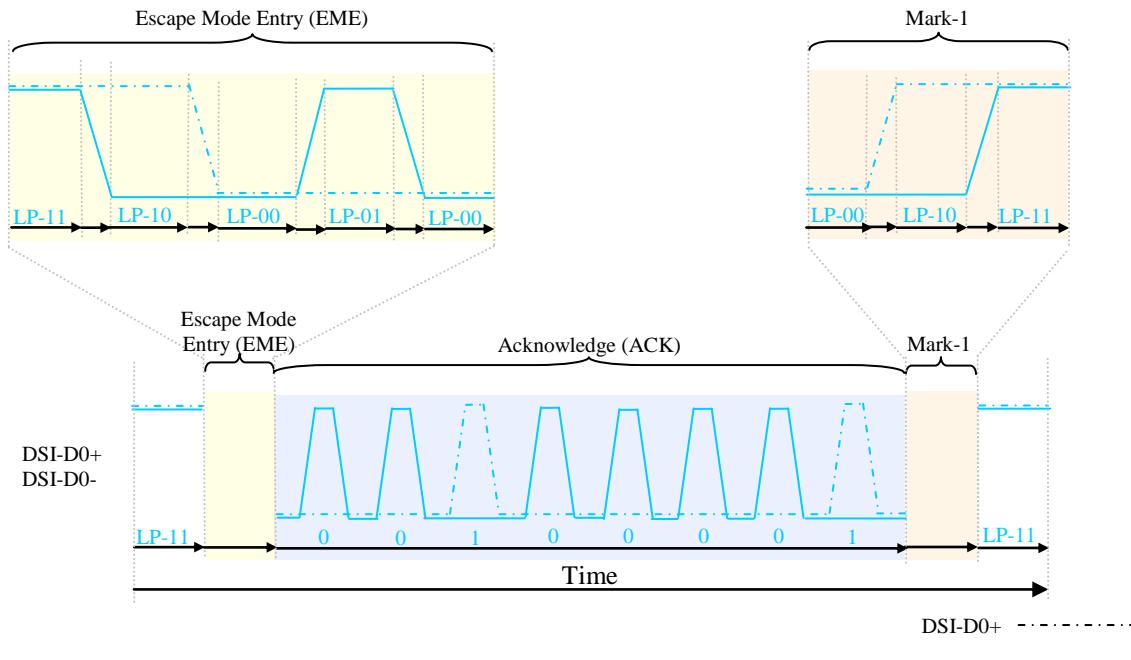


Figure 36: Acknowledge (ACK)

8.1.2.3.3 High-Speed Data Transmission (HSDT)

8.1.2.3.3.1 Entering High-Speed Data Transmission (T_{SOT} of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode (HSCM) by the MCU. See more information on chapter “8.1.2.2.3 High-Speed Clock Mode (HSCM)”.

Data lanes DSI-D0+/- of the display module are entering (T_{SOT}) in the High-Speed Data Transmission (HSDT) as follows

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (T_{SOT} of HSDT) sequence is illustrated below

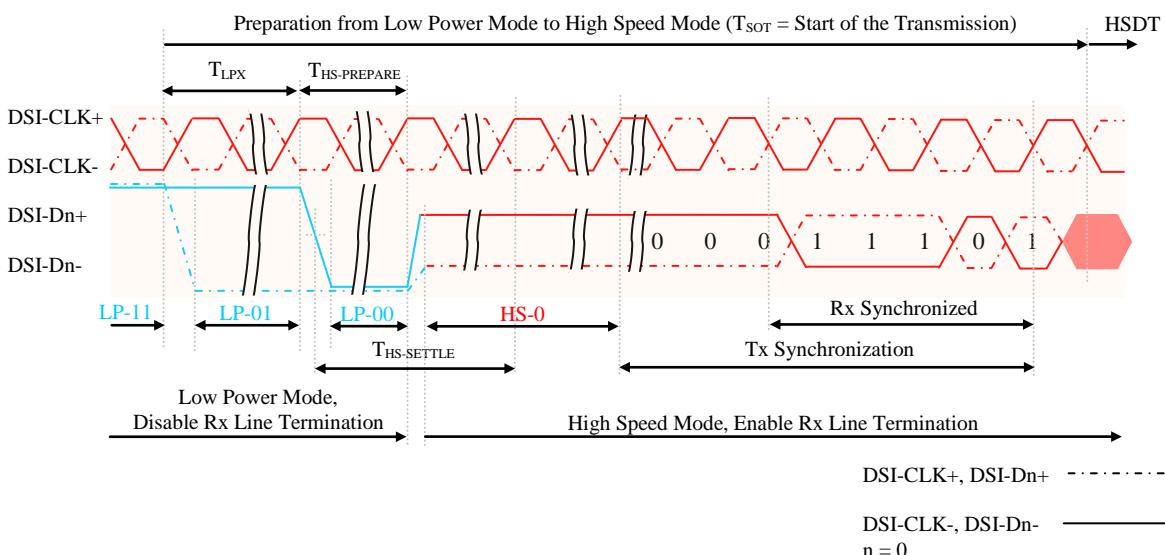


Figure 37: Entering High-Speed Data Transmission (T_{SOT} of HSDT)

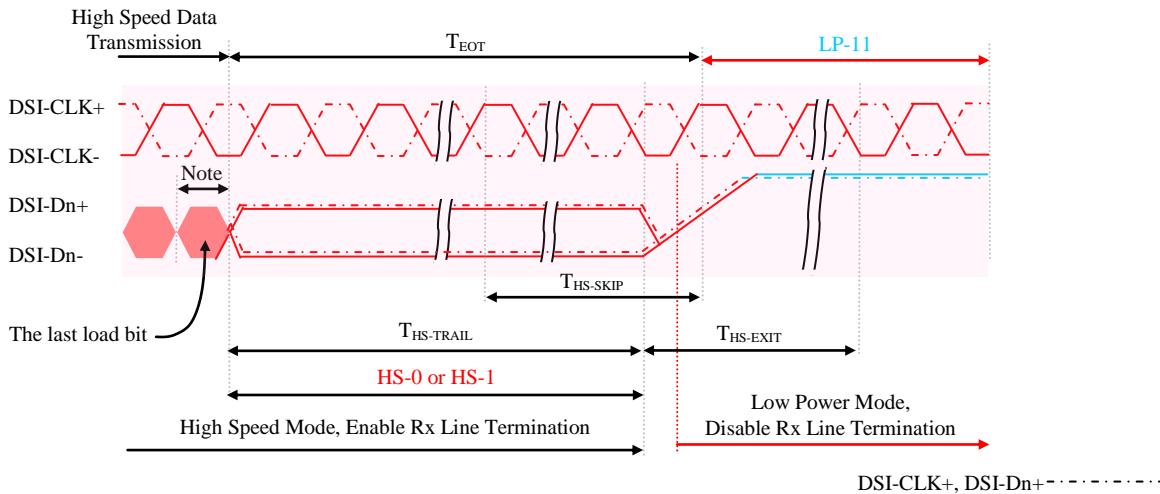
8.1.2.3.3.2 Leaving High-Speed Data Transmission (T_{EOT} of HSDT)

The display module is leaving the High-Speed Data Transmission (T_{EOT} of HSDT) when Clock lanes DSI-CLK+/- are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes DSI-D0+/- are in LP-11 mode. See more information on chapter “8.1.2.2.3 High-Speed Clock Mode (HSCM)”.

Data lanes DSI-D0+/- of the display module are leaving from the High-Speed Data Transmission (T_{EOT} of HSDT) as follows

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
 - MCU changes to HS-1, if the last load bit is HS-0
 - MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (T_{EOT} of HSDT) sequence is illustrated below



Note:

If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

DSI-CLK+, DSI-Dn+ - - - - -

DSI-CLK-, DSI-Dn- - - - -
 $n = 0$

Figure 38: Leaving High-Speed Data Transmission (T_{EOT} of HSDT)

8.1.2.3.3.3 Burst of the High-Speed Data Transmission (HSDT)

The burst of the “High-Speed Data Transmission” (HSDT) can consist of one data packet or several data packets.

These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined on chapter “8.1.3.1 Short Packet (SPa) and Long Packet (LPa) Structures“.

These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

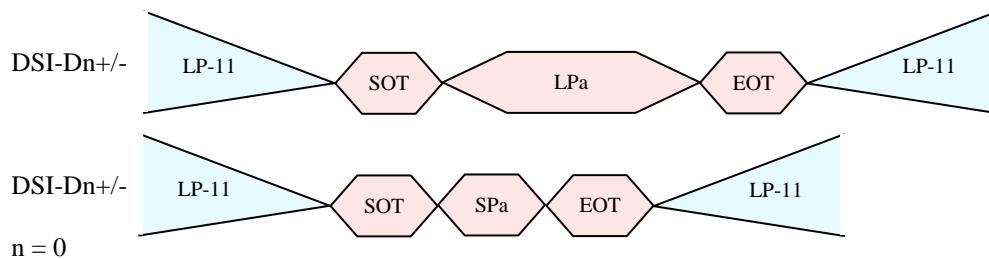


Figure 39: Single Packet in High-Speed Data Transmissions

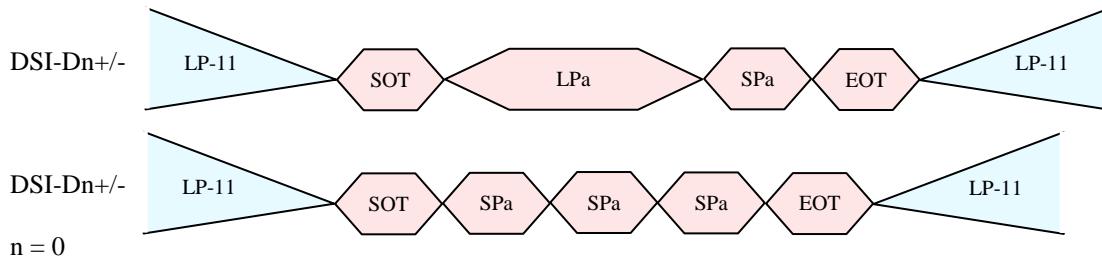


Figure 40: Multiple Packets in High-Speed Data Transmission – Examples

Table 21: Abbreviations

Abbreviation	Explanation
EOT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Data lanes are '1's (Stop Mode)
SPa	Short Packet
SOT	Start of the Transmission

Byte orders of the sent packet is in High-Speed Data Transmission (HSDT) as follows.

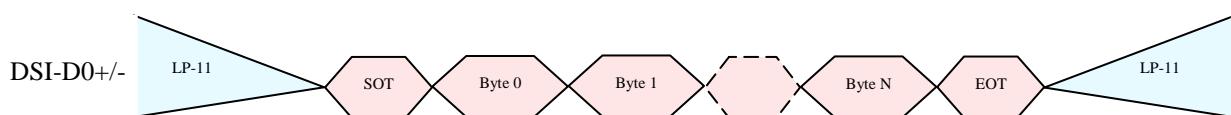


Figure 41: Single Packet in HSDT

8.1.2.3.4 Bus Turnaround (BTA)

The MCU or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or display module.

The MCU and display module are using the same sequence when this bus turnaround procedure is used. This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to the display module, as follows.

- Start (MCU): LP-11
- Turnaround Request (MCU): LP-11 =>LP-10 =>LP-00 => LP-10 => LP-00
- The MCU waits until the display module is starting to control DSI-D0+/- data lanes and the MCU stops to control DSI-D0+/- data lanes (= High-Z)
- The display module changes to the stop mode: LP-00 =>LP-10 =>LP-11

The same bus turnaround procedure (From the MCU to the display module) is illustrated below

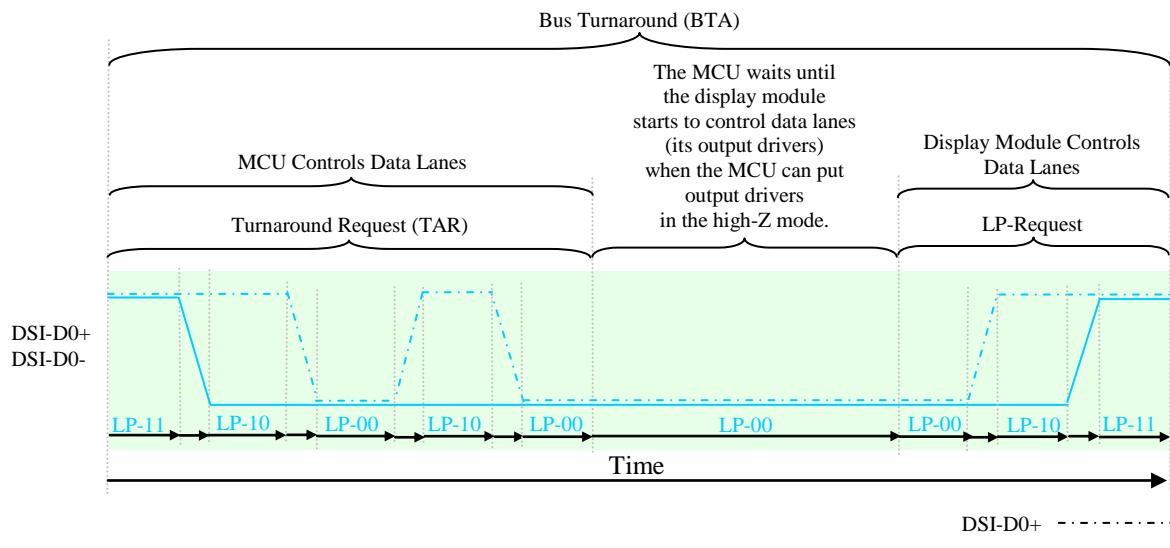


Figure 42: Bus Turnaround Procedure

MCU and display module terms are switched on “Figure 42: Bus Turnaround Procedure”, if the Bus Turnaround (BTA) is from the display module to the MCU.

8.1.3 Packet Level Communication

8.1.3.1 Short Packet (SPa) and Long Packet (LPa) Structures

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes.

The lengths of the packets are

- Short Packet (SPa): 4 bytes
- Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).

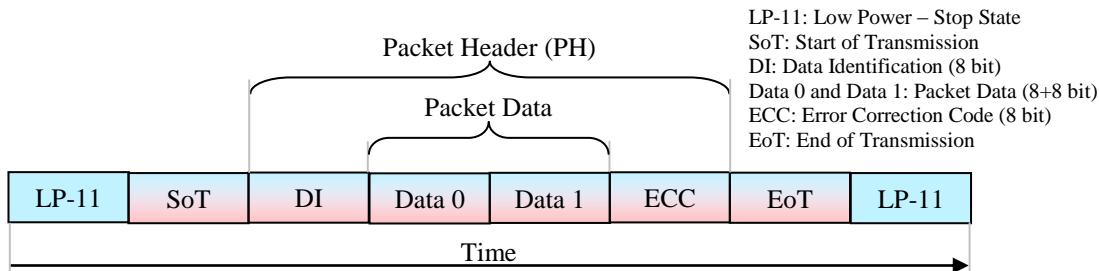


Figure 43: Short Packet (SPa) Structure

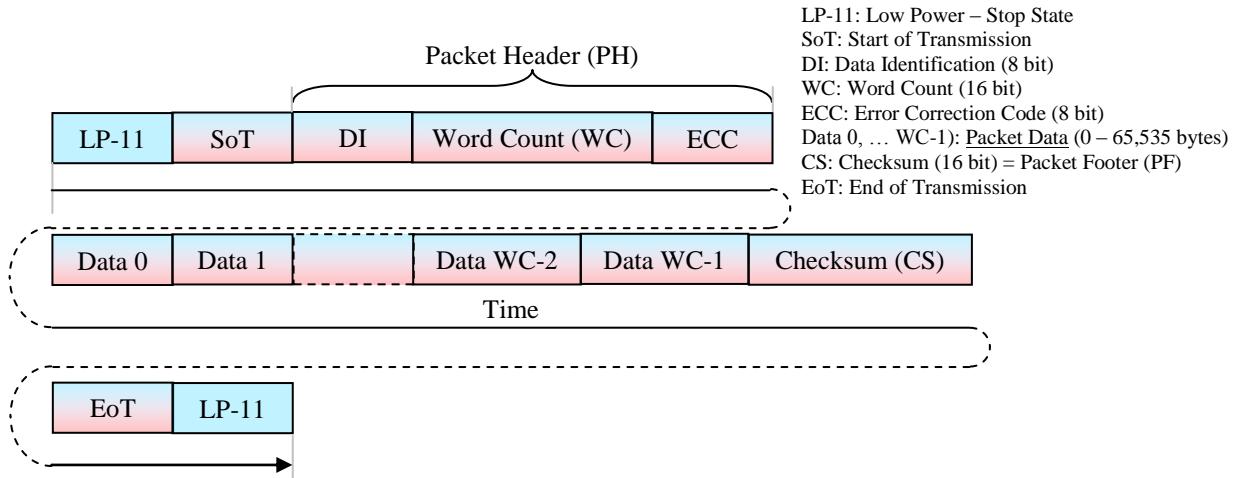


Figure 44: Long Packet (LPa) Structure

Note:

"Figure 43: Short Packet (SPa) Structure" and "Figure 44: Long Packet (LPa) Structure" are presenting a single packet sending (= Includes LP-11, SoT and EoT for each packet sendings).

The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple packet format e.g.

- LP-11 => SoT => SPa => LPa => SPa => SPa => EoT => LP-11
- LP-11 => SoT => SPa => SPa => SPa => EoT => LP-11
- LP-11 => SoT => LPa => LPa => LPa => EoT => LP-11

8.1.3.1.1 Bit Order of the Byte on Packets

The bit order of the byte, what is used on packets, is that the Least Significant Bit (LSB) of the byte is sent in the first and the Most Significant Bit (MSB) of the byte is sent in the last.

This same order is illustrated for reference purposes below.

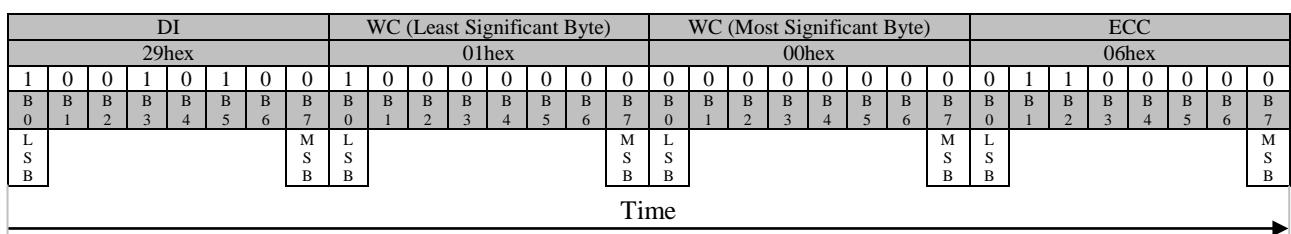


Figure 45: Bit Order of the Byte on Packets

8.1.3.1.2 Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last.

This same order is illustrated for reference purposes below.

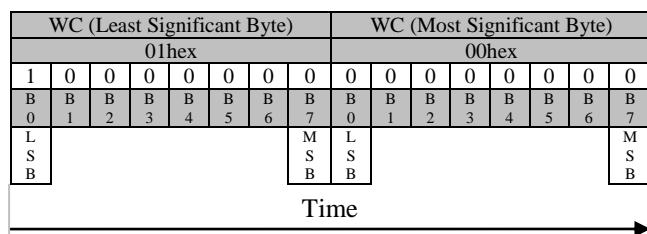


Figure 46: Byte Order of the Multiple Byte Information on Packets

8.1.3.1.3 Packet Header (PH)

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different if it is used to Short Packet (SPa) or Long Packet (LPa).

Short Packet (SPa):

- 1st byte: Data Identification (DI) => Identification that this is Short Packet (SPa)
- 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1
- 4th byte: Error Correction Code (ECC)

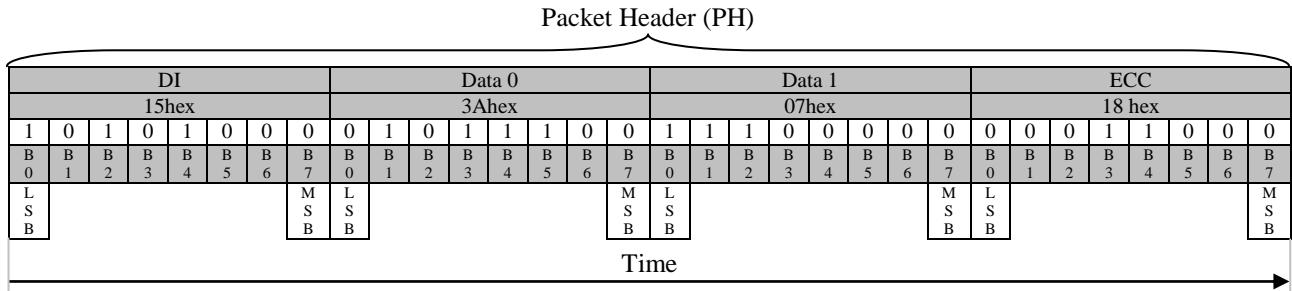


Figure 47: Packet Header (PH) on Short Packet (SPa)

Long Packet (LPa):

- 1st byte: Data Identification (DI) => Identification that this is Long Packet (LPa)
- 2nd and 3rd bytes: Word Count (WC)
- 4th byte: Error Correction Code (ECC)

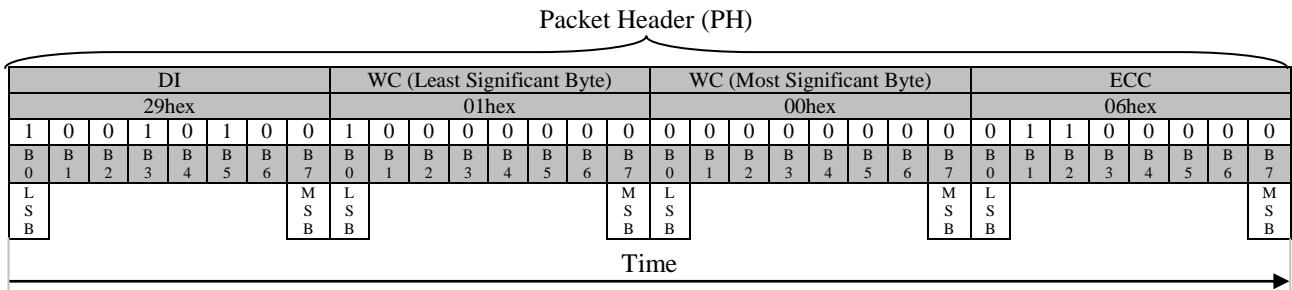


Figure 48: Packet Header (PH) on Long Packet (LPa)

8.1.3.1.3.1 Data Identification (DI)

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

- Virtual Channel (VC), 2 bits, DI[7...6]
- Data Type (DT), 6 bits, DI[5...0]

The Data Identification (DI) structure is illustrated on a table below.

Table 22: Data Identification (DI) Structure

Data Identification (DI)							
Virtual Channel (VC)		Data Type (DT)					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Data Identification (DI) is illustrated on Packet Header (PH) for reference purposes below.

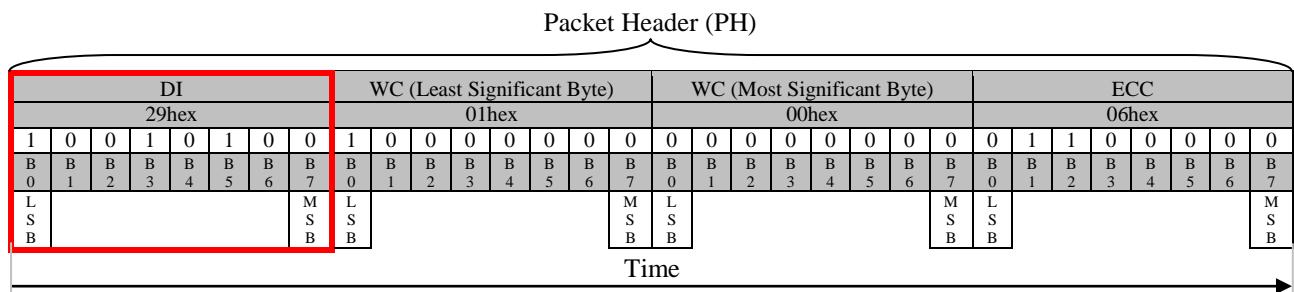


Figure 49: Data Identification (DI) on the Packet Header (PH)

8.1.3.1.3.1.1 Virtual Channel (VC)

Virtual Channel (VC) is a part of Data Identification (DI[7...6]) structure and it is used to address where a packet is wanted to send from the MCU.

Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

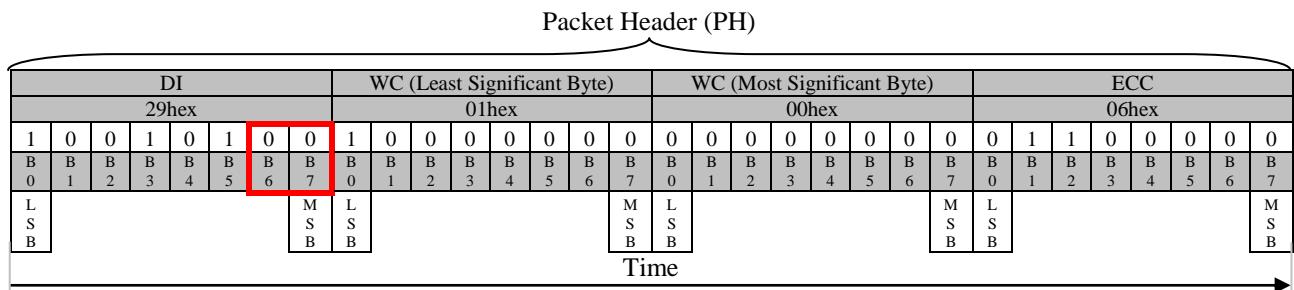


Figure 50: Virtual Channel (VC) on the Packet Header (PH)

Virtual Channel (VC) can address 4 different channels for e.g. 4 different display modules.

Devices are using the same virtual channel what the MCU is using to send packets to them e.g.

- The MCU is using the virtual channel 0 when it sends packets to this display module
- This display module is also using the virtual channel 0 when it sends packets to the MCU

This functionality is illustrated below.

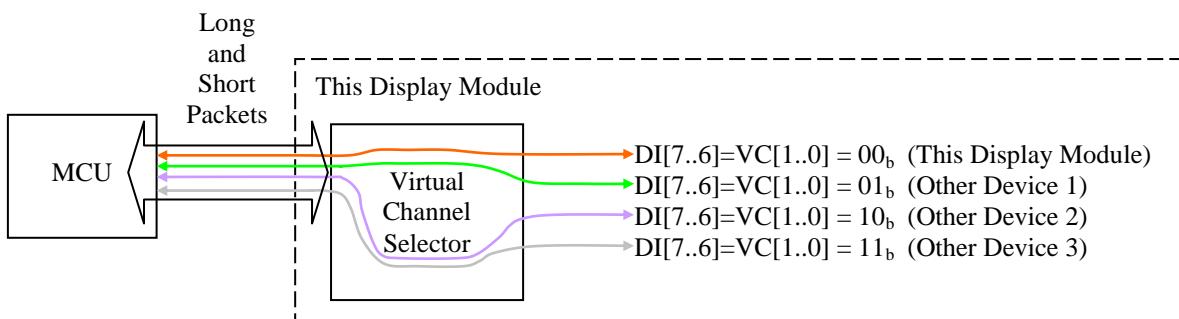


Figure 51: Virtual Channel (VC) Configuration

Virtual Channel (VC) is always 0 (DI[7..6]=VC[1..0]=00_b) when the MCU is sending “End of Transmission Packet” to the display module. See chapter “8.1.3.2.1.7 End of Transmission Packet (EoTP)”.

This display module is not supporting the virtual channel selector for other devices (1 to 3) when the only possible virtual channel (VC[1..0]) is 00b for this display module.

8.1.3.1.3.1.2 Data Type (DT)

Data Type (DT) is a part of Data Identification (DI[5...0]) structure and it is used to define a type of the used data on a packet.

Bits of the Data Type (DT) are illustrated for reference purposes below.

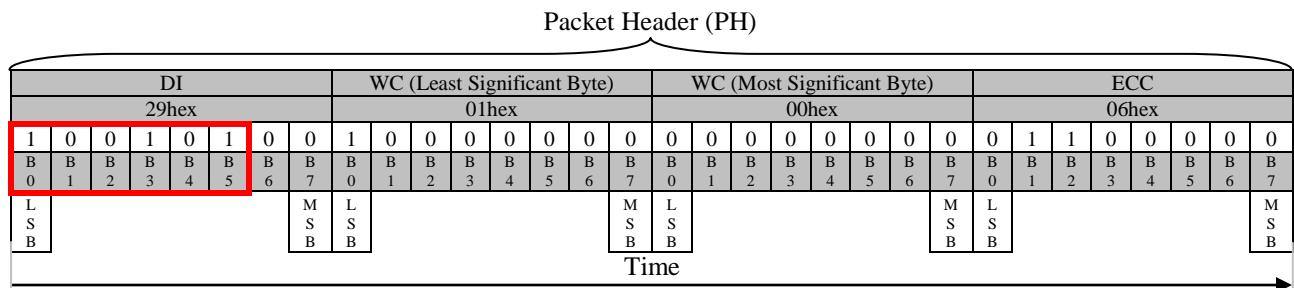


Figure 52: Data Type (DT) on the Packet Header (PH)

This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa).

Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa.

These Data Type (DT) are defined on tables below.

Table 23: Data Type (DT) from the MCU to the Display Module (or Other Devices)

From the MCU to the Display Module (or Other Devices)								Short/Long Packet	Abbreviation
Hex	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Description		
08	0	0	1	0	0	0	End of Transmission Packet, See Note 1	Short Packet	EoTP
05	0	0	0	1	0	1	DCS Write, No Parameter	Short Packet	DCSWN-S
15	0	1	0	1	0	1	DCS Write, 1 Parameter	Short Packet	DCSW1-S
06	0	0	0	1	1	0	DCS Read, No Parameter	Short Packet	DCSRN-S
37	1	1	0	1	1	1	Set Maximum Return Packet Size	Short Packet	SMRPS-S
09	0	0	1	0	0	1	Null Packet, No Data, See Note 2	Long Packet	NP-L
39	1	1	1	0	0	1	DCS Write Long	Long Packet	DCSW-L

Notes:

1. This can be used when the MCU wants to secure that there is the end of the transmission in High Speed Data Transferring (HSDT) mode.
2. This can be used when data lanes are wanted to keep in High Speed Data Transferring (HSDT) Mode.

Table 24: Data Type (DT) from the Display Module (or Other Devices) to the MCU

From the Display Module (or Other Devices) to the MCU								Short/Long Packet	Abbreviation
Hex	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Description		
02	0	0	0	0	1	0	Acknowledge with Error Report	Short Packet	AwER
1C	0	1	1	1	0	0	DCS Read Long Response	Long Packet	DCSRR-L
21	1	0	0	0	0	1	DCS Read Short Response, 1 byte returned	Short Packet	DCSRR1-S
22	1	0	0	0	1	0	DCS Read Short Response, 2 byte returned	Short Packet	DCSRR2-S

The receiver is ignored other Data Type (DT) if they are not defined on tables: “Table 23: Data Type (DT) from the MCU to the Display Module (or Other Devices)” or “Table 24: Data Type (DT) from the Display Module (or Other Devices) to the MCU”.

8.1.3.1.3.2 Packet Data (PD) on the Short Packet (SPa)

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send.

The Word Count (WC) indicates the number of Bytes of Packet Data (PD) sent after the Packet Header (PH).

Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1.

Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last.

Bits of Data 1 are set to '0' if the information length is 1 byte.

Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below, when Virtual Channel (VC) is 0.

Packet Data (PD) information:

- Data 0: 35hex (Display Command Set (DCS) with 1 Parameter => DI(Data Type (DT)) = 15hex)
- Data 1: 01hex (DCS's parameter)

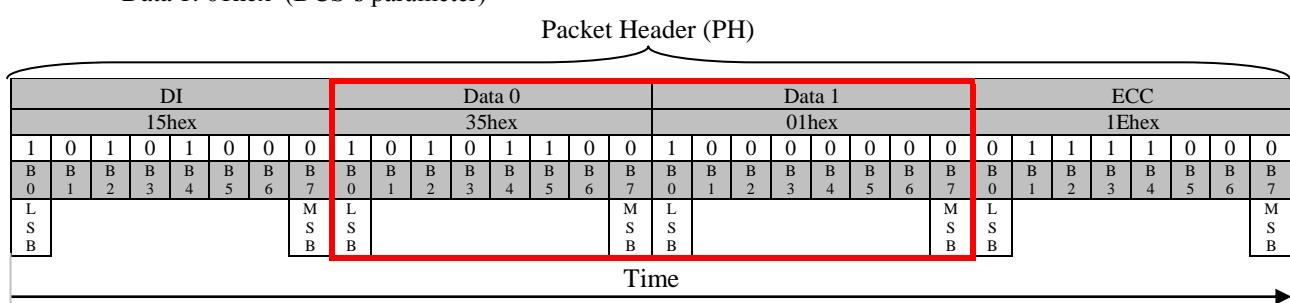


Figure 53: Packet Data (PD) for Short Packet (SPa), 2 Bytes Information

Packet Data (PD) information:

- Data 0: 10hex (DCS without parameter => DI(Data Type (DT)) = 05hex)
- Data 1: 00hex (Null)

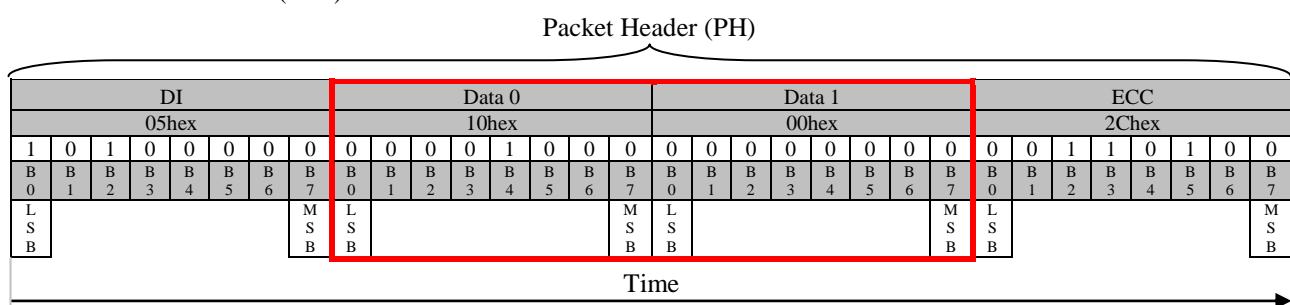


Figure 54: Packet Data (PD) for Short Packet (SPa), 1 Byte Information

8.1.3.1.3.3 Word Count (WC) on the Long Packet (LPa)

Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Long Packet (LPa) is wanted to send.

Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) is placed in the Packet Header (PH).

Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.

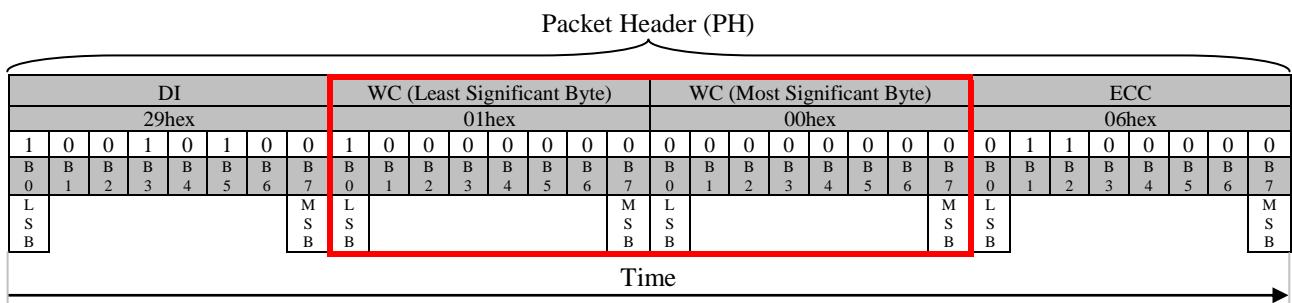


Figure 55: Word Count (WC) on the Long Packet (LPa)

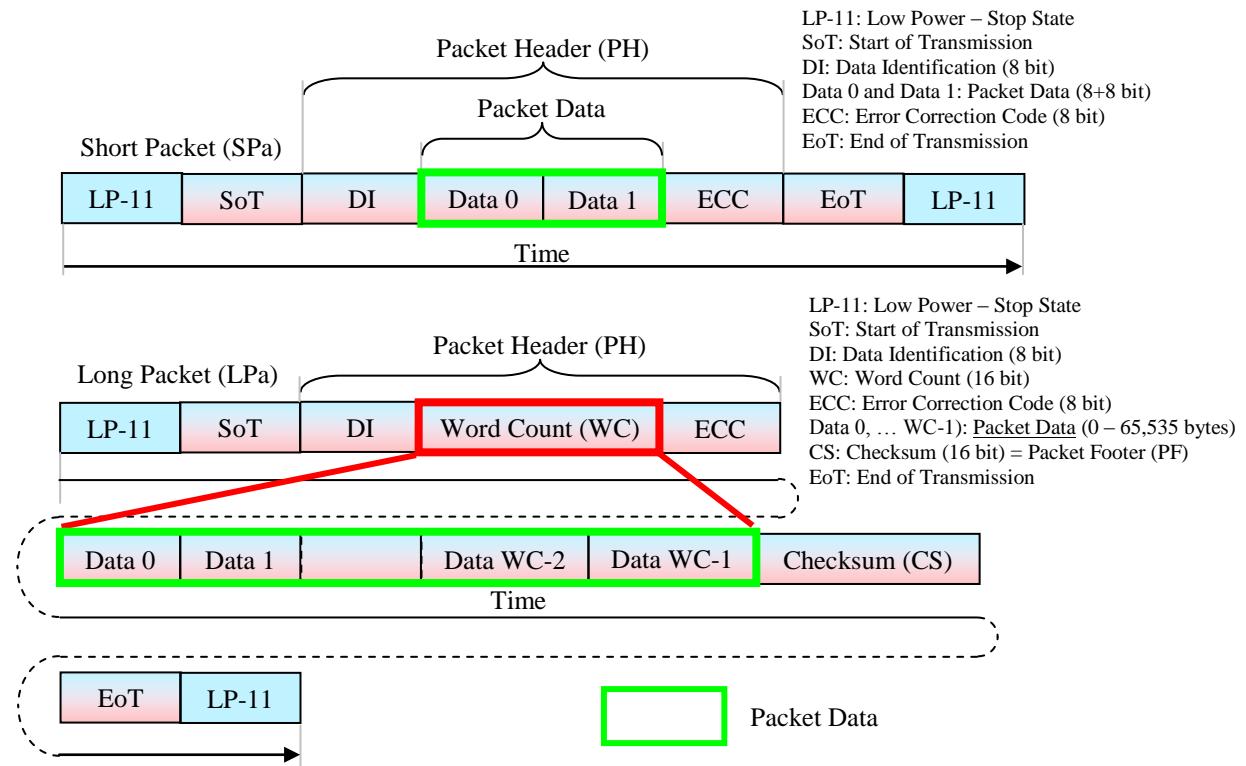


Figure 56: Packet Data in Short and Long Packets

8.1.3.1.3.4 Error Correction Code (ECC)

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors on the Packet Header (PH).

The ECC protects the following fields:

- Short Packet (SPa): Data Identification (DI) byte (8 bits: D[0...7]), Packet Data (PD) bytes (16 bits: D[8...23]) and ECC (8 bits: P[0...7])
- Long Packet (LPa): Data Identification (DI) byte (8 bits: D[0...7]), Word Count (WC) bytes (16 bits: D[8...23]) and ECC (8 bits: P[0...7])

D[23...0] and P[7...0] are illustrated for reference purposes below.

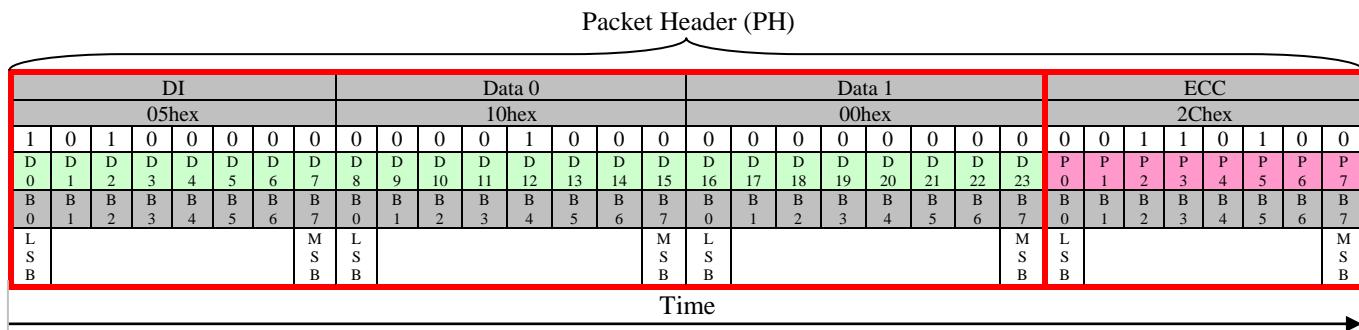


Figure 57: D[23...0] and P[7...0] on the Short Packet (SPa)

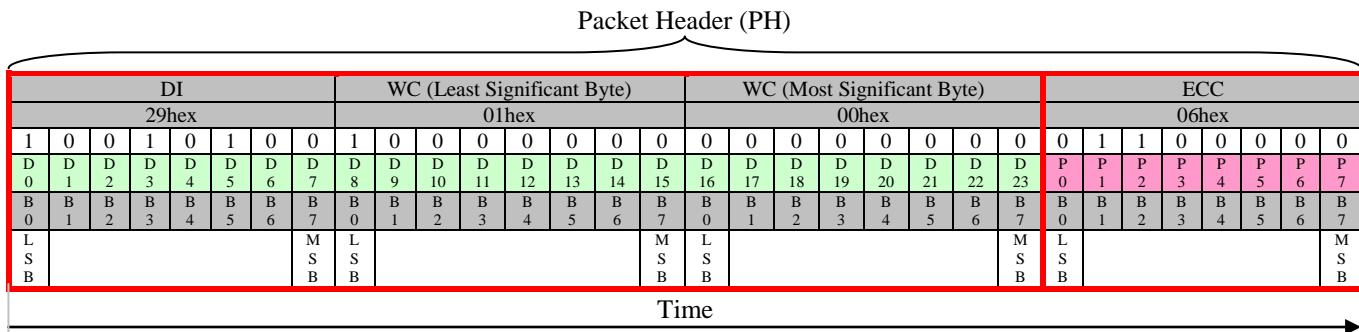


Figure 58: D[23...0] and P[7...0] on the Long Packet (LPa)

Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case.

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Bits (P[7...0]) of the Error Correction Code (ECC) are defined, where the symbol ‘^’ is presenting XOR function (Pn is ‘1’ if there is odd number of ‘1’s and Pn is ‘0’ if there is even number of ‘1’s), as follows.

- P7 = 0
- P6 = 0
- P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
- P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
- P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
- P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22
- P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
- P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to ‘0’ because Error Correction Code (ECC) is based on 64 bit value ([D63...0]), but this implementation is based on 24 bit value (D[23...0]). Therefore, there is only needed 6 bits (P[5...0]) for Error Correction Code (ECC).

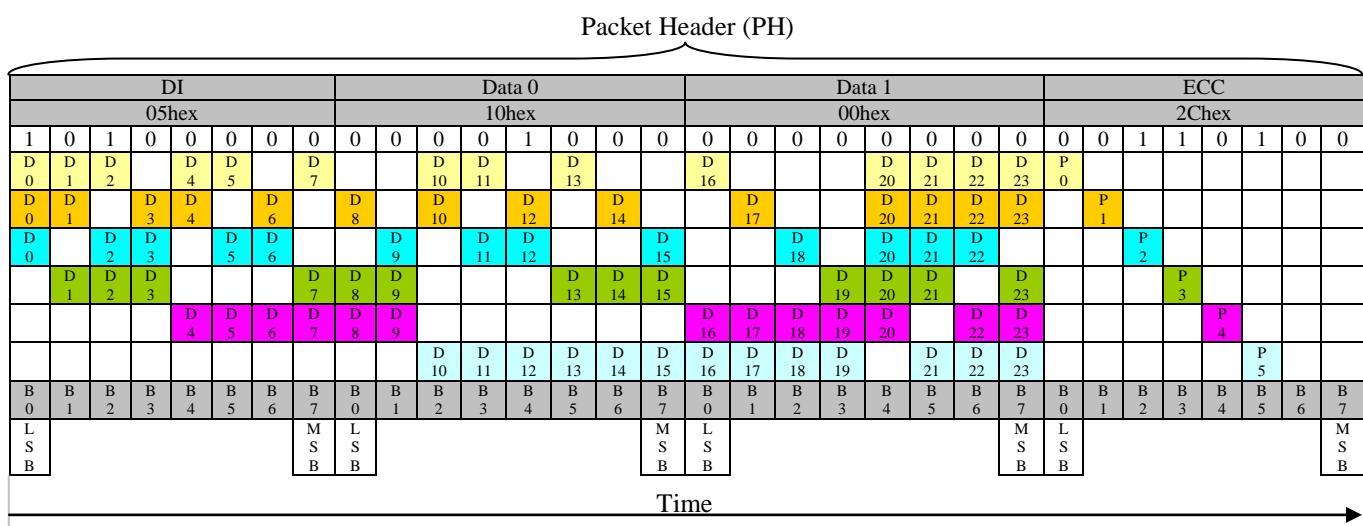


Figure 59: XOR Functionality on the Short Packet (SPa)

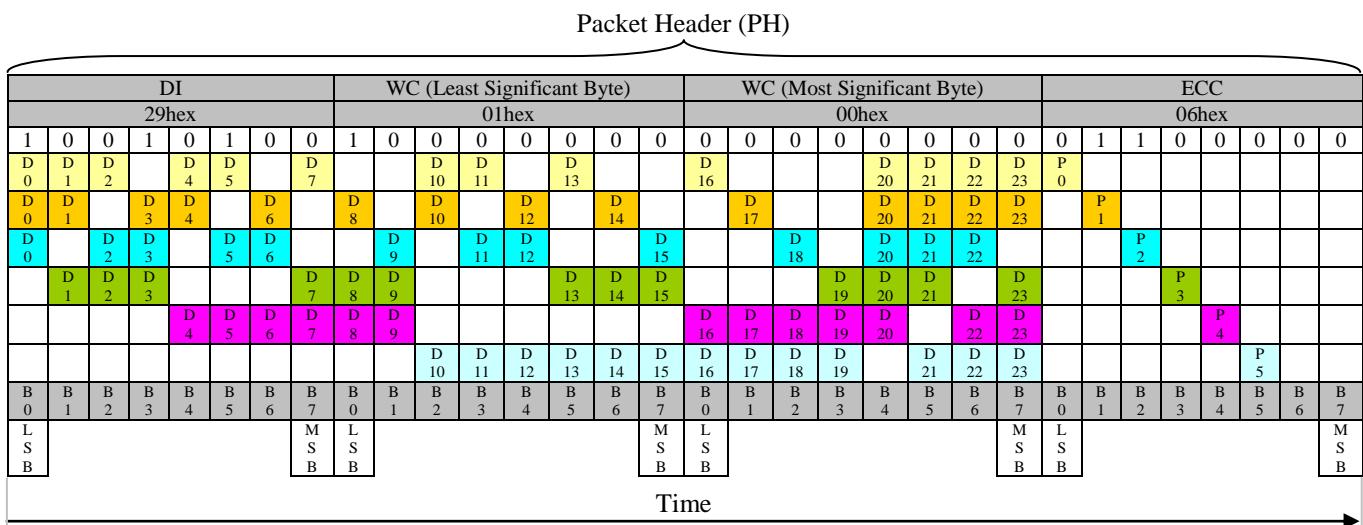


Figure 60: XOR Functionality on the Long Packet (LPa)

The transmitter (The MCU or the Display Module) is sending data bits D[23...0] and Error Correction Code (ECC) P[7...0]. The receiver (The Display module or the MCU) is calculate an Internal Error Correction Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have been done XOR function. The result of this function is PO[7...0].

This functionality, where the transmitter is the MCU and the receiver is the display module, is illustrated for reference purposes below.

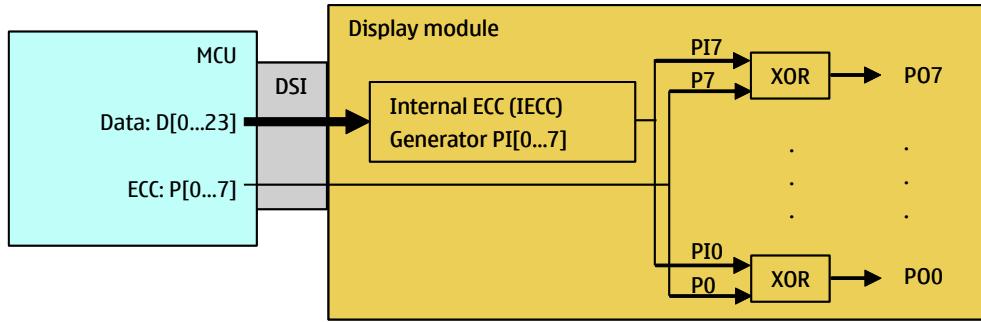


Figure 61: Internal Error Correction Code (IECC) on the Display Module (The Receiver)

The sent data bits (D[23...0]) and ECC (P[7...0]) are received correctly, if a value of the PO[7...0] is 00h. The sent data bits (D[23...0]) and ECC (P[7...0]) are not received correctly, if a value of the PO[7...0] is not 00h.

ECC P[7...0]	1	1	0	0	0	0	0	03h
IECC PI[7...0]	1	1	0	0	0	0	0	03h
XOR(ECC, IECC) => PO[7...0]	0	0	0	0	0	0	0	= 00h => No Error
	L				M			
	S				S			
	B				B			

Figure 62: Internal XOR Calculation between ECC and IECC Values – No Error

ECC P[7...0]	1	1	0	0	0	0	0	03h
IECC PI[7...0]	1	1	1	1	0	0	0	0Fh
XOR(ECC, IECC) => PO[7...0]	0	0	1	1	0	0	0	= 0Ch => Error
	L				M			
	S				S			
	B				B			

Figure 63: Internal XOR Calculation between ECC and IECC Values - Error

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) functionality is not used for data values D[23...0] on the transmitter side.

The number of the errors (one or more) can be defined when the value of the PO[7...0] is compared to values on the following table.

Table 25: One Bit Error Value of the Error Correction Code (ECC)

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D[0]	0	0	0	0	0	1	1	1	07h
D[1]	0	0	0	0	1	0	1	1	0Bh
D[2]	0	0	0	0	1	1	0	1	0Dh
D[3]	0	0	0	0	1	1	1	0	0Eh
D[4]	0	0	0	1	0	0	1	1	13h
D[5]	0	0	0	1	0	1	0	1	15h
D[6]	0	0	0	1	0	1	1	0	16h
D[7]	0	0	0	1	1	0	0	1	19h
D[8]	0	0	0	1	1	0	1	0	1Ah
D[9]	0	0	0	1	1	1	0	0	1Ch
D[10]	0	0	1	0	0	0	1	1	23h
D[11]	0	0	1	0	0	1	0	1	25h
D[12]	0	0	1	0	0	1	1	0	26h
D[13]	0	0	1	0	1	0	0	1	29h
D[14]	0	0	1	0	1	0	1	0	2Ah
D[15]	0	0	1	0	1	1	0	0	2Ch
D[16]	0	0	1	1	0	0	0	1	31h
D[17]	0	0	1	1	0	0	1	0	32h
D[18]	0	0	1	1	0	1	0	0	34h
D[19]	0	0	1	1	1	0	0	0	38h
D[20]	0	0	0	1	1	1	1	1	1Fh
D[21]	0	0	1	0	1	1	1	1	2Fh
D[22]	0	0	1	1	0	1	1	1	37h
D[23]	0	0	1	1	1	0	1	1	3Bh

One error is detected if the value of the PO[7...0] is on Table 25: One Bit Error Value of the Error Correction Code (ECC) and the receiver can correct this one bit error because this found value also defines what is a location of the corrupt bit e.g.

- PO[7...0] = 0Eh
- The bit of the data (D[23...0]), what is not correct, is D[3]

More than one error is detected if the value of the PO[7...0] is not on Table 25: One Bit Error Value of the Error Correction Code (ECC) e.g. PO[7...0] = 0Ch.

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8.1.3.1.4 Packet Data (PD) on the Long Packet (LPa)

Packet Data (PD) of the Long Packet (LPa) is defined after Packet Header (PH) of the Long Packet (LPa). The number of the data bytes is defined on chapter “8.1.3.1.3.3 Word Count (WC) on the Long Packet (LPa)”.

8.1.3.1.5 Packet Footer (PF) on the Long Packet (LPa)

Packet Footer (PF) of the Long Packet (LPa) is defined after the Packet Data (PD) of the Long Packet (LPa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPa).

The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial $X^{16}+X^{12}+X^5+X^0$ as it is illustrated below.

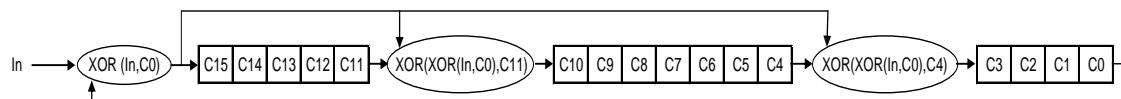


Figure 64: 16-bit Cyclic Redundancy Check (CRC) Calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations.

The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).

An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (LPa) is 01h, is illustrated (step-by-step) below.

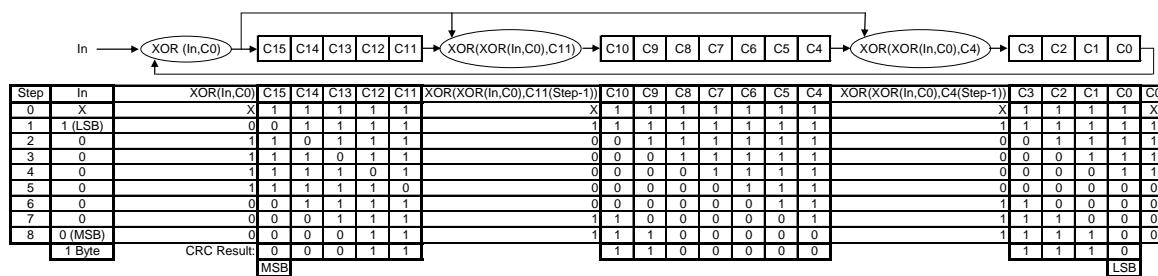


Figure 65: CRC Calculation – Packet Data (PD) is 01h

A value of the Packet Footer (PF) is 1E0Eh in this example. This example (Command 01h has been sent) is illustrated below.

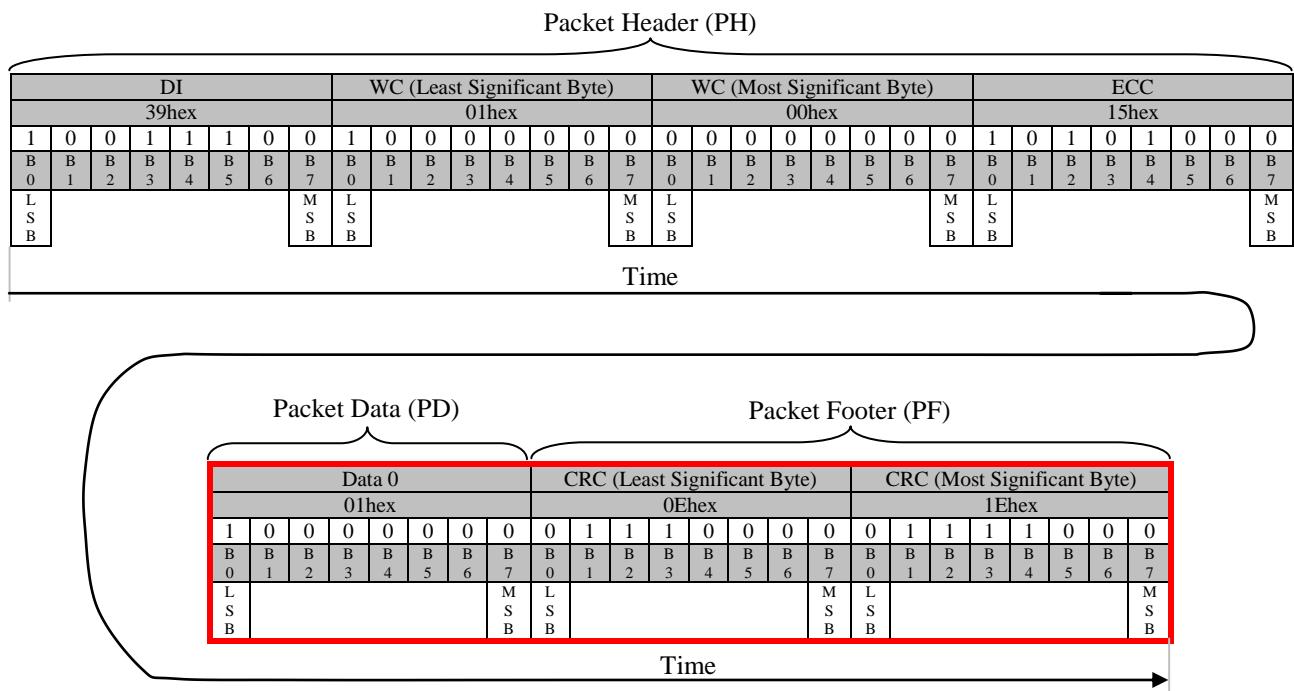


Figure 66: Packet Footer (PF) Example

The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent.

The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) are equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

8.1.3.2 Packet Transmissions

8.1.3.2.1 Packet from the MCU to the Display Module

8.1.3.2.1.1 Display Command Set (DCS)

Display Command Set (DCS), which is defined on chapter “9.2 Command Description” is used from the MCU to the display module. This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD), which is included in Short Packet (SPa) and Long packet (LPa) as these are illustrated below.

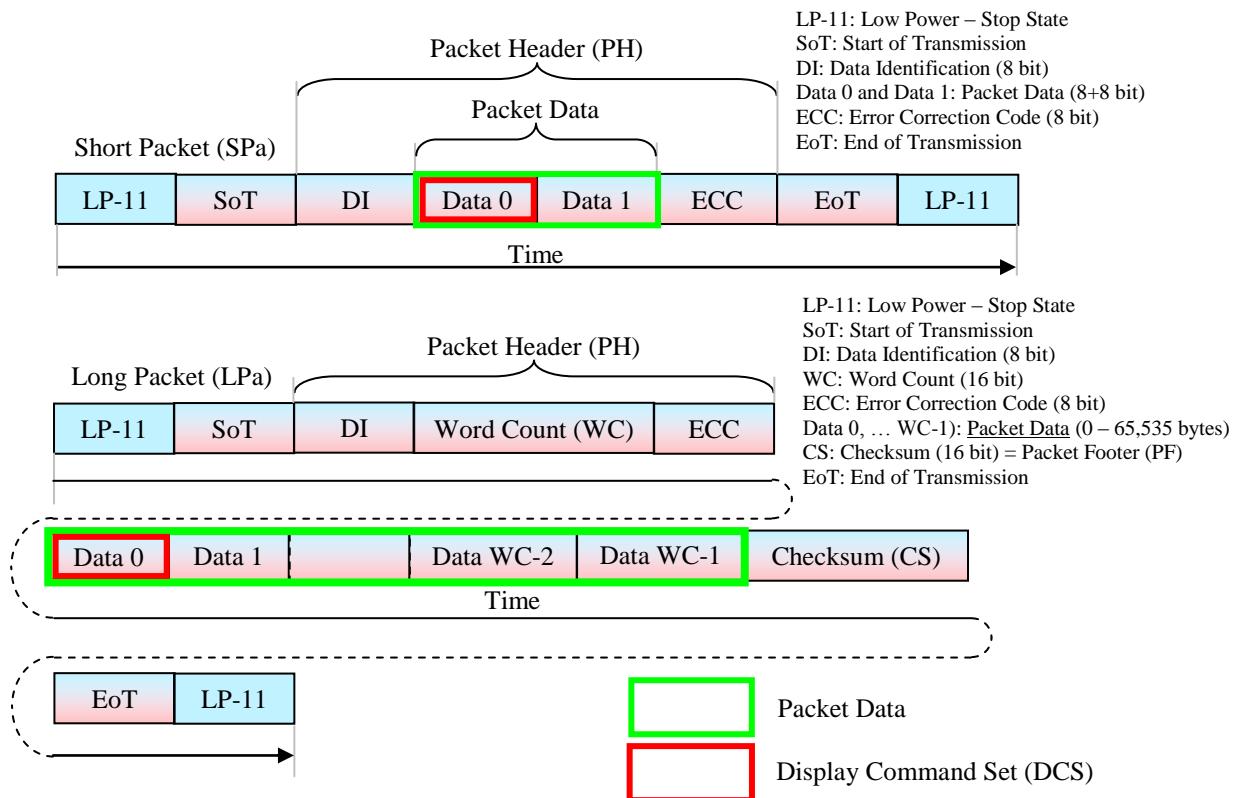


Figure 67: Display Command Set (DCS) on Short Packet (SPa) and Long Packet (LPa)

8.1.3.2.1.2 Display Command Set (DCS) Write, No Parameter (DCSWN-S)

“Display Command Set (DCS) Write, No Parameter” is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0101b), from the MCU to the display module. These commands are defined on a table (See chapter “9.2 Command Description”) below.

Table 26: Display Command Set (DCS) Write, No Parameters (DCSWN-S)

Command
NOP (00h)
Software Reset (01h)
Sleep In (10h)
Sleep Out (11h)
Partial Mode On (12h)
Normal Display Mode On (13h)
All Pixels Off (22h)
All Pixels On (23h)
Display Off (28h)
Display On (29h)
Tearing Effect Line Off (34h)
Idle Mode Off (38h)
Idle Mode On (39h)

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 00 0101b
- Packet Data (PD)
 - Data 0: “Sleep In (10h)”, Display Command Set (DCS)
 - Data 1: Always 00hex
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

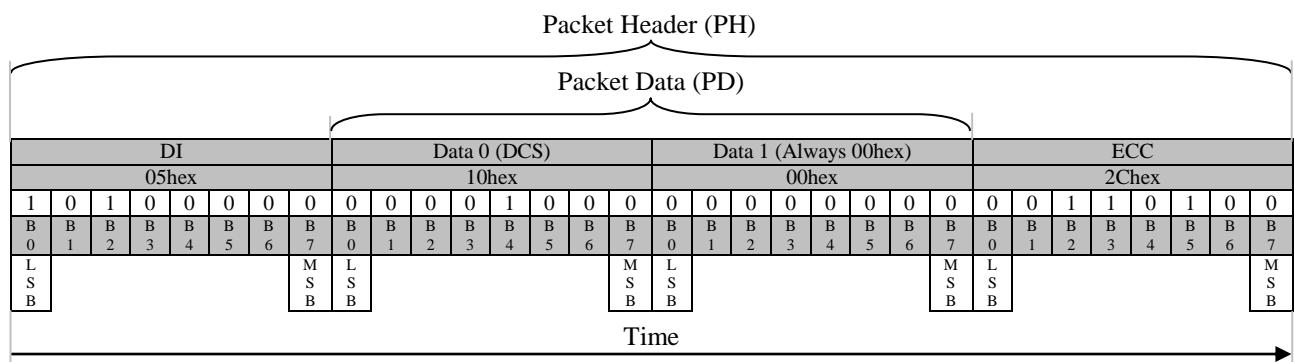


Figure 68: Display Command Set (DCS) Write, No Parameter (DCSWN-S) - Example

8.1.3.2.1.3 Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)

“Display Command Set (DCS) Write, 1 Parameter” (DCSW1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0101b), from the MCU to the display module. These commands are defined on a table (See chapter “9.2 Command Description”) below.

Table 27: Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)

Command
Gamma Set (26h)
Memory Write (2Ch), Note
Tearing Effect Line On (35h)
Memory Access Control (36h)
Interface Pixel Format (3Ah)
Memory Write Continue (3Ch), Note
Write Display Brightness (51h)
Write CTRL Display (53h)
Write Current limit (55h)
Error! Reference source not found.

Note: One Subpixel has been written

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 01 0101b
- Packet Data (PD)
 - Data 0: “Gamma Set (26h)”, Display Command Set (DCS)
 - Data 1: 01hex, Parameter of the DCS
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

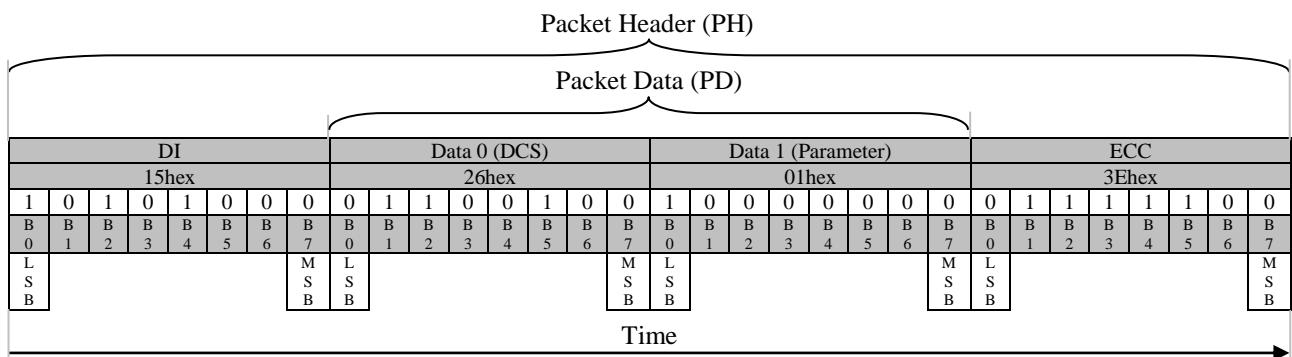


Figure 69: Display Command Set (DCS) Write, 1 Parameter (DCSW1-S) – Example

8.1.3.2.1.4 Display Command Set (DCS) Write Long (DCSW-L)

“Display Command Set (DCS) Write Long” (DCSW-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 11 1001b), from the MCU to the display module. Command (No Parameters) and Write (1 or more parameters), are defined on a table (See chapter “9.2 *Command Description*”) below.

Table 28: Display Command Set (DCS) Write Long (DCSW-L)

Command
NOP (00h), Note 1
Software Reset (01h), Note 1
Sleep In (10h), Note 1
Sleep Out (11h), Note 1
Partial Mode On (12h), Note 1
Normal Display Mode On (13h), Note 1
All Pixels Off (22h)
All Pixels On (23h)
Gamma Set (26h), Note 2
Display Off (28h), Note 1
Display On (29h), Note 1
Column Address Set (2Ah)
Page Address Set (2Bh)
Memory Write (2Ch), Note 2
Partial Area (30h)
Tearing Effect Line Off (34h), Note 1
Tearing Effect Line On (35h), Note 2
Memory Access Control (36h), Note 2
Idle Mode Off (38h), Note 1
Idle Mode On (39h), Note 1
Interface Pixel Format (3Ah)
Memory Write Continue (3Ch), Note 2
Write Display Brightness (51h), Note 2
Write CTRL Display (53h), Note 2
Write Current limit (55h), Note 2
Error! Reference source not found.

Notes:

1. Also Short Packet (SPa) can be used; See chapter “8.1.3.2.1.2 Display Command Set (DCS) Write, No Parameter”
2. Also Short Packet (SPa) can be used; See chapter “8.1.3.2.1.3 Display Command Set (DCS) Write, 1 Parameter”

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Long Packet (LPa), when a command (No Parameter) was sent, is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 11 1001b
- Word Count (WC)
 - Word Count (WC): 0001h
- Error Correction Code (ECC)
- Packet Data (PD): Data 0: “Sleep In (10h)”, Display Command Set (DCS)
- Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

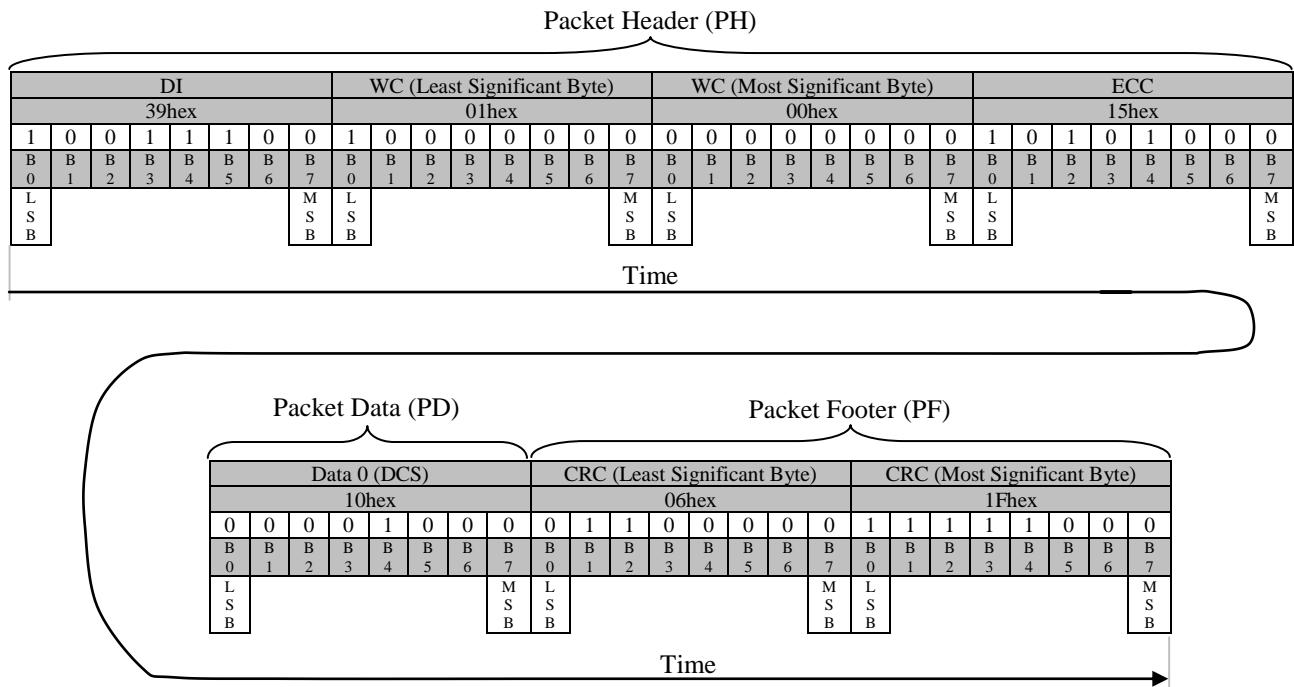


Figure 70: Display Command Set (DCS) Write Long (DCSW-L) with DCS Only - Example

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Long Packet (LPa), when a Write (1 parameter) was sent, is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 11 1001b
- Word Count (WC)
 - Word Count (WC): 0002h
- Error Correction Code (ECC)
- Packet Data (PD):
 - Data 0: "Gamma Set (26h)", Display Command Set (DCS)
 - Data 1: 01hex, Parameter of the DCS
- Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

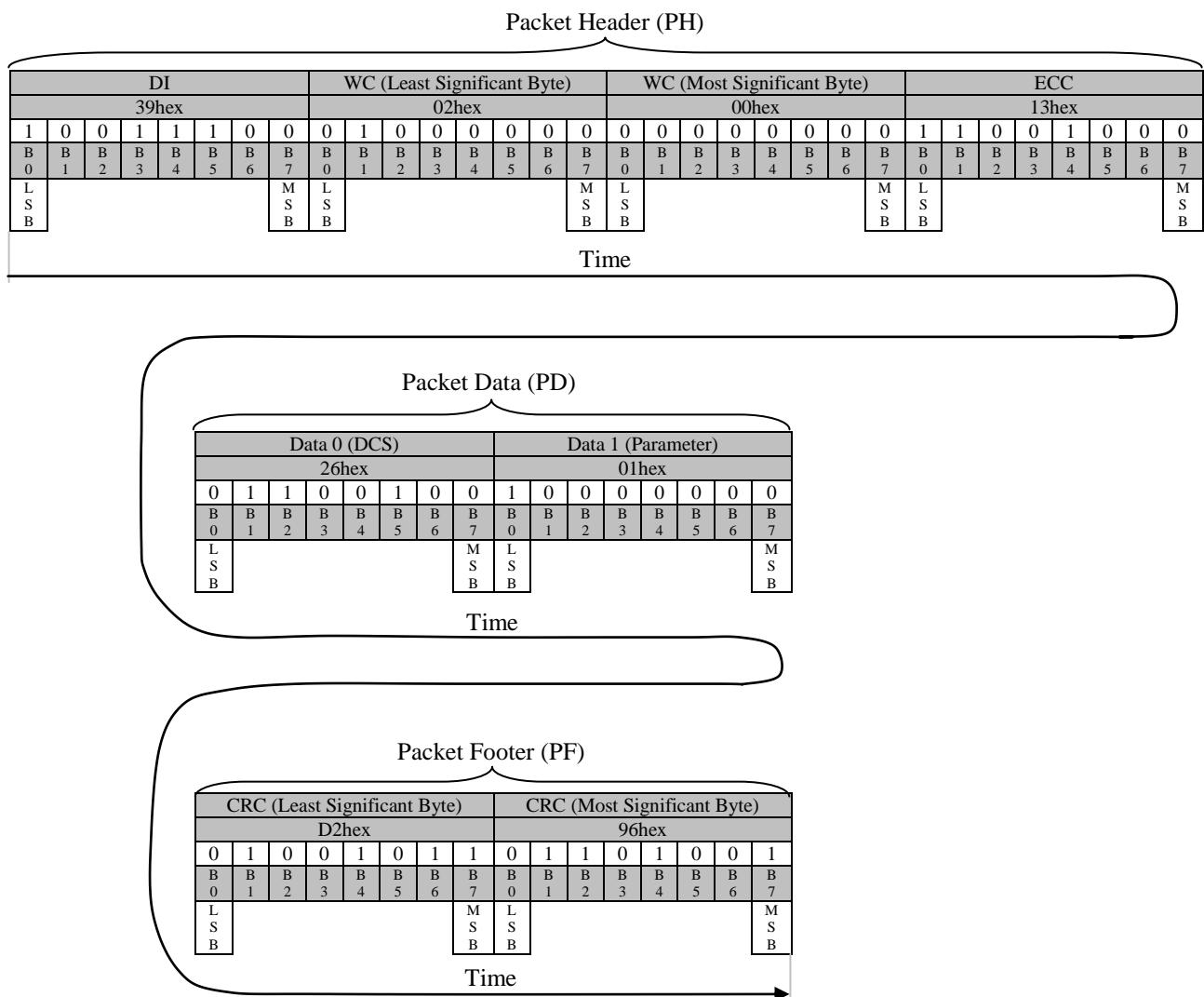


Figure 71: Display Command Set (DCS) Write Long with DCS and 1 Parameter - Example

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Long Packet (LPa), when a Write (4 parameters) was sent, is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 11 1001b
- Word Count (WC)
 - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
 - Data 0: "Column Address Set (2Ah)", Display Command Set (DCS)
 - Data 1: 00hex, 1st Parameter of the DCS, Start Column SC[15...8]
 - Data 2: 12hex, 2nd Parameter of the DCS, Start Column SC[7...0]
 - Data 3: 01hex, 3rd Parameter of the DCS, End Column EC[15...8]
 - Data 4: EFhex, 4th Parameter of the DCS, End Column EC[7...0]
- Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

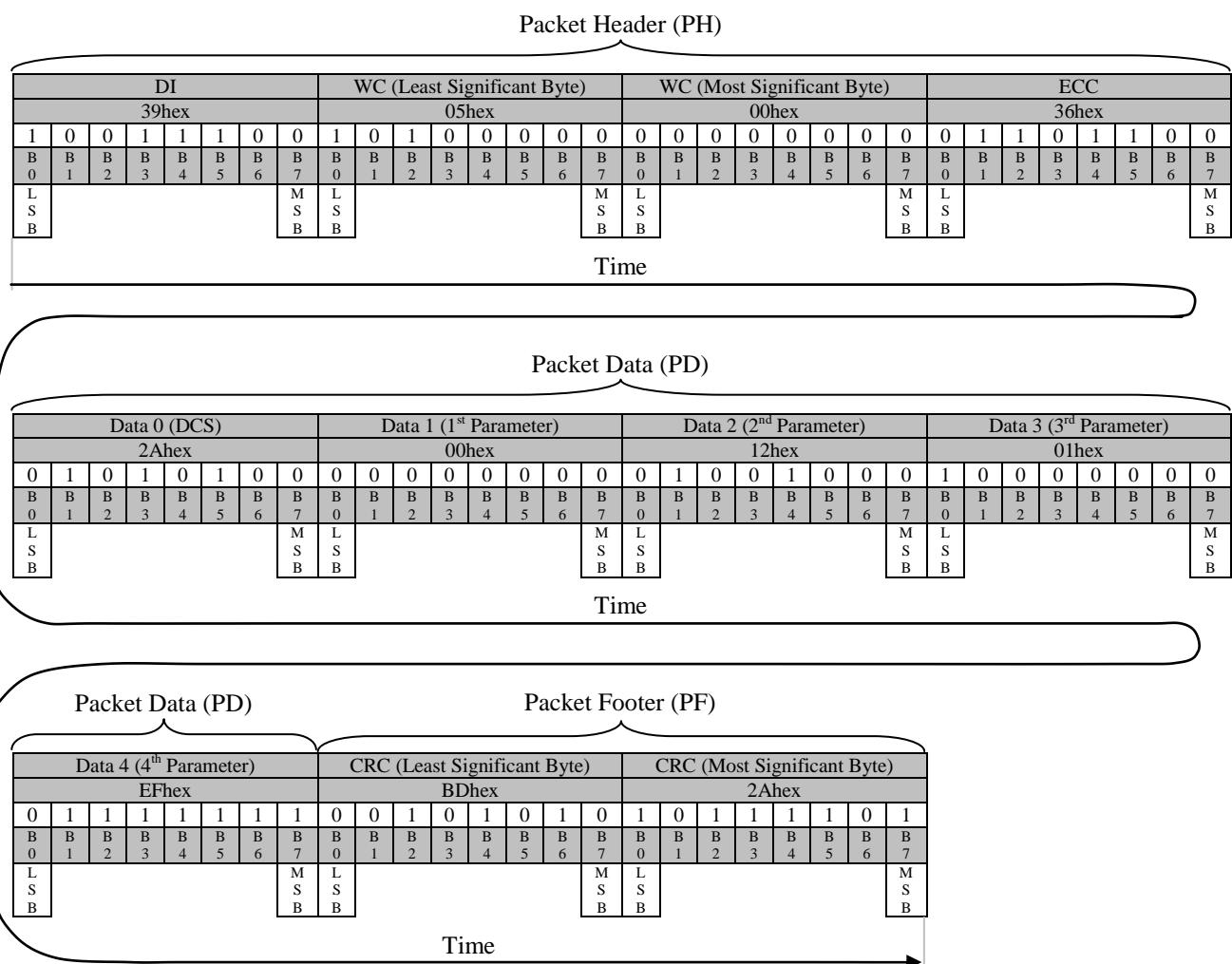


Figure 72: Display Command Set (DCS) Write Long with DCS and 4 Parameters - Example

8.1.3.2.1.5 Display Command Set (DCS) Read, No Parameter (DCSRN-S)

“Display Command Set (DCS) Read, No Parameter” (DCSRN-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0110b), from the MCU to the display module. These commands are defined on a table (See chapter “*9.2 Command Description*” below).

Table 29: Display Command Set (DCS) Read, No Parameter (DCSRN-S)

The MCU has to define to the display module, what is the maximum size of the return packet. A command, what is used for this purpose, is “Set Maximum Return Packet Size” (SMRPS-S), which Data Type (DT) is 11 0111b and which is using Short Packet (SPa) before the MCU can send “Display Command Set (DCS) Read, No Parameter” to the display module. This same sequence is illustrated for reference purposes below.

Step 1:

- The MCU sends “Set Maximum Return Packet Size” (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module
- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 11 0111b
- Maximum Return Packet Size (MRPS)
 - Data 0: 01hex
 - Data 1: 00hex
- Error Correction Code (ECC)

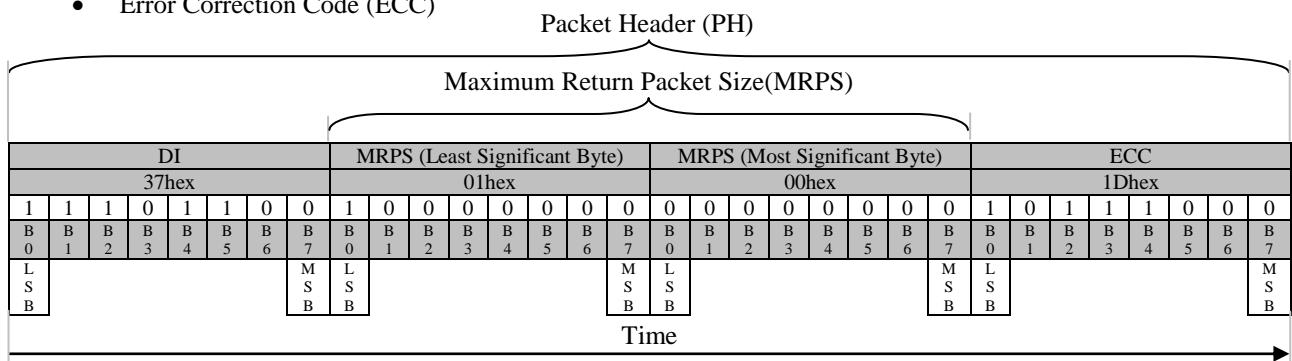


Figure 73: Set Maximum Return Packet Size (SMRPS-S) - Example

Step 2:

- The MCU wants to receive a value of the “Read ID1 (DAh)” from the display module when the MCU sends “Display Command Set (DCS) Read, No Parameter” to the display module
- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 00 0110b
- Packet Data (PD)
 - Data 0: “Read ID1 (DAh)”, Display Command Set (DCS)
 - Data 1: Always 00hex
- Error Correction Code (ECC)

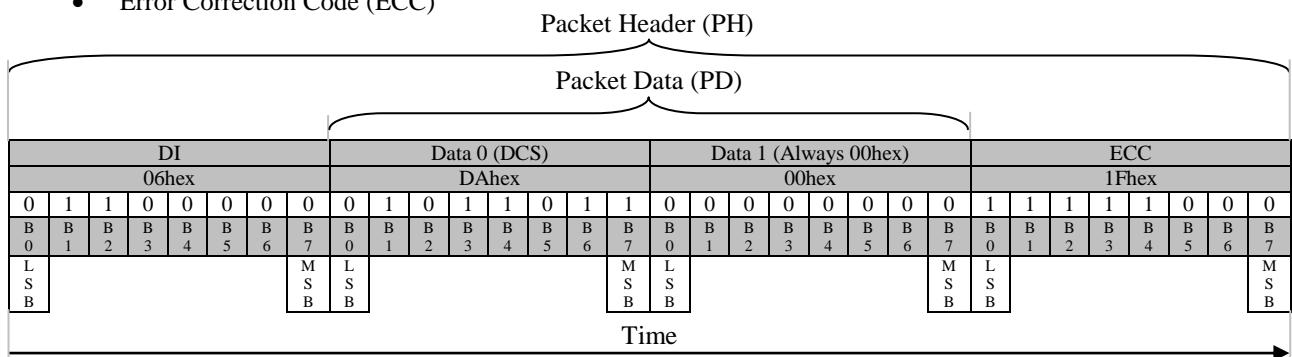


Figure 74: Display Command Set (DCS) Read, No Parameter (DCSRN-S) - Example

Step 3: The display module can send 2 different information to the MCU after Bus Turnaround (BTA)

1. Information of the received command. Short Packet (SPa) or Long Packet (LPa)
2. An acknowledge with Error Report (AwER), which is using a Short Packet (SPa), if there is an error to receive a command, See chapter “8.1.3.2.2 Acknowledge with Error Report (AwER)”

8.1.3.2.1.6 Null Packet, No Data (NP-L)

“Null Packet, No Data” (NP-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 00 1001b), from the MCU to the display module. The purpose of this command is keeping data lanes in the high speed mode (HSDT), if it is needed.

The display module is ignored Packet Data (PD) what the MCU is sending.

Long Packet (LPa), when 5 random data bytes of the Packet Data (PD) were sent, is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 00 1001b
 - Word Count (WC)
 - Word Count (WC): 0005hex
 - Error Correction Code (ECC)
 - Packet Data (PD):
 - Data 0: 89hex (Random data)
 - Data 1: 23hex (Random data)
 - Data 2: 12hex (Random data)
 - Data 3: A2hex (Random data)
 - Data 4: E2hex (Random data)
 - Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

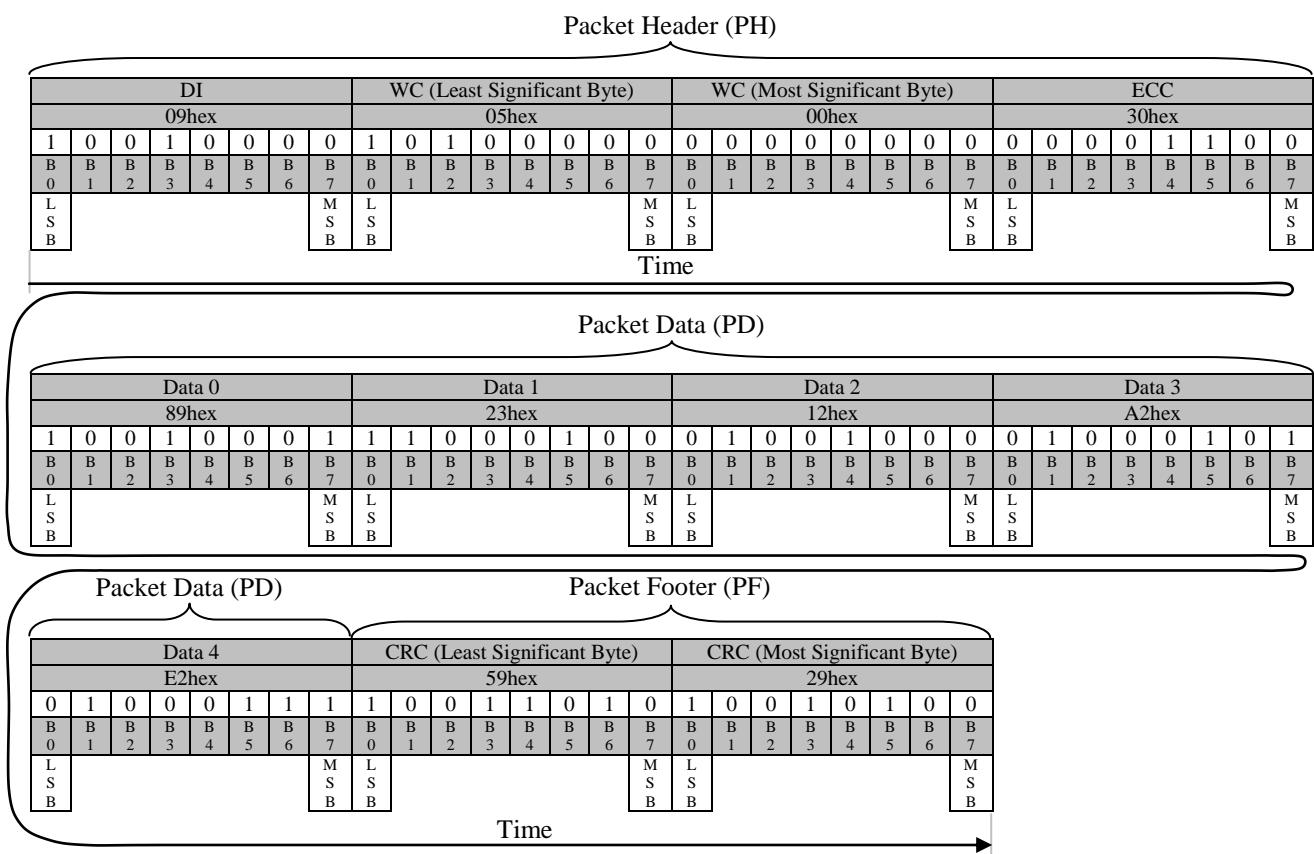


Figure 75: Null Packet, No Data (NP-L) - Example

8.1.3.2.1.7 End of Transmission Packet (EoTP)

“End of Transmission Packet” (EoTP) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 1000b), from the MCU to the display module. The purposes of this command is terminated the high Speed Data Transmission (HSDT) mode properly when there is added this extra packet after the last payload packet before “End of Transmission” (EoT), which is an interface level functionality.

The MCU can decide if it wants to use the “End of Transmission Packet” (EoTP) or not. The display shall have the capability to support both: i.e. If the MCU applies the EoTP, it shall report the “DSI Protocol Violation Error” when the EoTP is not detected in the High-Speed (HS). The display module error reporting shall be enabled/disabled statistically, according to the module application.

The display module **is or isn't receiving** “End of Transmission Packet” (EoTP) from the MCU during the Low Power Data Transmission (LPDT) mode before “Mark-1” (= Leaving Escape mode) what ends the Low Power Data Transmission (LPDT) mode.

The display module **is not allowed** to send “End of Transmission Packet” (EoTP) to the MCU during the Low Power Data Transmission (LPDT) mode.

The summary of the receiving and transmitting EoTP is listed below.

Table 30: Receiving and Transmitting EoTP during LPDT

Direction	Display Module (DM) in High Speed Data Transmission (HSDT)	Display Module (DM) in Low Power Data Transmission (LPDT)
MCU => Display Module	With or Without EoTP is Supported	With or Without EoTP is Supported
Display Module => MCU	HS Mode is not available (EoTP is not available)	EoTP cannot be sent by the Display Module (DM)

Short Packet (SPa) is using a fixed format as follows

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 00 1000b
- Packet Data (PD)
 - Data 0: 0Fhex
 - Data 1: 0Fhex
- Error Correction Code (ECC)
 - ECC: 01hex

This is defined on the Short Packet (SPa) as follows.

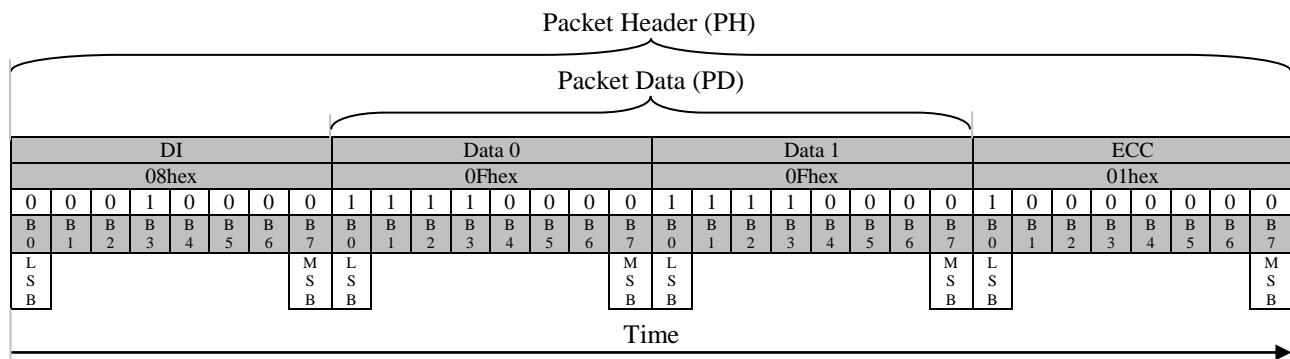


Figure 76: End of Transmission Packet (EoTP)

Some use cases of the “End of Transmission Packet” (EoTP) are illustrated only for reference purposes below.

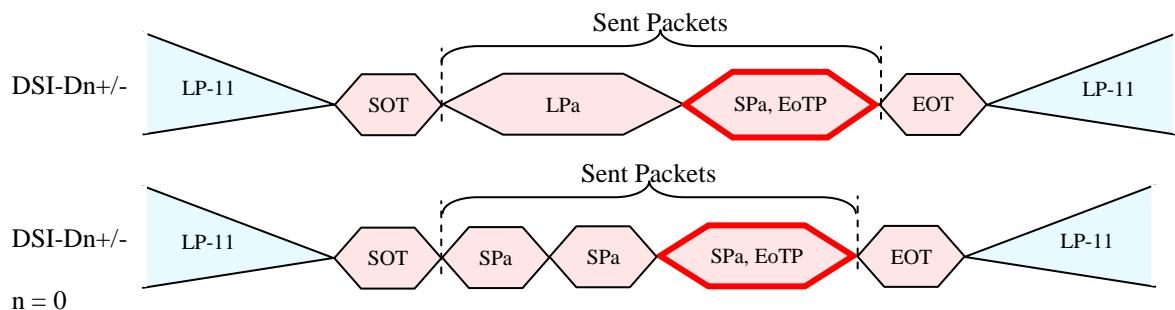


Figure 77: End of Transmission Packet (EoTP) - Examples

8.1.3.2.2 Packet from the Display Module to the MCU

8.1.3.2.2.1 Used Packet types

The display module is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS) (See chapter “8.1.3.2.1.5 Display Command Set (DCS) Read, No Parameter” (DCSRN-S)) or an Acknowledge with Error Report (See chapter: “8.1.3.2.2.2 Acknowledge with Error Report (AwER)” (AwER)).

The used packet type is defined on Data Type (DT). See chapter “8.1.3.1.3.1.2 Data Type (DT)”.

It is **not** possible that the display module is sending return bytes in several packets even if the maximum size of the Packet Data (PD) could be sent in one packet.

Both cases are illustrated for reference purposes below.

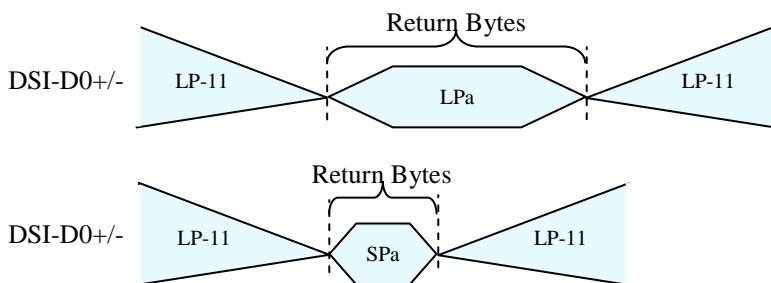


Figure 78: Return Bytes on Single Packet

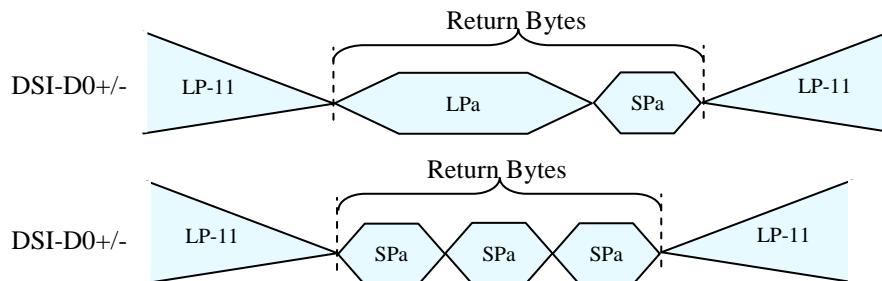
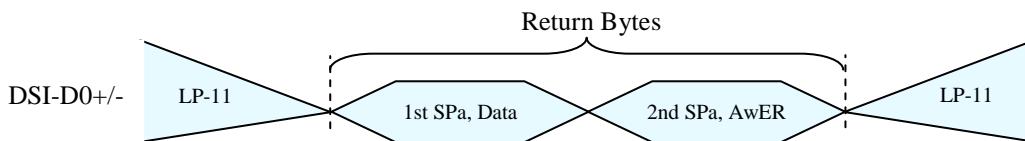


Figure 79: Return Bytes on Several Packets – Not Possible

Exception:

The display module is returning 2 packets (1st packet: Data, 2nd Packet: Acknowledge with Error Report) to the MCU when the display module has received a read command (See chapter “8.1.3.2.1.5 Display Command Set (DCS) Read, No Parameter (DCSRN-S)”) where has been detected and corrected a single bit error by the EEC (See bit 8 on “Table 32: Acknowledge with Error Report (AwER) for Short Packet (SPa) Response”). These return packets are illustrated for reference purposes below.



AwER = Acknowledge with Error Report

Figure 80: Exception when Return Bytes on Several Packets

8.1.3.2.2.2 Acknowledge with Error Report (AwER)

“Acknowledge with Error Report” (AwER) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0010b), from the display module to the MCU.

The Packet Data (PD) can include bits, which are defining the current error, when a corresponding bit is set to ‘1’, as they are defined on the following table.

Table 31: Acknowledge with Error Report (AwER) for Long Packet (LPa) Response

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to ‘0’ internally
15	DSI Protocol Violation

Table 32: Acknowledge with Error Report (AwER) for Short Packet (SPa) Response

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Set to ‘0’ internally (Only for Long Packet (LP))
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to ‘0’ internally
15	DSI Protocol Violation

These errors are included from all packages what has been received from the MCU to the display module, before Bus Turnaround (BTA).

The display module ignores the received packet which includes error or errors.

Acknowledge with Error Report (AwER) of the Short Packet (SPa) is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 00 0010b
- Packet Data (PD)
 - Bit 8: ECC Error, single-bit (detected and corrected)
 - AwER: 0100h
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

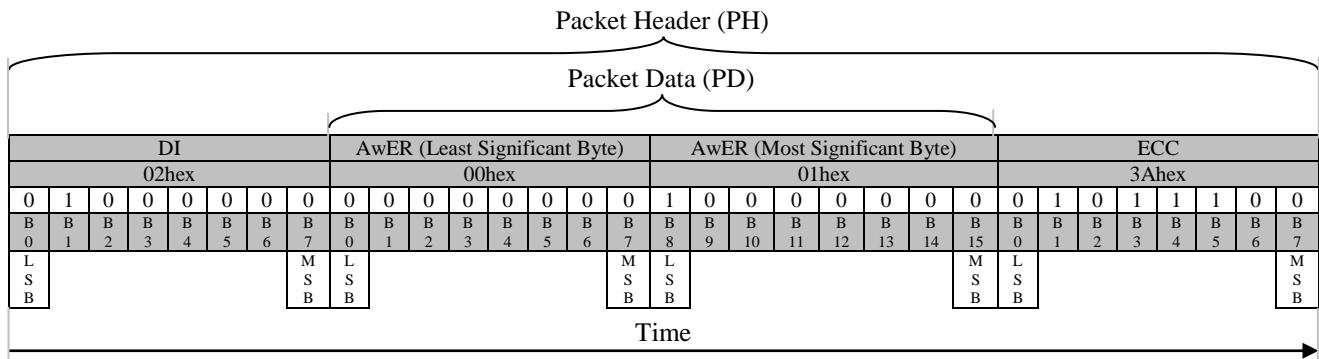


Figure 81: Acknowledge with Error Report (AwER) – Example

It is possible that the display module has received several packets, which have included errors, from the MCU before the MCU is doing Bus Turnaround (BTA). Some examples are illustrated for reference purposes below.

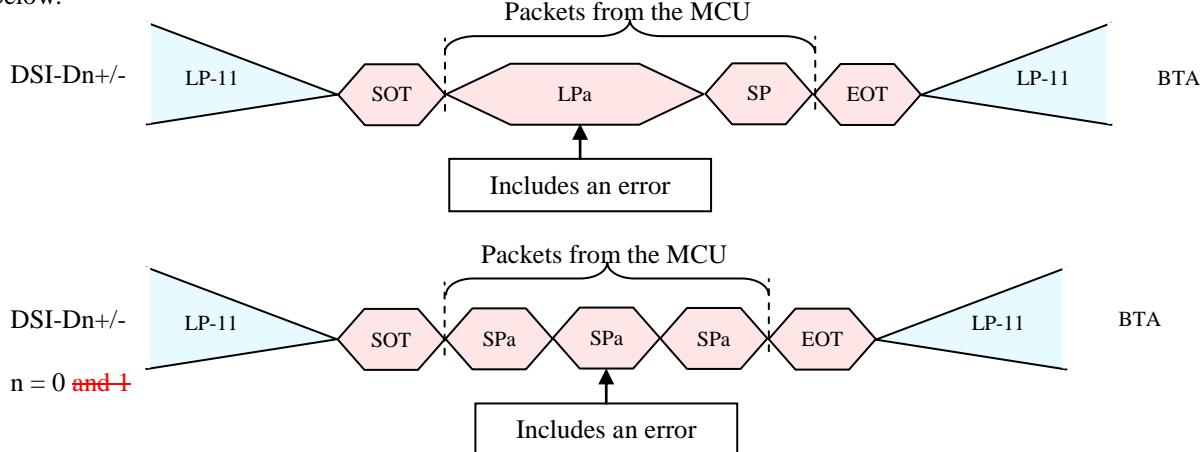


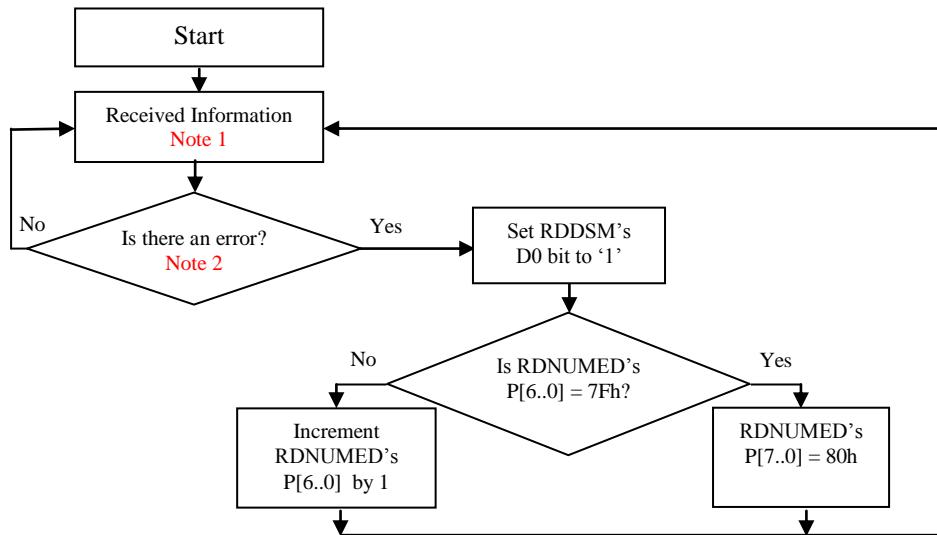
Figure 82: Errors Packets

Therefore, there is needed a method to check if there has been errors on the previous packets. These errors of the previous packets can check “9.2.8 Read Display Signal Mode (0Eh)” and “9.2.3 Read Number of the Errors on DSI (05h)” commands.

The bit D0 of the “9.2.8 Read Display Signal Mode (0Eh)” command has been set to ‘1’ if a received packet includes an error.

The number of the packets, which are including an **ECC or CRC** error, are calculated on the RDNUMED register, which can read “9.2.3 Read Number of the Errors on DSI (05h)” command. This command also sets the RDNUMED register to 00h as well as set the bit D0 of the “9.2.8 Read Display Signal Mode (0Eh)” command to ‘0’ after the MCU has read the RDNUMED register from the display module.

The functionality of the RDNUMED register is illustrated for reference purposes below.



Notes:

1. This information can be Interface or Packet Level Communication but it is always from the MCU to the display module in this case.
2. CRC or ECC error

Figure 83: Flow Chart for Errors on DSI

8.1.3.2.2.3 DCS Read Long Response (DCSRR-L)

“DCS Read Long Response” (DCSRR-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 01 1100b), from the display module to the MCU.

“DCS Read Long Response” (DCSRR-L) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 01 1100b
- Word Count (WC)
 - Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
 - Data 0: 89hex
 - Data 1: 23hex
 - Data 2: 12hex
 - Data 3: A2hex
 - Data 4: E2hex
- Packet Footer (PF)

This is defined on the Long Packet (LP) as follows.

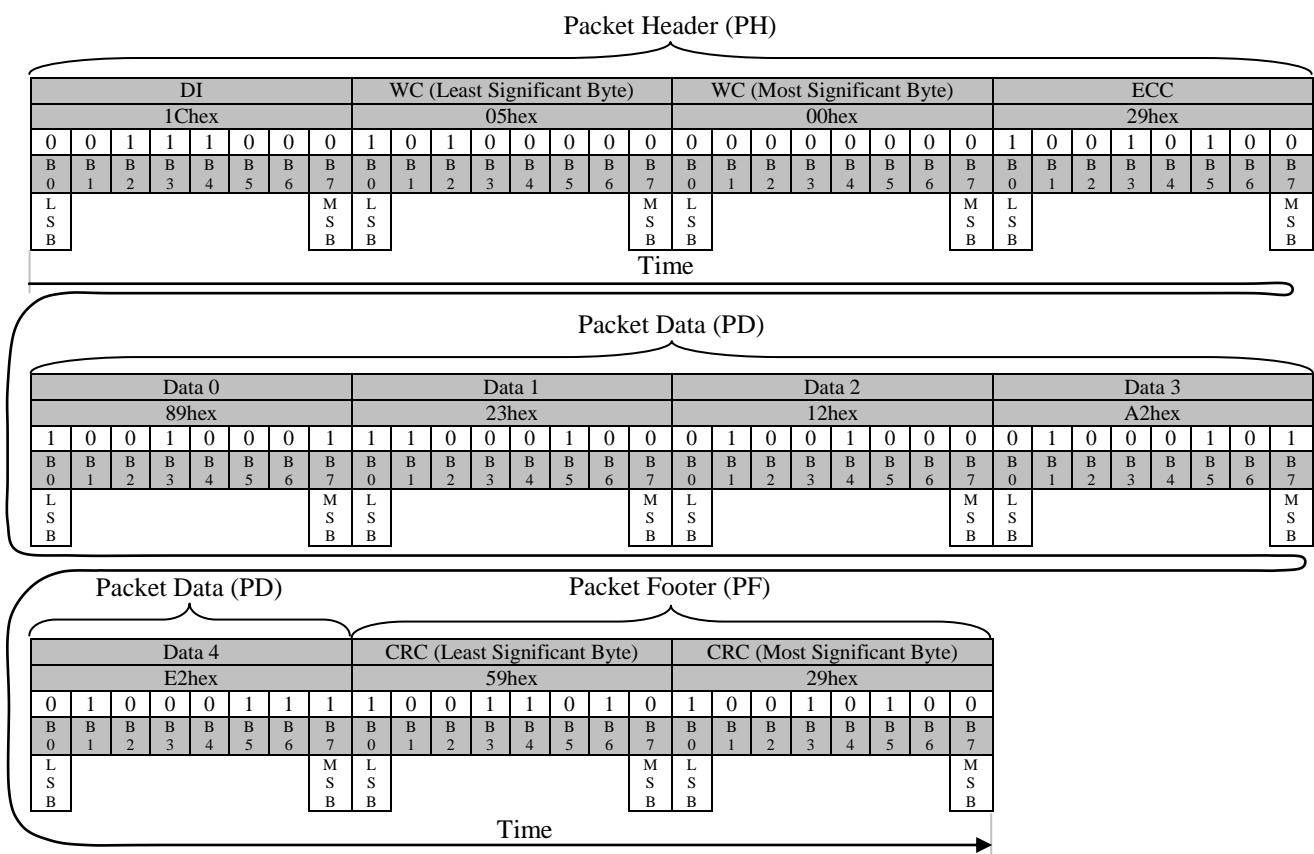


Figure 84: DCS Read Long Response (DCSRR-L) - Example

8.1.3.2.2.4 DCS Read Short Response, 1 Byte Returned (DCSRR1-S)

“DCS Read Short Response, 1 Byte Returned” (DCSRR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0001b), from the display module to the MCU.

“DCS Read Short Response, 1 Byte Returned” (DCSRR1-S) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 10 0001b
- Packet Data (PD)
 - Data 0: 45hex
 - Data 1: 00hex (Always)
- Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.

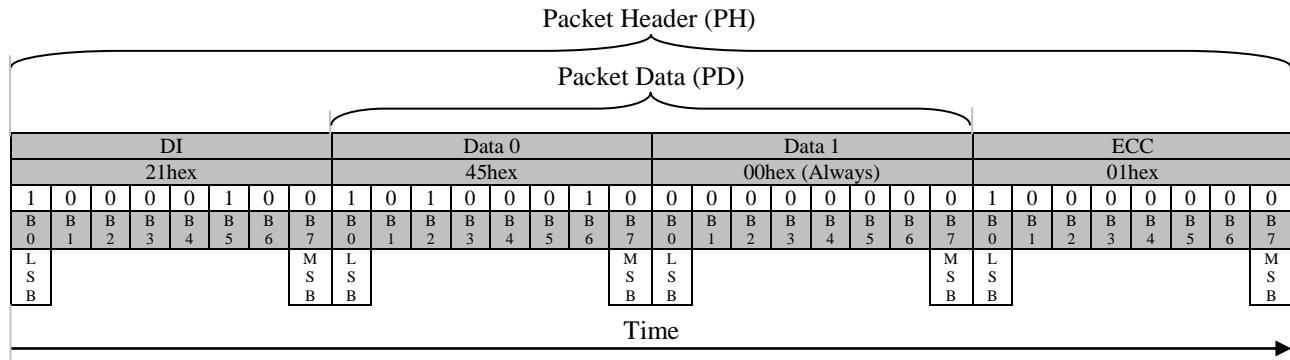


Figure 85: DCS Read Short Response, 1 Byte Returned (DCSRR1-S) - Example

8.1.3.2.2.5 DCS Read Short Response, 2 Bytes Returned (DCSRR2-S)

“DCS Read Short Response, 2 Bytes Returned” (DCSRR2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0010b), from the display module to the MCU.

“DCS Read Short Response, 2 Bytes Returned” (DCSRR2-S) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 10 0010b
- Packet Data (PD)
 - Data 0: 45hex
 - Data 1: 32hex
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

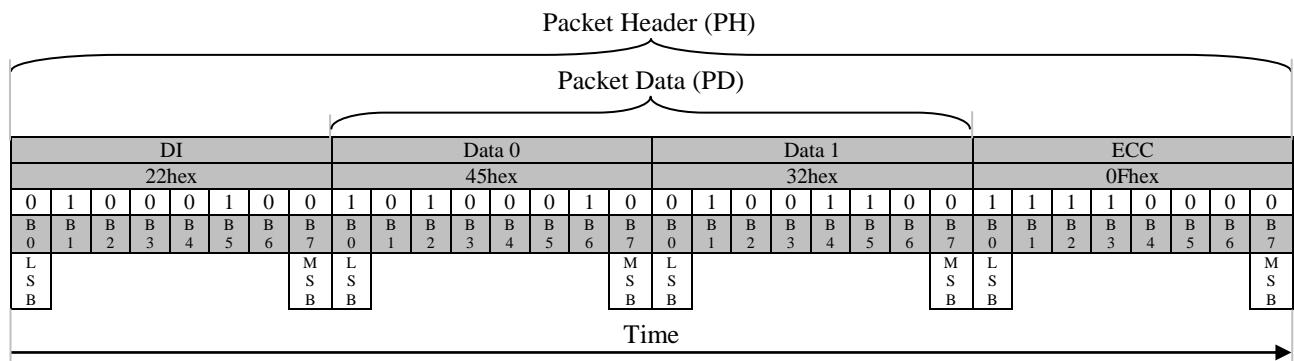


Figure 86: DCS Read Short Response, 2 Bytes Returned (DCSRR2-S) - Example

8.1.3.3 Communication Sequences

8.1.3.3.1 General

The communication sequences can be done on interface or packet levels between the MCU and the display module. See chapters “8.1.2 Interface Level Communication” and “8.1.3 Packet Level Communication”.

This communication sequence description is for DSI data lanes (DSI-D0+/-) and it has been assumed that the needed low level communication is done on DSI clock lanes (DSI-CLK+/-) automatically. See chapter “8.1.2.2 DSI-CLK Lanes”.

Functions of the interface level communication is described on the following table.

Table 33: Interface Level Communication

Interface Mode	Abbreviation	Interface Action Description
Low Power	LP-11	Stop State
	LPDT	Low Power Data Transmission
	ULPS	Ultra-Low Power State
	RAR	Remote Application Reset
	TEE	Tearing Effect Event
	ACK	Acknowledge (No error)
	BTA	Bus Turnaround
High Speed	HSDT	High Speed Data Transmission

Functions of the packet level communication is described on the following table.

Table 34: Packet Level Communication

Packet Sender	Abbreviation	Packet Size	Packet Description
MCU	DCSW1-S	SPa	DCS Write, 1 Parameter
	DCSWN-S	SPa	DCS Write, No Parameter
	DCSW-L	LPa	DCS Write Long
	DCSRN-S	SPa	DCS Read, No Parameter
	SMRPS-S	SPa	Set Maximum Return Packet Size
	NP-L	LPa	Null Packet, No Data
	EoTP	SPa	End of Transmission Packet
Display Module	AwER	SPa	Acknowledge with Error Report
	DCSRR-L	LPa	DCS Read Long Response
	DCSRR1-S	SPa	DCS Read Short Response
	DCSRR2-S	SPa	DCS Read Short Response

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8.1.3.3.2 Sequences

8.1.3.3.2.1 DCS Write, 1 Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” is defined on chapter “8.1.3.2.1.3 Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” and example sequences, how this packet is used, is described on following tables.

Table 35: DCS Write, 1 Parameter Sequence – Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

Table 36: DCS Write, 1 Parameter Sequence – Example 2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4 3	-	LP-11	=>	-	-	End

Table 37: DCS Write, 1 Parameter Sequence – Example 3

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4 3	-	LP-11	=>	-	-	
5 4	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
6 5	-	-	<=	LP-11	-	If No Error => Goto Line 8 7 If Error => Goto Line 13 12
7 6						
8 7	-	-	<=	ACK	-	No Error
9 8	-	-	<=	LP-11	-	
10 9	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
11 10	-	LP-11	=>	-	-	End
12 11						
13 12	-	-	<=	LPDT	AwER	Error Report
14 13	-	-	<=	LP-11	-	
15 14	-	BTA	<=>	BTA	-	
16 15	-	LP-11	=>	-	-	End

8.1.3.3.2.2 DCS Write, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, No Parameter (DCSWN-S)” is defined on chapter “8.1.3.2.1.2 Display Command Set (DCS) Write, No Parameter (DCSWN-S)” and example sequences, how this packet is used, is described on following tables.

Table 38: DCS Write, No Parameter Sequence – Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

Table 39: DCS Write, No Parameter Sequence – Example 2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4 3	-	LP-11	=>	-	-	End

Table 40: DCS Write, No Parameter Sequence – Example 3

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4 3	-	LP-11	=>	-	-	
5 4	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
6 5	-	-	<=	LP-11	-	If No Error => Goto Line 8 7 If Error => Goto Line 13 12
7 6						
8 7	-	-	<=	ACK	-	No Error
9 8	-	-	<=	LP-11	-	
10 9	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
11 10	-	LP-11	=>	-	-	End
12 11						
13 12	-	-	<=	LPDT	AwER	Error Report
14 13	-	-	<=	LP-11	-	
15 14	-	BTA	<=>	BTA	-	
16 15	-	LP-11	=>	-	-	End

8.1.3.3.2.3 DCS Write Long Sequence

A Long Packet (LPa) of “Display Command Set (DCS) Write Long (DCSW-L)” is defined on chapter “8.1.3.2.1.4 Display Command Set (DCS) Write Long (DCSW-L)” and example sequences, how this packet is used, is described on following tables.

Table 41: DCS Write Long Sequence – Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

Table 42: DCS Write Long Sequence – Example 2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
3 4	-	LP-11	=>	-	-	End

Table 43: DCS Write Long Sequence – Example 3

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4 3	-	LP-11	=>	-	-	
5 4	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
6 5	-	-	<=	LP-11	-	If No Error => Goto Line 8 7 If Error => Goto Line 13 +2
7 6						
8 7	-	-	<=	ACK	-	No Error
9 8	-	-	<=	LP-11	-	
10 9	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
11 10	-	LP-11	=>	-	-	End
12 11						
13 12	-	-	<=	LPDT	AwER	Error Report
14 13	-	-	<=	LP-11	-	
15 14	-	BTA	<=>	BTA	-	
16 15	-	LP-11	=>	-	-	End

Table 44: DCS Write Long Sequence – Example 4

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	Memory Write (2Ch)
3	DCSW-L	HSDT	=>	-	-	Memory Write Continue (3Ch)
4	DCSW-L	HSDT	=>	-	-	Memory Write Continue (3Ch)
5	DCSW1-S	HSDT	=>	-	-	Memory Write Continue (3Ch) with 1 parameter
6	EoTP	HSDT	=>	-	-	End of Transmission Packet
7 6	-	LP-11	=>	-	-	End

Note: This is an example where is wanted to send image data in 4 packets

8.1.3.3.2.4 DCS Read, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” is defined on chapter “8.1.3.2.1.5 Display Command Set (DCS) Read, No Parameter (DCSRN-S)” and example sequences, how this packet is used, is described on following tables.

Table 45: DCS Read, No Parameter Sequence – Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	SMRPS-S	HSDT	=>	-	-	Defined how many data byte is wanted to read: 1 byte
3	DCSRN-S DCSW-L	HSDT	=>	-	-	Wanted to get a response ID1 (DAh)
4	EoTP	HSDT	=>	-	-	End of Transmission Packet
5 4	-	LP-11	=>	-	-	
6 5	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
7 6	-	-	<=	LP-11	-	If No Error => Goto Line 9 8 If Error => Goto Line 14 43 If Error is Corrected by ECC => Goto Line 19 48
8 7						
9 8	-	-	<=	LPDT	DCSRR1-S	Responded 1 byte return
10 9	-	-	<=	LP-11	-	
11 40	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
12 41	-	LP-11	=>	-	-	End
13 42						
14 43	-	-	<=	LPDT	AwER	Error Report
15 44	-	-	<=	LP-11	-	
16 45	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
17 46	-	LP-11	=>	-	-	End
18 47						
19 48	-	-	<=	LPDT	DCSRR1-S	Responded 1 byte return
20 49	-	-	<=	LPDT	AwER	Error Report (Error is Corrected by ECC)
21 50	-	-	<=	LP-11	-	
22 41	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
23 42	-	LP-11	=>	-	-	End

Table 46: DCS Read, No Parameter Sequence – Example 2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	SMRPS-S	HSDT	=>	-	-	Defined how many data byte is wanted to read: 200 bytes
3	DCSW-L	HSDT	=>	-	-	Wanted to get a response "Memory Read" (2Eh)
4	EoTP	HSDT	=>	-	-	End of Transmission Packet
5 4	-	LP-11	=>	-	-	
6 5	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
7 6	-	-	<=	LP-11	-	If No Error => Goto Line 9 8 If Error => Goto Line 14 43 If Error is Corrected by ECC => Goto Line 19 48
8 7						
9 8	-	-	<=	LPDT	DCSRR-L	Responded 200 bytes return
10 9	-	-	<=	LP-11	-	
11 10	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
12 11	-	LP-11	=>	-	-	End
13 12						
14 13	-	-	<=	LPDT	AwER	Error Report
15 14	-	-	<=	LP-11	-	
16 15	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
17 16	-	LP-11	=>	-	-	End
18 17						
19 18	-	-	<=	LPDT	DCSRR-L	Responded 200 bytes return
20 19	-	-	<=	LPDT	AwER	Error Report (Error is Corrected by ECC)
21 20	-	-	<=	LP-11	-	
22 21	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
23 22	-	LP-11	=>	-	-	End

8.1.3.3.2.5 Null Packet, No Data Sequence

A Long Packet (LPa) of “Null Packet, No Data (NP-L)” is defined on chapter “8.1.3.2.1.6 Null Packet, No Data (NP-L)” and an example sequence, how this packet is used, is described on the following table.

Table 47: Null Packet, No Data Sequence - Example

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	NP-L	HSDT	=>	-	-	Only High Speed Data Transmision is used
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4 3	-	LP-11	=>	-	-	End

8.1.3.3.2.6 End of Transmission Packet

A Short Packet (SPa) of “End of Transmission (EoTP)” is defined on chapter “8.1.3.2.1.7 End of Transmission Packet (EoTP)” and an example sequence, how this packet is used, is described on the following table.

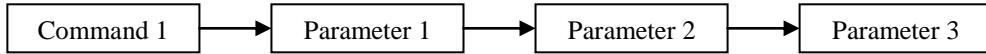
Table 48: End of Transmission Packet - Example

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	NP-L	HSDT	=>	-	-	Only High Speed Data Transmision is used
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

8.1.4 Display Module Data Transfer Break

Display module data transfer break is illustrated for reference purposes below.

Without break



With break (See and check also exceptions *)

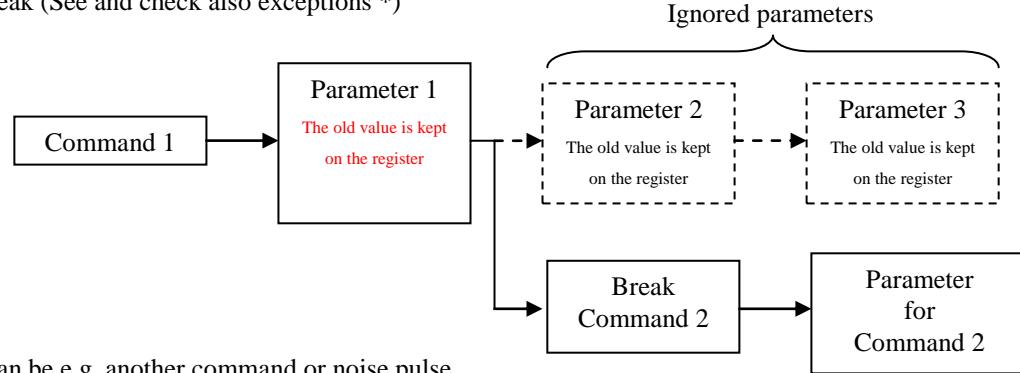


Figure 87: Break During Parameter

*) See also an exception for ~~the break sequence (Command 1 + Parameter 1)~~ on section “9.1 Command List” and Note 4.

The MCU can create a break condition when it is forcing DSI data lanes in the LP-11 mode.

The display module stops to control DSI data lanes (change from a transmitter mode to a received mode) if it was controlling DSI data lanes as a transmitter when the MCU is forcing DSI data lanes in the LP-11.

This break condition can be done any time when the MCU or the display module is controlling DSI data lanes e.g. the display module is sending data to the MCU.

8.1.5 Display Module Data Transfer Pause

Pause can be done on DSI between Packets when they are sent to same or different receiver (Virtual Channel (VC)) e.g.

1. Same receiver: Packet 1 (VC = 00) => Packet 2 (VC = 00) => Packet 3 (VC = 00) => ...
2. Diffrent receiver: Packet 1 (VC = 00) => Packet 2 (VC = 01) => Packet 3 (VC = 00) => ...

This means that "=>" symbol means a pause on DSI.

8.1.6 Display Module Data Transfer Modes

The display module have two colour modes ~~has one colour mode~~ for transferring data to the Frame Memory and they are ~~it is~~ 16-bit and 24-bit colour per pixel. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

8.1.6.1 Method 1

The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written.

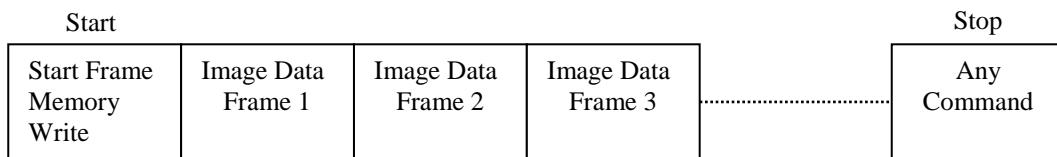


Figure 88: Data Transfer Method 1

8.1.6.2 Method 2

Image Data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame is downloaded.

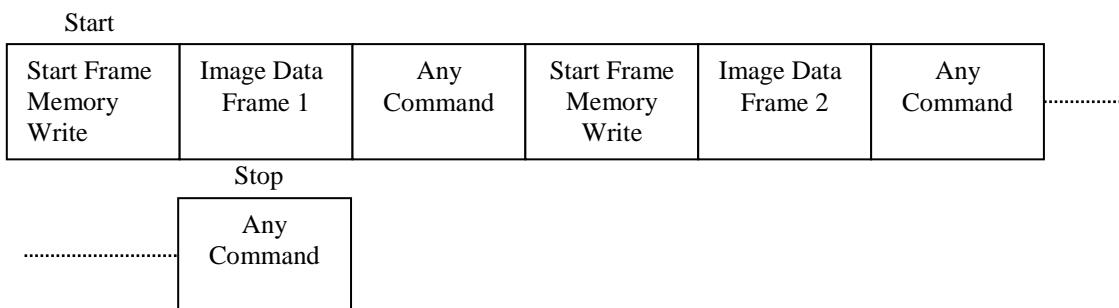


Figure 89: Data Transfer Method 2 with “Any Command” Break

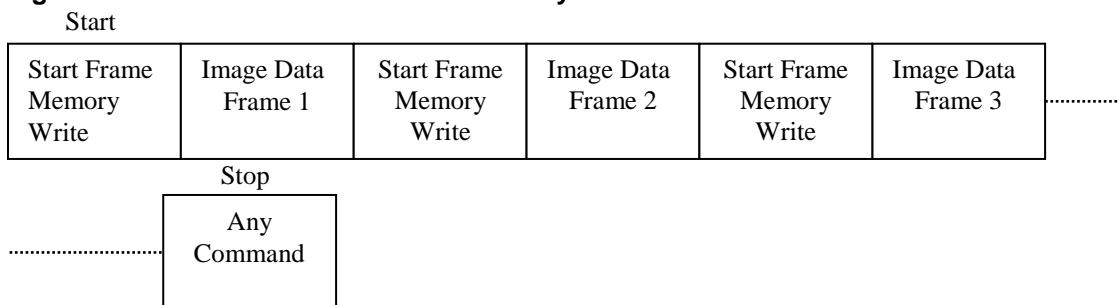


Figure 90: Data Transfer Method 2 with “Start Frame Memory Write” Break

Notes:

1. The display module can receive image frames in both methods what can contain odd or even number of pixels. Only complete pixel data will be stored in the Frame Memory.
2. "9.2.30 Memory Write Continue (3Ch)" or "9.2.31 Memory Read Continue (3Eh)" commands are not stopping writing or reading to/from the frame memory. These commands can be used if there is wanted to continue the writing or reading to/from the frame memory when "Any command" has stopped the memory writing or reading.
3. "Any Command" can be as same as "Start Frame Memory Write".

8.1.7 Display Module Data Colour Coding

8.1.7.1 Meaning of the Pixel Information on DSI

The meaning of the pixel information, when there are used 3 components/pixel (Red, Green and Blue) on DSI, is described for main colours on the following table:

Table 49: Meaning of the Pixel Information for Main Colors on DSI

Pixel Colour	R Component	G Component	B Component
Black	All bits are 0	All bits are 0	All bits are 0
Blue	All bits are 0	All bits are 0	All bits are 1
Green	All bits are 0	All bits are 1	All bits are 0
Cyan	All bits are 0	All bits are 1	All bits are 1
Red	All bits are 1	All bits are 0	All bits are 0
Magenta	All bits are 1	All bits are 0	All bits are 1
Yellow	All bits are 1	All bits are 1	All bits are 0
White	All bits are 1	All bits are 1	All bits are 1

Note: There are only defined main colours on this table - Not all grey levels of colours.

8.1.7.2 16 bit/pixel Writing

See reference from MIPI DCS for 16bpp write colour order.

8.1.7.3 24 bit/pixel Writing

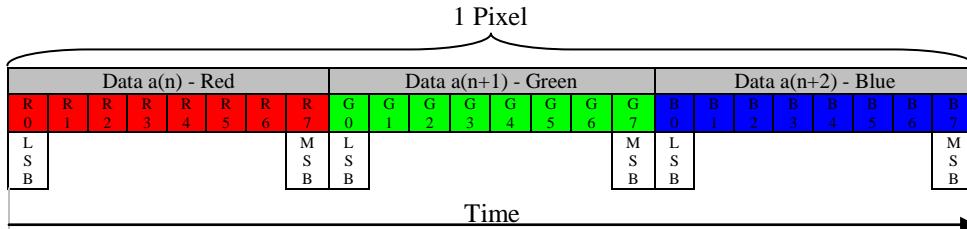
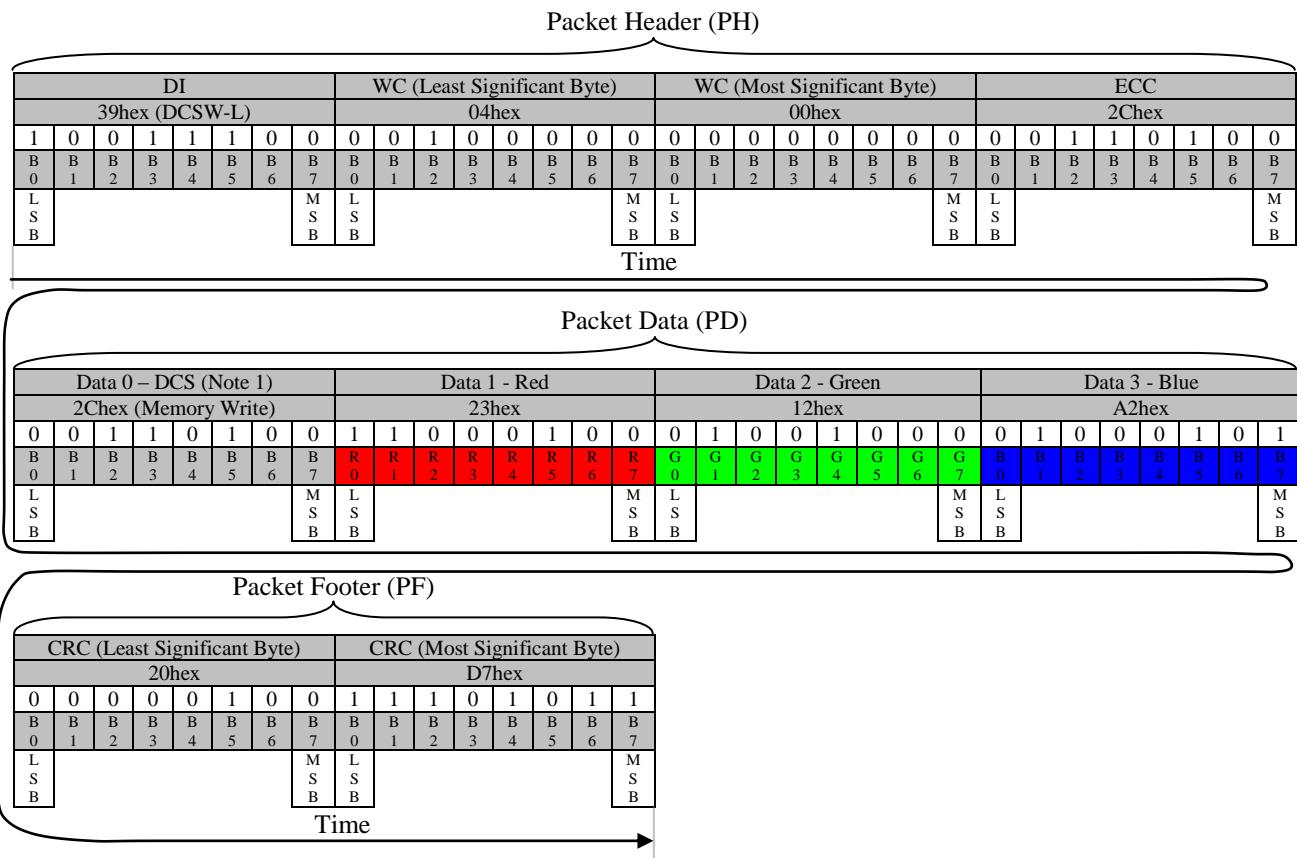


Figure 91: One Pixel Bit and Colour Write Orders

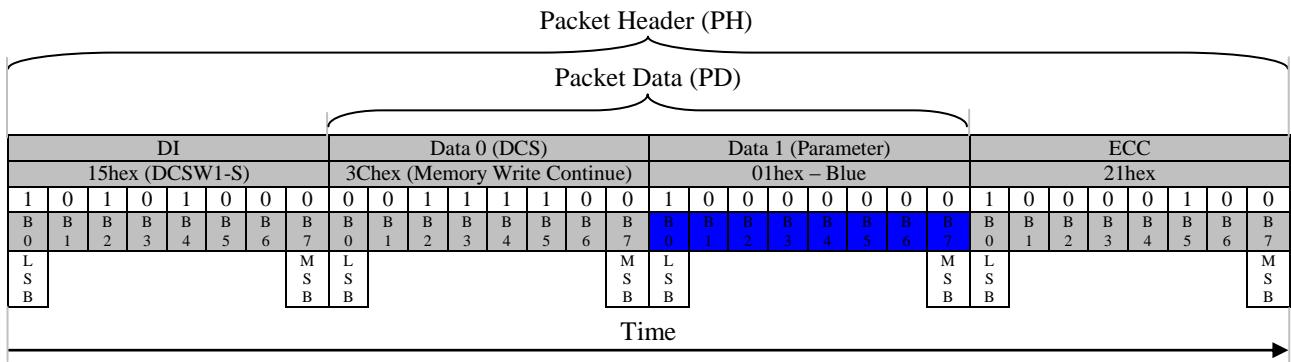
The MCU can send to the display module a following packet.



Notes:

1. Memory Write (2Ch) or Memory Write Continue (3Ch)
2. It is possible that one pixel information is split in two or three different packets which are ending and starting as follows:
 - R – GB (2 packets)
 - RG – B (2 packets)
 - R – G – B (3 packets)
3. Packet can include several pixels (Not only one pixel as in this example)

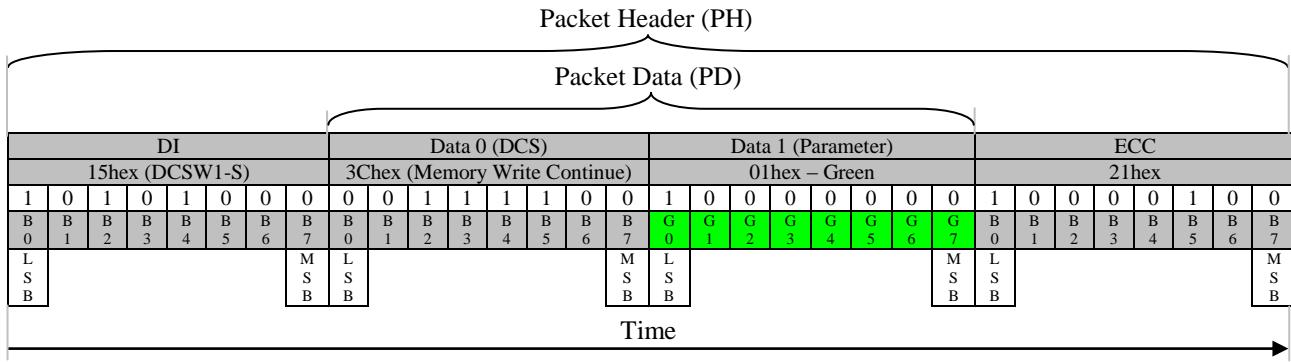
Figure 92: One Pixel Write (DCSW-L) – Example 1



Notes:

1. DCS (Data 0) cannot be “Memory Write” (2Ch) command. It must always be “Memory Write Continue” (3Ch)
2. Previous data byte was G[0:7]

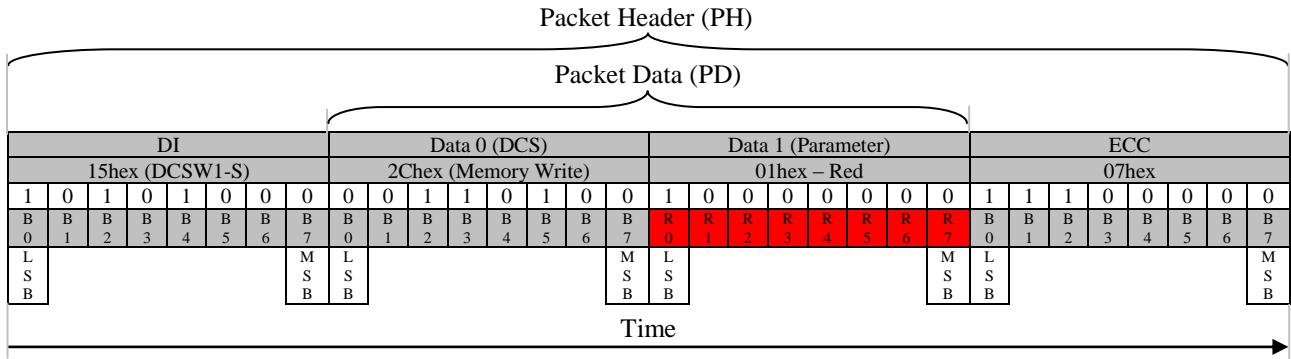
Figure 93: Blue Subpixel Write (DCSW1-S) – Example 2



Notes:

1. DCS (Data 0) cannot be “Memory Write” (2Ch) command. It must always be “Memory Write Continue” (3Ch)
2. Previous data byte was R[0:7]

Figure 94: Green Subpixel Write (DCSW1-S) – Example 3



Note: DCS (Data 0) can also be “Memory Write Continue” (3Ch) command

Figure 95: Red Subpixel Write (DCSW1-S) – Example 4

8.1.7.3.1 24 bit/pixel Reading

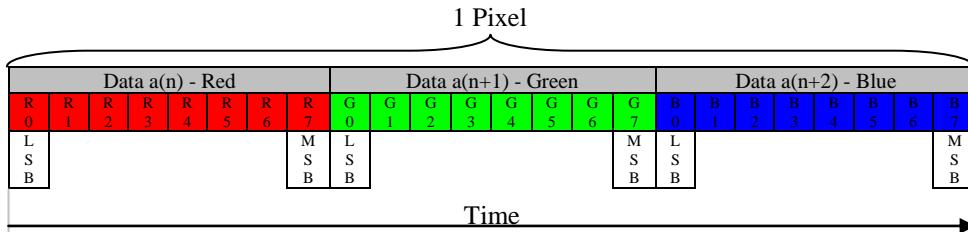
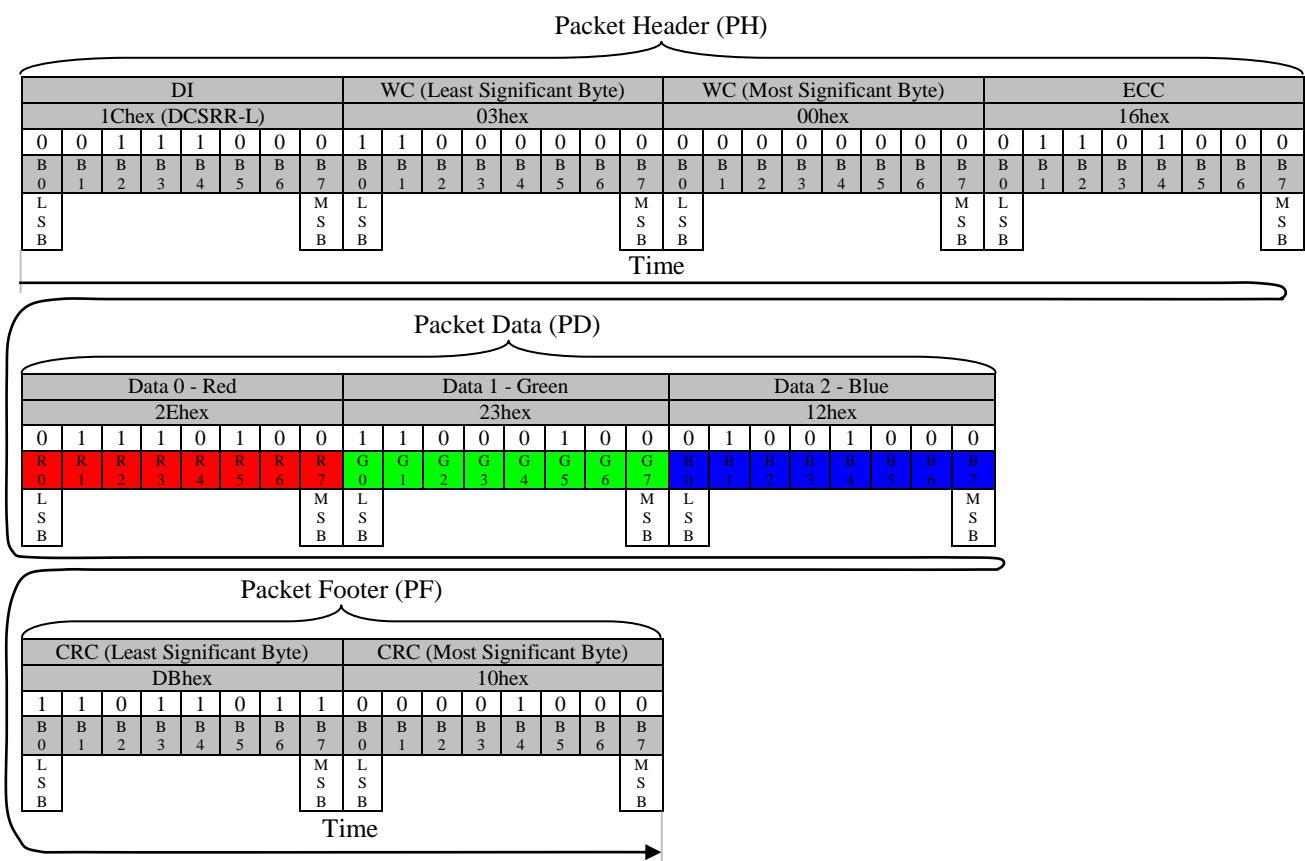


Figure 96: One Pixel Bit and Colour Read Order

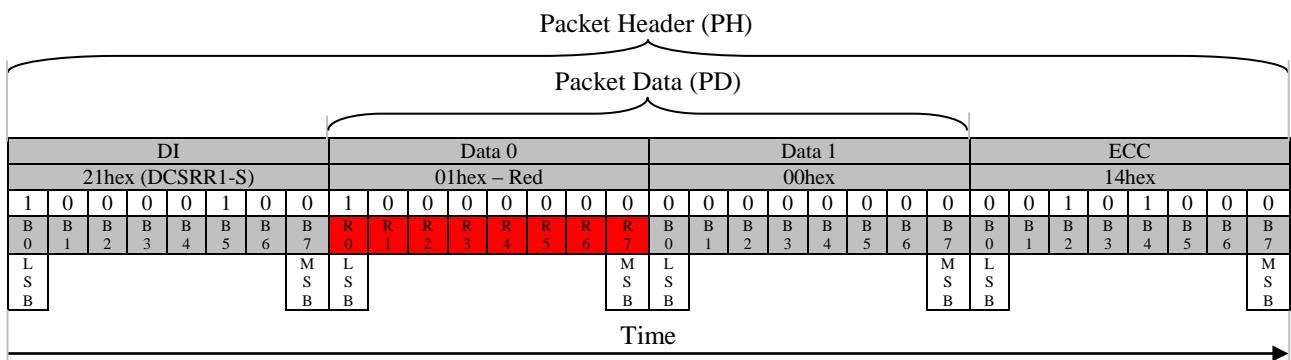
The display module can send to the MCU following packets after the MCU has sent a read command "Memory Read (2Eh)" or "Memory Read Continue (3Eh)".



Note: It is possible that one pixel information is split in two or three different packets:

- R – GB (2 packets)
- RG – B (2 packets)
- R – G – B (3 packets)

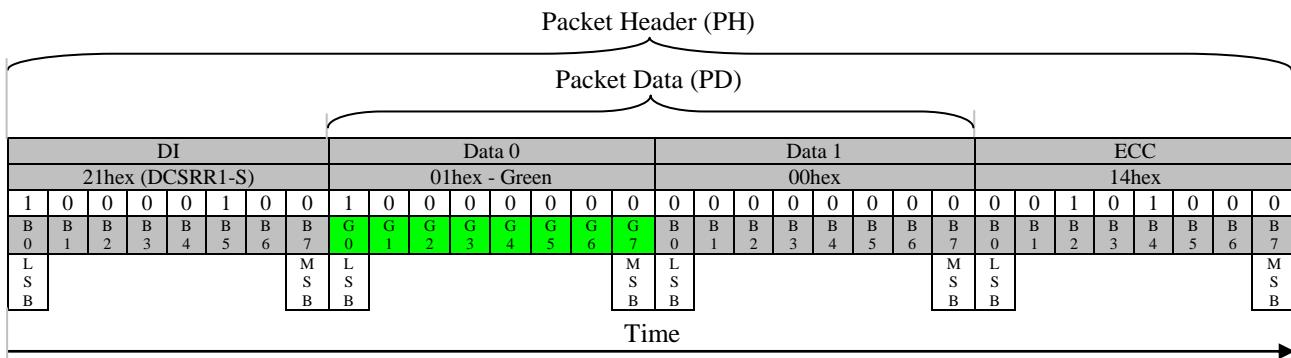
Figure 97: One Pixel Read Response (DCSRR-L) – Example 1



Notes:

1. Data 1 is always 00h
2. Previous data byte was B[0:7]

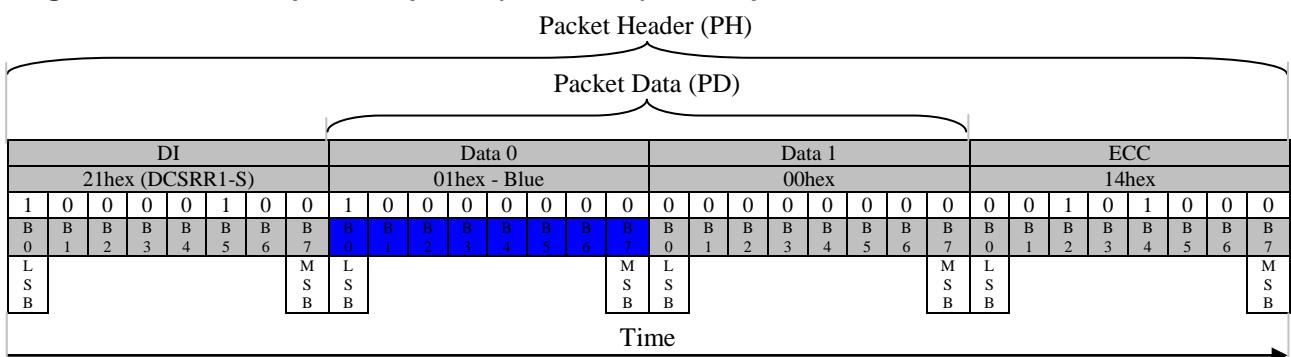
Figure 98: Red Subpixel Response (DCSRR1-S) – Example 2



Notes:

1. Data 1 is always 00h
2. Previous data byte was R[0:7]

Figure 99: Green Subpixel Response (DCSRR1-S) – Example 3



Notes:

1. Data 1 is always 00h
2. Previous data byte was G[0:7]

Figure 100: Blue Subpixel Response (DCSRR1-S) – Example 4

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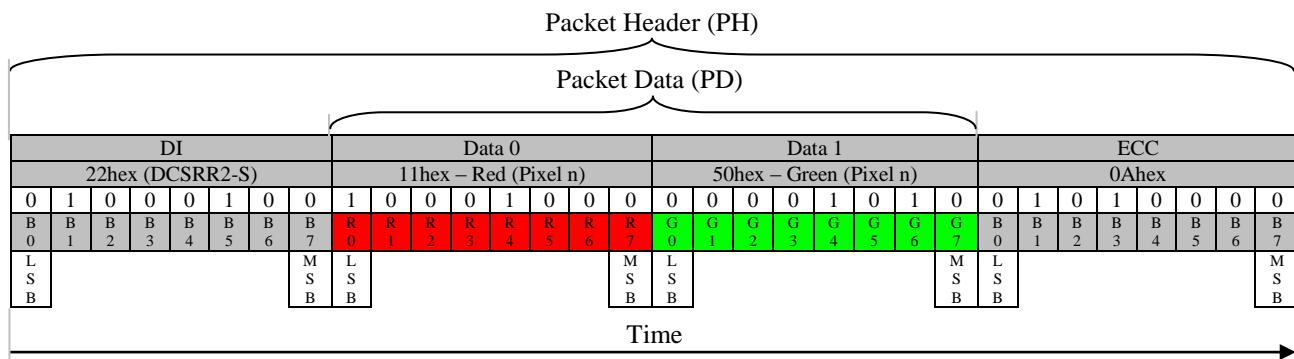
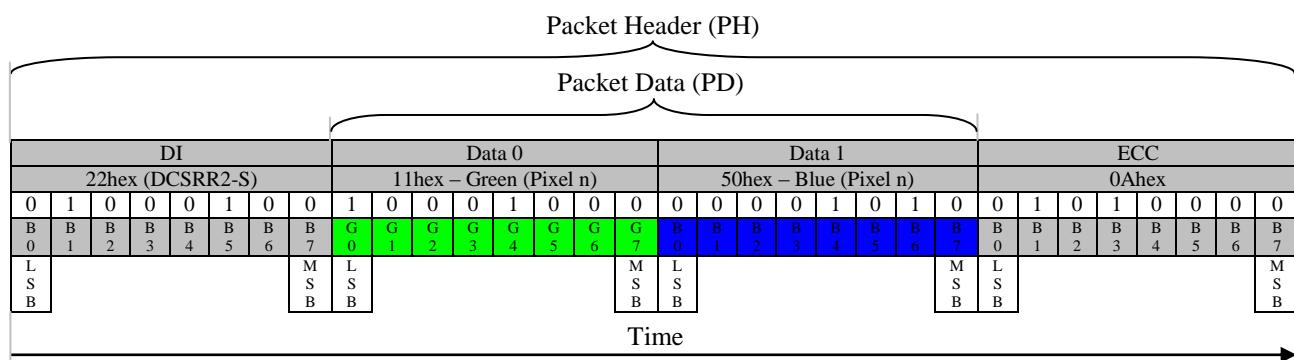
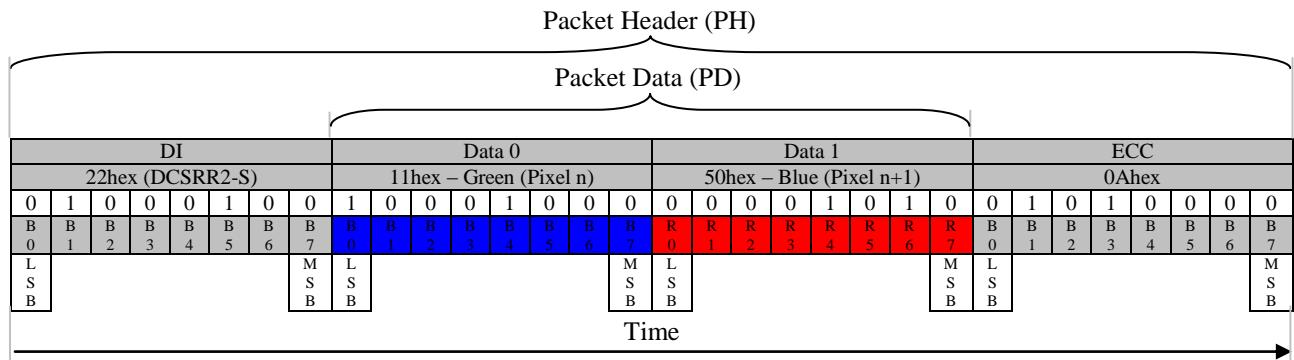


Figure 101: Red and Green Subpixels Response (DCSRR2-S) – Example 5



Note: Previous data byte was R[0:7]

Figure 102: Green and Blue Subpixels Response (DCSRR2-S) – Example 6



Note: Previous data byte was G[0:7]

Figure 103: Blue and Red Subpixels Response (DCSRR2-S) – Example 7

8.2 Frame Memory

8.2.1 Configuration

The frame memory stores display dots on the display module and it consists of 5,529,600 bits (360x24x640 bits).

There is no restriction on access to the frame memory even when the display data on the same address is loaded to the display panel side.

There will be no abnormal visible effect on the display panel when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

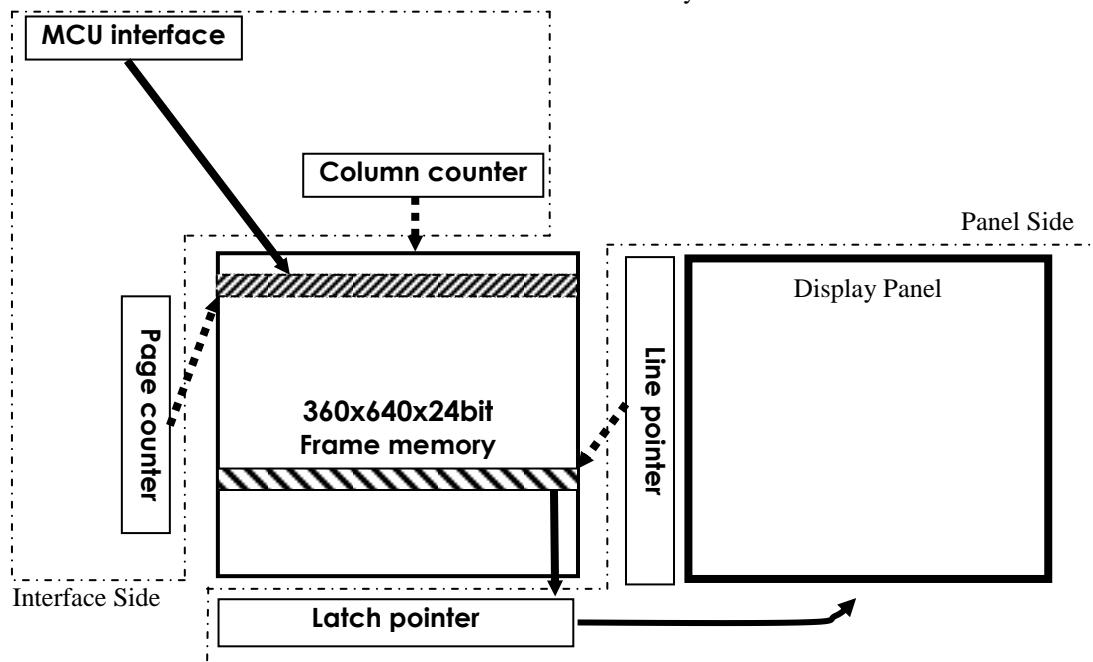


Figure 104: Frame Memory Configuration

8.2.2 Frame Memory to Display Address Mapping

The content of the frame memory within an area, where latch pointer is 0000h to 0167h and line pointer is 0000h to 027Fh, is displayed where the first dot is on leftmost top corner, store the dot data at (latch pointer, line pointer) = (0,0).

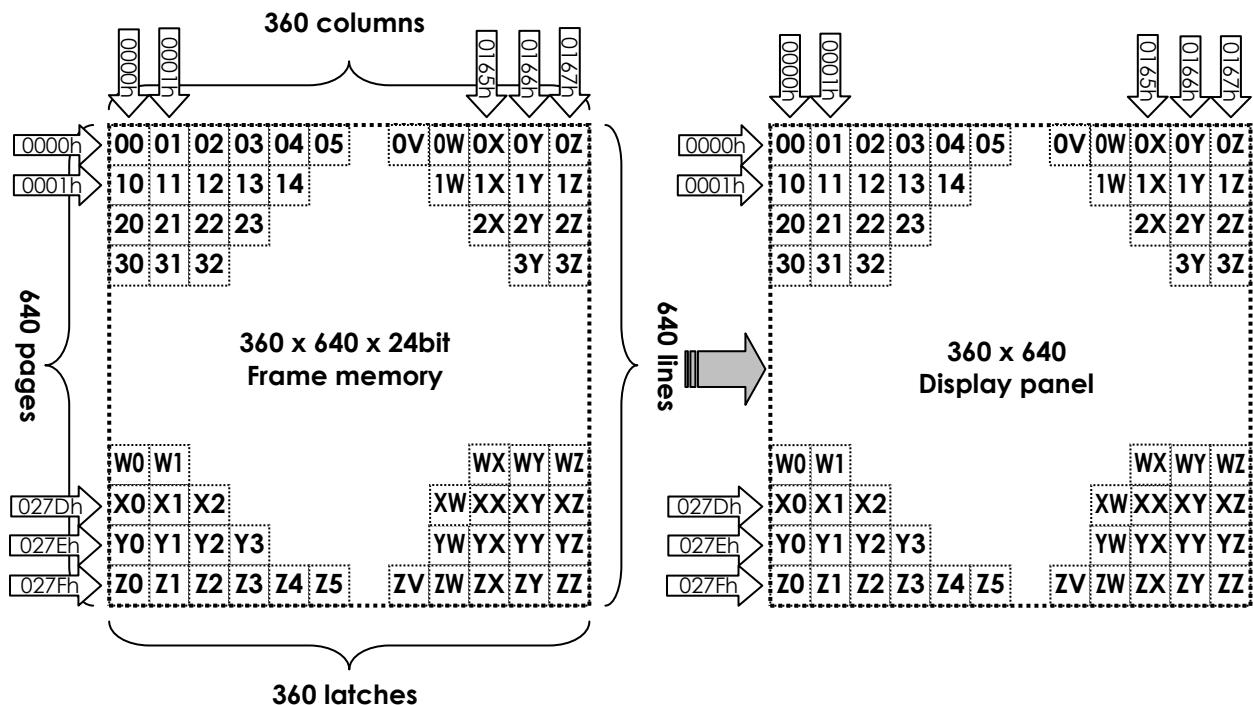


Figure 105: Memory Mapping versus Display Panel

8.2.3 MCU to Memory Write/Read Direction

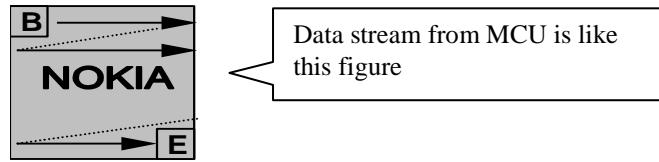


Figure 106: Pixel Sending Order from the MCU

The data is sending in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Access Control (36h)” Command, Bits B5, B6, and B7 as described below.

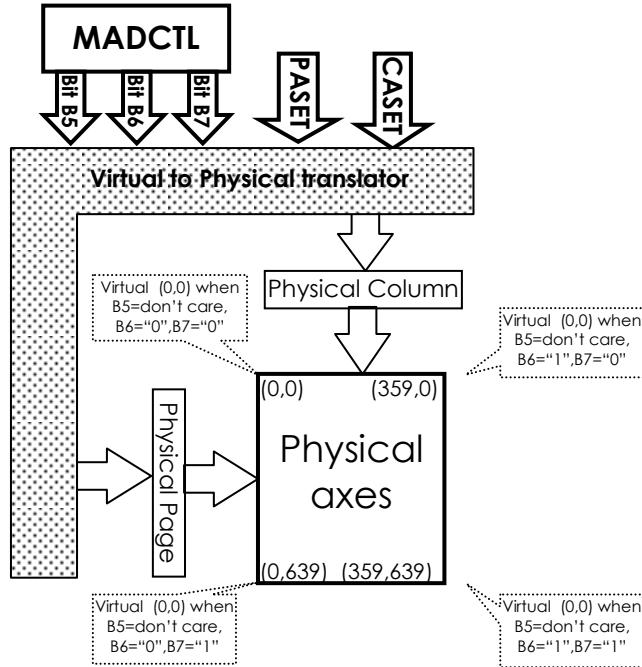


Figure 107: Image Data Writing Control

Table 50: CASET and PASET Control for Physical Column/Page

B5	B6	B7	CASET	PASET
0	0	0	Direct to Physical Column	Direct to Physical Page
0	0	1	Direct to Physical Column	Direct to (639-Physical Page)
0	1	0	Direct to (359-Physical Column)	Direct to Physical Page
0	1	1	Direct to (359-Physical Column)	Direct to (639-Physical Page)
1	0	0	Direct to Physical Page	Direct to Physical Column
1	0	1	Direct to (639-Physical Page)	Direct to Physical Column
1	1	0	Direct to Physical Page	Direct to (359-Physical Column)
1	1	1	Direct to (639-Physical Page)	Direct to (359-Physical Column)

For each image orientation, the controls for the column and page counters apply as below: -

Table 51: Column and Page Counter Control

Condition	Column Counter	Page Counter
When RAMWR/RAMRD command is accepted (Note 1)	Return to “Start Column”	Return to “Start Page”
Complete Pixel Read/Write action	Increment by 1	No change
The Column counter value is larger than “End column.”	Return to “Start Column”	Increment by 1
The Page counter value is larger than “End page”.	Return to “Start Column”	Return to “Start Page”

Notes

1. Commands “Memory Write Continue (3Ch)” and “Memory Read Continue (3Eh)” do not return the column counter to “Start Column” and the page counter to “Start Page”
2. Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7, B6 and B5. The write order for each pixel unit is

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

Figure 108: Bit Order of the Pixel on the Memory

3. One pixel unit represents 1 column and 1 page counter value on the Frame Memory.

The resultant image for each orientation setting is illustrated below:

Memory Writing Rotation/Flipping	Image in Frame Memory	B5	B6	B7
0 Degree	Normal 	0	0	0
0 Degree with V-Flipping	Y-Invert 	0	0	1
0 Degree with H-Flipping	X-Invert 	0	1	0
180 Degree	X Invert + Y Invert 	0	1	1
270 Degree with H-Flipping	Exchange Row-Column 	1	0	0
270 Degree	Exchange Row-Column + X Invert (270 deg rotation) 	1	0	1
90 Degree	Exchange Row-Column + Y Invert (90 deg rotation) 	1	1	0
270 Degree with V-Flipping	Exchange Row-Column + X Invert + Y Invert 	1	1	1

Figure 109: Image Data Writing Order on the Memory

Example for rotation with B7, B6 and B5

This example is using following values: start page = 0, end page = 40, start column = 0 and end column = 20
 => commands: page address set (0, 40) and column address set (0, 20).

The sent figure is as follows and its sending order is as follows.

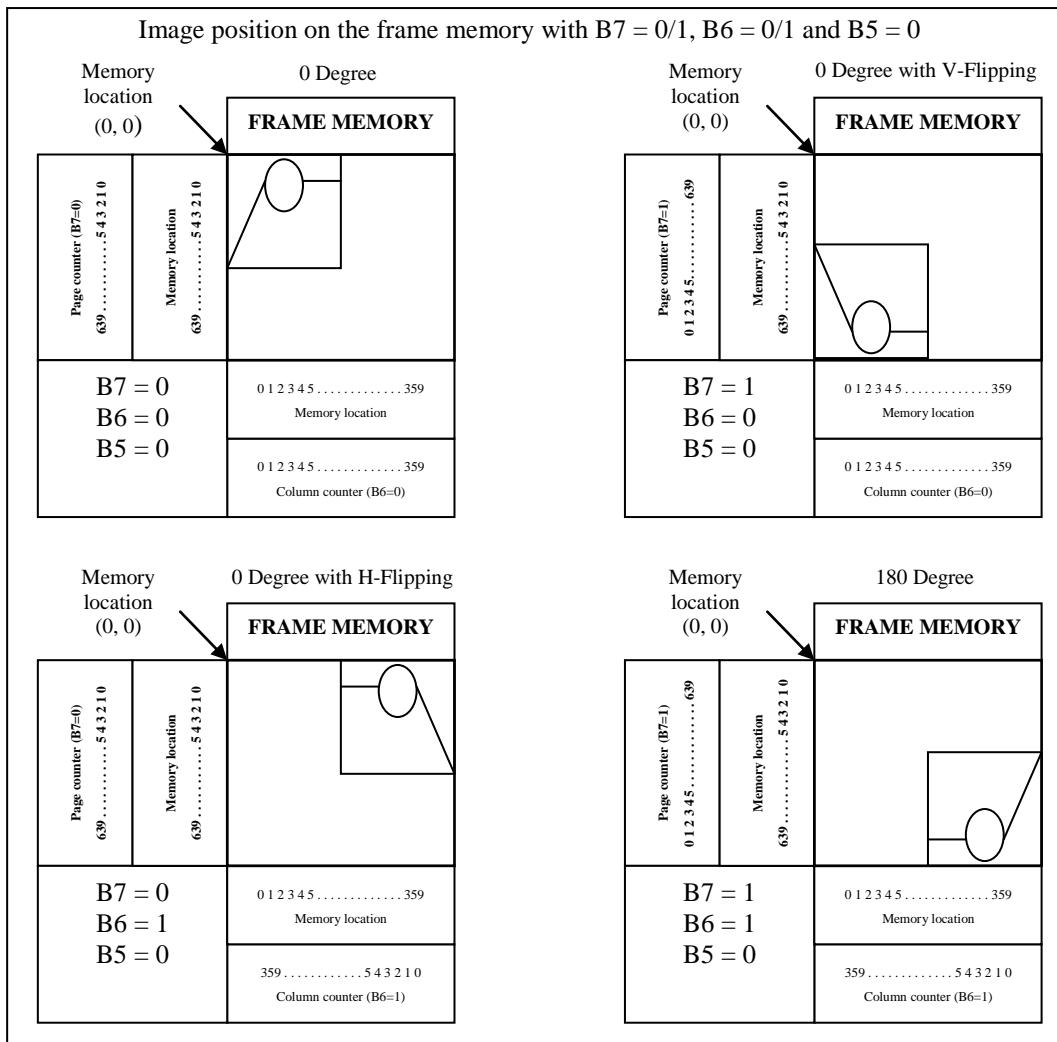
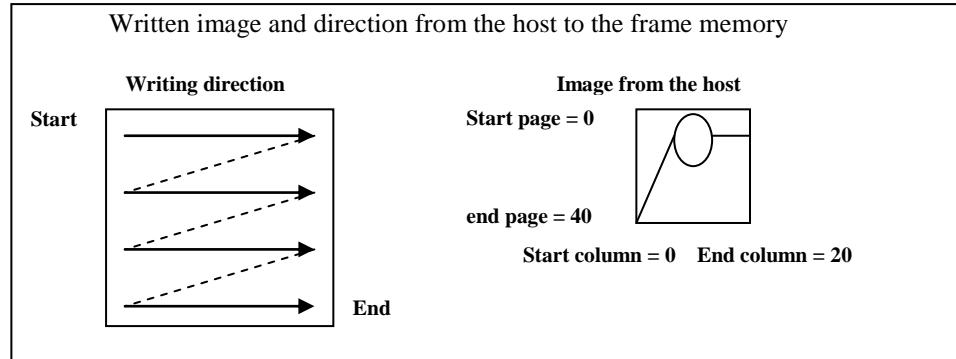


Figure 110: Image Data Rotation Example on the Memory, When B5 = 0

The sent figure is as follows and its sending order is as follows.

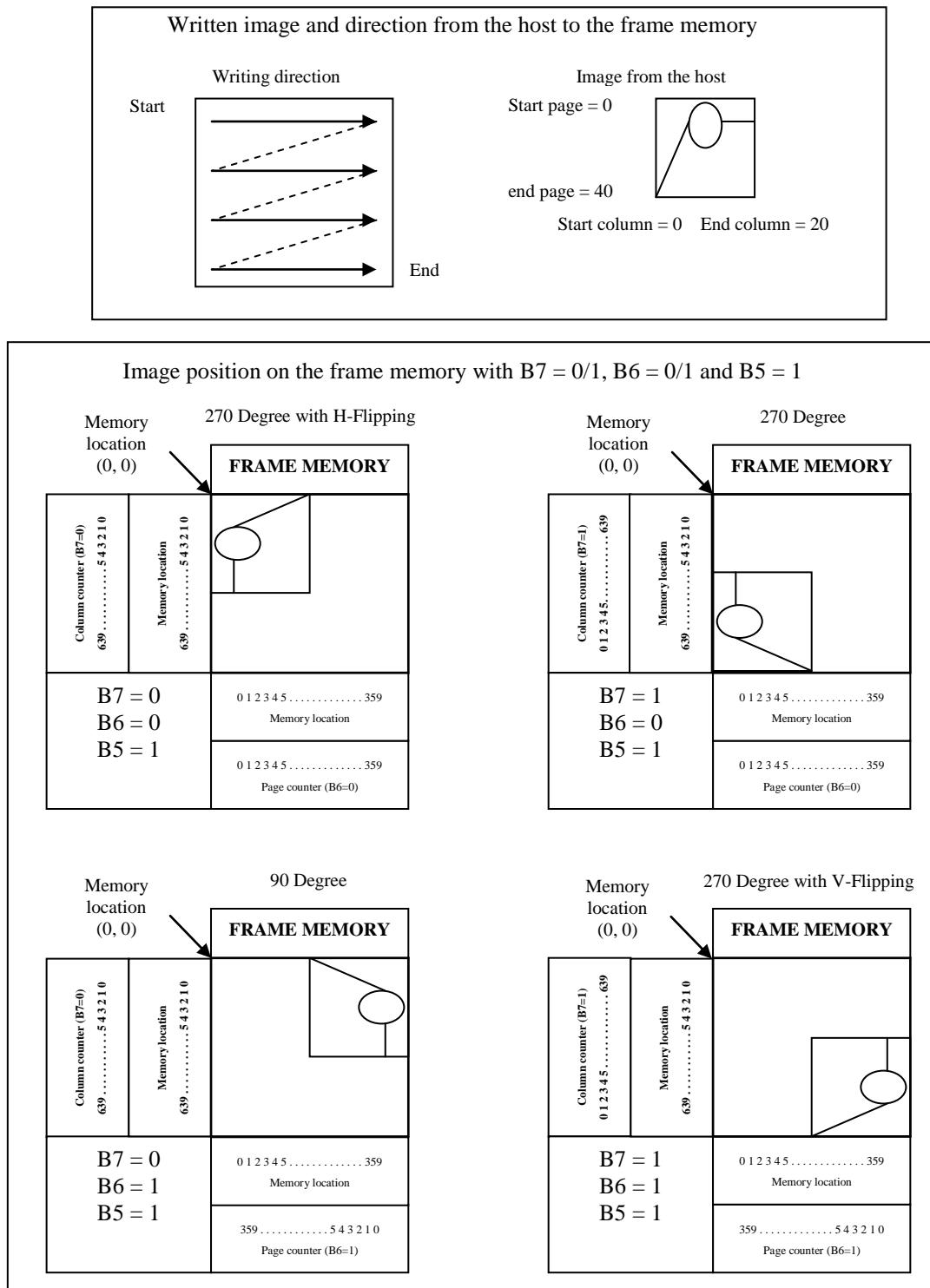


Figure 111: Image Data Rotation Example on the Memory, When B5 = 1

Example for rotation with B7, B6 and B5=1

This example is using following values: start page = 0, end page = 499, start column = 0 and end column = 399 => commands: *page address set (0, 499) and column address set (0, 399)*, when B5 = 0. B5 is set to '1' and the image is sent to the frame memory.

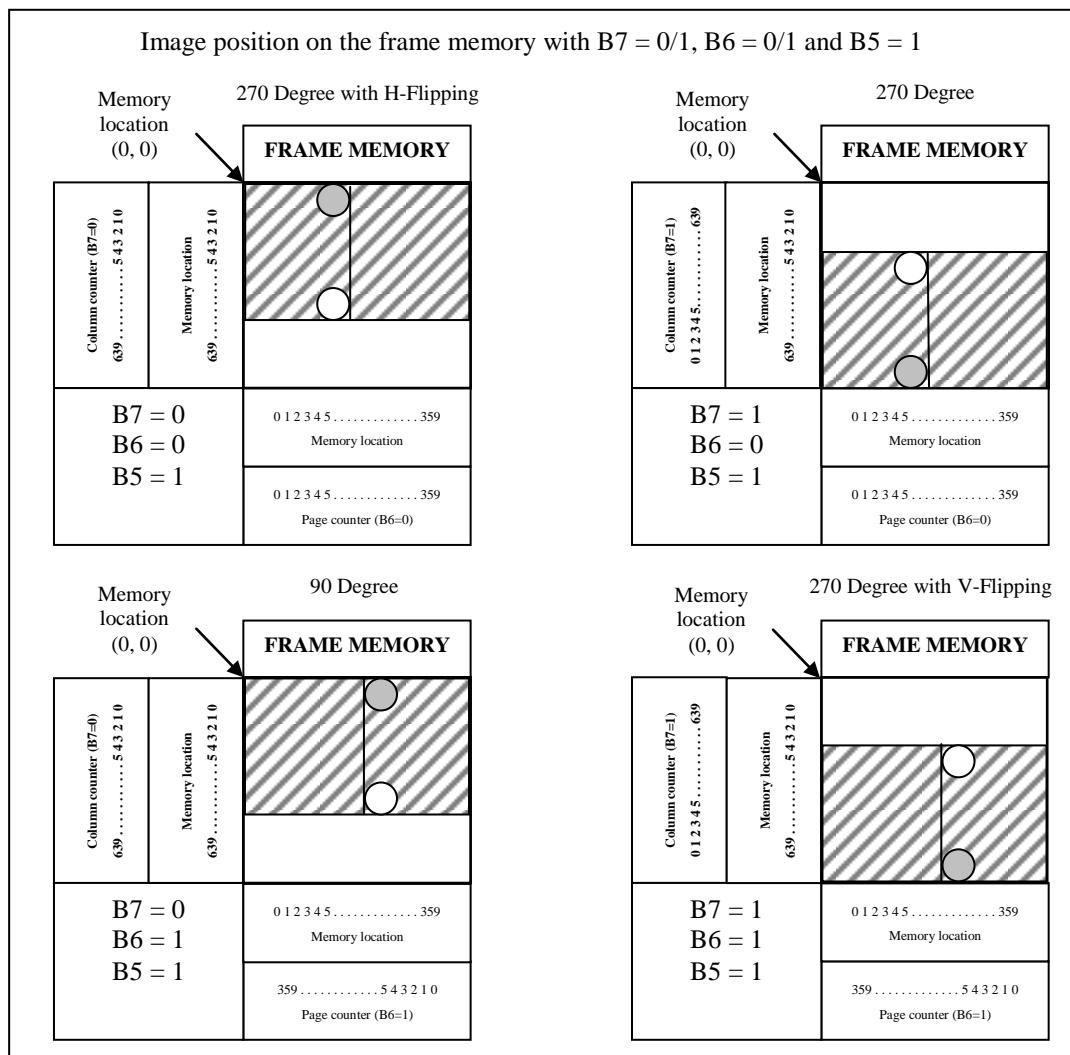
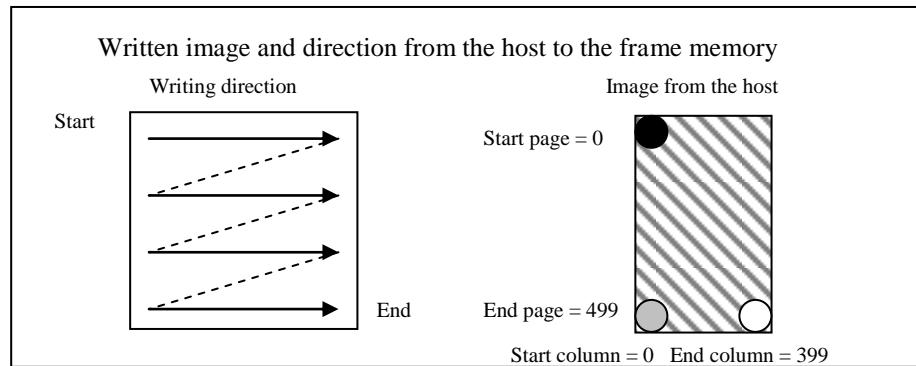


Figure 112: Image Data Rotation Example on the Memory, When B5 = 1

8.3 Tearing Effect Information

8.3.1 General

The MCU is updating the frame memory of the display module via its interface (DSI).

The display module is refreshing the display panel from the frame memory independently and it does not know what is happening on the interface of the display module (The MCU is sending image information to the display module). It is possible that this asynchronous updating is causing an abnormal visual effect on the display panel of the display module.

Therefore, the display module is sending a synchronous information (= Tearing Effect Information), which is telling the position of the refreshing on the display panel, to the MCU which can decide when it can send image information to the display module (Mainly used for a moving image e.g. video clips) that there can avoid the abnormal visual effect on the display panel of the display module.

This Tearing Effect information can be sent in two different ways:

- Separated Line, which is so-called Tearing Effect (TE) line
- Bus, which is so-called Tearing Effect (TEE) Bus Trigger, when the display module is sending a trigger to the MCU

The TE line can be used in DSI case if the tearing Effect (TEE) Bus Trigger is not possible to use.

The Tearing Effect (TEE) Bus Trigger is only used in DSI case.

8.3.2 Tearing Effect Line

The Tearing Effect line supplies to the MCU a Panel synchronisation signal and this signal can be enabled or disabled by the Tearing Effect Line Off & On commands.

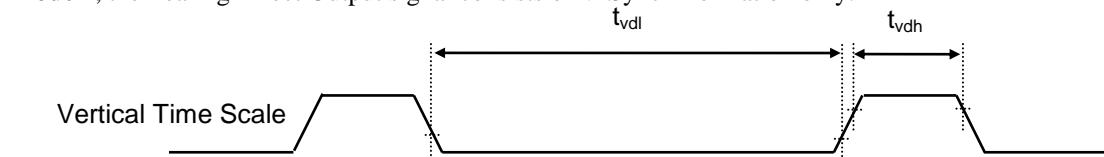
The mode of the Tearing Effect Signal is defined by the Parameter of the Tearing Effect Line On command.

The Tearing Effect Line can use in DSI case. See chapters: “5.3.1 DSI with TE Line”.

See also a specific functionality on chapter “8.10 Sleep Out –Command and Self-Diagnostic Functions of the Display Module”.

8.3.2.1 Tearing Effect Line Modes

Mode 1, the Tearing Effect Output signal consists of V-Sync information only:

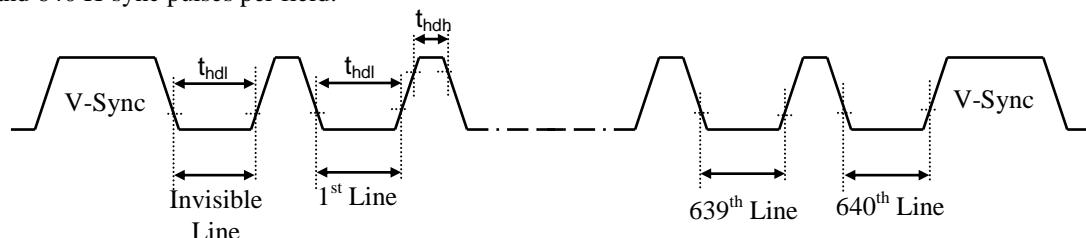


t_{vdl} = The display panel is not updated from the Frame Memory.

t_{vdl} = The display panel is updated from the Frame Memory (except Invisible Line – see below).

Figure 113: TE Line Mode 1

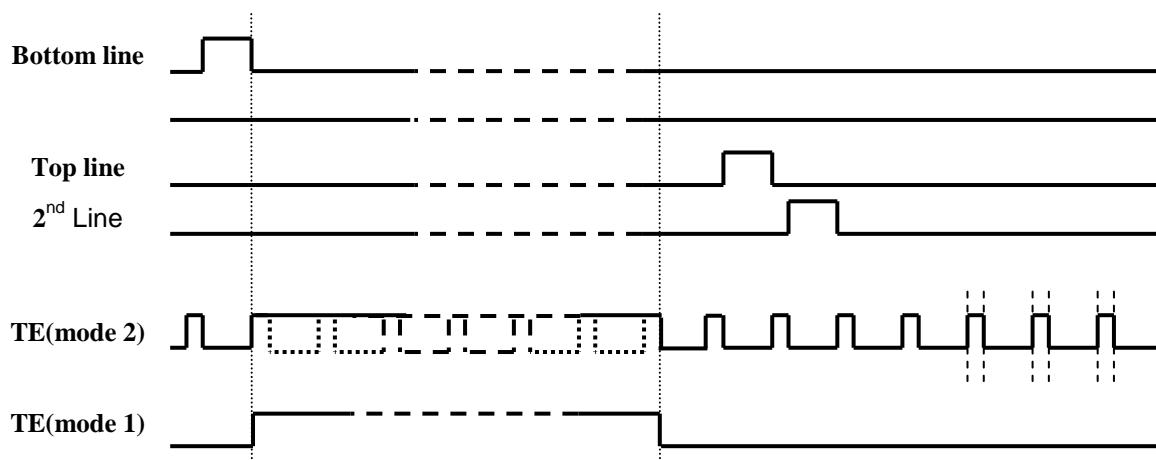
Mode 2, the Tearing Effect Output signal consists of V-Sync and H-Sync information; There is one V-sync and 640 H-sync pulses per field:



t_{hdf} = The display panel is not updated from the Frame Memory.

t_{hdl} = The display panel is updated from the Frame Memory (except Invisible Line – see above).

Figure 114: TE Line Mode 2



Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

Figure 115: TE Line Mode 1 and 2

8.3.2.2 Tearing Effect Line Timings

The Tearing Effect signal is described below:-

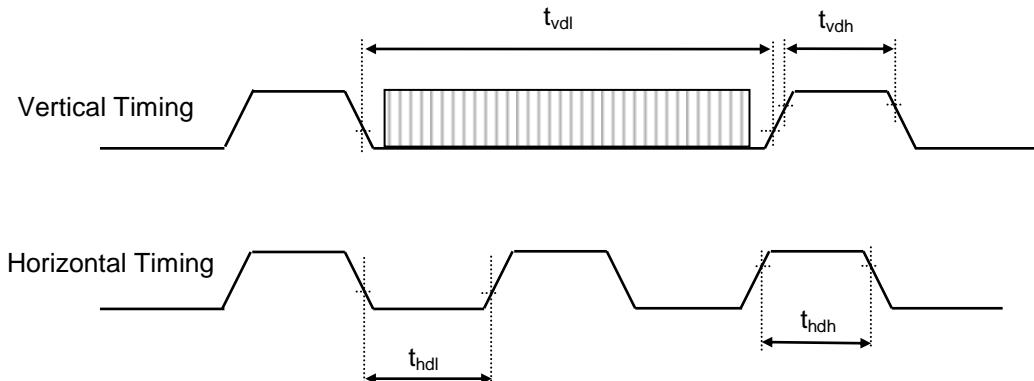


Figure 116: TE Line Timings

Table 52: TE Line AC Characteristics

Idle Mode Off/On

Symbol	Parameter	min	max	unit	description
t_{vdl}	Vertical Timing Low Duration	TBD	TBD	ms	
t_{vdh}	Vertical Timing High Duration	1000	TBD	μ s	
t_{hdl}	Horizontal Timing Low Duration	TBD	-	μ s	
t_{hdh}	Horizontal Timing High Duration	TBD	500	μ s	

Notes:

1. The timings in Table 52: TE Line AC Characteristics apply when MADCTL B4=0 and B4=1
2. Minimum frequency of the TE-line cannot be less than 25Hz, when the TE-line is active, on Mode 1.
3. The signal's rise and fall times (tf , tr) are stipulated to be equal to or less than 15ns when the maximum load is TBD Ω .

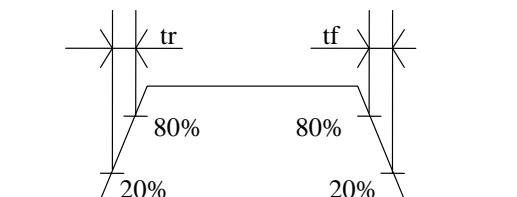


Figure 117: TE Signal Rise and Fall Timings

The Tearing Effect Output Line is fed back to the MCU and should be used as shown below to avoid Tearing Effect.

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8.3.2.3 Example 1 MCU Write is Faster than Panel Read.

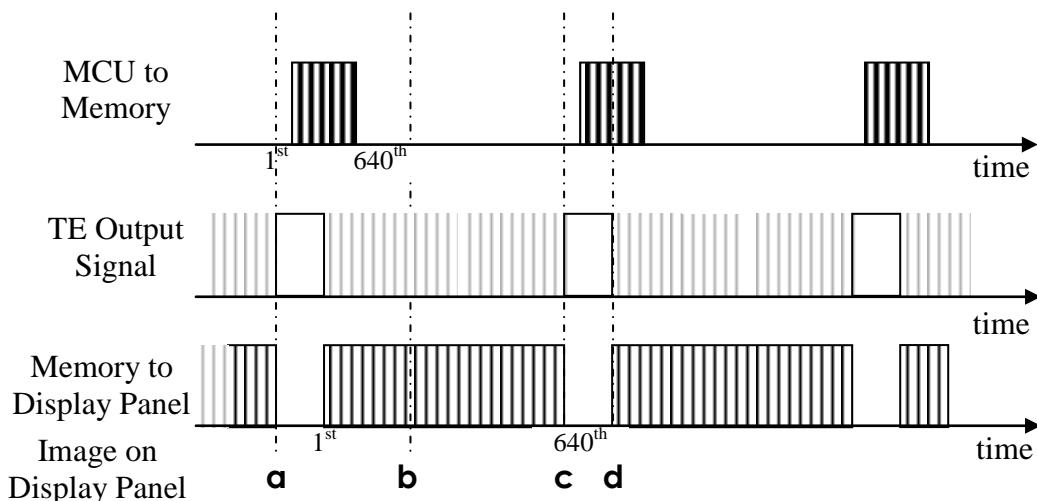


Figure 118: Example 1 - MCU Write is Faster than Panel Read

Data write to Frame Memory is now synchronised to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image: -

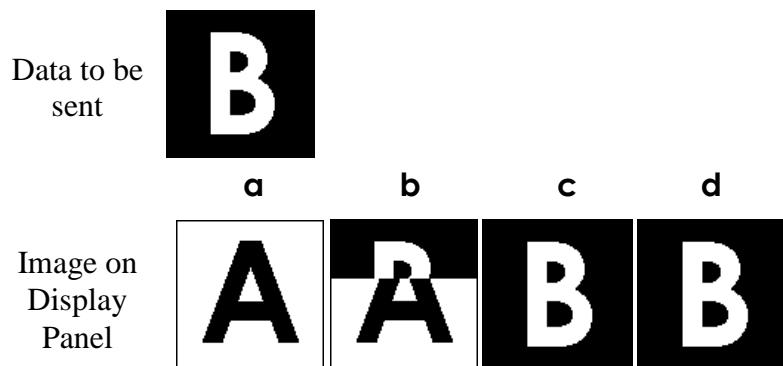


Figure 119: Example 1 – Image on the Display Panel

May 18th, 2012

8.3.2.4 Example 2 MCU Write is Slower than Panel Read.

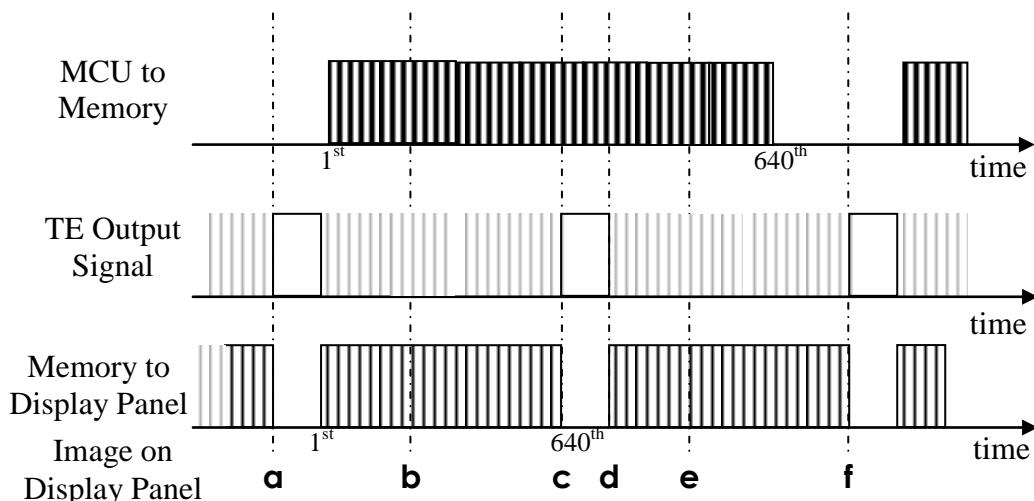


Figure 120: Example 2 – MCU Write is Slower than Panel Read

The MCU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MCU to Frame memory write position.

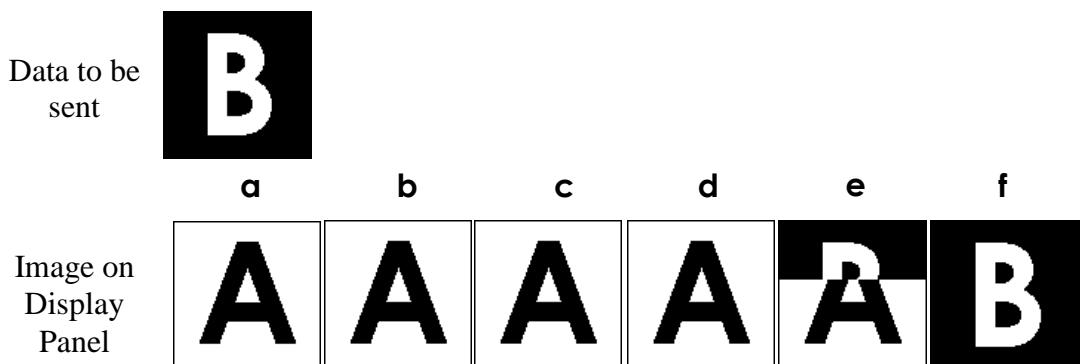


Figure 121: Example 2 – Image on the Display Panel

8.3.3 Tearing Effect Bus Trigger

A Tearing Effect Bus Trigger information supplies to the MCU a Panel synchronisation trigger and this Tearing Effect Bus Trigger information can be enabled or disabled by “9.2.24 Tearing Effect Line Off (34h)” and “9.2.25 Tearing Effect Line On (35h)” commands when the only mode of the Tearing Effect Signal is V-Sync. information.

The display module is sending this trigger information in Escape Mode after the Bus Turnaround (BTA). See chapter: “8.1.2.3.2.4 Tearing Effect (TEE)”.

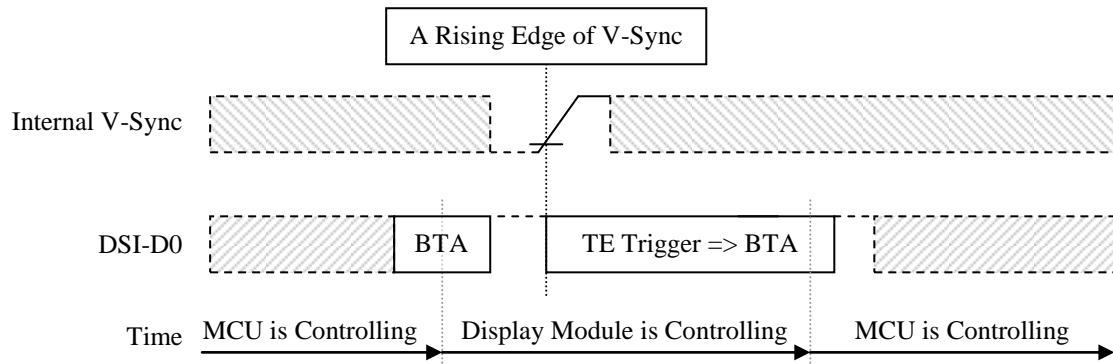


Figure 122: A Rising Edge of the V-Sync and DSI-D0

The Tearing Effect Bus Trigger can only use in DSI case without the TE line. See chapter “5.3.2 DSI without TE Line”.

8.3.3.1 Tearing Effect Bus Trigger Enable

The MCU can enable the Tearing Effect Bus Trigger on the display module in 2 different ways when a Short Packet (SPa) or Long Packet (LPa) is used. These cases are illustrated below.

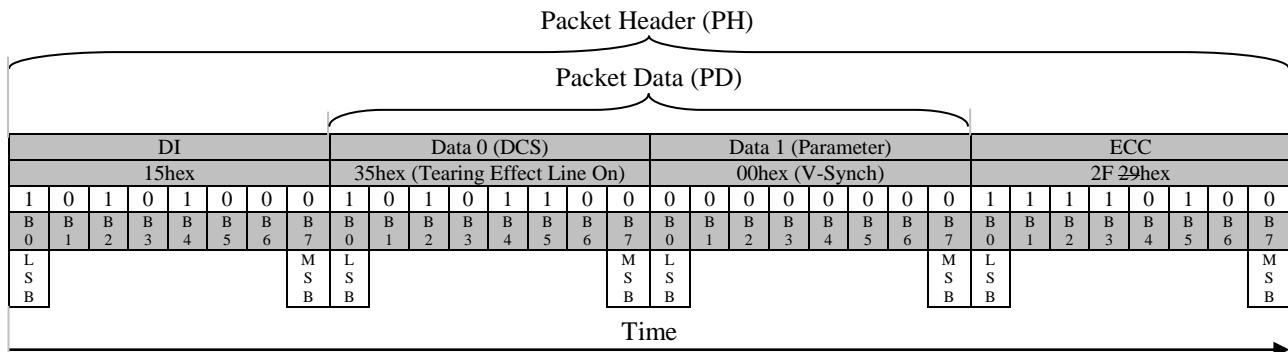


Figure 123: Tearing Effect Bus Trigger Enable (DCSW1-S) – Short Packet (SPa)

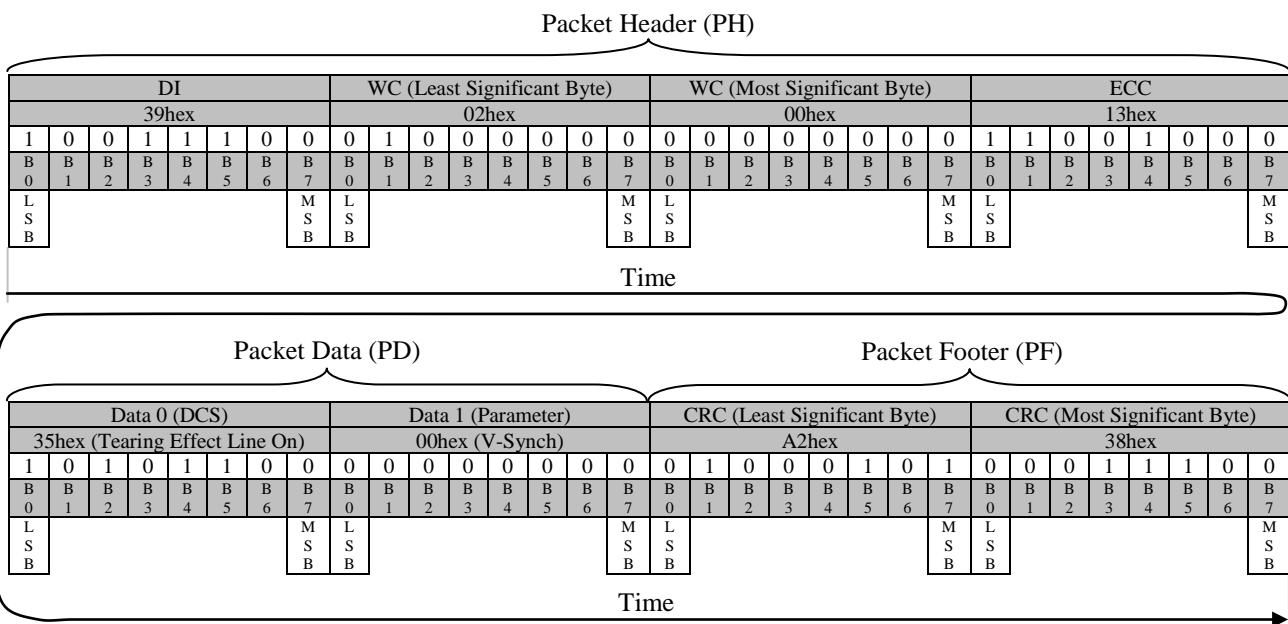


Figure 124: Tearing Effect Bus Trigger Enable (DCSW-L) – Long Packet (LPa)

8.3.3.2 Tearing Effect Bus Trigger Disable

The MCU can enable the Tearing Effect Bus Trigger on the display module in 2 different ways when a Short Packet (SPa) or Long Packet (LPa) is used. These both possibilities are illustrated below.

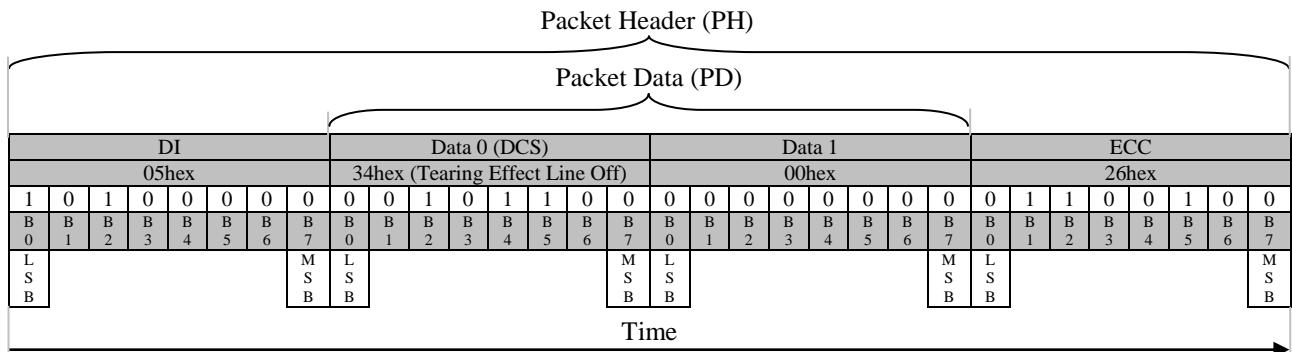


Figure 125: Tearing Effect Bus Trigger Disable (DCSWN-S) – Short Packet (SPa)

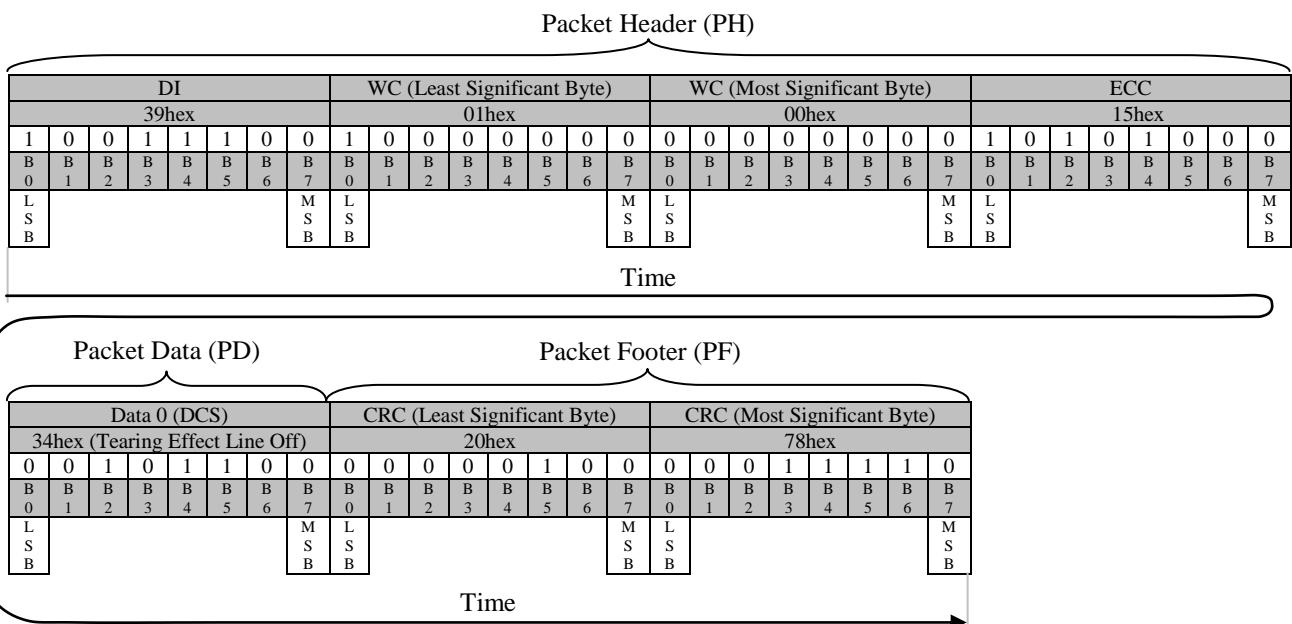


Figure 126: Tearing Effect Bus Trigger Disable (DCSW-L) – Long Packet (LPa)

8.3.3.3 Tearing Effect Bus Trigger Sequences

8.3.3.3.1 Tearing Effect Bus Trigger Enable Sequences

Table 53: Tearing Effect Bus Trigger Enable Sequence – DCSW-L and HSDT

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	Tearing Effect Bus Trigger Enable
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	3	LP-11	=>	-	-	
5	4	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
6	5	-	-	<=	LP-11	If No Error => Goto Line 8 7 If Error is Corrected by ECC => Goto Line 19 48 If Error => Goto Line 30 29
7	6					
8	7	-	-	<=	ACK	No Error
9	8	-	-	<=	LP-11	-
10	9	-	BTA	<=>	BTA	Interface Control Change from the display module to the MCU
11	10	-	LP-11	=>	-	-
12	11	-	BTA	<=>	BTA	Interface Control Change from the MCU to the display module
13	12	-	-	<=	LP-11	-
14	13	-	-	<=	TEE	TE (Escape Trigger) on the next V-Synch.
15	14	-	-	<=	LP-11	-
16	15	-	BTA	<=>	BTA	Interface Control Change from the display module to the MCU
17	16	-	LP-11	=>	-	End
18	17					
19	18	-	-	<=	LPDT	Error Report (Error is Corrected by ECC)
20	19	-	-	<=	LP-11	-
21	20	-	BTA	<=>	BTA	Interface Control Change from the display module to the MCU
22	21	-	LP-11	=>	-	-
23	22	-	BTA	<=>	BTA	Interface Control Change from the MCU to the display module
24	23	-	-	<=	LP-11	-
25	24	-	-	<=	TEE	TE (Escape Trigger) on the next V-Synch.
26	25	-	-	<=	LP-11	-
27	26	-	BTA	<=>	BTA	Interface Control Change from the display module to the MCU
28	27	-	LP-11	=>	-	End
29	28					
30	29	-	-	<=	LPDT	Error Report
31	30	-	-	<=	LP-11	-
32	31	-	BTA	<=>	BTA	Interface Control Change from the display module to the MCU
33	32	-	LP-11	=>	-	If the MCU is not forcing BTA => Goto Line 34 33 If the MCU is forcing BTA => Goto Line 36 35
34	33	-	LP-11	=>	-	End
35	34					
36	35	-	BTA	<=>	BTA	Interface Control Change from the MCU to the display module
37	36	-	-	<=	LP-11	-
38	37	-	LP-11	=>	-	The MCU is forced to start to control the interface. The display module detects Bus Connection Error (BCE)
39	38	-	BTA	<=>	BTA	Interface Control Change from the MCU to the display module
40	39	-	-	<=	LP-11	-
41	40	-	-	<=	LPDT	Error Report (Bus Connection Error (BCE) is reported) See Note 2
42	41	-	-	<=	LP-11	-
43	42	-	BTA	<=>	BTA	Interface Control Change from the display module to the MCU
44	43	-	LP-11	=>	-	End

Notes:

1. Lines 1 – 17 are needed for every frame.
2. Bits 5 and 7 of the AwER are applied.

Table 54: Tearing Effect Bus Trigger Enable Sequence – DCSW-L and LPDT

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	LPDT	=>	-	-	Tearing Effect Bus Trigger Enable
3	-	LP-11	=>	-	-	
4	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
5	-	-	<=	LP-11	-	If No Error => Goto Line 7 If Error is Corrected by ECC => Goto Line 18 If Error => Goto Line 29
6						
7	-	-	<=	ACK	-	No Error
8	-	-	<=	LP-11	-	
9	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
10	-	LP-11	=>	-	-	
11	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
12	-	-	<=	LP-11	-	
13	-	-	<=	TEE	-	TE (Escape Trigger) on the next V-Synch.
14	-	-	<=	LP-11	-	
15	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
16	-	LP-11	=>	-	-	End
17						
18	-	-	<=	LPDT	AwER	Error Report (Error is Corrected by ECC)
19	-	-	<=	LP-11	-	
20	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
21	-	LP-11	=>	-	-	
22	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
23	-	-	<=	LP-11	-	
24	-	-	<=	TEE	-	TE (Escape Trigger) on the next V-Synch.
25	-	-	<=	LP-11	-	
26	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
27	-	LP-11	=>	-	-	End
28						
29	-	-	<=	LPDT	AwER	Error Report
30	-	-	<=	LP-11	-	
31	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
32	-	LP-11	=>	-	-	If the MCU is not forcing BTA => Goto Line 33 If the MCU is forcing BTA => Goto Line 35
33	-	LP-11	=>	-	-	End
34						
35	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
36	-	-	<=	LP-11	-	Dead-Lock (No TE information) Note 2
37	-	LP-11	=>	-	-	The MCU is forced to start to control the interface. The display module detects Bus Connection Error (BCE)
38	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
39	-	-	<=	LP-11	-	
40	-	-	<=	LPDT	AwER	Error Report (Bus Connection Error (BCE) is reported) Note 2
41	-	-	<=	LP-11	-	
42	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
43	-	LP-11	=>	-	-	End

Notes:

1. Lines 1 – 16 are needed for every frame.
2. Bits 5 and 7 of the AwER are applied.

Table 55: Tearing Effect Bus Trigger Enable Sequence – DCSW1-S and HSDT

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	Tearing Effect Bus Trigger Enable
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4 5	-	LP-11	=>	-	-	
5 4	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module If No Error => Goto Line 8 7 If Error is Corrected by ECC => Goto Line 19 48 If Error => Goto Line 30 29
6 5	-	-	=<	LP-11	-	
7 6						
8 7	-	-	=<	ACK	-	No Error
9 8	-	-	=<	LP-11	-	
10 9	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
11 10	-	LP-11	=>	-	-	
12 11	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
13 12	-	-	=<	LP-11	-	
14 13	-	-	=<	TEE	-	TE (Escape Trigger) on the next V-Synch.
15 14	-	-	=<	LP-11	-	
16 15	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
17 16	-	LP-11	=>	-	-	End
18 17						
19 18	-	-	=<	LPDT	AwER	Error Report (Error is Corrected by ECC)
20 19	-	-	=<	LP-11	-	
21 20	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
22 21	-	LP-11	=>	-	-	
23 22	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
24 23	-	-	=<	LP-11	-	
25 24	-	-	=<	TEE	-	TE (Escape Trigger) on the next V-Synch.
26 25	-	-	=<	LP-11	-	
27 26	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
28 27	-	LP-11	=>	-	-	End
29 28						
30 29	-	-	=<	LPDT	AwER	Error Report
31 30	-	-	=<	LP-11	-	
32 31	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
33 32	-	LP-11	=>	-	-	If the MCU is not forcing BTA => Goto Line 34 33 If the MCU is forcing BTA => Goto Line 36 35
34 33	-	LP-11	=>	-	-	End
35 34						
36 35	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
37 36	-	-	=<	LP-11	-	Dead-Lock (No TE information) Note 2
38 37	-	LP-11	=>	-	-	The MCU is forced to start to control the interface. The display module detects Bus Connection Error (BCE)
39 38	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
40 39	-	-	=<	LP-11	-	
41 40	-	-	=<	LPDT	AwER	Error Report (Bus Connection Error (BCE) is reported) Note 2
42 41	-	-	=<	LP-11	-	
43 42	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
44 43	-	LP-11	=>	-	-	End

Notes:

1. Lines 1 – 17 are needed for every frame.
2. Bits 5 and 7 of the AwER are applied.

Table 56: Tearing Effect Bus Trigger Enable Sequence – DCSW1-S and LPDT

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	LPDT	=>	-	-	Tearing Effect Bus Trigger Enable
3	-	LP-11	=>	-	-	
4	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
5	-	-	<=	LP-11	-	If No Error => Goto Line 7 If Error is Corrected by ECC => Goto Line 18 If Error => Goto Line 29
6						
7	-	-	<=	ACK	-	No Error
8	-	-	<=	LP-11	-	
9	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
10	-	LP-11	=>	-	-	
11	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
12	-	-	<=	LP-11	-	
13	-	-	<=	TEE	-	TE (Escape Trigger) on the next V-Synch.
14	-	-	<=	LP-11	-	
15	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
16	-	LP-11	=>	-	-	End
17						
18	-	-	<=	LPDT	AwER	Error Report (Error is Corrected by ECC)
19	-	-	<=	LP-11	-	
20	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
21	-	LP-11	=>	-	-	
22	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
23	-	-	<=	LP-11	-	
24	-	-	<=	TEE	-	TE (Escape Trigger) on the next V-Synch.
25	-	-	<=	LP-11	-	
26	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
27	-	LP-11	=>	-	-	End
28						
29	-	-	<=	LPDT	AwER	Error Report
30	-	-	<=	LP-11	-	
31	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
32	-	LP-11	=>	-	-	If the MCU is not forcing BTA => Goto Line 33 If the MCU is forcing BTA => Goto Line 35
33	-	LP-11	=>	-	-	End
34						
35	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
36	-	-	<=	LP-11	-	Dead-Lock (No TE information) Note 2
37	-	LP-11	=>	-	-	The MCU is forced to start to control the interface. The display module detects Bus Connection Error (BCE)
38	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
39	-	-	<=	LP-11	-	
40	-	-	<=	LPDT	AwER	Error Report (Bus Connection Error (BCE) is reported) Note 2
41	-	-	<=	LP-11	-	
42	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
43	-	LP-11	=>	-	-	End

Notes:

1. Lines 1 – 16 are needed for every frame.
2. Bits 5 and 7 of the AwER are applied.

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8.3.3.3.2 Tearing Effect Bus Trigger Disable Sequences

Table 57: Tearing Effect Bus Trigger Disable Sequence – DCSWN-S and LPDT

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	LPDT	=>	-	-	Tearing Effect Bus Trigger Disable
3	-	LP-11	=>	-	-	End

Table 58: Tearing Effect Bus Trigger Disable Sequence – DCSWN-S and HSDT

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	HSDT	=>	-	-	Tearing Effect Bus Trigger Disable
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4 3	-	LP-11	=>	-	-	End

8.4 Checksums

The display module consists of two 8-bit checksum registers, which are used checksum calculations for Nokia area registers (includes the frame memory), on the display module. Nokia area registers are registers which values Nokia can change a command directly.

One of the checksum registers is “First Checksum” (FCS) and another is “Continue Checksum” (CCS).

These register values are set to 00h as an initial value when there is started to calculate a new checksum.

The display module is starting to calculate the new checksum after there is a write access on Nokia area registers. This means that read commands are not used as a calculation starting trigger in this case.

The checksum calculation is always interrupted, when there is a new write access on Nokia area registers. The checksum calculation is also started from the beginning.

The result of the first finished checksum calculation is stored on the FCS register, which value is kept until there is the new write access on Nokia area registers and the new checksum value is calculated in the first time again.

The maximum time, when the FCS is readable, is 150ms after there is the last write access on Nokia area registers.

The checksum calculation is continuing after the finished first checksum calculation where the FCS has gotten the checksum value. These new checksum values are always stored on CCS register (Old value is replaced a new one) after the last Nokia area register has been calculated to the checksum.

The maximum time, when the CCS is readable in the first time, is 300ms after there is the last write access on Nokia area registers.

There is always updated a checksum comparison bit (See section: “9.2.9 Read Display Self-Diagnostic Result (0Fh)” and bit D0) when there is compared FCS and CCS checksums after a new checksum value is stored on CCS.

The maximum time, when the comparison has been done between FCS and CCS in the first time, is 300ms then the comparison has been done in every 150ms (this is maximum time).

Nokia can read FCS, CCS and Comparison bit D0 values. See section: “9.2.55 Read First Checksum (AAh)”, “9.2.56 Read Continue Checksum (AFh)” and ”9.2.9 Read Display Self-Diagnostic Result (0Fh)”.

There can be an overflow during a checksum calculation. These overflow bits are not needed to store anywhere. This means that these overflow bits can be ignored by the display module.

An example of the checksum calculation:

- Register Values: A1h, 12h, 81h, DEh, F2h
- Calculated Value: 304h (= A1h + 12h + 81h + DEh + F2h)
- Ignored Bits: 3h
- Stored Checksum: 04h

This checksum calculation function is only running in “Sleep Out” mode and it is stopped in “Sleep In” mode.

Table 59: Checksum Sequence

Step Note 1	Time Note 2	Action	Temporary Register	First Checksum Register (FCS)	Continue Checksum Register (CCS)	Comment
1	0	Initialization	Set to 00h	Set to 00h	Set to 00h	The last write action on Nokia area registers => FCS and CCS registers are initialized.
2	0 – 150ms	Counting Sum of Nokia Area Registers	Counting	-	-	The first register counting is running
3	150ms	Stores Sum of Registers on FCS Register	Set to 00h after Value is Moved to FCS Register	Stores Sum of Nokia Area Registers on FCS Register	-	The result of the first register counting is stored on the FCS register. The result of the FCS is available to the MCU.
4	150 – 300ms	Counting Sum of Nokia Area Registers	Counting	-	-	The second register counting is running
5	300ms	1) Stores Sum of Registers on CCS Register 2) Compares Stored FCS and CCS Values	Set to 00h after Value is Moved to CCS Register	-	Stores Sum of Nokia Area Registers on CCS Register	The result of the comparison is stored on separated registers, which can read separated read commands. The result of the CCS and comparison result are available to the MCU.
6	300 – 450ms	Counting Sum of Nokia Area Registers	Counting	-	-	The third register counting is running
7	450ms	1) Stores Sum of Registers on CCS Register 2) Compares Stored FCS and CCS Values	Set to 00h after Value is Moved to CCS Register	-	Stores Sum of Nokia Area Registers on CCS Register	The result of the comparison is stored on separated registers, which can read separated read commands. The latest result of the CCS and comparison result are available to the MCU.
8	450 – 600ms	Counting Sum of Nokia Area Registers	Counting	-	-	The fourth register counting is running
9	600ms	1) Stores Sum of Registers on CCS Register 2) Compares Stored FCS and CCS Values	Set to 00h after Value is Moved to CCS Register	-	Stores Sum of Nokia Area Registers on CCS Register	The result of the comparison is stored on separated registers, which can read separated read commands. The latest result of the CCS and comparison result are available to the MCU.
10	etc	-	-	-	-	Same Sequence Continue e.g. steps 4 and 5

Notes:

1. This function is restarted at Step 1 if there is any write action on Nokia area registers.
2. These time can be shorter on the display module.

8.5 Power ON/OFF Sequence

8.5.1 General

V_{PNL} and V_{DDI} can be applied in any order.

V_{PNL} and V_{DDI} can be powered down in any order.

During power off, if the display module is in the Sleep Out mode, V_{PNL} and V_{DDI} must be powered down minimum 120msec after RESX has been released.

During power off, if the display module is in the Sleep In mode, V_{PNL} or V_{DDI} can be powered down minimum 0msec after RESX has been released.

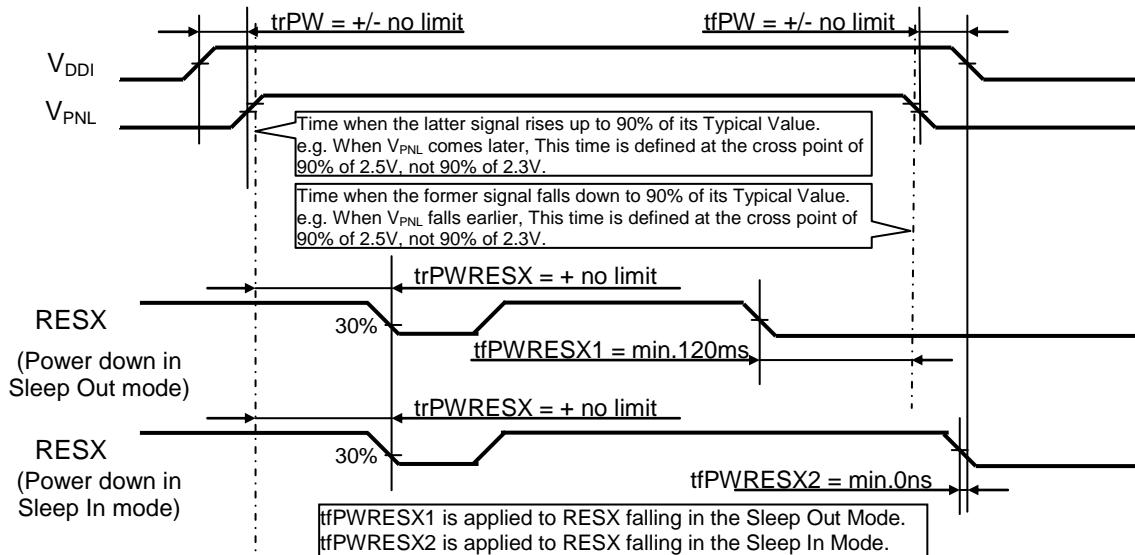
Notes:

1. There will be no damage to the display module if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display panel between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
4. If RESX line is not held stable by host during Power On Sequence as defined in Sections 8.5.2.1 and 8.5.2.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.
5. There is not a limit for Rise/Fall time on V_{PNL} or V_{DDI} .
6. The display module can also initialize and calibrate DSI-CLK+/- and DSI-D0+/- lanes within 5ms after LP-11 (Clock and Data Channels), V_{PNL} and V_{DDI} are applied and HW Reset is not active (5ms is as same as the Reset Cancelling Time).

8.5.2 Cases

8.5.2.1 Case 1 – RESX line is held High or Unstable by MCU at Power On

If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after V_{PNL} and V_{DDI} have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



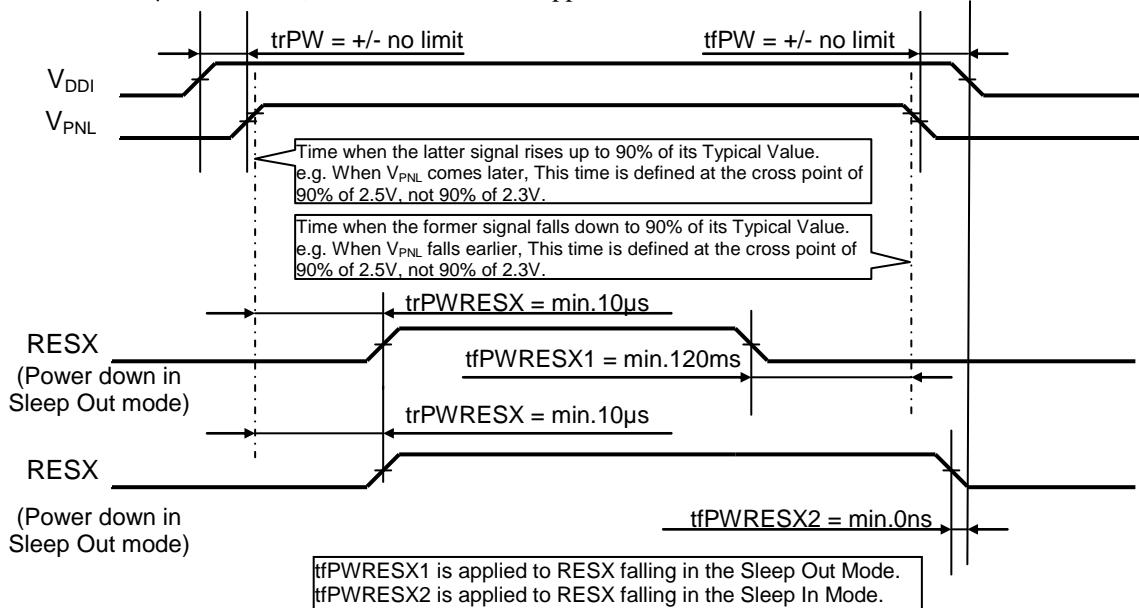
Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Figure 127: Case 1 – RESX Line is Held High or Unstable by MCU at Power On

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8.5.2.2 Case 2 – RESX line is held Low by MCU at Power On

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10μsec after V_{PNL} and V_{DDI} have been applied.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Figure 128: Case 2 – RESX Line is Held Low by MCU at Power On

8.5.3 Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. The display module must meet following requirements:

1. There cannot be any damages for the display module or the display module cannot cause any damages for the host or lines of the interface.
2. There cannot be any abnormal visible effects (= display must be blank) with in 1 second on the display and remains blank until “Power On Sequence” powers it up.

8.6 Power Modes

8.6.1 Power Modes Definition

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
In this mode, the display is able to show maximum 16,777,216 colours.
2. Partial Mode On, Idle Mode Off, Sleep Out.
In this mode part of the display is used with maximum 16,777,216 colours.
3. Normal Mode On (full display), Idle Mode On, Sleep Out.
In this mode, the full display area is used but with 8 colours.
4. Partial Mode On, Idle Mode On, Sleep Out.
In this mode, part of the display is used but with 8 colours.
5. Sleep In Mode.
In this mode, the DC:DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and registers are working with V_{DDI} power supply. Contents of the memory can or cannot be safe.
6. Power Off Mode.
In this mode, V_{PNL} and V_{DDI} are removed.

Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

8.6.2 Power Modes Flow Chart

Commands:

Normal display mode on = NORON
 Partial mode on = PTLON
 Idle mode off = IDMOFF
 Idle mode on = IDMON
 Sleep out = SLPOUT
 Sleep in = SLPIN

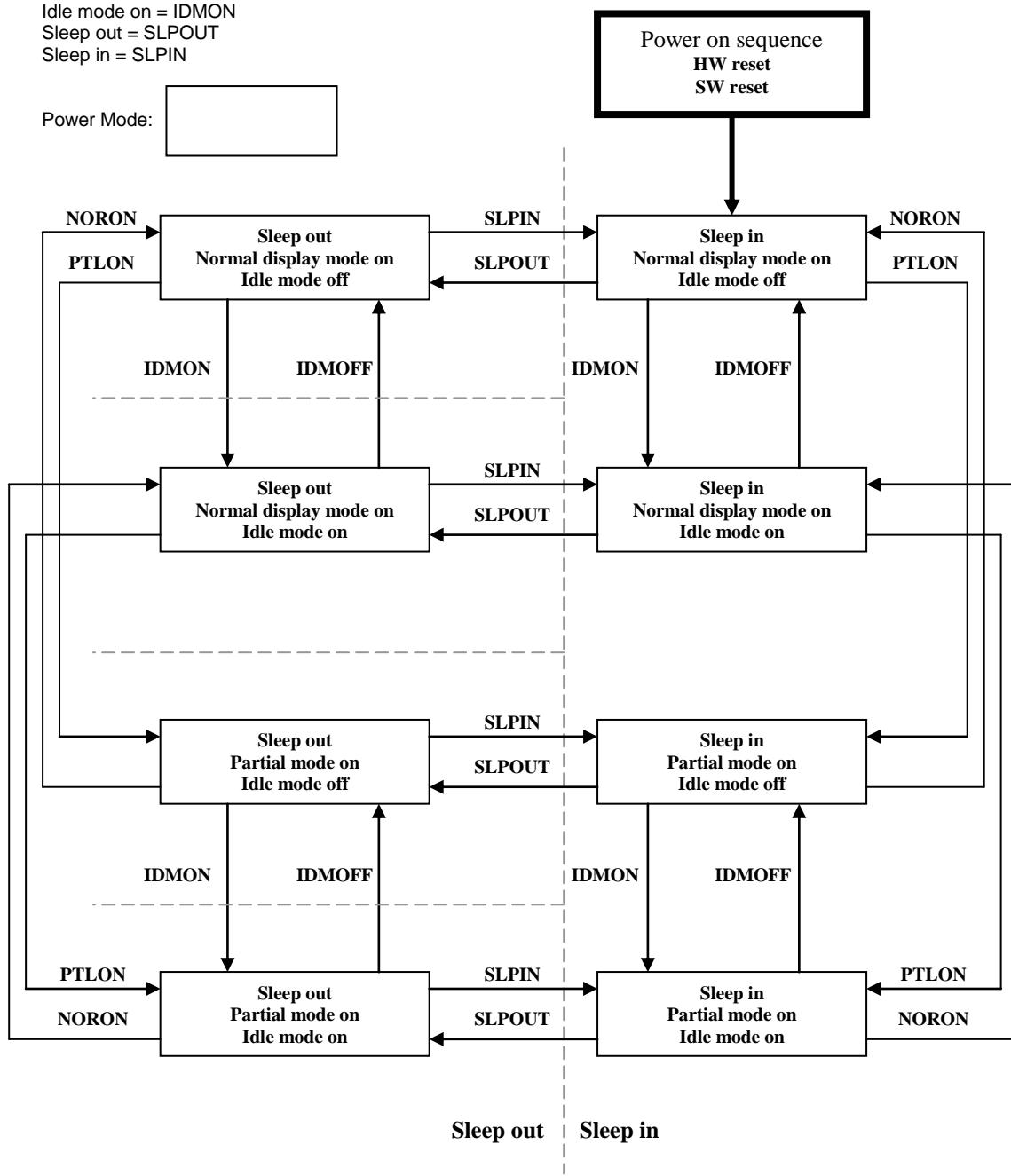


Figure 129: Power Modes Flow Chart

Notes:

1. There is not any abnormal visual effect when there is changing from one power mode to another power mode.
2. There is not any limitation, which is not specified by Nokia, when there is changing from one power mode to another power mode.

8.7 Gamma Curves

The display module contains of 1 gamma curve which is defined in the optical level on the display panel.

See also chapter “9.2.16 Gamma Set (26h)” for gamma curve selection.

8.7.1 Gamma Curve 1 (GC0), applies the function $y=x^{2.2}$

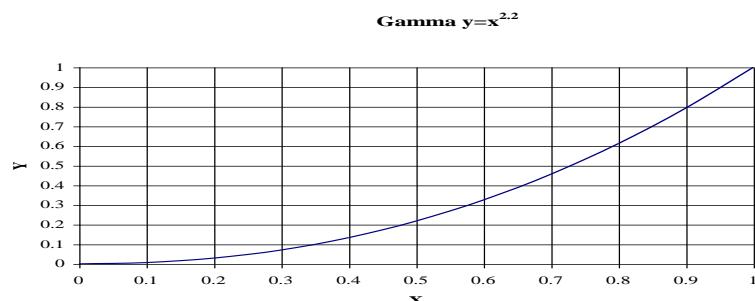


Figure 130: Gamma Curve 1 (GC0)

8.8 Reset

8.8.1 Registers

The registers that are initialised are listed below.

Table 60: Registers

Register	After Powered On	After Hardware Reset	After Software Reset
Frame memory	Random	Random	Random
Sleep	In	In	In
Display mode	Normal	Normal	Normal
Display	Off	Off	Off
Idle	Off	Off	Off
All Pixels Off	Off	Off	Off
All Pixels On	Off	Off	Off
Column Start Address	0000h	0000h	0000h
Column End Address	0167h	0167h	0167h
Page Start Address	0000h	0000h	0000h
Page End Address	027Fh	027Fh	027Fh
Gamma setting	GC0	GC0	GC0
Partial Area start	0000h	0000h	0000h
Partial Area end	027Fh	027Fh	027Fh
MADCTL	00h	00h	00h
RDNUMED	00h	00h	00h
RDDPM	08h	08h	08h
RDDMADCTL	00h	00h	00h
RDDCOLMOD	07h	07h	07h
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
Colour Pixel Format	24 Bit/Pixel	24 Bit/Pixel	24 Bit/Pixel
TE Output Line	Off	Off	Off
TE Line Mode	Mode 1 ⁽³⁾	Mode 1 ⁽³⁾	Mode 1 ⁽³⁾
RDDISBV	00h	00h	00h
RDCTRLD	00h	00h	00h
RDCL	00h	00h	00h
RDFCS	00h	00h	00h
RDCCS	00h	00h	00h
MRPS	01h	01h	01h

Notes:

1. There will be no abnormal visible effects on the display when S/W or H/W Resets are applied.
2. After Powered-On Reset finishes within 10µs after V_{PNL} and V_{DDI} are applied.
3. Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

8.8.2 Display Module Input/Output Pins

8.8.2.1 Output Pins, I/O Pins

Table 61: Output Pins

Line/Pin	After Powered On	After Hardware Reset	After Software Reset
DSI-D0+	High Z(Inactive)	High Z(Inactive)	High Z(Inactive)
DSI-D0-	High Z(Inactive)	High Z(Inactive)	High Z(Inactive)
TE Line	Low	Low	Low

Notes:

1. There will be no output from TE, DSI-D0+/- or DSI-CLK+/- during Power On/Off sequences, Hardware Reset and Software Reset.
2. If this is implemented for external use.

8.8.2.2 Input pins

Table 62: Input Pins

Line/Pin	During Power On Process	After Powered On	After Hardware Reset	After Software Reset	During Power Off Process
RESX	See 8.5	Input valid	Input valid	Input valid	See 8.5
DSI-CLK+	Input invalid	Input valid	Input valid	Input valid	Input invalid
DSI-CLK-	Input invalid	Input valid	Input valid	Input valid	Input invalid
DSI-D0+	Input invalid	Input valid	Input valid	Input valid	Input invalid
DSI-D0-	Input invalid	Input valid	Input valid	Input valid	Input invalid

Note: "Input valid" means LP-Rx without instructions of the MCU.

8.8.3 Reset Timing

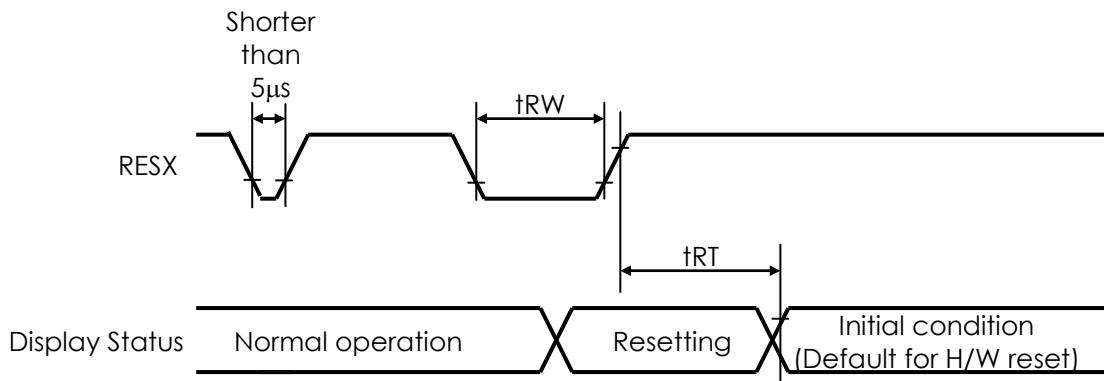


Figure 131: Reset Timings

Table 63: Reset Timings

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		μs
	tRT	Reset cancel (Note 1, 9)		5 (note 5) 120 (notes 6, 7)	ms

Notes:

1. The reset cancel includes also required time for loading ID bytes (or similar) from EEPROM (or similar) to ID (or similar) registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

Table 64: Reset Description

RESX Pulse	Action
Shorter than 5μs	Reset Rejected
Longer than 9μs	Reset
Between 5μs and 9μs	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out -mode. The display remains the blank state in Sleep In -mode.) and then return to Default condition for Hardware Reset.

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4. Spike Rejection also applies during a valid reset pulse as shown below:

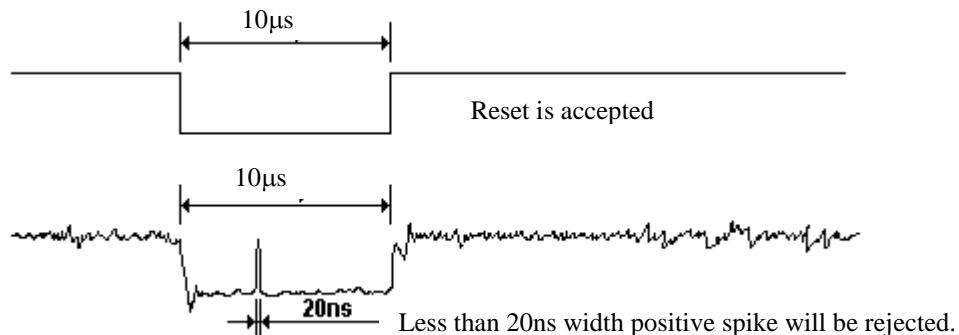


Figure 132: Positive Noise Pulse when Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.
8. HW reset cannot cause any spike/glitch on control or data lines or spike/glitch/noise on power (V_{PNL} and V_{DDI}) lines.
9. The display module can also initialize and calibrate DSI-CLK+/- and DSI-D0+/- lanes within 5ms if it is needed when DSI has been selected to use.

8.9 Display Panel Colour Characteristics

Colour characteristics of the display panel are stored on the display module that they can be read via the used interface by the engine what is using this display panel colour characteristics information to adjust a color information of the image frame, what is on the engine, to match a wanted colour outlook of the image on the display panel.

Used colour characteristics can share 2 categories: Mandatory and Optional. The mandatory colour characteristics are Black, White, Red, Green and Blue. The optional colour characteristics is used if it is needed and it is called as A colour (e.g. Cyan). The bits of the A colour are set to '0's they are not used on the display module.

A read colour characteristic value is based on 10 bit floating value where the MSB is 9th bit and the LSB is 0th bit. All power values of the bits are listed below:

- Bit 9: $2^{-1} = 0.5$,
- Bit 8: $2^{-2} = 0.25$,
- Bit 7: $2^{-3} = 0.125$,
- Bit 6: $2^{-4} = 0.0625$,
- Bit 5: $2^{-5} = 0.03125$,
- Bit 4: $2^{-6} = 0.015625$,
- Bit 3: $2^{-7} = 0.007813$,
- Bit 2: $2^{-8} = 0.003906$,
- Bit 1: $2^{-9} = 0.001953$,
- Bit 0: $2^{-10} = 0.000977$.

The wanted value is an approximation in the most of the cases when there is used binary numbers. Therefore, there is used the nearest value what can get e.g. Rx can be:

- Actual value: 0.6400, Stored value Rx[9:0] = 10 1000 1111b = 0.6396,
- Actual value: 0.3300, Stored value Rx[9:0] = 01 0101 0010b = 0.3301,
- Actual value: 0.3000, Stored value Rx[9:0] = 01 0011 0011b = 0.2998,
- Actual value: 0.6000, Stored value Rx[9:0] = 10 0110 0101b = 0.5986,
- Actual value: 0.1500, Stored value Rx[9:0] = 00 1001 1010b = 0.1504,
- Actual value: 0.0600, Stored value Rx[9:0] = 00 0011 1101b = 0.0596,
- Actual value: 0.3127, Stored value Rx[9:0] = 01 0100 0000b = 0.3125,
- Actual value: 0.3290, Stored value Rx[9:0] = 01 0101 0001b = 0.3291.

The value 0.6396 has calculated as follows:

- Binary value: 10 1000 1111b
- Formula: Rx[9]x0.5 + Rx[8]x0.25 + Rx[7]x0.125 + Rx[6]x0.0625 + Rx[5]x0.03125 + Rx[4]x0.015625 + Rx[3]x0.007813 + Rx[2]x0.003906 + Rx[1]x0.001953 + R[0]x0.000977
- Use: 1x0.5 + 0x0.25 + 1x0.125 + 0x0.0625 + 0x0.03125 + 0x0.015625 + 1x0.007813 + 1x0.003906 + 1x0.001953 + 1x0.000977

See also sections: “0

Read Black/White Low Bits (70h)”, “9.2.39 Read Bkx (71h)”, “9.2.40 Read Bky (72h)”, “9.2.41 Read Wx (73h)”, “9.2.42 Read Wy (74h)”, “9.2.43 Read Red/Green Low bits (75h)”, “9.2.44 Read Rx (76h)”, “9.2.45 Read Ry (77h)”, “9.2.46 Read Gx (78h)”, “9.2.47 Read Gy (79h)”, “9.2.48 Read Blue/AColour Low Bits (7Ah)”, “9.2.49 Read Bx (7Bh)”, “9.2.50 Read By (7Ch)”, “9.2.51 Read Ax (7Dh)”, “9.2.52 Read Ay (7Eh)”.

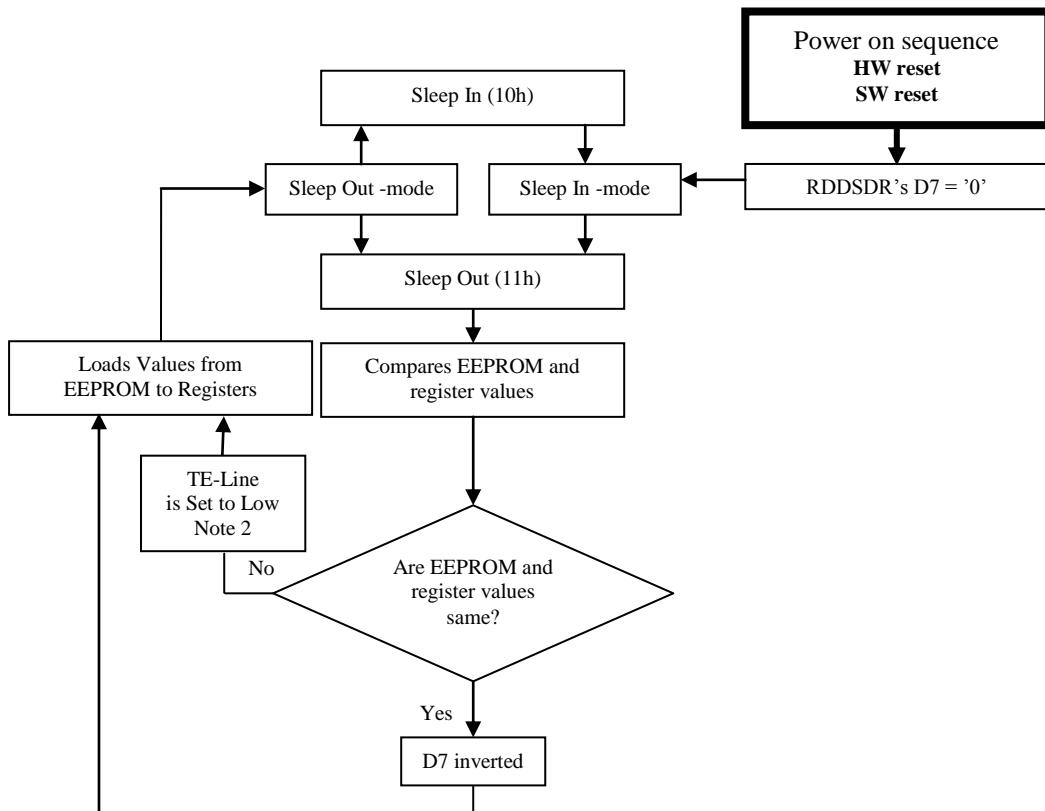
8.10 Sleep Out –Command and Self-Diagnostic Functions of the Display Module

8.10.1 Register loading Detection

Sleep Out-command (See section 9.2.11 “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EEPROM (or similar device) to registers of the display controller is working properly.

There are compared factory values of the EEPROM and register values of the display controller by the display controller (1st step: Compares register and EEPROM values, 2nd step: Loads EEPROM value to register). If those both values (EEPROM and register values) are same, there is inverted (= increased by 1) a bit, which is defined in command 9.2.9 “Read Display Self-Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= not increased by 1) and the used TE-line is set to low (Registers, what are set by “9.2.25 Tearing Effect Line On (35h)” – command, are keeping their current values) when it can only be reactivated by “9.2.25 Tearing Effect Line On (35h)” –command.

The flow chart for this internal function is following:



Notes:

1. There is not compared and loaded register values, which can be changed by Nokia (Nokia area commands: 00h to AFh and DAh to DDh), by the display module.
2. This information is only used if TE line is used.

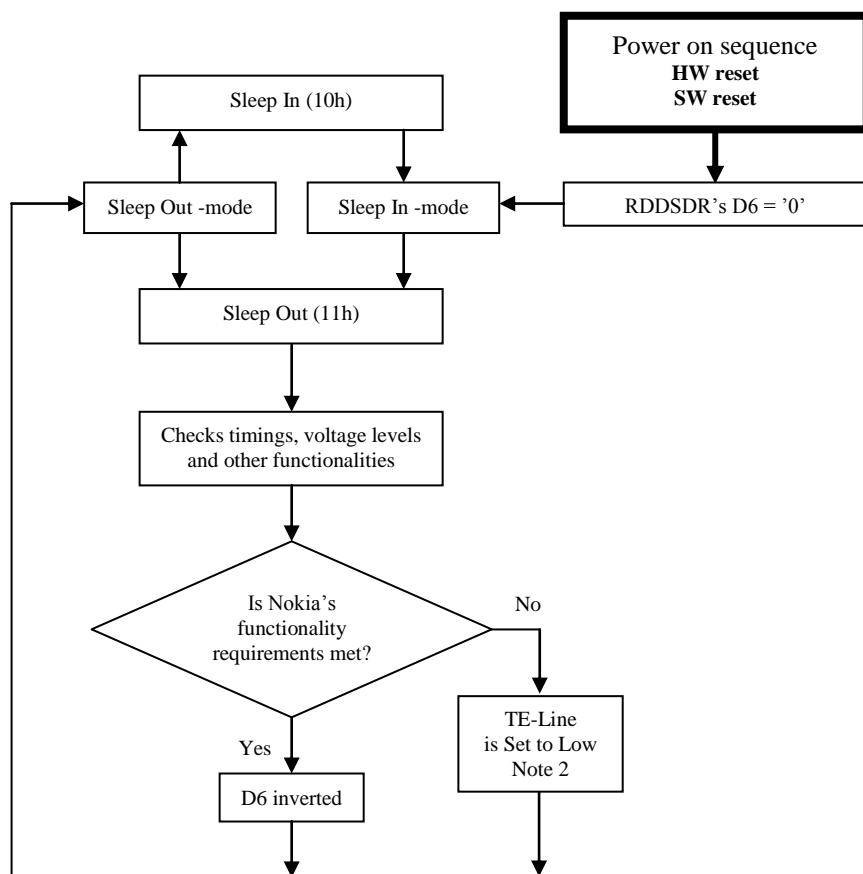
Figure 133: Register Loading Detection Flow Chart

8.10.2 Functionality Detection

Sleep Out-command (See section 9.2.11 “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets Nokia’s functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting Nokia’s functionality requirements (e.g. booster voltage levels, timings, etc.). If Nokia’s functionality requirement is met, there is inverted (= increased by 1) a bit, which defined in command 9.2.9 “Read Display Self-Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D6). If Nokia’s functionality requirement is not same, this bit (D6) is not inverted (= not increased by 1) and the used TE-line is set to low (Registers, what are set by “9.2.25 Tearing Effect Line On (35h)” –command, are keeping their current values) when it can only be reactivated by “9.2.25 Tearing Effect Line On (35h)” –command.

The flow chart for this internal function is following:



Notes:

1. There is needed 120msec after Sleep Out -command, when there is changing from Sleep In -mode to Sleep Out -mode, before there is possible to check if Nokia’s functionality requirements are met and a value of RDDSDR’s D6 is valid. Otherwise, there is 5msec delay for D6’s value, when Sleep Out –command is sent in Sleep Out -mode.
2. This function is only used if TE-line is used.

Figure 134: Functionality Detection Flow Chart

8.11 Temperature compensation

The purpose of the temperature compensation is that the optical quality of the picture (The customer of the display module defines these parameters) will not change when the temperature will change.

The range of the temperature compensation is from -30°C to +70 °C for the display module.

The temperature compensation of the display module has to be covered all parts of it (driver IC, power IC, display element, etc.).

The function of the temperature compensation cannot cause any extra actions (commands, etc.) on MCU side. This means, that this function is an internal function what the display module suppliers have implemented on the display module.

8.12 Preset Values

Display module suppliers store preset values (e.g. adjustment values for optics) on display module on their production line. Customer SWs do not have to support these preset values.

8.13 Display Brightness Control

8.13.1.1 General System Block Diagram and Description

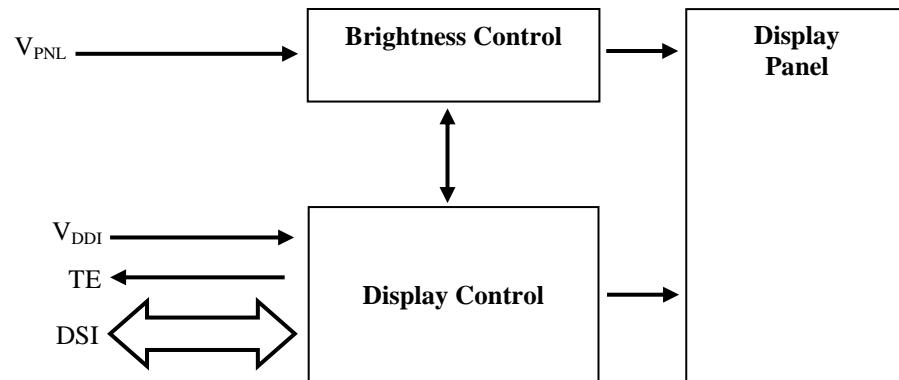


Figure 135: General System Block Diagram

8.13.1.2 Brightness Control Block

Brightness Control block is used to control brightness of the display as follows:

- Panel voltage is inputted into this block and as an output there is adjusted brightness control value. The brightness control method should be taken into account to avoid abnormal visible effect related with scanning frame frequency.

The brightness control block can be used in manual mode, see chapter “9.2.34 Write CTRL Display (53h)” for the display.

The user can adjust brightness, see chapter “0 Write Display Brightness (51h)” for the display .

Register values for display brightness should be updated during V-sync. They specify the current brightness values for display, even if display is in the transition time to new target brightness. E.g. If brightness is changing in the transition time for dimming function register value of display brightness should follow the output brightness of display. They can be read by “9.2.33 Read Display Brightness Value (52h)” .

8.13.1.3 Display Brightness Control

8.13.1.4 General

This OLED display has 8 separate brightness steps. Steps are controlled with register 51h parameter DBV (display brightness value). ***The step 9 should only be used temporarily if very high brightness is needed, like in outdoor conditions. If step 9 is used too long, module OLED material aging will be happening.***

Automatic current limit must be enabled when step 9 is used.

Step	Luminance level	Luminance ratio	Parameter
9	400 cd/m ²	Note	(EAh < DBV ≤ FFh)
8	300 cd/m ²	100%	(B7h < DBV ≤ EAh)
7	(250) cd/m ²	(83%)	(86h < DBV ≤ B7h)
6	(180) cd/m ²	(60%)	(5Eh < DBV ≤ 86h)
5	(130) cd/m ²	(43%)	(40h < DBV ≤ 5Eh)
4	(90) cd/m ²	(30%)	(26h < DBV ≤ 40h)
3	(60) cd/m ²	(20%)	(13h < DBV ≤ 26h)
2	(30) cd/m ²	(10%)	(5h < DBV ≤ 13h)
1	(0) cd/m ²	(0%)	(0h ≤ DBV ≤ 5h)

8.13.2 Display and Dimming

8.13.2.1 General

A dimming function (how fast to change the brightness from old to new level and what are brightness levels during the change) is used when changing from one brightness level to another. This dimming function curve is the same in increment and decrement directions. The basic idea is described below.

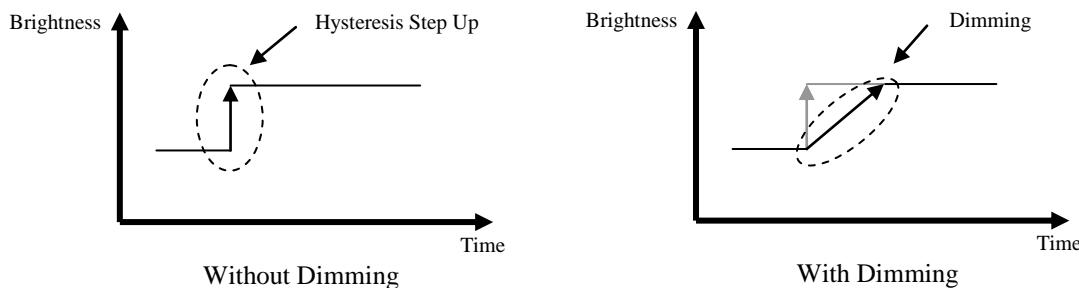


Figure 136: Dimming Curves

Dimming function can be enabled and disabled. See chapters “9.2.34 Write CTRL Display (53h)” (bit DD).

8.13.2.2 Dimming Requirement

The dimming function should be working as follows.

Dimming function in the display module should be implemented so that 400 – 600ms is used for the transition between the original brightness value and the target brightness value. The transferring time steps between these two brightness values are equal making the transition linear.

The dimming function is working similarly in both upward and downward directions.

An upward example is illustrated below

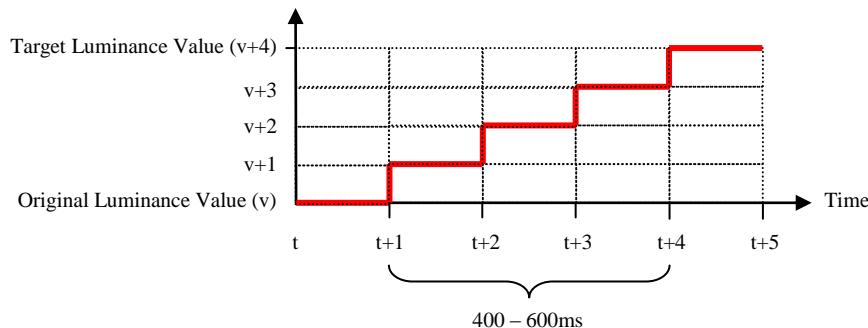


Figure 137: Example – Upward Dimming

9 Display Commands

9.1 Command List

Table 65: Command List

Operational Code	Function	Read/ Write/ Command	Number Of Parameter	Parameters
00	No Operation	C	0	-
01	Software reset	C	0	-
05	Read Number of the Errors on DSI	R	1	Number of the Error on DSI
0A	Read Display Power Mode	R	1	-
0B	Read Display MADCTL	R	1	-
0C	Read Display Pixel Format	R	1	-
0D	Read Display Image Mode	R	1	-
0E	Read Display Signal Mode	R	1	-
0F	Read Display Self Diagnostic Result	R	1	-
10	Sleep in	C	0	-
11	Sleep out	C	0	-
12	Partial Mode On	C	0	-
13	Normal Display Mode On	C	0	-
22	All Pixels Off	C	0	-
23	All Pixels On	C	0	-
26	Gamma Set	W	1	1 byte for curve selection
28	Display off	C	0	-
29	Display on	C	0	-
2A Note 4	Column Address Set	W	4	2 bytes for leftmost Column counter 2 bytes for rightmost Column counter
2B Note 4	Page Address Set	W	4	2 bytes for top line pointer 2 bytes for bottom line pointer
2C	Memory Write	W	Any length	Successive video data stream format: R[7..0]G[7..0]B[7..0] or G[3..], R[0..4] B[0..4] G[0..2]
2E	Memory Read	R	Any length	Successive video data stream format: R[7..0]G[7..0] B[7..0]
30 Note 4	Partial area	W	4	2 byte for top line pointer 2 byte for bottom line pointer
34	Tearing Effect Line Off	C	0	-
35	Tearing Effect Line On	W	1	1 byte for Tearing Effect Line Mode selection.
36	Memory Access Control	W	1	1 byte for memory scan direction
38	Idle Mode off	C	0	-
39	Idle Mode on	C	0	-
3A	Interface Pixel Format	C	1	1 byte for Interface Color Selection
3C	Memory Write Continue	W	Any length	Successive video data stream format: R[7..0]G[7..0]B[7..0] or R[4..0]G[5..0]B[4..0]
3E	Memory Read Continue	R	Any length	Successive video data stream format: R[7..0]G[7..0]B[7..0]

Operational Code	Function	Read/ Write/ Command	Bytes Of Parameter	Parameters
50 Note 4	Write Profile Values for Display	W	16	16 bytes for Display Profile Values 1 st – 16 th phases: Level Values
51	Write Display Brightness	W	1	1 byte for display brightness value
52	Read Display Brightness Value	R	1	-
53	Write CTRL Display	W	1	1 byte for control
54	Read CTRL Display	R	1	-
55	Write Current limit	W	1	1 byte for ACL
56	Read Current limit	R	1	-

Operational Code	Function	Read/ Write/ Command	Bytes Of Parameter	Parameters
70	Read Black/White Low Bits	R	1	Bkx[1:0]Bky[1:0]Wx[1:0]Wy[1:0]
71	Read Bkx	R	1	Bkx[9:2]
72	Read Bky	R	1	Bky[9:2]
73	Read Wx	R	1	Wx[9:2]
74	Read Wy	R	1	Wy[9:2]
75	Read Red/Green Low Bits	R	1	Rx[1:0]Ry[1:0]Gx[1:0]Gy[1:0]
76	Read Rx	R	1	Rx[9:2]
77	Read Ry	R	1	Ry[9:2]
78	Read Gx	R	1	Gx[9:2]
79	Read Gy	R	1	Gy[9:2]
7A	Read Blue/AColour Low Bits	R	1	Bx[1:0]By[1:0]Ax[1:0]Ay[1:0]
7B	Read Bx	R	1	Bx[9:2]
7C	Read By	R	1	By[9:2]
7D	Read Ax	R	1	Ax[9:2]
7E	Read Ay	R	1	Ay[9:2]
A1	Read DDB Start	R	5	-
A8	Read DDB Continue	R	Any length	-
AA	Read First Checksum	R	1	-
AF	Read Continue Checksum	R	1	-
DA	Read ID1	R	1	xx for xx Corporation
DB	Read ID2	R	1	128 to 255 for module version.
DC	Read ID3	R	1	xx for this project.

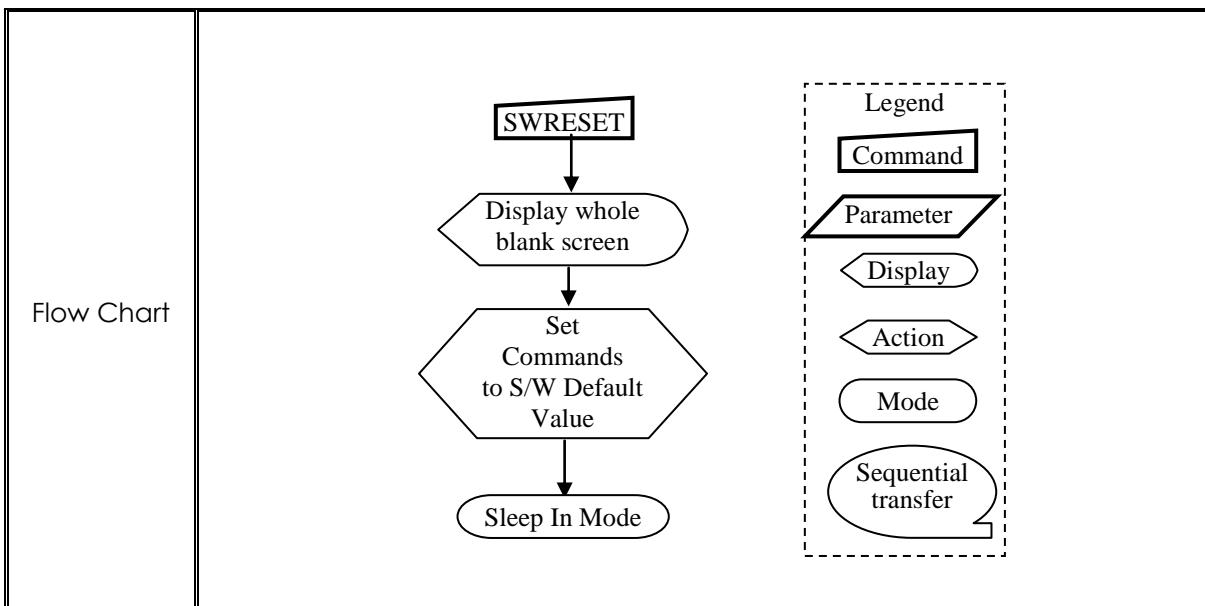
9.2 Command Description

9.2.1 NOP (00h)

00H		NOP (No Operation)																					
		Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	Write	0	0	0	0	0	0	0	0	0	00												
Parameter	NO PARAMETER																						
Description	<p>This command is an empty command; it does not have any effect on the display module.</p> <p>However, it can be used to terminate Memory Write, Memory Read, Memory Write Continue or Memory Read Continue as described in RAMWR (Memory Write), RAMRD (Memory Read), RAMWRC (Memory Write Continue) and RAMRDC (Memory Read Continue) Commands.</p>																						
Restriction																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
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Sleep In	Yes																						
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>N/A</td> </tr> <tr> <td>SW Reset</td> <td>N/A</td> </tr> <tr> <td>HW Reset</td> <td>N/A</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	N/A	SW Reset	N/A	HW Reset	N/A					
Status	Default Value																						
Power On Sequence	N/A																						
SW Reset	N/A																						
HW Reset	N/A																						
Flow Chart																							

9.2.2 Software Reset (01h)

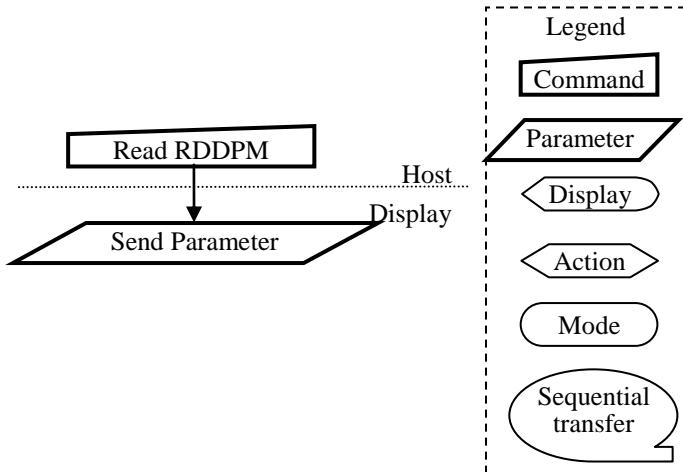
01H		SWRESET (Software Reset)																				
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	Write	0	0	0	0	0	0	0	1	01												
Parameter	NO PARAMETER																					
Description	<p>When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values (See default tables in each command description.).</p> <p>The display is blank immediately.</p> <p>Note: The Frame Memory content contents are unaffected is kept or not by this command</p>																					
Restriction	<p>It will be necessary to wait 5msec before sending new command following software reset.</p> <p>The display module loads all display supplier's factory default values to the registers during this 5msec.</p> <p>If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep out command.</p> <p>Software Reset Command cannot be sent during Sleep Out sequence.</p>																					
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																					
Power On Sequence	N/A																					
SW Reset	N/A																					
HW Reset	N/A																					



9.2.3 Read Number of the Errors on DS1 (05h)

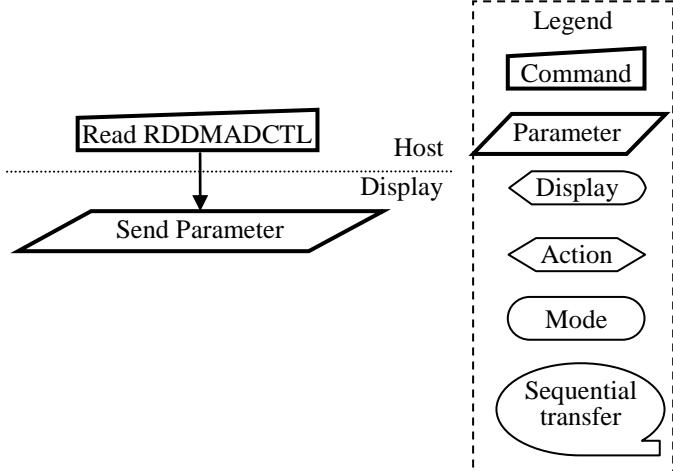
9.2.4 Read Display Power Mode (0Ah)

0AH		RDDPM (Read Display Power Mode)																																			
		Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX																										
Command		Write	0	0	0	0	1	0	1	0	0A																										
Parameter		Read	D7	D6	D5	D4	D3	D2	0	0	xx																										
Description	This command indicates the current status of the display as described in the table below:																																				
	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Comment</th> </tr> </thead> <tbody> <tr> <td>D7</td> <td>Booster Voltage Status</td> <td></td> </tr> <tr> <td>D6</td> <td>Idle Mode On/Off</td> <td></td> </tr> <tr> <td>D5</td> <td>Partial Mode On/Off</td> <td></td> </tr> <tr> <td>D4</td> <td>Sleep In/Out</td> <td></td> </tr> <tr> <td>D3</td> <td>Display Normal Mode On/Off</td> <td></td> </tr> <tr> <td>D2</td> <td>Display On/Off</td> <td></td> </tr> <tr> <td>D1</td> <td>Not Defined</td> <td>Set to '0'</td> </tr> <tr> <td>D0</td> <td>Not Defined</td> <td>Set to '0'</td> </tr> </tbody> </table>										Bit	Description	Comment	D7	Booster Voltage Status		D6	Idle Mode On/Off		D5	Partial Mode On/Off		D4	Sleep In/Out		D3	Display Normal Mode On/Off		D2	Display On/Off		D1	Not Defined	Set to '0'	D0	Not Defined	Set to '0'
Bit	Description	Comment																																			
D7	Booster Voltage Status																																				
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D4	Sleep In/Out																																				
D3	Display Normal Mode On/Off																																				
D2	Display On/Off																																				
D1	Not Defined	Set to '0'																																			
D0	Not Defined	Set to '0'																																			
	<u>Bit D7 – Booster Voltage Status</u> '0' = Booster Off or has a fault. '1' = Booster On and working OK (Meets Nokia's optical requirements).																																				
	<u>Bit D6 - Idle Mode On/Off</u> '0' = Idle Mode Off. '1' = Idle Mode On.																																				
	<u>Bit D5 – Partial Mode On/Off</u> '0' = Partial Mode Off. '1' = Partial Mode On.																																				
	<u>Bit D4 – Sleep In/Out</u> '0' = Sleep In Mode. '1' = Sleep Out Mode.																																				
	<u>Bit D3 – Display Normal Mode On/Off</u> '0' = Display Normal Mode Off. '1' = Display Normal Mode On.																																				
	<u>Bit D2 – Display On/Off</u> '0' = Display is Off. '1' = Display is On.																																				
	<u>Bit D1 – Not Defined</u> 'This bit is not applicable for this project, so it is set to '0'																																				
	<u>Bit D0 – Not Defined</u> 'This bit is not applicable for this project, so it is set to '0'																																				
Restriction																																					

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Status	Availability												
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Default	<table border="1"><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>08_{HEX}</td></tr><tr><td>SW Reset</td><td>08_{HEX}</td></tr><tr><td>HW Reset</td><td>08_{HEX}</td></tr></tbody></table>	Status	Default Value	Power On Sequence	08 _{HEX}	SW Reset	08 _{HEX}	HW Reset	08 _{HEX}				
Status	Default Value												
Power On Sequence	08 _{HEX}												
SW Reset	08 _{HEX}												
HW Reset	08 _{HEX}												
Flow Chart	 <pre>graph TD; A[Read RDDPM] --> B[/Send Parameter/];</pre> <p>The flowchart illustrates a process flow between a Host and a Display. The process starts with a 'Read RDDPM' step, followed by a 'Send Parameter' step. The 'Send Parameter' step is shown with a double-headed arrow, indicating bidirectional communication between the Host and the Display.</p> <p>Legend:</p> <ul style="list-style-type: none">Command (rectangle)Parameter (parallelogram)Display (left-pointing triangle)Action (right-pointing triangle)Mode (oval)Sequential transfer (double-headed oval)												

9.2.5 Read Display MADCTL (0Bh)

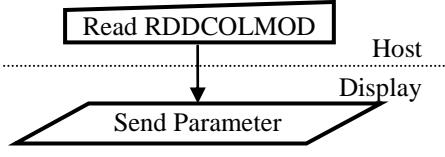
OBH		RDDMADCTL (Read Display MADCTL)																																				
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX																												
Command	Write	0	0	0	0	1	0	1	1	0B																												
Parameter	Read	D7	D6	D5	D4	D3	D2	0	0	xx																												
Description	<p>This command indicates the current status of the display as described in the table below:</p> <table border="1"> <thead> <tr> <th>Bit</th><th>Description</th><th>Comment</th></tr> </thead> <tbody> <tr> <td>D7</td><td>Page Address Order</td><td></td></tr> <tr> <td>D6</td><td>Column Address Order</td><td></td></tr> <tr> <td>D5</td><td>Page/Column Order</td><td></td></tr> <tr> <td>D4</td><td>Line Address Order</td><td></td></tr> <tr> <td>D3</td><td>RGB/BGR Order</td><td></td></tr> <tr> <td>D2</td><td>Display Data Latch Order</td><td></td></tr> <tr> <td>D1</td><td>Switching between Segment outputs and RAM</td><td>Set to '0'</td></tr> <tr> <td>D0</td><td>Switching between Common outputs and RAM</td><td>Set to '0'</td></tr> </tbody> </table> <p><u>Bit D7 – Page Address Order</u> '0' = Top to Bottom (When MADCTL B7='0'). '1' = Bottom to Top (When MADCTL B7='1').</p> <p><u>Bit D6 – Column Address Order</u> '0' = Left to Right (When MADCTL B6='0'). '1' = Right to Left (When MADCTL B6='1').</p> <p><u>Bit D5 - Page/Column Order</u> '0' = Normal Mode (When MADCTL B5='0'). '1' = Reverse Mode (When MADCTL B5='1').</p> <p>Note: For Bits D7 to D5, also refer to Section 8.2.3 MCU to Memory Write/Read Direction.</p> <p><u>Bit D4 – Line Address Order</u> '0' = Display Panel Refresh Top to Bottom (When MADCTL B4='0'). '1' = Display Panel Refresh Bottom to Top (When MADCTL B4='1').</p> <p><u>Bit D3 – RGB/BGR Order</u> '0' = RGB (When MADCTL B3='0'). '1' = BGR (When MADCTL B3='1').</p> <p><u>Bit D2 – Display Data Latch Data Order</u> '0' = Display Panel Refresh Left to Right (When MADCTL B2='0'). '1' = Display Panel Refresh Right to Left (When MADCTL B2='1').</p> <p>Note: For Bits D4, D3 and D2 also refer to 9.2.26 Memory Access Control (36h).</p> <p><u>Bit D1 – Switching Between Segment Outputs and RAM</u> This bit is not applicable for this project, so it is set to '0'</p> <p><u>Bit D0 – Switching Between Common Outputs and RAM</u> This bit is not applicable for this project, so it is set to '0'</p>											Bit	Description	Comment	D7	Page Address Order		D6	Column Address Order		D5	Page/Column Order		D4	Line Address Order		D3	RGB/BGR Order		D2	Display Data Latch Order		D1	Switching between Segment outputs and RAM	Set to '0'	D0	Switching between Common outputs and RAM	Set to '0'
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Status	Availability												
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Default	<table border="1"><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>00_{HEX}</td></tr><tr><td>SW Reset</td><td>00_{HEX}</td></tr><tr><td>HW Reset</td><td>00_{HEX}</td></tr></tbody></table>	Status	Default Value	Power On Sequence	00 _{HEX}	SW Reset	00 _{HEX}	HW Reset	00 _{HEX}				
Status	Default Value												
Power On Sequence	00 _{HEX}												
SW Reset	00 _{HEX}												
HW Reset	00 _{HEX}												
Flow Chart	 <p>The flowchart illustrates a process flow between a Host and a Display. It starts with a rectangular box labeled "Read RDDMADCTL". An arrow points down to a trapezoidal box labeled "Send Parameter". Above this arrow is a horizontal dotted line with the text "Host Display" written below it. To the right of the flowchart is a legend enclosed in a dashed box, defining six symbols:</p> <ul style="list-style-type: none">Command: A rectangle.Parameter: A parallelogram.Display: A diamond.Action: A hexagon.Mode: An oval.Sequential transfer: An oval containing a diagonal line.												

9.2.6 Read Display Pixel Format (0Ch)

0CH		RDDCOLMOD (Read Display COLMOD)																																																																																	
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																									
Command	Write	0	0	0	0	1	1	0	0	0C																																																																									
Parameter	Read	0	0	0	0	0	D2	D1	D0	xx																																																																									
Description	This command indicates the current status of the display as described in the table below:																																																																																		
	<table border="1"> <thead> <tr> <th>Bit</th><th colspan="3">Description</th><th>Comment</th></tr> </thead> <tbody> <tr> <td>D7</td><td colspan="3">RGB Interface Colour Format</td><td>Set to '0'</td></tr> <tr> <td>D6</td><td colspan="3"></td><td>Set to '0'</td></tr> <tr> <td>D5</td><td colspan="3"></td><td>Set to '0'</td></tr> <tr> <td>D4</td><td colspan="3"></td><td>Set to '0'</td></tr> <tr> <td>D3</td><td colspan="3">Control Interface Colour Format</td><td>Set to '0'</td></tr> <tr> <td>D2</td><td colspan="3"></td><td></td></tr> <tr> <td>D1</td><td colspan="3"></td><td></td></tr> <tr> <td>D0</td><td colspan="3"></td><td></td></tr> </tbody> </table> <ul style="list-style-type: none"> Bit D7 – RGB Interface Colour Format Selection This bit is not applicable for this project, so it is set to '0'. Bits D6, D5, D4 – RGB Interface Colour Pixel Format Definition These bits are not applicable for this project, so they are set to '0's. Bit D3 – Control Interface Colour Format Selection This bit is not applicable for this project, so it is set to '0'. Bit D2, D1, D0 – Control Interface Colour Pixel Format Definition. See section "9.2.29 Interface Pixel Format (3Ah)". <table border="1"> <thead> <tr> <th>Control Interface Colour Format</th><th>D2</th><th>D1</th><th>D0</th></tr> </thead> <tbody> <tr> <td>Not Defined</td><td>0</td><td>0</td><td>0</td></tr> <tr> <td>Not defined</td><td>0</td><td>0</td><td>1</td></tr> <tr> <td>Not defined</td><td>0</td><td>1</td><td>0</td></tr> <tr> <td>Not defined</td><td>0</td><td>1</td><td>1</td></tr> <tr> <td>Not Defined</td><td>1</td><td>0</td><td>0</td></tr> <tr> <td>16 bit/pixel</td><td>1</td><td>0</td><td>1</td></tr> <tr> <td>Not defined</td><td>1</td><td>1</td><td>0</td></tr> <tr> <td>24 bit/pixel</td><td>1</td><td>1</td><td>1</td></tr> </tbody> </table>		Bit	Description			Comment	D7	RGB Interface Colour Format			Set to '0'	D6				Set to '0'	D5				Set to '0'	D4				Set to '0'	D3	Control Interface Colour Format			Set to '0'	D2					D1					D0					Control Interface Colour Format	D2	D1	D0	Not Defined	0	0	0	Not defined	0	0	1	Not defined	0	1	0	Not defined	0	1	1	Not Defined	1	0	0	16 bit/pixel	1	0	1	Not defined	1	1	0	24 bit/pixel	1	1	1
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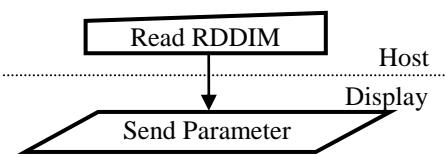
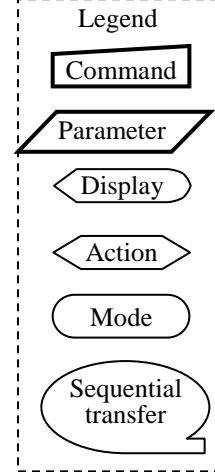
Default	Status		Default Value	
	Power On Sequence		07 _{HEX}	
	SW Reset		07 _{HEX}	
	HW Reset		07 _{HEX}	

Flow Chart			Legend					
	Host	Display	Command	Parameter	Display	Action	Mode	Sequential transfer

9.2.7 Read Display Image Mode (0Dh)

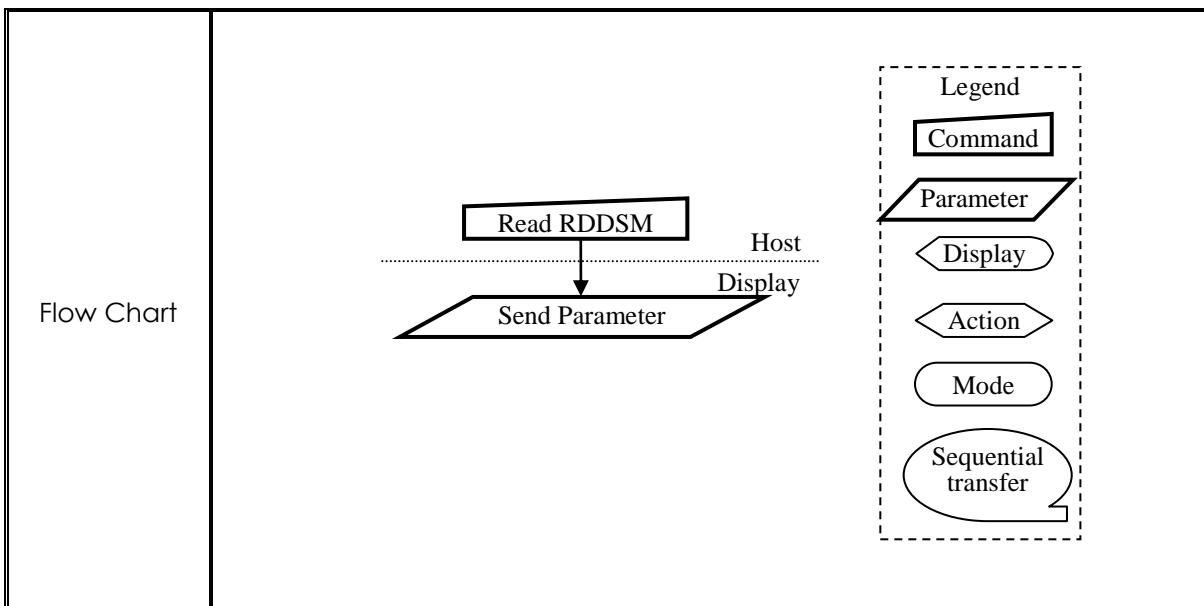
0DH		RDDIM (Read Display Image Mode)																																																						
		Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																													
Command	Write	0	0	0	0	1	1	0	1	0D																																														
Parameter	Read	0	0	0	D4	D3	D2	D1	D0	xx																																														
Description	<p>This command indicates the current status of the display as described in the table below:</p> <p><u>Bit D7 – Vertical Scrolling On/Off</u> This bit is not applicable for this project, so it is set to '0'</p> <p><u>Bit D6 – Horizontal Scrolling Status</u> This bit is not applicable for this project, so it is set to '0'</p> <p><u>Bit D5 – Inversion On/Off</u> This bit is not applicable for this project, so it is set to '0'</p> <p><u>Bit D4 – All Pixels On</u> '0' = Normal Display '1' = White Display</p> <p><u>Bit D3 – All Pixels Off</u> '0' = Normal Display '1' = Black Display</p> <p><u>Bits D2, D1, D0 – Gamma Curve Selection</u></p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Gamma Curve Selection</th> <th>D2</th> <th>D1</th> <th>D0</th> <th>Gamma Set (26h) Parameter</th> </tr> </thead> <tbody> <tr> <td>Gamma Curve 1</td> <td>0</td> <td>0</td> <td>0</td> <td>GC0</td> </tr> <tr> <td>Gamma Curve 2</td> <td>0</td> <td>0</td> <td>1</td> <td>NA</td> </tr> <tr> <td>Gamma Curve 3</td> <td>0</td> <td>1</td> <td>0</td> <td>NA</td> </tr> <tr> <td>Gamma Curve 4</td> <td>0</td> <td>1</td> <td>1</td> <td>NA</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>0</td> <td>0</td> <td>Not Defined</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>0</td> <td>1</td> <td>Not Defined</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>1</td> <td>0</td> <td>Not Defined</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>1</td> <td>1</td> <td>Not Defined</td> </tr> </tbody> </table>											Gamma Curve Selection	D2	D1	D0	Gamma Set (26h) Parameter	Gamma Curve 1	0	0	0	GC0	Gamma Curve 2	0	0	1	NA	Gamma Curve 3	0	1	0	NA	Gamma Curve 4	0	1	1	NA	Not Defined	1	0	0	Not Defined	Not Defined	1	0	1	Not Defined	Not Defined	1	1	0	Not Defined	Not Defined	1	1	1	Not Defined
Gamma Curve Selection	D2	D1	D0	Gamma Set (26h) Parameter																																																				
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Default	Status	Default Value
	Power On Sequence	00 _{HEX}
SW Reset		00 _{HEX}
HW Reset		00 _{HEX}

Flow Chart		
		

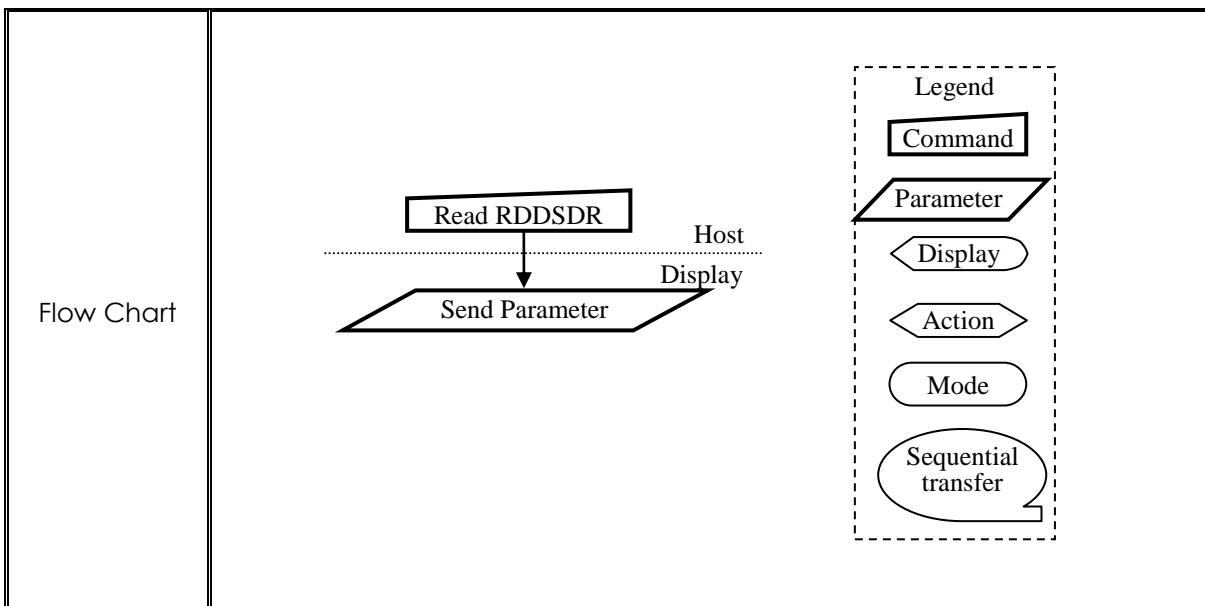
9.2.8 Read Display Signal Mode (0Eh)

OEH	RDDSM (Read Display Signal Mode)																					
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	Write	0	0	0	0	1	1	1	0	0E												
Parameter	Read	D7	D6	0	0	0	0	0	D0	xx												
Description	<p>This command indicates the current status of the display as described in the table below:</p> <p><u>Bit D7 – Tearing Effect Line On/Off</u> '0' = Tearing Effect Line Off. '1' = Tearing Effect On.</p> <p><u>Bit D6 – Tearing Effect Line Output Mode</u>, see section 8.3 for mode definitions. '0' = Mode 1. '1' = Mode 2.</p> <p><u>Bit D5 –</u> This bit is not applicable for this project, so it is set to '0'</p> <p><u>Bit D4 –</u> This bit is not applicable for this project, so it is set to '0'</p> <p><u>Bit D3 –</u> This bit is not applicable for this project, so it is set to '0'</p> <p><u>Bit D2 –</u> This bit is not applicable for this project, so it is set to '0'</p> <p><u>Bit D1 –</u> This bit is not applicable for this project, so it is set to '0'</p> <p><u>Bit D0 – Error on DS1</u>, See sections: "8.1.3.2.2.2 Acknowledge with Error Report (AwER)" and "9.2.3 Read Number of the Errors on DS1 (05h)" '0' = No Error. '1' = Error.</p>																					
Restriction																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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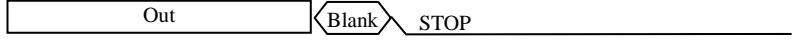
9.2.9 Read Display Self-Diagnostic Result (0Fh)

0Fh		RDDSDR (Read Display Self-Diagnostic Result)																					
		Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	Write	0	0	0	0	1	1	1	1	0F													
Parameter	Read	D7	D6	D5	D4	0	0	0	D0	xx													
Description	<p>This command indicates the status of the display self-diagnostic results after Sleep Out -command as described in the table below:</p> <p><u>Bit D7 – Register Loading Detection</u> See section 8.10.1.</p> <p><u>Bit D6 – Functionality Detection</u> See section 8.10.2.</p> <p><u>Bit D5 –</u> this function is not implemented.</p> <p><u>Bit D4 –</u> this function is not implemented.</p> <p><u>Bits D3, D2 and D1 for future use</u> Set to '0'.</p> <p><u>Bit D0 – Checksums comparison</u> See sections: "8.4 Checksums", "9.2.55 Read First Checksum (AAh)" and "9.2.56 Read Continue Checksum (AFh)" '0' = Checksums are same '1' = Checksums are not same</p>																						
Restriction	It will be necessary to wait 300ms after there is the last write access on Nokia area registers before there can read Bit D0 value.																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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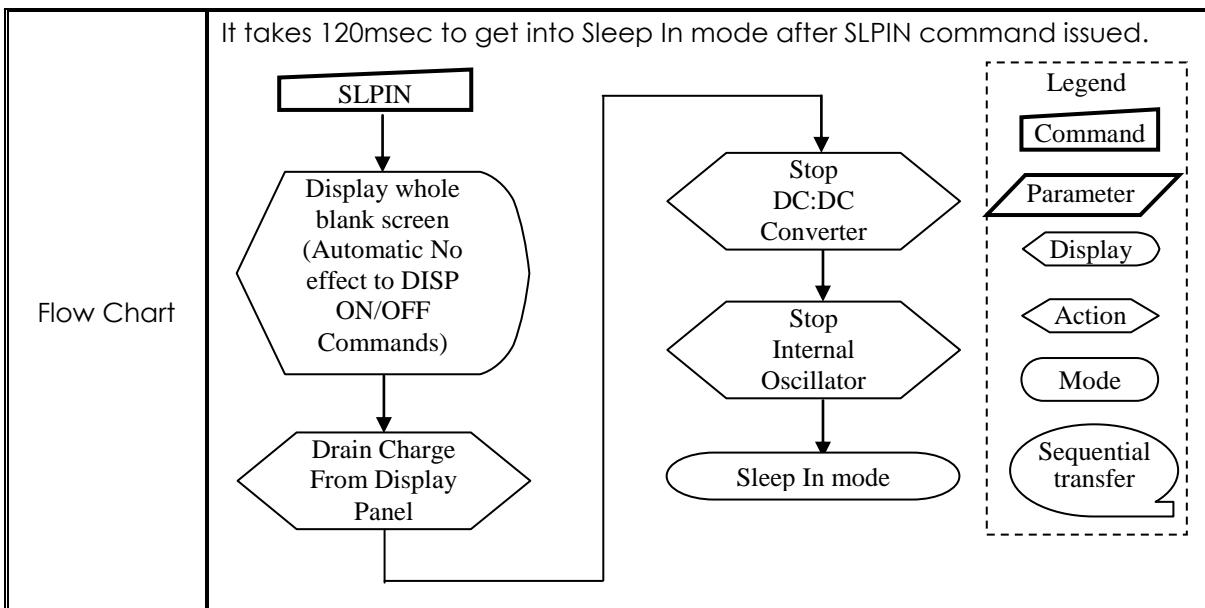


May 18th, 2012

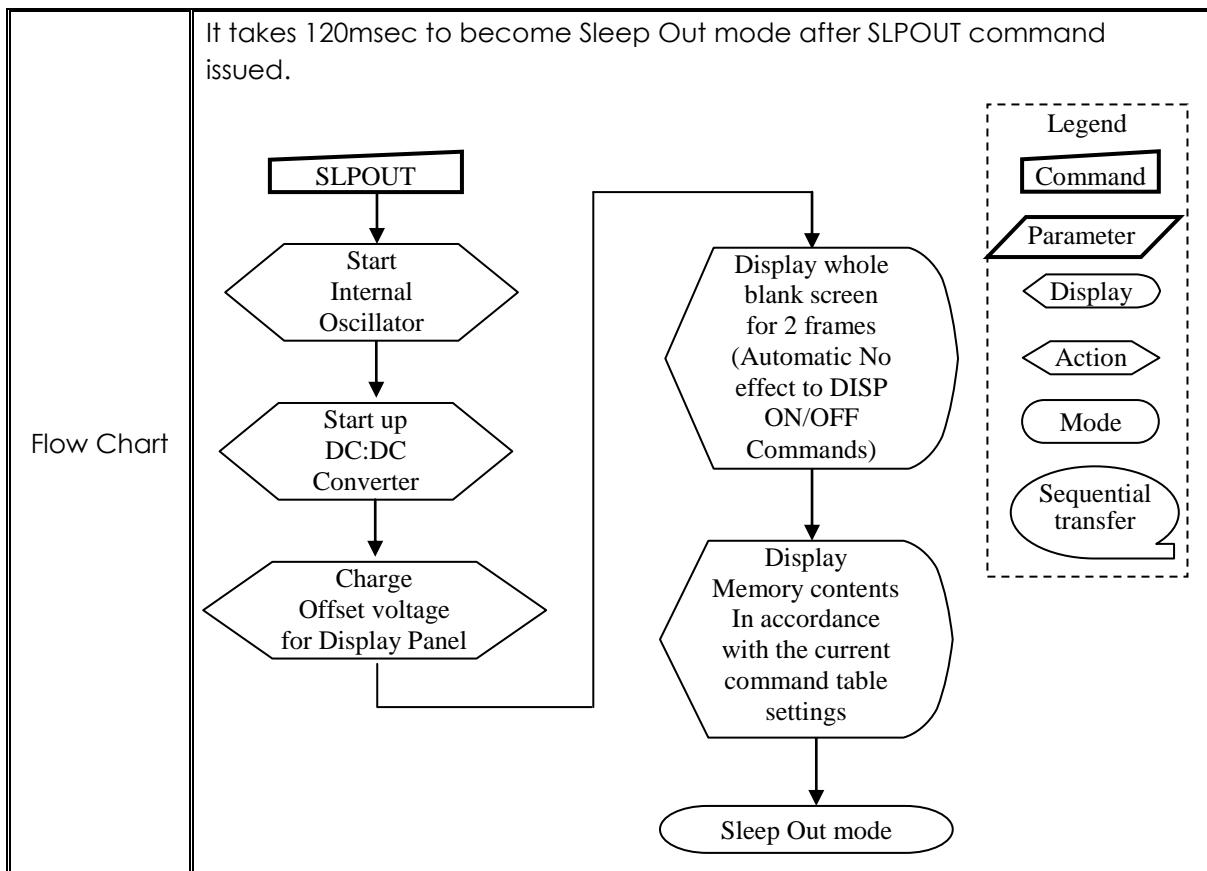
9.2.10 Sleep In (10h)

10H		SLPIN (Sleep In)																				
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	Write	0	0	0	1	0	0	0	0	10												
Parameter	NO PARAMETER																					
Description	<p>This command causes the display module to enter the minimum power consumption mode.</p> <p>In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.</p>  <p>MCU interface and memory are still working and the memory can or cannot keep its contents.</p> <p>See also section 8.6.2.</p> <p>Dimming function does not work when there is changing mode from Sleep Out to Sleep In.</p>																					
Restriction	<p>This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h).</p> <p>It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilise.</p> <p>It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</p>																					
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
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Status	Default Value																					
Power On Sequence	Sleep In Mode																					
SW Reset	Sleep In Mode																					
HW Reset	Sleep In Mode																					

May 18th, 2012



9.2.11 Sleep Out (11h)



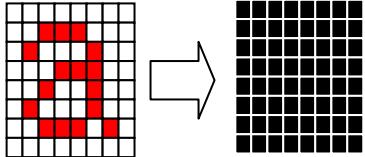
9.2.12 Partial Mode On (12h)

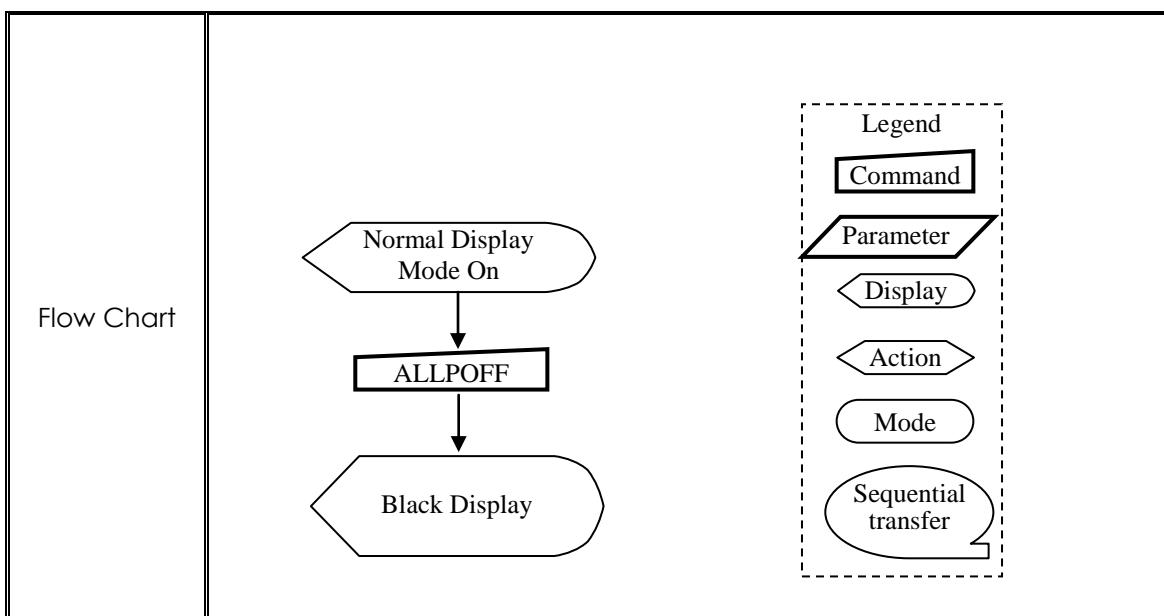
12H		PTLON (Partial Mode On)																				
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	Write	0	0	0	1	0	0	1	0	12												
Parameter	NO PARAMETER																					
Description	<p>This command turns on partial mode. The partial mode window is described by the Partial Area command (30H).</p> <p>To leave Partial mode, the Normal Display Mode On command (13H) should be written.</p> <p>See also section 8.6.2.</p>																					
Restriction	This command has no effect when Partial mode is active.																					
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
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Status	Default Value																					
Power On Sequence	Normal Display Mode On																					
SW Reset	Normal Display Mode On																					
HW Reset	Normal Display Mode On																					
Flow Chart	See Partial Area (30h)																					

9.2.13 Normal Display Mode On (13h)

13H		NORON (Normal Display Mode On)																					
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	Write	0	0	0	1	0	0	1	1	13													
Parameter	NO PARAMETER																						
Description	<p>This command returns the display to normal mode.</p> <p>Normal display mode on means Partial mode off.</p> <p>See also section 8.6.2.</p>																						
Restriction	This command has no effect when Normal Display mode is active.																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																						
Normal Mode On, Idle Mode On, Sleep Out	Yes																						
Partial Mode On, Idle Mode Off, Sleep Out	Yes																						
Partial Mode On, Idle Mode On, Sleep Out	Yes																						
Sleep In	Yes																						
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Normal Display Mode On</td> </tr> <tr> <td>SW Reset</td> <td>Normal Display Mode On</td> </tr> <tr> <td>HW Reset</td> <td>Normal Display Mode On</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	Normal Display Mode On	SW Reset	Normal Display Mode On	HW Reset	Normal Display Mode On				
Status	Default Value																						
Power On Sequence	Normal Display Mode On																						
SW Reset	Normal Display Mode On																						
HW Reset	Normal Display Mode On																						
Flow Chart	See Partial Area Descriptions for details of when to use this command.																						

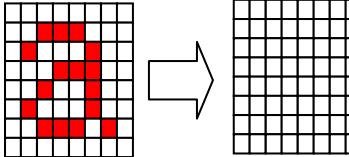
9.2.14 All Pixels Off (22h)

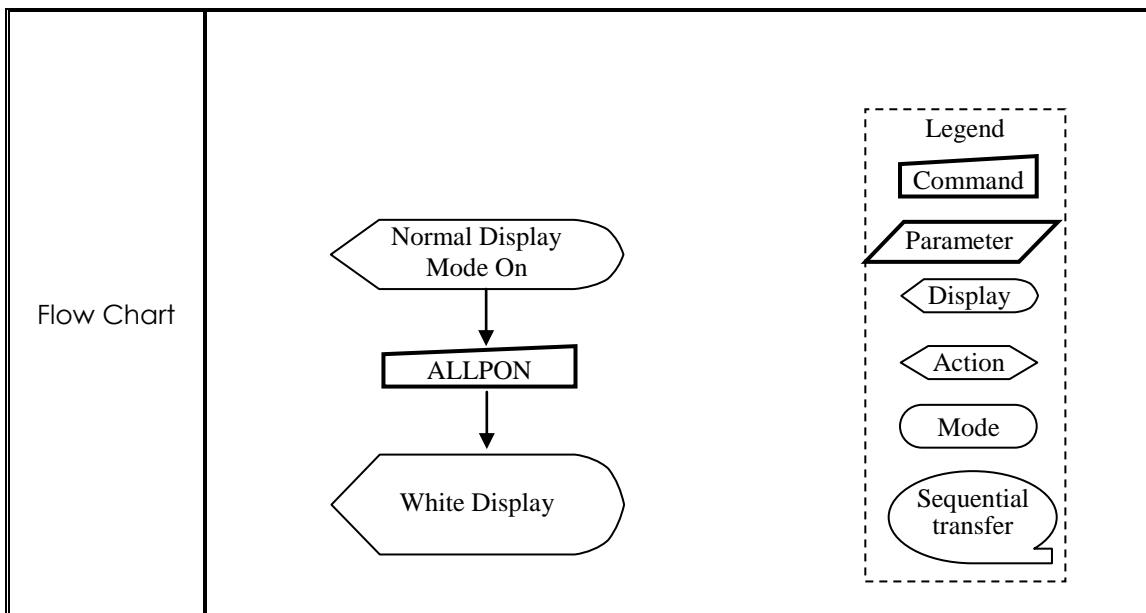
22 H		ALLPOFF (All Pixels Off)																				
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	Write	0	0	1	0	0	0	1	0	22												
Parameter	NO PARAMETER																					
Description	<p>This command turns the display panel black in 'Sleep Out' -mode and a status of the 'Display On/Off' -register can be 'on' or 'off'. This command makes no change of contents of frame memory. This command does not change any other status.</p> <p style="text-align: center;">(Example)</p> <p style="text-align: center;">memory display</p>  <p>'All Pixels On', 'Normal Display Mode On' or 'Partial Mode On' - commands are used to leave this mode. The display panel is showing the content of the frame memory after 'Normal Display Mode On' and 'Partial Mode On' -commands.</p>																					
Restriction	This command has no effect when module is already in all pixels off mode.																					
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Partial Mode On, Idle Mode Off, Sleep Out	Yes																					
Partial Mode On, Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Off</td> </tr> <tr> <td>SW Reset</td> <td>Off</td> </tr> <tr> <td>HW Reset</td> <td>Off</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Off	SW Reset	Off	HW Reset	Off				
Status	Default Value																					
Power On Sequence	Off																					
SW Reset	Off																					
HW Reset	Off																					



May 18th, 2012

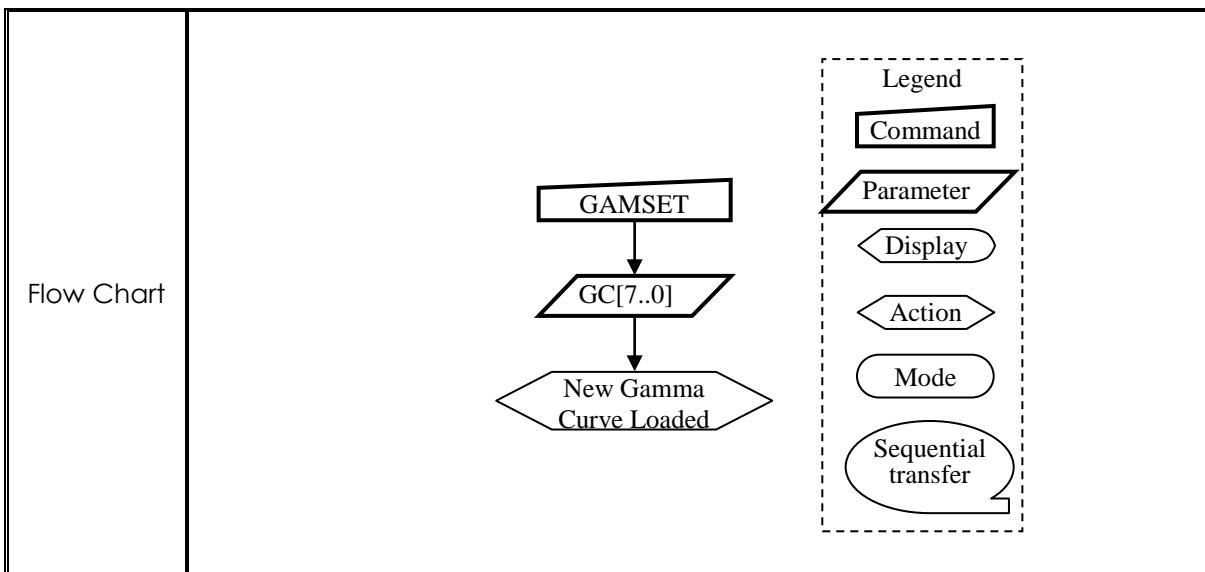
9.2.15 All Pixels On (23h)

23 H		ALLPON (All Pixels On)																				
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	Write	0	0	1	0	0	0	1	1	23												
Parameter	NO PARAMETER																					
Description	<p>This command turns the display panel white in 'Sleep out' –mode and a status of the 'Display On/Off' –register can be 'on' or 'off'. This command makes no change of contents of frame memory. This command does not change any other status.</p> <p style="text-align: center;">(Example)</p> <p style="text-align: center;">memory display</p>  <p>'All Pixels Off', 'Normal Display Mode On' or 'Partial Mode On' – commands are used to leave this mode. The display is showing the content of the frame memory after 'Normal Display Mode On' and 'Partial Mode On' –commands.</p>																					
Restriction	This command has no effect when module is already in all pixels on mode.																					
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #cccccc;">Status</th> <th style="background-color: #cccccc;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Partial Mode On, Idle Mode Off, Sleep Out	Yes																					
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Sleep In	Yes																					
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #cccccc;">Status</th> <th style="background-color: #cccccc;">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Off</td> </tr> <tr> <td>SW Reset</td> <td>Off</td> </tr> <tr> <td>HW Reset</td> <td>Off</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Off	SW Reset	Off	HW Reset	Off				
Status	Default Value																					
Power On Sequence	Off																					
SW Reset	Off																					
HW Reset	Off																					

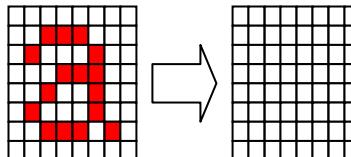


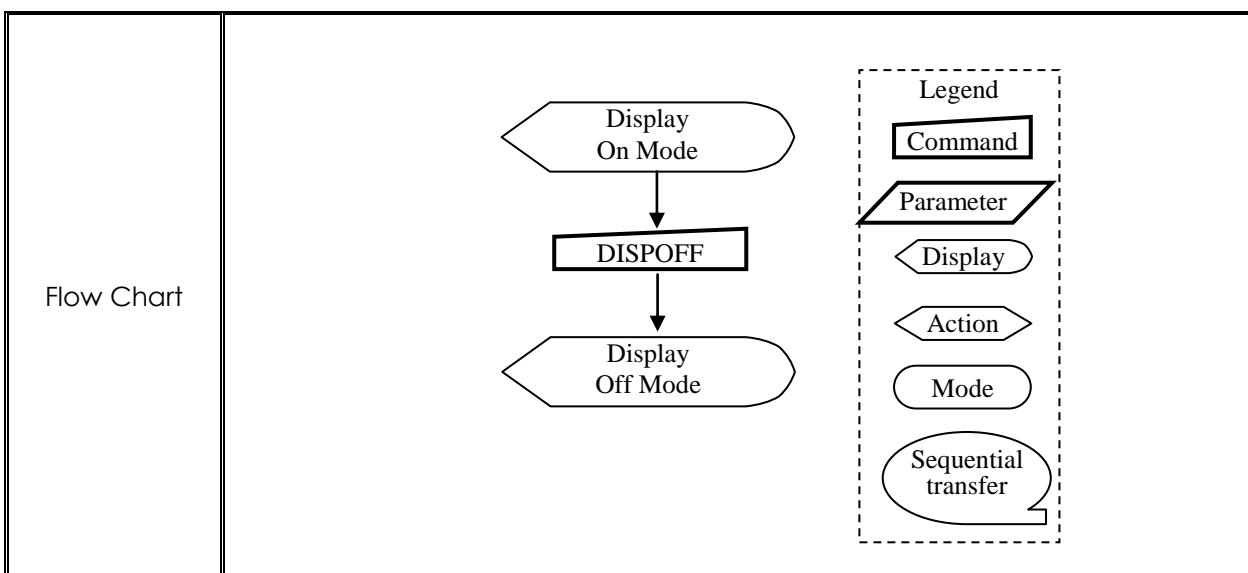
9.2.16 Gamma Set (26h)

GAMSET (Gamma Set)																									
26H	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
Command	Write	0	0	1	0	0	1	1	0	26															
Parameter	Write	GC 7	GC 6	GC 5	GC 4	GC 3	GC 2	GC 1	GC 0	1..08															
Description	<p>This command is used to select the desired Gamma curve for the current display. A maximum of 4 fixed gamma curves can be selected. The curves are defined in Section 8.7 γCurve Correction Power Supply Circuit. The curve is selected by setting the appropriate bit in the parameter as described in the Table:</p> <table border="1"> <thead> <tr> <th>GC[7...0]</th><th>Parameter</th><th>Curve Selected</th></tr> </thead> <tbody> <tr> <td>01h</td><td>GC0</td><td>Gamma Curve 1</td></tr> <tr> <td>02h</td><td>GC1</td><td>NA</td></tr> <tr> <td>04h</td><td>GC2</td><td>NA</td></tr> <tr> <td>08h</td><td>GC3</td><td>NA</td></tr> </tbody> </table> <p>Note: All other values are undefined.</p>										GC[7...0]	Parameter	Curve Selected	01h	GC0	Gamma Curve 1	02h	GC1	NA	04h	GC2	NA	08h	GC3	NA
GC[7...0]	Parameter	Curve Selected																							
01h	GC0	Gamma Curve 1																							
02h	GC1	NA																							
04h	GC2	NA																							
08h	GC3	NA																							
Restriction	Values of GC[7..0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes			
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
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Sleep In	Yes																								
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Status	Default Value																								
Power On Sequence	01 _{HEX}																								
SW Reset	01 _{HEX}																								
HW Reset	01 _{HEX}																								



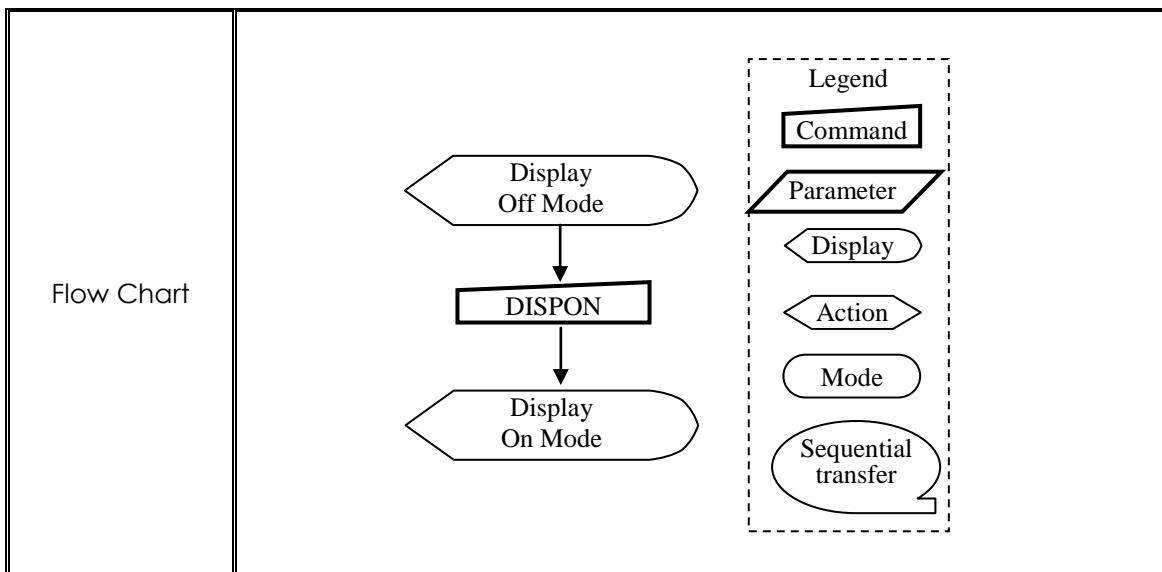
9.2.17 Display Off (28h)

28H		DISPOFF (Display Off)																				
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	Write	0	0	1	0	1	0	0	0	28												
Parameter	NO PARAMETER																					
Description	<p>This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted.</p> <p>This command makes no change of contents of frame memory.</p> <p>This command does not change any other status.</p> <p>There will be no abnormal visible effect on the display.</p> <p style="text-align: center;">(Example)</p> <div style="text-align: center;"> memory  display </div>																					
Restriction	This command has no effect when module is already in display off mode.																					
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #cccccc; text-align: center;">Status</th> <th style="background-color: #cccccc; text-align: center;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
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Sleep In	Yes																					
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #cccccc; text-align: center;">Status</th> <th style="background-color: #cccccc; text-align: center;">Default Value</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Power On Sequence</td> <td style="text-align: center;">Display Off</td> </tr> <tr> <td style="text-align: center;">SW Reset</td> <td style="text-align: center;">Display Off</td> </tr> <tr> <td style="text-align: center;">HW Reset</td> <td style="text-align: center;">Display Off</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Display Off	SW Reset	Display Off	HW Reset	Display Off				
Status	Default Value																					
Power On Sequence	Display Off																					
SW Reset	Display Off																					
HW Reset	Display Off																					

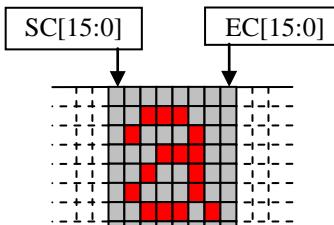


9.2.18 Display On (29h)

29H		DISPON (Display On)																					
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	Write	0	0	1	0	1	0	0	1	29													
Parameter	NO PARAMETER																						
Description	<p>This command is used to recover from DISPLAY OFF mode.</p> <p>Output from the Frame Memory is enabled.</p> <p>This command makes no change of contents of frame memory.</p> <p>This command does not change any other status.</p> <p style="text-align: center;">(Example) memory display</p>																						
Restriction	This command has no effect when module is already in display on mode.																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																						
Normal Mode On, Idle Mode On, Sleep Out	Yes																						
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Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Off</td> </tr> <tr> <td>SW Reset</td> <td>Display Off</td> </tr> <tr> <td>HW Reset</td> <td>Display Off</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	Display Off	SW Reset	Display Off	HW Reset	Display Off				
Status	Default Value																						
Power On Sequence	Display Off																						
SW Reset	Display Off																						
HW Reset	Display Off																						



9.2.19 Column Address Set (2Ah)

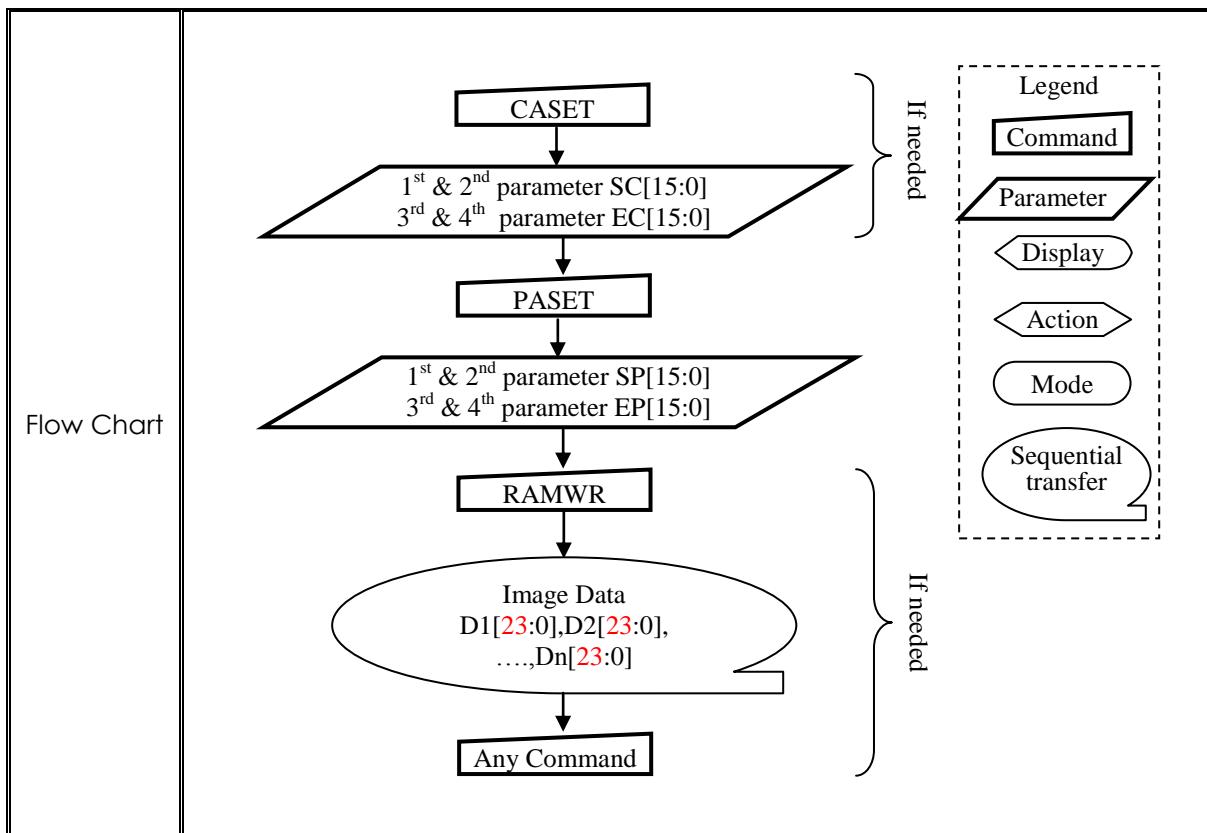
2AH		CASET (Column Address Set)																					
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	Write	0	0	1	0	1	0	1	0	2A													
1 st parameter	Write	SC 15	SC 14	SC 13	SC 12	SC 11	SC 10	SC 9	SC 8	Note 1													
2 nd parameter	Write	SC 7	SC 6	SC 5	SC 4	SC 3	SC 2	SC 1	SC 0														
3 rd parameter	Write	EC 15	EC 14	EC 13	EC 12	EC 11	EC 10	EC 9	EC 8	Note 1													
4 th parameter	Write	EC 7	EC 6	EC 5	EC 4	EC 3	EC 2	EC 1	EC 0														
Description	<p>This command is used to define area of frame memory where MCU can access.</p> <p>This command makes no change on the other driver status.</p> <p>Each value represents one column line in the Frame Memory.</p> <p>(Example)</p> 																						
Restriction	<p>SC[15:0] always must be equal to or less than EC[15:0].</p> <p>Note 1: When SC[15:0] or EC[15:0] is greater than 0167h (When MADCTL's B5 = 0) or 027Fh (When MADCTL's B5 = 1), data of out of range will be ignored.</p>																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																						
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Partial Mode On, Idle Mode On, Sleep Out	Yes																						
Sleep In	Yes																						

Default	<table border="1"><thead><tr><th>Status</th><th colspan="2">Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>SC[15:0]=0000_{HEX}</td><td>EC[15:0]=0167_{HEX}</td></tr><tr><td>SW Reset</td><td>SC[15:0]=0000_{HEX}</td><td>EC[15:0]=0167_{HEX}</td></tr><tr><td>HW Reset</td><td>SC[15:0]=0000_{HEX}</td><td>EC[15:0]=0167_{HEX}</td></tr></tbody></table>	Status	Default Value		Power On Sequence	SC[15:0]=0000 _{HEX}	EC[15:0]=0167 _{HEX}	SW Reset	SC[15:0]=0000 _{HEX}	EC[15:0]=0167 _{HEX}	HW Reset	SC[15:0]=0000 _{HEX}	EC[15:0]=0167 _{HEX}
Status	Default Value												
Power On Sequence	SC[15:0]=0000 _{HEX}	EC[15:0]=0167 _{HEX}											
SW Reset	SC[15:0]=0000 _{HEX}	EC[15:0]=0167 _{HEX}											
HW Reset	SC[15:0]=0000 _{HEX}	EC[15:0]=0167 _{HEX}											
Flow Chart	<p>The flowchart illustrates the sequence of commands:</p> <ul style="list-style-type: none">CASET (Command) followed by 1st & 2nd parameter SC[15:0] and 3rd & 4th parameter EC[15:0] (Parameter).PASET (Command) followed by 1st & 2nd parameter SP[15:0] and 3rd & 4th parameter EP[15:0] (Parameter).RAMWR (Command).Image Data (Oval): $D1[23:0], D2[23:0], \dots, Dn[23:0]$.Any Command (Command). <p>A legend on the right side defines the symbols:</p> <ul style="list-style-type: none">Command: RectangleParameter: TrapezoidDisplay: DiamondAction: ParallelogramMode: OvalSequential transfer: Oval with a diagonal line <p>A bracket labeled "If needed" groups the Image Data and Any Command steps.</p>												

9.2.20 Page Address Set (2Bh)

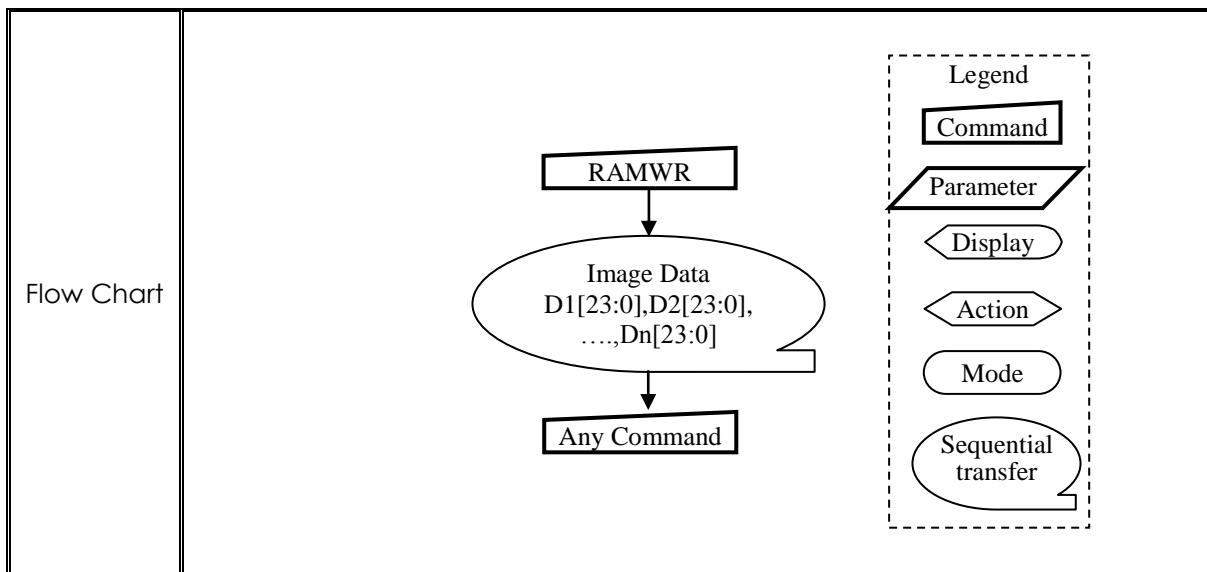
2BH		PASET (Page Address Set)																				
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	Write	0	0	1	0	1	0	1	1	2B												
1 st parameter	Write	SP 15	SP 14	SP 13	SP 12	SP 11	SP 10	SP 9	SP 8	Note 1												
2 nd parameter	Write	SP 7	SP 6	SP 5	SP 4	SP 3	SP 2	SP 1	SP 0													
3 rd parameter	Write	EP 15	EP 14	EP 13	EP 12	EP 11	EP 10	EP 9	EP 8	Note 1												
4 th parameter	Write	EP 7	EP 6	EP 5	EP 4	EP 3	EP 2	EP 1	EP 0													
Description	<p>This command is used to define area of frame memory where MCU can access.</p> <p>This command makes no change on the other driver status.</p> <p>Each value represents one Page line in the Frame Memory.</p> <p>(Example)</p>																					
Restriction	<p>SP[15:0] always must be equal to or less than EP[15:0].</p> <p>Note 1: When SP[15:0] or EP[15:0] is greater than 027Fh (When MADCTL's B5 = 0) or 0167h (When MADCTL's B5 = 1), data of out of range will be ignored.</p>																					
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
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Status	Default Value																					
Power On Sequence	SP[15:0]=0000 _{HEX}	EP[15:0]=027F _{HEX}																				
SW Reset	SP[15:0]=0000 _{HEX}	EP[15:0]=027F _{HEX}																				
HW Reset	SP[15:0]=0000 _{HEX}	EP[15:0]=027F _{HEX}																				

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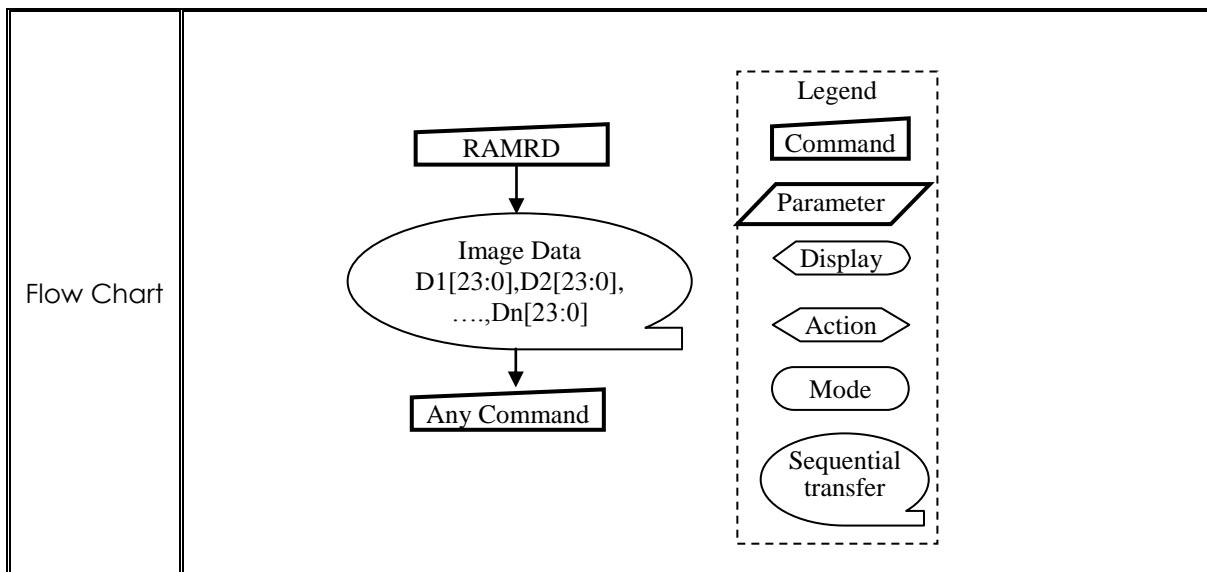
9.2.21 Memory Write (2Ch)

2CH		RAMWR (Memory Write)																				
	Write/Read	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	HEX												
Command	Write	0	0	1	0	1	1	0	0	2C												
1 st parameter	Write	D1 23	D1 22	D1 21	D1 20	D1 19	D1 18	D1 17	D1 16	0000 ... FFFF												
:	Write	Dx 7	Dx 6	Dx 5	Dx 4	Dx 3	Dx 2	Dx 1	Dx 0	0000 ... FFFF												
N TH parameter	Write	Dn 7	Dn 6	Dn 5	Dn 4	Dn 3	Dn 2	Dn 1	Dn 0	0000 ... FFFF												
Description	<p>This command is used to transfer data from MCU to frame memory.</p> <p>This command makes no change to the other driver status.</p> <p>When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions.</p> <p>The Start Column/Start Page positions are different in accordance with MADCTL setting. (See 8.2.3)</p> <p>Then D[23:0] is stored in frame memory and the column register and the page register incremented as in Table 51: Column and Page Counter Control.</p> <p>Sending any other command can stop frame Write.</p> <p>See section "8.1.7 Display Module Data Colour Coding" for colour coding.</p>																					
Restriction	<p>There is no restriction on length of parameters.</p> <p>No access in the frame memory in Sleep In mode.</p>																					
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>No</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	No
Status	Availability																					
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Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Partial Mode On, Idle Mode Off, Sleep Out	Yes																					
Partial Mode On, Idle Mode On, Sleep Out	Yes																					
Sleep In	No																					
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>SW Reset</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>HW Reset</td> <td>Contents of memory is set randomly</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Contents of memory is set randomly	SW Reset	Contents of memory is set randomly	HW Reset	Contents of memory is set randomly				
Status	Default Value																					
Power On Sequence	Contents of memory is set randomly																					
SW Reset	Contents of memory is set randomly																					
HW Reset	Contents of memory is set randomly																					

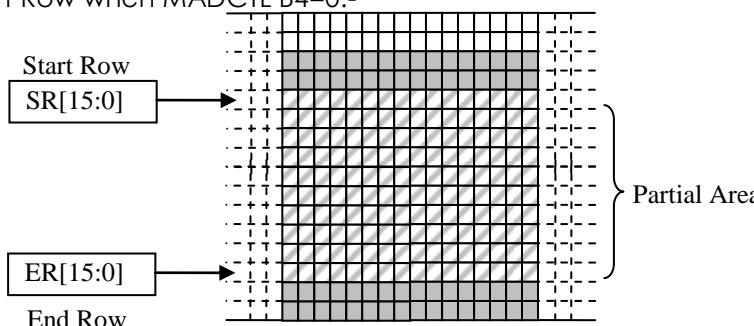
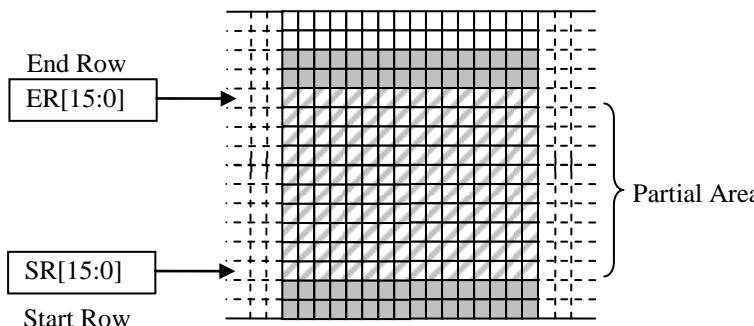
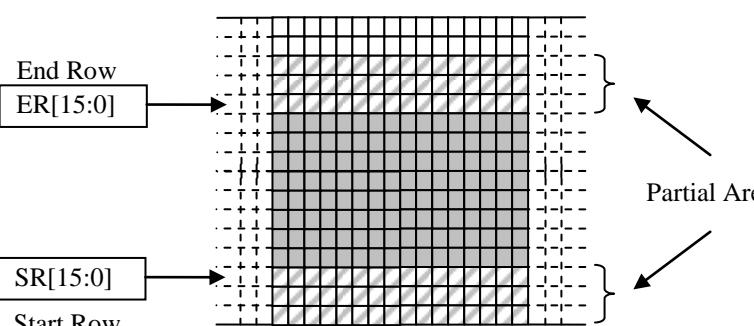


9.2.22 Memory Read (2Eh)

2EH		RAMRD (Memory Read)																				
	Write/Read	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	HEX												
Command	Write	0	0	1	0	1	1	1	0	2E												
1 st Parameter	Read	D1 23	D1 22	D1 21	D1 20	D1 19	D1 18	D1 17	D1 16	0000 .. FFFF												
:	Read	Dx 7	Dx 6	Dx 5	Dx 4	Dx 3	Dx 2	Dx 1	Dx 0	0000 .. FFFF												
(N+1) TH parameter	Read	Dn 7	Dn 6	Dn 5	Dn 4	Dn 3	Dn 2	Dn 1	Dn 0	0000 .. FFFF												
Description	<p>This command is used to transfer data from frame memory to MCU and this command makes no change to the other driver status.</p> <p>When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions.</p> <p>The Start Column/Start Page positions are different in accordance with MADCTL setting (See 8.2.3).</p> <p>Then D[23:0] is read back from the frame memory and the column register and the page register incremented as in Table 51: Column and Page Counter Control.</p> <p>Frame Read can be stopped by sending any other command.</p> <p>See section "8.1.7 Display Module Data Colour Coding" for colour coding.</p>																					
Restriction	No access in the frame memory in Sleep In mode.																					
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>No</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	No
Status	Availability																					
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Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Partial Mode On, Idle Mode Off, Sleep Out	Yes																					
Partial Mode On, Idle Mode On, Sleep Out	Yes																					
Sleep In	No																					
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>SW Reset</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>HW Reset</td> <td>Contents of memory is set randomly</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Contents of memory is set randomly	SW Reset	Contents of memory is set randomly	HW Reset	Contents of memory is set randomly				
Status	Default Value																					
Power On Sequence	Contents of memory is set randomly																					
SW Reset	Contents of memory is set randomly																					
HW Reset	Contents of memory is set randomly																					

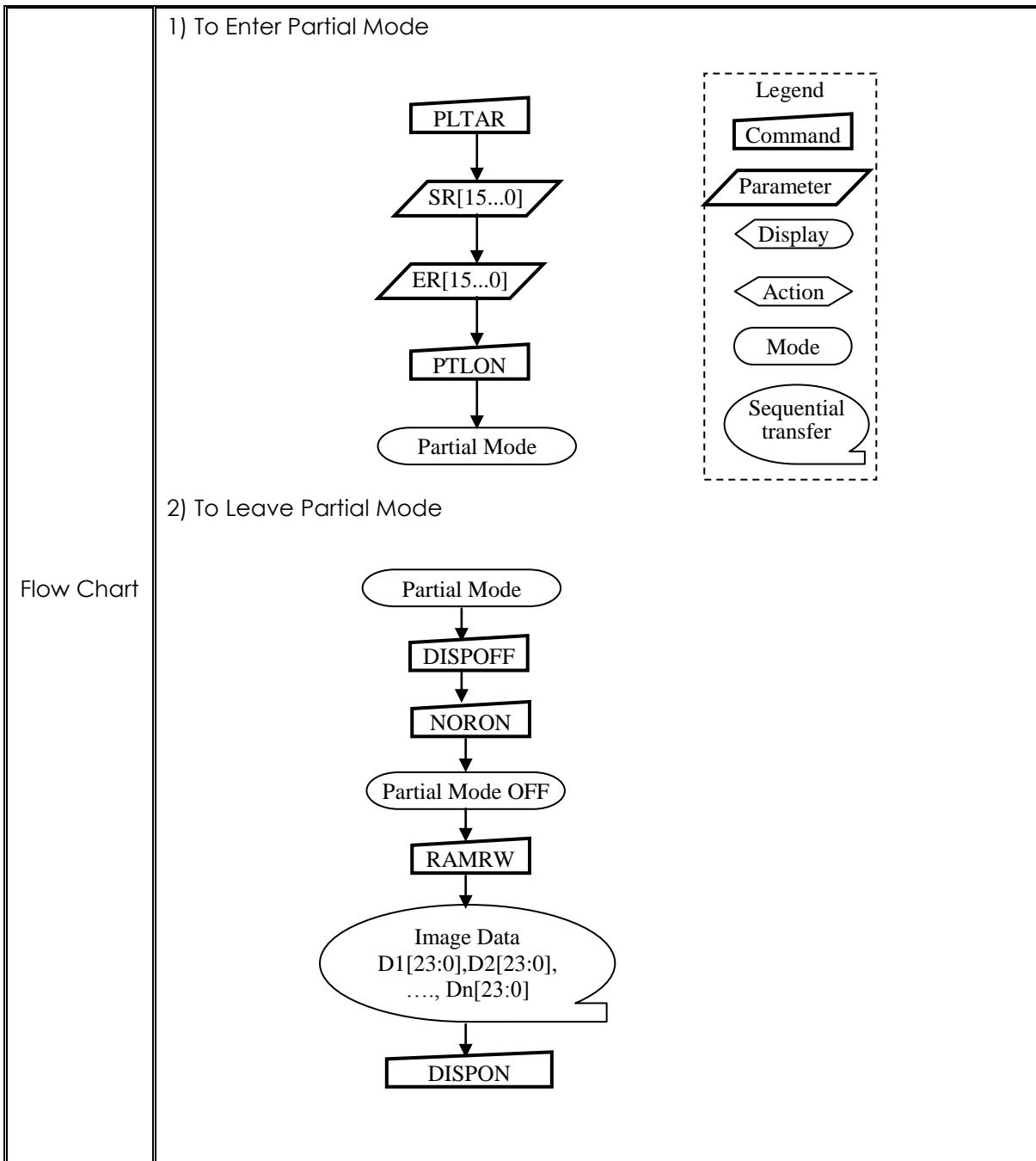


9.2.23 Partial Area (30h)

30H		PLTAR (Partial Area)									
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	Write	0	0	1	1	0	0	0	0	30	
1 st parameter	Write	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	0000	
2 nd parameter	Write	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	... 027F	
3 rd parameter	Write	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	0000	
4 th parameter	Write	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	... 027F	
Description	<p>This command defines the partial mode's display area. There are 4 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer.</p> <p>If End Row>Start Row when MADCTL B4=0:-</p>  <p>If End Row>Start Row when MADCTL B4=1:-</p>  <p>If End Row<Start Row when MADCTL B4=0:-</p>  <p>If End Row = Start Row then the Partial Area will be one row deep.</p>										
Restriction	SR[15...0] and ER[15...0] cannot be 0000h nor exceed 027Fh.										

Register Availability	Status		Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value	
	Power On Sequence	SR[15...0] = 0000 _{HEX} ER[15...0] = 027F _{HEX}	
	SW Reset	SR[15...0] = 0000 _{HEX} ER[15...0] = 027F _{HEX}	
	HW Reset	SR[15...0] = 0000 _{HEX} ER[15...0] = 027F _{HEX}	

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9.2.24 Tearing Effect Line Off (34h)

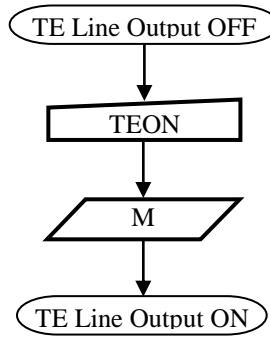
34H		TEOFF (Tearing Effect Line OFF)																					
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	Write	0	0	1	1	0	1	0	0	34													
Parameter	NO PARAMETER																						
Description	<p>This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.</p> <p>See also chapter "8.10 Sleep Out –Command and Self-Diagnostic Functions of the Display Module".</p>																						
Restriction	This command has no effect when Tearing Effect output is already OFF.																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
Status	Availability																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																						
Normal Mode On, Idle Mode On, Sleep Out	Yes																						
Partial Mode On, Idle Mode Off, Sleep Out	Yes																						
Partial Mode On, Idle Mode On, Sleep Out	Yes																						
Sleep In	Yes																						
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Off</td></tr> <tr> <td>SW Reset</td><td>Off</td></tr> <tr> <td>HW Reset</td><td>Off</td></tr> </tbody> </table>										Status	Default Value	Power On Sequence	Off	SW Reset	Off	HW Reset	Off					
Status	Default Value																						
Power On Sequence	Off																						
SW Reset	Off																						
HW Reset	Off																						
Flow Chart	<pre> graph TD A([TE Line Output ON]) --> B[TEOFF] B --> C([TE Line Output OFF]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																						

9.2.25 Tearing Effect Line On (35h)

35H		TEON (Tearing Effect Line ON)																					
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	Write	0	0	1	1	0	1	0	1	35													
Parameter	Write	X	X	X	X	X	X	X	M	XX													
Description	<p>This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit B4.</p> <p>The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. (X=Don't Care).</p> <p>When M=0:</p> <p>The Tearing Effect Output line consists of V-Blanking information only:</p> <p>When M=1:</p> <p>The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:</p> <p>Notes:</p> <ol style="list-style-type: none"> 1. During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low. 2. See also chapter "8.10 Sleep Out –Command and Self-Diagnostic Functions of the Display Module". <p>X = Don't care.</p>																						
Restriction	This command has no effect when Tearing Effect output is already ON.																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																						
Normal Mode On, Idle Mode On, Sleep Out	Yes																						
Partial Mode On, Idle Mode Off, Sleep Out	Yes																						
Partial Mode On, Idle Mode On, Sleep Out	Yes																						
Sleep In	Yes																						

Default		Status		Default Value
		Power On Sequence	SW Reset	
			Off	
			Off	
			Off	

Flow Chart		TE Line Output OFF		Legend
		TEON	M	
				<p>Legend</p> <ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer



9.2.26 Memory Access Control (36h)

36H		MADCTL (Memory Access Control)																																			
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX																											
Command	Write	0	0	1	1	0	1	1	0	36																											
Parameter	Write	D7	D6	D5	D4	D3	D2	X	X	XX																											
		This command defines read/write scanning direction of frame memory.																																			
		This command makes no change on the other driver status.																																			
		<table border="1"> <thead> <tr> <th>Bit</th><th>Description</th><th>Comment</th></tr> </thead> <tbody> <tr> <td>D7</td><td>Page Address Order</td><td></td></tr> <tr> <td>D6</td><td>Column Address Order</td><td></td></tr> <tr> <td>D5</td><td>Page/Column Order</td><td></td></tr> <tr> <td>D4</td><td>Line Address Order</td><td></td></tr> <tr> <td>D3</td><td>RGB/BGR Order</td><td></td></tr> <tr> <td>D2</td><td>Display Data Latch Order</td><td></td></tr> <tr> <td>D1</td><td>Switching between Segment outputs and RAM</td><td>Don't care</td></tr> <tr> <td>D0</td><td>Switching between Common outputs and RAM</td><td>Don't care</td></tr> </tbody> </table>									Bit	Description	Comment	D7	Page Address Order		D6	Column Address Order		D5	Page/Column Order		D4	Line Address Order		D3	RGB/BGR Order		D2	Display Data Latch Order		D1	Switching between Segment outputs and RAM	Don't care	D0	Switching between Common outputs and RAM	Don't care
Bit	Description	Comment																																			
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D6	Column Address Order																																				
D5	Page/Column Order																																				
D4	Line Address Order																																				
D3	RGB/BGR Order																																				
D2	Display Data Latch Order																																				
D1	Switching between Segment outputs and RAM	Don't care																																			
D0	Switching between Common outputs and RAM	Don't care																																			
		<p><u>Bit D7 – Page Address Order</u> '0' = Top to Bottom (When MADCTL B7='0'). '1' = Bottom to Top (When MADCTL B7='1').</p> <p><u>Bit D6 – Column Address Order</u> '0' = Left to Right (When MADCTL B6='0'). '1' = Right to Left (When MADCTL B6='1').</p> <p><u>Bit D5 - Page/Column Order</u> '0' = Normal Mode (When MADCTL B5='0'). '1' = Reverse Mode (When MADCTL B5='1').</p> <p>Note: For Bits D7 to D5, also refer to Section 8.2.3 MCU to Memory Write/Read Direction.</p> <p><u>Bit D4 – Line Address Order</u> '0' = Display Panel Refresh Top to Bottom (When MADCTL B4='0'). '1' = Display Panel Refresh Bottom to Top (When MADCTL B4='1').</p> <p><u>Bit D3 – RGB/BGR Order</u> '0' = RGB (When MADCTL B3='0'). '1' = BGR (When MADCTL B3='1').</p> <p><u>Bit D2 – Display Data Latch Data Order</u> '0' = Display Panel Refresh Left to Right (When MADCTL B2='0'). '1' = Display Panel Refresh Right to Left (When MADCTL B2='1').</p> <p><u>Bit D1 – Switching Between Segment Outputs and RAM</u> This bit is not applicable for this project, so it is set to '0'</p> <p><u>Bit D0 – Switching Between Common Outputs and RAM</u> This bit is not applicable for this project, so it is set to '0'</p> <p>X = don't care.</p>																																			

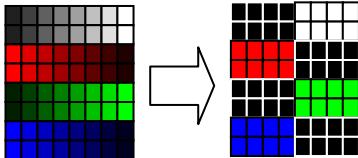
	<p>B4 – Vertical Updating order</p> <p>B4=”0”</p> <p>B4=”1”</p>												
Description	<p>B3 – RGB-BGR Order</p> <p>B3=”0”</p> <p>B3=”1”</p>												
	<p>B2 – Horizontal Updating order</p> <p>B2=”0”</p> <p>B2=”1”</p>												
	<p>Note: Top-Left (0,0) means a physical memory location.</p>												
Restriction													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Default	<table border="1"><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>00_{HEX}</td></tr><tr><td>SW Reset</td><td>00_{HEX}</td></tr><tr><td>HW Reset</td><td>00_{HEX}</td></tr></tbody></table>	Status	Default Value	Power On Sequence	00 _{HEX}	SW Reset	00 _{HEX}	HW Reset	00 _{HEX}
Status	Default Value								
Power On Sequence	00 _{HEX}								
SW Reset	00 _{HEX}								
HW Reset	00 _{HEX}								
<p>Flow Chart</p> <pre>graph TD; MADCTL[MADCTL] --> B["1st parameter B[7:0]"];</pre> <p>Legend</p> <ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer									

9.2.27 Idle Mode Off (38h)

38H		IDMOFF (Idle mode off)																					
		Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	Write	0	0	1	1	1	0	0	0	38													
Parameter	NO PARAMETER																						
Description	<p>This command is used to recover from Idle mode on.</p> <p>In the idle off mode, display panel can display maximum 16,777,216 colours.</p> <p>See also section 8.6.2.</p>																						
Restriction	This command has no effect when module is already in idle off mode.																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
Status	Availability																						
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Normal Mode On, Idle Mode On, Sleep Out	Yes																						
Partial Mode On, Idle Mode Off, Sleep Out	Yes																						
Partial Mode On, Idle Mode On, Sleep Out	Yes																						
Sleep In	Yes																						
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Idle Mode Off</td> </tr> <tr> <td>SW Reset</td> <td>Idle Mode Off</td> </tr> <tr> <td>HW Reset</td> <td>Idle Mode Off</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Idle Mode Off	SW Reset	Idle Mode Off	HW Reset	Idle Mode Off					
Status	Default Value																						
Power On Sequence	Idle Mode Off																						
SW Reset	Idle Mode Off																						
HW Reset	Idle Mode Off																						
Flow Chart	<pre> graph TD A([Idle on mode]) --> B[IDMOFF] B --> C([Idle off mode]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																						

9.2.28 Idle Mode On (39h)

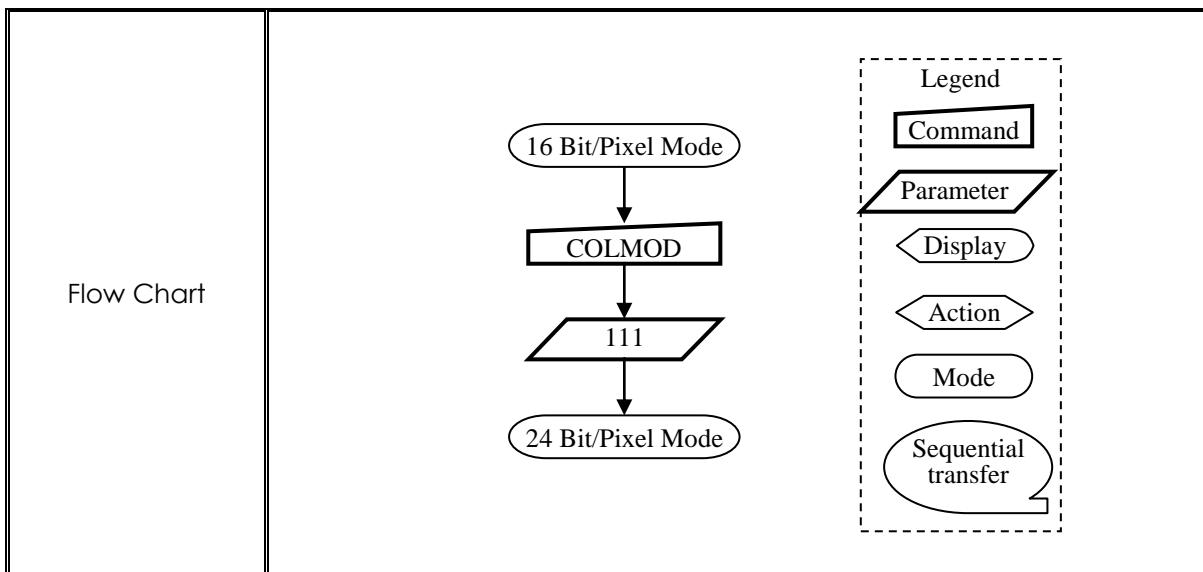
39H		IDMON (Idle mode on)																																																	
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																									
Command	Write	0	0	1	1	1	0	0	1	39																																									
Parameter	NO PARAMETER																																																		
Description	<p>This command is used to enter into Idle mode on.</p> <p>In the idle on mode, colour expression is reduced. The primary and the secondary colours using MSB of each R, G and B in the Frame Memory, 8 colour depth data is displayed. This command is also entering the display in so called ALPM (advanded lo power mode) if used together with PARTIAL mode on command. In ALPM, module shows 8 bit colors with dimmed luminance and reduced refresh rate, to achieve very low power consumption.</p> <p style="text-align: center;">(Example) memory display </p> <table border="1"> <thead> <tr> <th colspan="4">Memory contents vs Display Colour</th> </tr> <tr> <th></th><th>R₇R₆R₅R₄R₃R₂R₁R₀</th><th>G₇G₆G₅G₄G₃G₂G₁G₀</th><th>B₇B₆B₅B₄B₃B₂B₁B₀</th></tr> </thead> <tbody> <tr> <td>Black</td><td>0XXXXXXX</td><td>0XXXXXXX</td><td>0XXXXXXX</td></tr> <tr> <td>Blue</td><td>0XXXXXXX</td><td>0XXXXXXX</td><td>1XXXXXXX</td></tr> <tr> <td>Red</td><td>1XXXXXXX</td><td>0XXXXXXX</td><td>0XXXXXXX</td></tr> <tr> <td>Magenta</td><td>1XXXXXXX</td><td>0XXXXXXX</td><td>1XXXXXXX</td></tr> <tr> <td>Green</td><td>0XXXXXXX</td><td>1XXXXXXX</td><td>0XXXXXXX</td></tr> <tr> <td>Cyan</td><td>0XXXXXXX</td><td>1XXXXXXX</td><td>1XXXXXXX</td></tr> <tr> <td>Yellow</td><td>1XXXXXXX</td><td>1XXXXXXX</td><td>0XXXXXXX</td></tr> <tr> <td>White</td><td>1XXXXXXX</td><td>1XXXXXXX</td><td>1XXXXXXX</td></tr> </tbody> </table> <p>See also section 8.6.2.</p>											Memory contents vs Display Colour					R ₇ R ₆ R ₅ R ₄ R ₃ R ₂ R ₁ R ₀	G ₇ G ₆ G ₅ G ₄ G ₃ G ₂ G ₁ G ₀	B ₇ B ₆ B ₅ B ₄ B ₃ B ₂ B ₁ B ₀	Black	0XXXXXXX	0XXXXXXX	0XXXXXXX	Blue	0XXXXXXX	0XXXXXXX	1XXXXXXX	Red	1XXXXXXX	0XXXXXXX	0XXXXXXX	Magenta	1XXXXXXX	0XXXXXXX	1XXXXXXX	Green	0XXXXXXX	1XXXXXXX	0XXXXXXX	Cyan	0XXXXXXX	1XXXXXXX	1XXXXXXX	Yellow	1XXXXXXX	1XXXXXXX	0XXXXXXX	White	1XXXXXXX	1XXXXXXX	1XXXXXXX
Memory contents vs Display Colour																																																			
	R ₇ R ₆ R ₅ R ₄ R ₃ R ₂ R ₁ R ₀	G ₇ G ₆ G ₅ G ₄ G ₃ G ₂ G ₁ G ₀	B ₇ B ₆ B ₅ B ₄ B ₃ B ₂ B ₁ B ₀																																																
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Blue	0XXXXXXX	0XXXXXXX	1XXXXXXX																																																
Red	1XXXXXXX	0XXXXXXX	0XXXXXXX																																																
Magenta	1XXXXXXX	0XXXXXXX	1XXXXXXX																																																
Green	0XXXXXXX	1XXXXXXX	0XXXXXXX																																																
Cyan	0XXXXXXX	1XXXXXXX	1XXXXXXX																																																
Yellow	1XXXXXXX	1XXXXXXX	0XXXXXXX																																																
White	1XXXXXXX	1XXXXXXX	1XXXXXXX																																																
Restriction	This command has no effect when module is already in idle off mode.																																																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																													
Status	Availability																																																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																																		
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Partial Mode On, Idle Mode On, Sleep Out	Yes																																																		
Sleep In	Yes																																																		

Default	<table border="1"><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Idle Mode Off</td></tr><tr><td>SW Reset</td><td>Idle Mode Off</td></tr><tr><td>HW Reset</td><td>Idle Mode Off</td></tr></tbody></table>	Status	Default Value	Power On Sequence	Idle Mode Off	SW Reset	Idle Mode Off	HW Reset	Idle Mode Off
Status	Default Value								
Power On Sequence	Idle Mode Off								
SW Reset	Idle Mode Off								
HW Reset	Idle Mode Off								
<p>Flow Chart</p> <pre>graph TD; A([Idle off mode]) --> B[IDMON]; B --> C([Idle on mode]);</pre> <p>The flowchart illustrates a sequence of states. It begins with an oval labeled "Idle off mode". An arrow points down to a rectangular box labeled "IDMON". From "IDMON", another arrow points down to an oval labeled "Idle on mode".</p> <p>Legend:</p> <ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer									

9.2.29 Interface Pixel Format (3Ah)

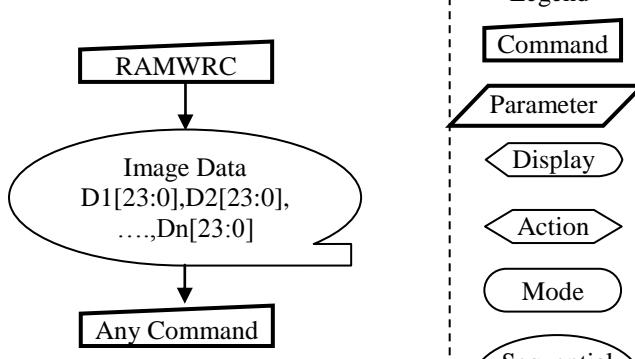
3A H		COLMOD (Interface Pixel Format)																																												
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																				
Command	Write	0	0	1	1	1	0	1	0	3A																																				
Parameter	Write	X	X	X	X	X	D2	D1	D0	101, 111																																				
Description	<p>This command is used to define the format of RGB picture data, which is to be transferred via the MCU Interface. The formats are shown in the table:</p> <table border="1"> <thead> <tr> <th>Control Interface Colour Format</th> <th>D2</th> <th>D1</th> <th>D0</th> </tr> </thead> <tbody> <tr> <td>Not Defined</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>Not defined</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>Not defined</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>Not defined</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>16 bit/pixel</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>Not defined</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>24 bit/pixel</td> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table> <p>Note: In 16 Bit/Pixel mode, the 16 bit/pixel is converted to 24 bit/pixel what is meeting Nokia's optical requirements.</p> <p>X = don't care.</p>										Control Interface Colour Format	D2	D1	D0	Not Defined	0	0	0	Not defined	0	0	1	Not defined	0	1	0	Not defined	0	1	1	Not Defined	1	0	0	16 bit/pixel	1	0	1	Not defined	1	1	0	24 bit/pixel	1	1	1
Control Interface Colour Format	D2	D1	D0																																											
Not Defined	0	0	0																																											
Not defined	0	0	1																																											
Not defined	0	1	0																																											
Not defined	0	1	1																																											
Not Defined	1	0	0																																											
16 bit/pixel	1	0	1																																											
Not defined	1	1	0																																											
24 bit/pixel	1	1	1																																											
Restriction	There is no visible effect until the Frame Memory is written to.																																													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																								
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Sleep In	Yes																																													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>24 bit/pixel</td> </tr> <tr> <td>SW Reset</td> <td>No Change 24 bit/pixel</td> </tr> <tr> <td>HW Reset</td> <td>24 bit/pixel</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	24 bit/pixel	SW Reset	No Change 24 bit/pixel	HW Reset	24 bit/pixel																												
Status	Default Value																																													
Power On Sequence	24 bit/pixel																																													
SW Reset	No Change 24 bit/pixel																																													
HW Reset	24 bit/pixel																																													

May 18th, 2012



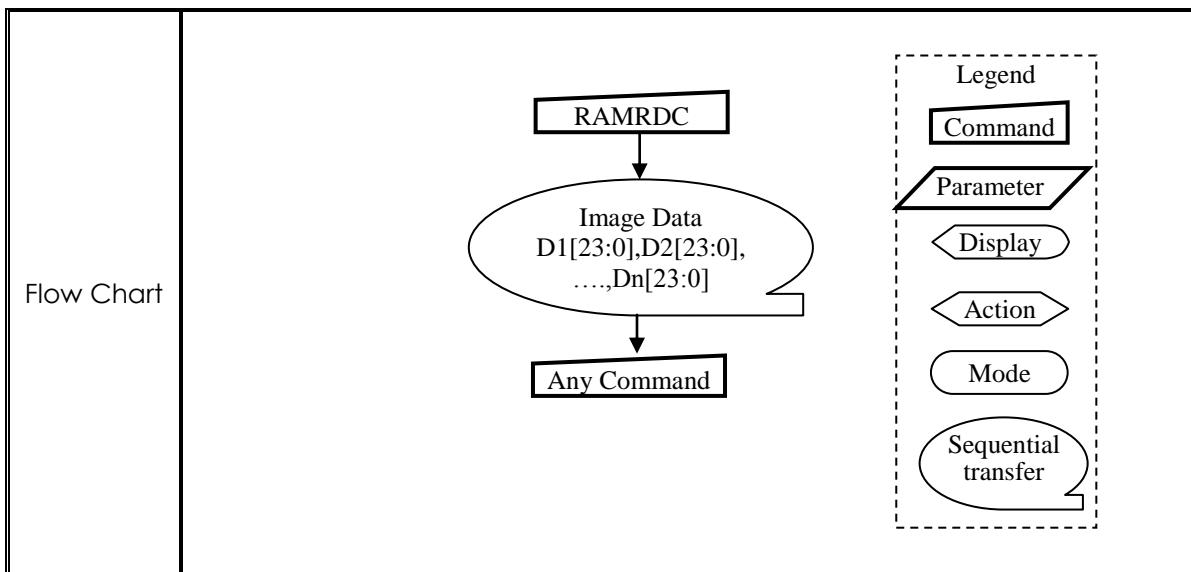
9.2.30 Memory Write Continue (3Ch)

3C H		RAMWRC (Memory Write Continue)																				
	Write/Read	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	HEX												
Command	Write	0	0	1	1	1	1	0	0	3C												
1 st parameter	Write	D1 23	D1 22	D1 21	D1 20	D1 19	D1 18	D1 17	D1 16	0000 ... FFFF												
:	Write	Dx 7	Dx 6	Dx 5	Dx 4	Dx 3	Dx 2	Dx 1	Dx 0	0000 ... FFFF												
N th parameter	Write	Dn 7	Dn 6	Dn 5	Dn 4	Dn 3	Dn 2	Dn 1	Dn 0	0000 ... FFFF												
Description	<p>This command is used to transfer data from MCU to frame memory, if there is wanted to continue memory write after "9.2.21 Memory Write (2Ch)" command.</p> <p>This command makes no change to the other driver status.</p> <p>When this command is accepted, the column register and the page register are not reset to the Start Column/Start Page positions as it has been done on "9.2.21 Memory Write (2Ch)" command.</p> <p>Then D[23:0] is stored in frame memory and the column register and the page register incremented as in Table 51: Column and Page Counter Control.</p> <p>Sending any other command can stop frame Write.</p> <p>See section 8.1.7 "Display Module Data Colour Coding" for colour coding.</p>																					
Restriction	<p>There is no restriction on length of parameters.</p> <p>No access in the frame memory in Sleep In mode.</p>																					
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>No</td></tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	No
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Partial Mode On, Idle Mode Off, Sleep Out	Yes																					
Partial Mode On, Idle Mode On, Sleep Out	Yes																					
Sleep In	No																					

Default	Status	Default Value
	Power On Sequence	Contents of memory is set randomly
	SW Reset	Contents of memory is set randomly
HW Reset		Contents of memory is set randomly
Flow Chart		

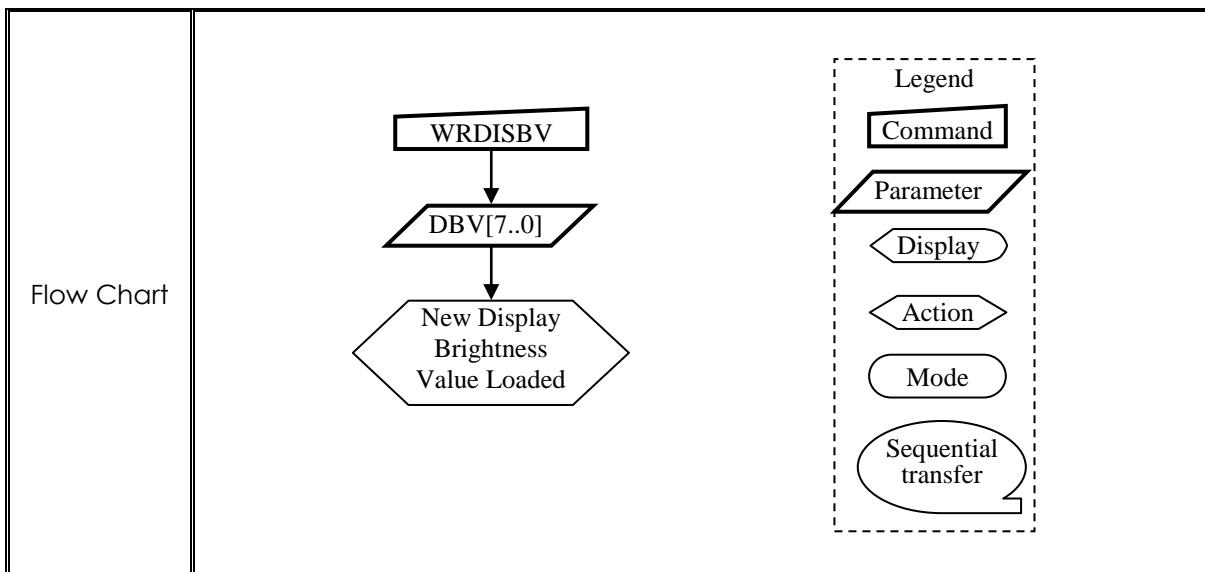
9.2.31 Memory Read Continue (3Eh)

3EH		RAMRDC (Memory Read Continue)																				
	Write/Read	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	HEX												
Command	Write	0	0	1	1	1	1	1	0	3E												
1 st Parameter	Read	D1 23	D1 22	D1 21	D1 20	D1 19	D1 18	D1 17	D1 16	0000 .. FFFF												
:	Read	Dx 7	Dx 6	Dx 5	Dx 4	Dx 3	Dx 2	Dx 1	Dx 0	0000 .. FFFF												
(n+1) th parameter	Read	Dn 7	Dn 6	Dn 5	Dn 4	Dn 3	Dn 2	Dn 1	Dn 0	0000 .. FFFF												
Description	<p>This command is used to transfer data from frame memory to MCU, if there is wanted to continue memory write after "9.2.22 Memory Read (2Eh)" command.</p> <p>This command makes no change to the other driver status.</p> <p>When this command is accepted, the column register and the page register are not reset to the Start Column/Start Page positions as it has been done on "9.2.22 Memory Read (2Eh)" command.</p> <p>Then D[23:0] is read back from the frame memory and the column register and the page register incremented as in Table 51: Column and Page Counter Control.</p> <p>Frame Read can be stopped by sending any other command.</p> <p>See section "8.1.7 Display Module Data Colour Coding" for colour coding.</p>																					
Restriction	No access in the frame memory in Sleep In mode.																					
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>No</td></tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	No
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
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Partial Mode On, Idle Mode On, Sleep Out	Yes																					
Sleep In	No																					
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr> <tr> <td>SW Reset</td><td>Contents of memory is set randomly</td></tr> <tr> <td>HW Reset</td><td>Contents of memory is set randomly</td></tr> </tbody> </table>										Status	Default Value	Power On Sequence	Contents of memory is set randomly	SW Reset	Contents of memory is set randomly	HW Reset	Contents of memory is set randomly				
Status	Default Value																					
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HW Reset	Contents of memory is set randomly																					



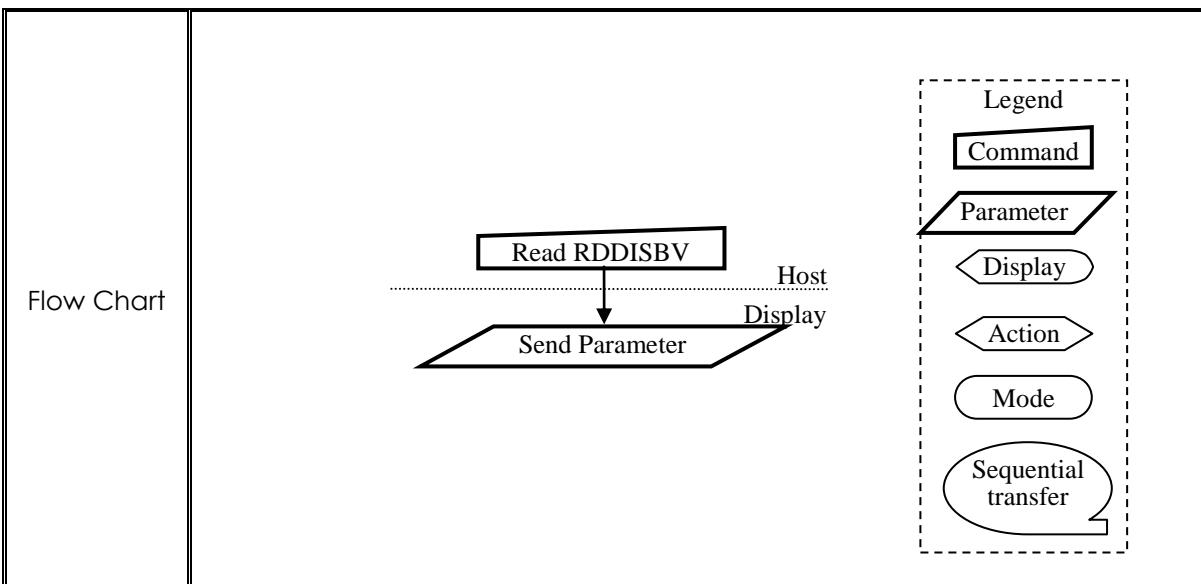
9.2.32 Write Display Brightness (51h)

51H		WRDISBV (Write Display Brightness)																					
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	Write	0	1	0	1	0	0	0	1	51													
Parameter	Write	DBV 7	DBV 6	DBV 5	DBV 4	DBV 3	DBV 2	DBV 1	DBV 0	00 .. FF													
Description	<p>This command is used to adjust the brightness value of the display.</p> <p>It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification.</p> <p>In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.</p> <p>See chapter "8.13.1.2 Brightness Control Block".</p>																						
Restriction	The display supplier cannot use this command for tuning (e.g. factory tuning, etc.), because this command is only for Nokia.																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																						
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Normal Mode On, Idle Mode On, Sleep Out	Yes																						
Partial Mode On, Idle Mode Off, Sleep Out	Yes																						
Partial Mode On, Idle Mode On, Sleep Out	Yes																						
Sleep In	Yes																						
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Status	Default Value																						
Power On Sequence	00 _{HEX}																						
SW Reset	00 _{HEX}																						
HW Reset	00 _{HEX}																						



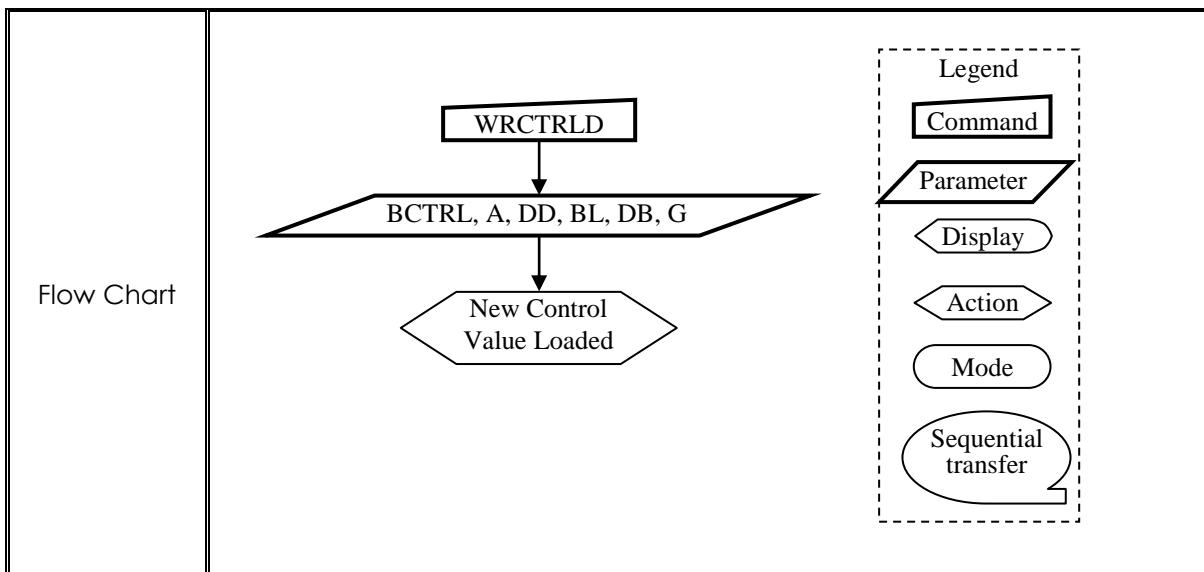
9.2.33 Read Display Brightness Value (52h)

52H		RDDISBV (Read Display Brightness Value)																				
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	Write	0	1	0	1	0	0	1	0	52												
Parameter	Read	DBV 7	DBV 6	DBV 5	DBV 4	DBV 3	DBV 2	DBV 1	DBV 0	Xx												
Description	<p>This command returns the brightness value of the display.</p> <p>It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification.</p> <p>In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.</p> <p>See chapters: "8.13.1.2 Brightness Control Block", Error! Reference source not found. Error! Reference source not found." and "0 Write Display Brightness (51h)".</p>																					
Restrictions																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																					
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Status	Default Value																					
Power On Sequence	00 _{HEX}																					
SW Reset	00 _{HEX}																					
HW Reset	00 _{HEX}																					

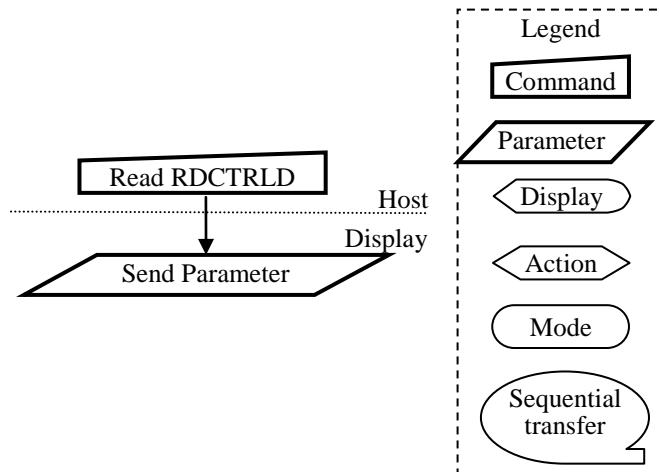


9.2.34 Write CTRL Display (53h)

53H		WRCTRLD (Write Control Display)																				
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	Write	0	1	0	1	0	0	1	1	53												
Parameter	Write	X	X	BCTRL	0	DD	BL	0	0	00 .. FF												
Description	<p>This command is used to control brightness settings.</p> <p><u>BCTRL: Brightness Control Block On/Off</u>, This bit is always used to switch brightness for display '0' = Off (Brightness registers are 00h) '1' = On (Brightness registers are active, according to the other parameters.) Needs to be 1 to enable display brightness.</p> <p><u>DD: Display Dimming</u> '0' = Display Dimming is off '1' = Display Dimming is on</p> <p><u>BL: Brightness /backligh On/Off</u> '0' = Off (Completely turn off backlight circuit. Control lines must be low.) '1' = On, Needs to be 1 to enable display brightness.</p>																					
Description	<p>When BL bit change from "On" to "Off", backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected.</p> <p>X = Don't care.</p>																					
Restriction																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																					
Power On Sequence	00 _{HEX}																					
SW Reset	00 _{HEX}																					
HW Reset	00 _{HEX}																					

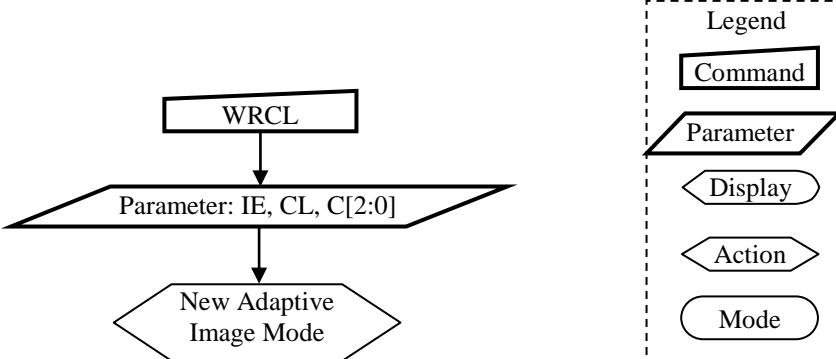


9.2.35 Read CTRL Value Display (54h)

54H		RDCTRLD (Read Control Value Display)																					
		Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command		Write	0	1	0	1	0	1	0	0	54												
Parameter		Read	0	0	BCTRL		DD	BL			xx												
Description	This command returns brightness control values, see chapter: "9.2.34 Write CTRL Display (53h)".																						
Restrictions																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Normal Mode On, Idle Mode Off, Sleep Out	Yes																						
Normal Mode On, Idle Mode On, Sleep Out	Yes																						
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Sleep In	Yes																						
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Status	Default Value																						
Power On Sequence	00 _{HEX}																						
SW Reset	00 _{HEX}																						
HW Reset	00 _{HEX}																						
Flow Chart	 <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																						

9.2.36 Write Current limit (55h)

55H		WRCL (Write Current limit)									
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	Write	0	1	0	1	0	1	0	1	55	
Parameter	Write	X	X	X	X	X	X	C1	C0	xx	
Description	<p>This command is used to set parameters for image content based adaptive brightness control functionality.</p> <p>This command is used to set parameters for Automatic Current Limit functionality. There is possible to use 2 different modes for ACL functionality, which are defined on a table below.</p> <p>D[7:0]</p> <p>00h ACL Off: function off</p> <p>10h ACL On (80%) ACL maximum brightness level is 80%</p> <p>11h ACL On (70%) ACL maximum brightness level is 70%</p> <p>12h ACL On (60%) ACL maximum brightness level is 60%</p> <p>NOTE: due to ACL operation nature, the most aggressive ACL mode will decrease the display refresh rate down to ~40Hz. The RR change is dependent on the content.</p>										
Restriction											

Register Availability	<table border="1"><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Normal Mode On, Idle Mode On, Sleep Out	Yes													
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Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
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Status	Default Value													
Power On Sequence	00 _{HEX}													
SW Reset	00 _{HEX}													
HW Reset	00 _{HEX}													
Flow Chart	 <p>WRCL</p> <p>Parameter: IE, CL, C[2:0]</p> <p>New Adaptive Image Mode</p> <p>Legend</p> <ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer													

9.2.37 Read Current limit (56h)

56H		RDCL (Read Current limit)									
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	Write	0	1	0	1	0	1	1	0	56	
Parameter	Read	0	0	0	0	0	0	C1	C0	xx	
Description	This command is used to read the settings for icurrent limit.										
Restrictions											
Register Availability	Status		Availability								
	Normal Mode On, Idle Mode Off, Sleep Out		Yes								
	Normal Mode On, Idle Mode On, Sleep Out		Yes								
	Partial Mode On, Idle Mode Off, Sleep Out		Yes								
	Partial Mode On, Idle Mode On, Sleep Out		Yes								
Default	Status		Default Value								
	Power On Sequence		00 _{HEX}								
	SW Reset		00 _{HEX}								
	HW Reset		00 _{HEX}								
Flow Chart	<pre> graph TD Host[Host] -- "Read RDCL" --> Display[Display] Display -- "Send Parameter" --> Host </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 										

9.2.38 Read Black/White Low Bits (70h)

70H		RDBWLB (Read Black/White Low Bits)																					
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	Write	0	1	1	1	0	0	0	0	70													
Parameter	Read	Bkx 1	Bkx 0	Bky 1	Bky 0	Wx 1	Wx 0	Wy 1	Wy 0	xx													
Description	This command returns the lowest bits of black and white color characteristics. Black: Bkx and Bky White: Wx and Wy See also section: "8.9 Display Panel Colour Characteristics".																						
Restriction																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Normal Mode On, Idle Mode On, Sleep Out	Yes																						
Partial Mode On, Idle Mode Off, Sleep Out	Yes																						
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Sleep In	Yes																						
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Status	Default Value																						
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SW Reset	XX _{HEX}																						
HW Reset	XX _{HEX}																						
Flow Chart	<p>The flow chart illustrates the interaction between the Host and the Display. The Host sends a parameter to the Display, which then processes it. The legend provides key symbols for interpreting the flowchart:</p> <ul style="list-style-type: none"> Command: Represented by a rectangle. Parameter: Represented by a diamond. Display: Represented by a parallelogram. Action: Represented by a triangle. Mode: Represented by an oval. Sequential transfer: Represented by an oval with a line extending from its bottom. 																						

May 18th, 2012

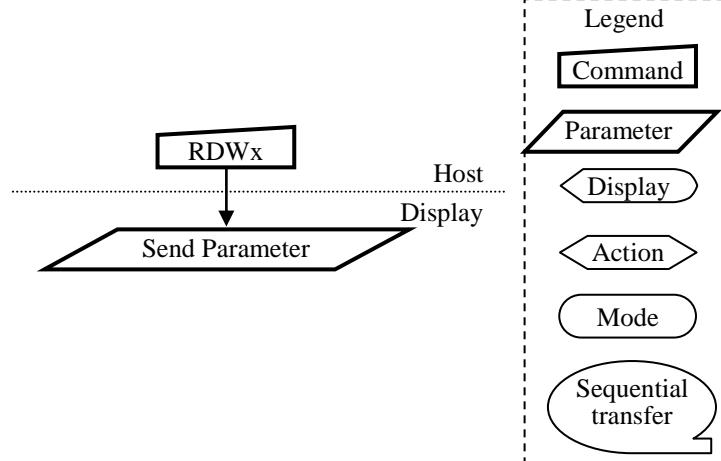
9.2.39 Read Bkx (71h)

71H		RDBkx (Read Bkx)																					
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	Write	0	1	1	1	0	0	0	1	71													
Parameter	Read	Bkx 9	Bkx 8	Bkx 7	Bkx 6	Bkx 5	Bkx 4	Bkx 3	Bkx 2	xx													
Description	This command returns the Bkx bits (Bkx[9:2]) of black color characteristics. See also section: "8.9 Display Panel Colour Characteristics".																						
Restriction																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																						
Power On Sequence	XX _{HEX}																						
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HW Reset	XX _{HEX}																						
Flow Chart	<p>The flow chart illustrates the interaction between the Host and the Display. An arrow labeled "Send Parameter" points from the Host to the Display. The "RDBkx" command is shown as a rectangle (Command) pointing to the "Send Parameter" arrow. The "Display" is represented by a parallelogram (Parameter).</p> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																						

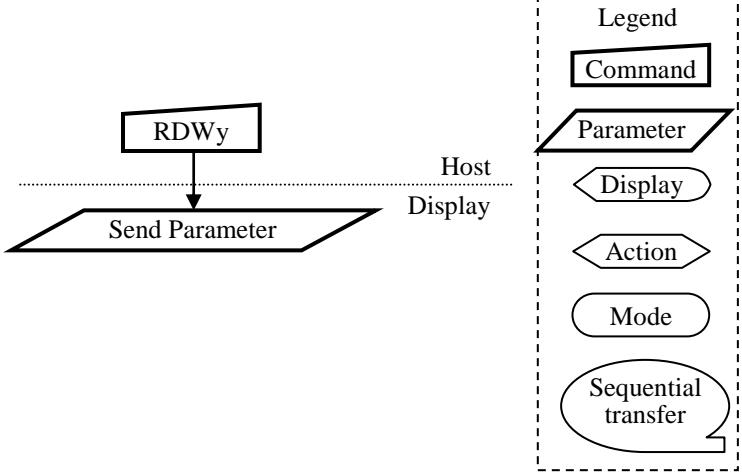
9.2.40 Read Bky (72h)

72H		RDBky (Read Bky)																					
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	Write	0	1	1	1	0	0	1	0	72													
Parameter	Read	Bky 9	Bky 8	Bky 7	Bky 6	Bky 5	Bky 4	Bky 3	Bky 2	xx													
Description	This command returns the Bky bits (Bky[9:2]) of black color characteristics. See also section: "8.9 Display Panel Colour Characteristics".																						
Restriction																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																						
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Normal Mode On, Idle Mode On, Sleep Out	Yes																						
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Partial Mode On, Idle Mode On, Sleep Out	Yes																						
Sleep In	Yes																						
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Status	Default Value																						
Power On Sequence	XX _{HEX}																						
SW Reset	XX _{HEX}																						
HW Reset	XX _{HEX}																						
Flow Chart	<pre> graph TD RDBky[RDBky] --> SendParam[/Send Parameter/] subgraph Legend [Legend] Command[Command] Parameter[Parameter] Display[Display] Action[Action] Mode[Mode] Sequential[Sequential transfer] end SendParam --> Host[Host] Host --> Display[Display] </pre> <p>The flow chart illustrates the interaction between the Host and Display. It starts with the RDBky command being sent from the Host to the Display via a 'Send Parameter' path. A legend on the right side defines the symbols used in the flowchart: a rectangle for Command, a parallelogram for Parameter, a diamond for Display, a trapezoid for Action, an oval for Mode, and a rounded rectangle for Sequential transfer.</p>																						

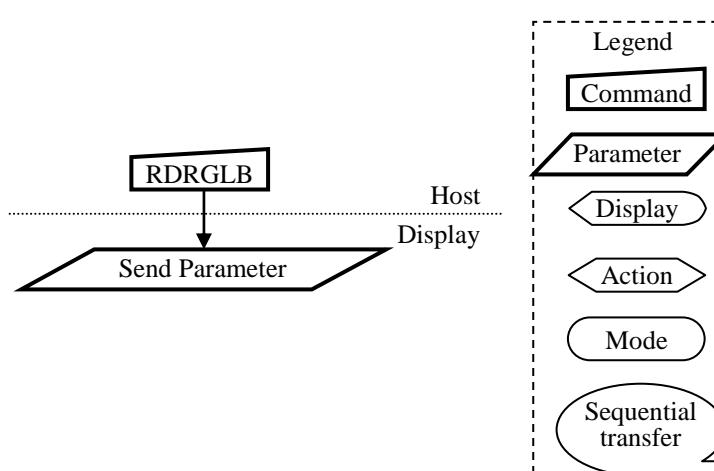
9.2.41 Read Wx (73h)

73H		RDWx (Read Wx)																				
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	Write	0	1	1	1	0	0	1	1	73												
Parameter	Read	Wx 9	Wx 8	Wx 7	Wx 6	Wx 5	Wx 4	Wx 3	Wx 2	xx												
Description	This command returns the Wx bits (Wx[9:2]) of white color characteristics. See also section: "8.9 Display Panel Colour Characteristics".																					
Restriction																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td> </tr> <tr> <td>Sleep In</td><td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																					
Power On Sequence	XX _{HEX}																					
SW Reset	XX _{HEX}																					
HW Reset	XX _{HEX}																					
Flow Chart	 <p>The flow chart illustrates the communication between the Host and the Display. An arrow labeled "Send Parameter" points from the Host to the Display. The Host sends a command (RDWx) to the Display. The legend defines the symbols used in the flow chart:</p> <ul style="list-style-type: none"> Command: Represented by a rectangle. Parameter: Represented by a diamond. Display: Represented by a left-pointing triangle. Action: Represented by a right-pointing triangle. Mode: Represented by an oval. Sequential transfer: Represented by a double-headed oval. 																					

9.2.42 Read Wy (74h)

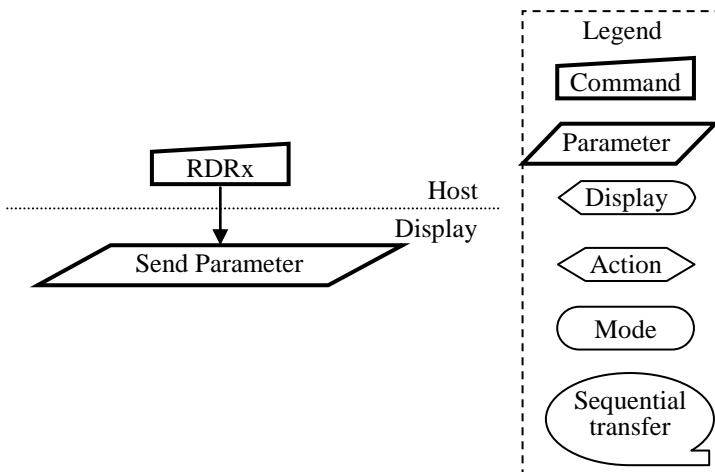
74H		RDWy (Read Wy)																				
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	Write	0	1	1	1	0	1	0	0	74												
Parameter	Read	Wy 9	Wy 8	Wy 7	Wy 6	Wy 5	Wy 4	Wy 3	Wy 2	xx												
Description	This command returns the Wy bits (Wy[9:2]) of white color characteristics. See also section: "8.9 Display Panel Colour Characteristics".																					
Restriction																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																					
Power On Sequence	XX _{HEX}																					
SW Reset	XX _{HEX}																					
HW Reset	XX _{HEX}																					
Flow Chart	 <p>The flow chart illustrates the transmission of the RDWy command. It starts with the 'RDWy' command being sent from the Host to the Display. This is represented by a rectangular box labeled 'RDWy' with an arrow pointing down to a trapezoidal box labeled 'Send Parameter'. To the right of the flow, a legend provides key symbols for interpreting the shapes in the diagram:</p> <ul style="list-style-type: none"> Command: Represented by a rectangle. Parameter: Represented by a parallelogram. Display: Represented by a left-pointing triangle. Action: Represented by a right-pointing triangle. Mode: Represented by an oval. Sequential transfer: Represented by a double-headed oval. 																					

9.2.43 Read Red/Green Low bits (75h)

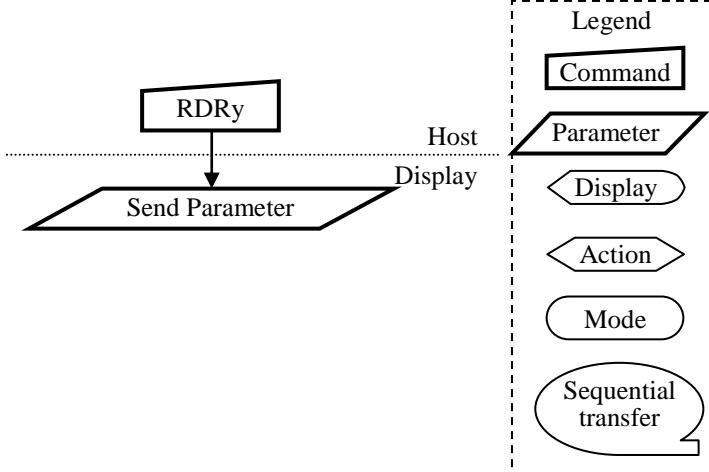
75H		RDRGLB (Read Red/Green Low Bits)																					
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	Write	0	1	1	1	0	1	0	1	75													
Parameter	Read	Rx 1	Rx 0	Ry 1	Ry 0	Gx 1	Gx 0	Gy 1	Gy 0	xx													
Description	This command returns the lowest bits of red and green color characteristics. Red: Rx and Ry Green: Gx and Gy See also section: "8.9 Display Panel Colour Characteristics".																						
Restriction																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																						
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																						
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Status	Default Value																						
Power On Sequence	XX _{HEX}																						
SW Reset	XX _{HEX}																						
HW Reset	XX _{HEX}																						
Flow Chart	 <p>The flowchart illustrates the transmission of the RDRGLB command from the Host to the Display. The command is sent as a single parameter. The legend provides key symbols for interpreting the flowchart elements:</p> <ul style="list-style-type: none"> Command: Represented by a rectangle. Parameter: Represented by a diamond. Display: Represented by a left-pointing triangle. Action: Represented by a right-pointing triangle. Mode: Represented by an oval. Sequential transfer: Represented by a double oval. 																						

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9.2.44 Read Rx (76h)

76H		RDRx (Read Rx)																					
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	Write	0	1	1	1	0	1	1	0	76													
Parameter	Read	Rx 9	Rx 8	Rx 7	Rx 6	Rx 5	Rx 4	Rx 3	Rx 2	xx													
Description	This command returns the Rx bits (Rx[9:2]) of red color characteristics. See also section: "8.9 Display Panel Colour Characteristics".																						
Restriction																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td> </tr> <tr> <td>Sleep In</td><td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																						
Normal Mode On, Idle Mode On, Sleep Out	Yes																						
Partial Mode On, Idle Mode Off, Sleep Out	Yes																						
Partial Mode On, Idle Mode On, Sleep Out	Yes																						
Sleep In	Yes																						
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>XX_{HEX}</td> </tr> <tr> <td>SW Reset</td><td>XX_{HEX}</td> </tr> <tr> <td>HW Reset</td><td>XX_{HEX}</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	XX _{HEX}	SW Reset	XX _{HEX}	HW Reset	XX _{HEX}				
Status	Default Value																						
Power On Sequence	XX _{HEX}																						
SW Reset	XX _{HEX}																						
HW Reset	XX _{HEX}																						
Flow Chart	 <p>The flow chart illustrates the communication sequence. It starts with a 'RDRx' command (rectangle) being sent from the 'Host' to the 'Display'. This is followed by a 'Send Parameter' action (trapezoid). A legend on the right side defines the symbols used in the flow chart:</p> <ul style="list-style-type: none"> Command: Rectangle Parameter: Trapezoid Display: Left-pointing arrow Action: Right-pointing arrow Mode: Oval Sequential transfer: Double-headed oval 																						

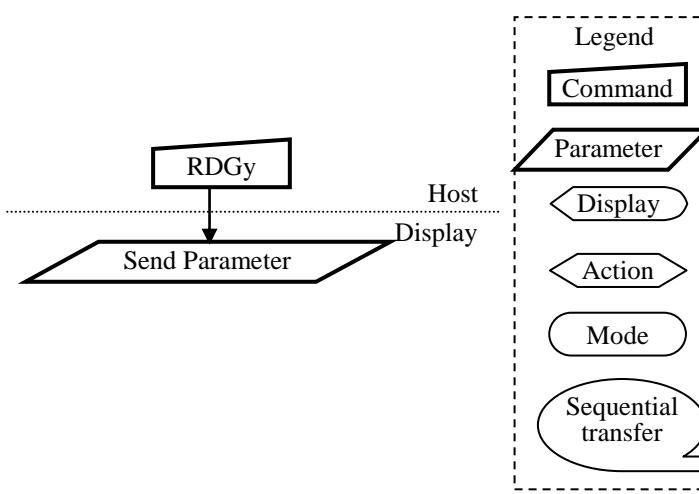
9.2.45 Read Ry (77h)

77H		RDRy (Read Ry)																				
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	Write	0	1	1	1	0	1	1	1	77												
Parameter	Read	Ry 9	Ry 8	Ry 7	Ry 6	Ry 5	Ry 4	Ry 3	Ry 2	xx												
Description	This command returns the Ry bits (Ry[9:2]) of red color characteristics. See also section: "8.9 Display Panel Colour Characteristics".																					
Restriction																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																					
Power On Sequence	XX _{HEX}																					
SW Reset	XX _{HEX}																					
HW Reset	XX _{HEX}																					
Flow Chart	 <p>The flow chart illustrates the communication between the Host and the Display. An arrow labeled "RDRy" points from the Host to the Display. The Host is represented by a rectangle, and the Display is represented by a trapezoid labeled "Send Parameter". To the right of the flow chart is a legend enclosed in a dashed box:</p> <ul style="list-style-type: none"> Command (rectangle) Parameter (triangle) Display (left-pointing triangle) Action (right-pointing triangle) Mode (oval) Sequential transfer (double-headed oval) 																					

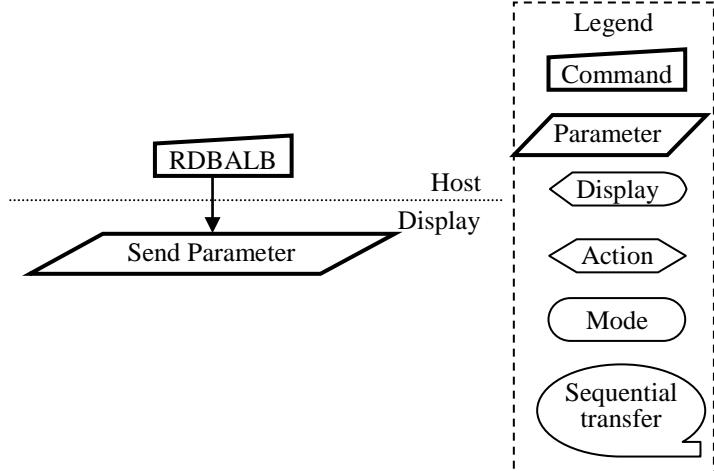
9.2.46 Read Gx (78h)

78H		RDGx (Read Gx)																					
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	Write	0	1	1	1	1	0	0	0	78													
Parameter	Read	Gx 9	Gx 8	Gx 7	Gx 6	Gx 5	Gx 4	Gx 3	Gx 2	xx													
Description	This command returns the Gx bits (Gx[9:2]) of green color characteristics. See also section: "8.9 Display Panel Colour Characteristics".																						
Restriction																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																						
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Status	Default Value																						
Power On Sequence	XX _{HEX}																						
SW Reset	XX _{HEX}																						
HW Reset	XX _{HEX}																						
Flow Chart	<p>The flow chart illustrates the communication between the Host and the Display. The Host sends a command (RDGx) to the Display, which then performs a sequential transfer (Send Parameter). The legend provides key symbols for interpreting the flowchart:</p> <ul style="list-style-type: none"> Command: Represented by a rectangle. Parameter: Represented by a double-headed arrow. Display: Represented by a left-pointing arrow. Action: Represented by a right-pointing arrow. Mode: Represented by an oval. Sequential transfer: Represented by an oval containing a diagonal line. 																						

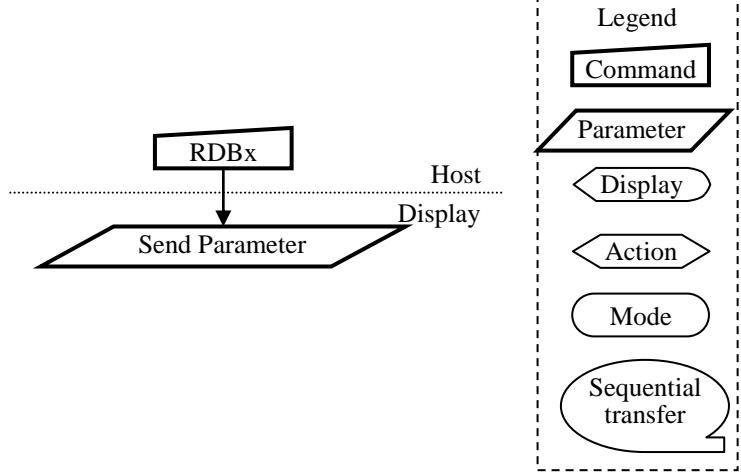
9.2.47 Read Gy (79h)

79H		RDGy (Read Gy)																					
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	Write	0	1	1	1	1	0	0	1	79													
Parameter	Read	Gy 9	Gy 8	Gy 7	Gy 6	Gy 5	Gy 4	Gy 3	Gy 2	xx													
Description	This command returns the Gy bits (Gy[9:2]) of green color characteristics. See also section: "8.9 Display Panel Colour Characteristics".																						
Restriction																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																						
Power On Sequence	XX _{HEX}																						
SW Reset	XX _{HEX}																						
HW Reset	XX _{HEX}																						
Flow Chart	 <p>The flow chart illustrates the communication between the Host and the Display. The Host sends the RDGy command to the Display, which then performs a sequential transfer of parameters. The legend provides key symbols for identifying the different components and their interactions.</p>																						

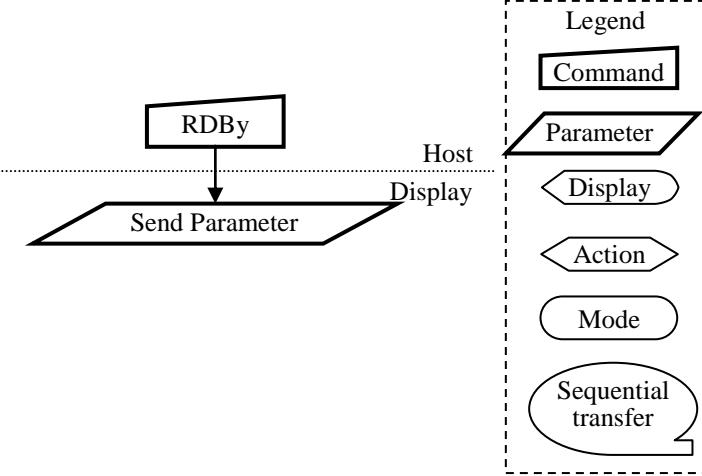
9.2.48 Read Blue/AColour Low Bits (7Ah)

7AH		RDBALB (Read Blue/AColour Low Bits)																					
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	Write	0	1	1	1	1	0	1	0	7A													
Parameter	Read	Bx 1	Bx 0	By 1	By 0	Ax 1	Ax 0	Ay 1	Ay 0	Xx													
Description	This command returns the lowest bits of blue and A color characteristics. Blue: Bx and By A: Ax and Ay If A is not used Ax[1:0] and Ay[1:0] bits are set to '0's. See also section: "8.9 Display Panel Colour Characteristics".																						
Restriction																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																						
Power On Sequence	XX _{HEX}																						
SW Reset	XX _{HEX}																						
HW Reset	XX _{HEX}																						
Flow Chart	 <p>The flow chart illustrates the interaction between the Host and the Display. The Host sends a parameter labeled "Send Parameter" to the Display. The RDBALB command is shown above the parameter. A legend on the right side defines the symbols used in the flow chart:</p> <ul style="list-style-type: none"> Command: Rectangle Parameter: Diamond Display: Left-pointing triangle Action: Right-pointing triangle Mode: Oval Sequential transfer: Double oval 																						

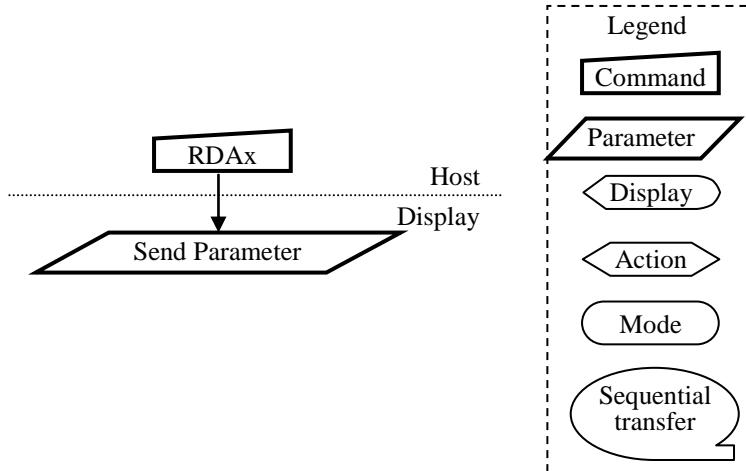
9.2.49 Read Bx (7Bh)

7BH		RDBx (Read Bx)																					
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	Write	0	1	1	1	1	0	1	1	7B													
Parameter	Read	Bx 9	Bx 8	Bx 7	Bx 6	Bx 5	Bx 4	Bx 3	Bx 2	xx													
Description	This command returns the Bx bits (Bx[9:2]) of blue color characteristics. See also section: "8.9 Display Panel Colour Characteristics".																						
Restriction																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																						
Power On Sequence	XX _{HEX}																						
SW Reset	XX _{HEX}																						
HW Reset	XX _{HEX}																						
Flow Chart	 <p>The flow chart illustrates the interaction between the Host and the Display. An arrow labeled "Send Parameter" points from the Host to the Display. The "RDBx" command is shown originating from the Host and being sent to the Display. The legend on the right side of the chart defines the symbols used in the flowchart:</p> <ul style="list-style-type: none"> Command: Represented by a rectangle. Parameter: Represented by a parallelogram. Display: Represented by a left-pointing arrow. Action: Represented by a right-pointing arrow. Mode: Represented by an oval. Sequential transfer: Represented by a double-headed oval. 																						

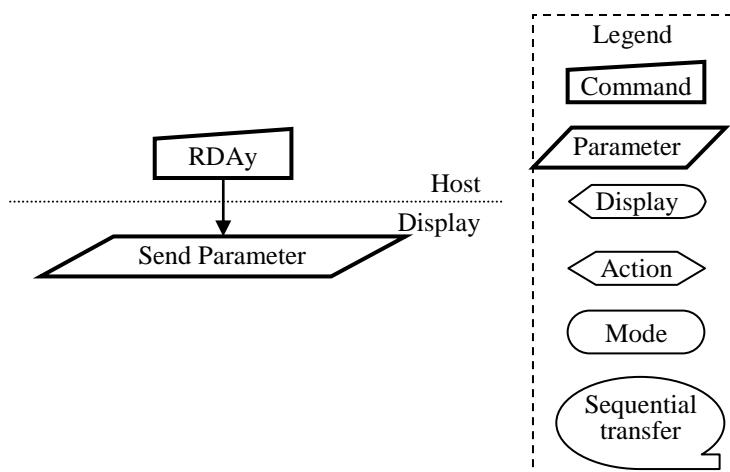
9.2.50 Read By (7Ch)

7CH		RDBy (Read By)																				
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	Write	0	1	1	1	1	1	0	0	7C												
Parameter	Read	By 9	By 8	By 7	By 6	By 5	By 4	By 3	By 2	xx												
Description	This command returns the By bits (By[9:2]) of blue color characteristics. See also section: "8.9 Display Panel Colour Characteristics".																					
Restriction																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																					
Power On Sequence	XX _{HEX}																					
SW Reset	XX _{HEX}																					
HW Reset	XX _{HEX}																					
Flow Chart	 <p>The flow chart illustrates the interaction between the Host and the Display. The Host initiates the process by sending a 'RDBy' command to the Display. The Display then responds by sending a parameter back to the Host. A legend on the right side of the chart defines the symbols used in the flowchart:</p> <ul style="list-style-type: none"> Command: Represented by a rectangle. Parameter: Represented by a triangle pointing towards the Host. Display: Represented by a triangle pointing away from the Host. Action: Represented by a right-pointing triangle. Mode: Represented by an oval. Sequential transfer: Represented by a double-headed arrow. 																					

9.2.51 Read Ax (7Dh)

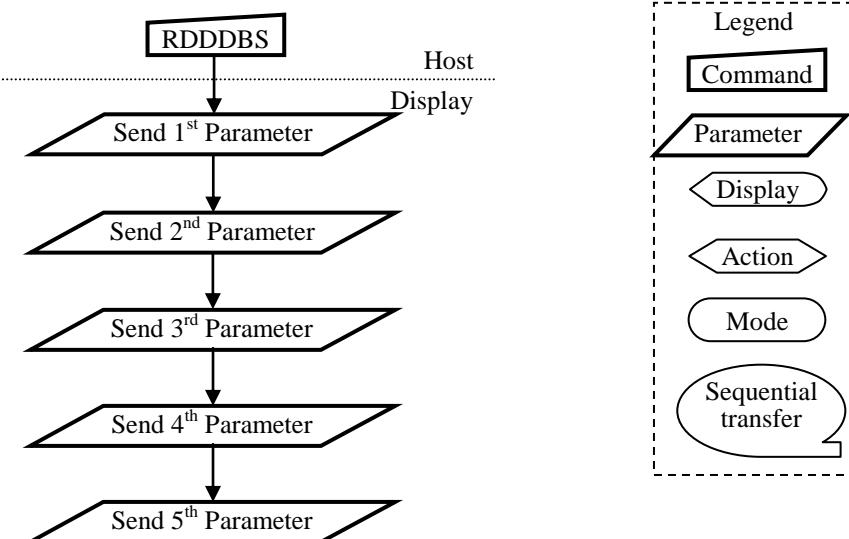
7DH		RDAX (Read Ax)																					
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	Write	0	1	1	1	1	1	0	1	7D													
Parameter	Read	Ax 9	Ax 8	Ax 7	Ax 6	Ax 5	Ax 4	Ax 3	Ax 2	xx													
Description	This command returns the Ax bits (Ax[9:2]) of A color characteristics. Ax[9:2] are set to '0's if they are not used. See also section: "8.9 Display Panel Colour Characteristics".																						
Restriction																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																						
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Status	Default Value																						
Power On Sequence	XX _{HEX}																						
SW Reset	XX _{HEX}																						
HW Reset	XX _{HEX}																						
Flow Chart	 <p>The flow chart illustrates the interaction between the Host and the Display. The Host sends a parameter, specifically the RDAX command, to the Display. The legend provides key symbols for interpreting the flowchart elements:</p> <ul style="list-style-type: none"> Command: Represented by a rectangle. Parameter: Represented by a trapezoid. Display: Represented by a parallelogram. Action: Represented by a diamond. Mode: Represented by an oval. Sequential transfer: Represented by an oval containing an arrow pointing to the right. 																						

9.2.52 Read Ay (7Eh)

7EH		RDAy (Read Ay)																					
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	Write	0	1	1	1	1	1	1	0	7E													
Parameter	Read	Ay 9	Ay 8	Ay 7	Ay 6	Ay 5	Ay 4	Ay 3	Ay 2	xx													
Description	This command returns the Ay bits (Ay[9:2]) of A color characteristics. Ay[9:2] are set to '0's if they are not used. See also section: "8.9 Display Panel Colour Characteristics".																						
Restriction																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																						
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Normal Mode On, Idle Mode On, Sleep Out	Yes																						
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Status	Default Value																						
Power On Sequence	XX _{HEX}																						
SW Reset	XX _{HEX}																						
HW Reset	XX _{HEX}																						
Flow Chart	 <p>The flow chart illustrates the interaction between the Host and the Display. The Host sends a parameter to the Display, which then processes it. The legend provides key symbols for interpreting the flowchart elements:</p> <ul style="list-style-type: none"> Command: Represented by a rectangle. Parameter: Represented by a parallelogram. Display: Represented by a left-pointing arrow. Action: Represented by a right-pointing arrow. Mode: Represented by an oval. Sequential transfer: Represented by a speech bubble. 																						

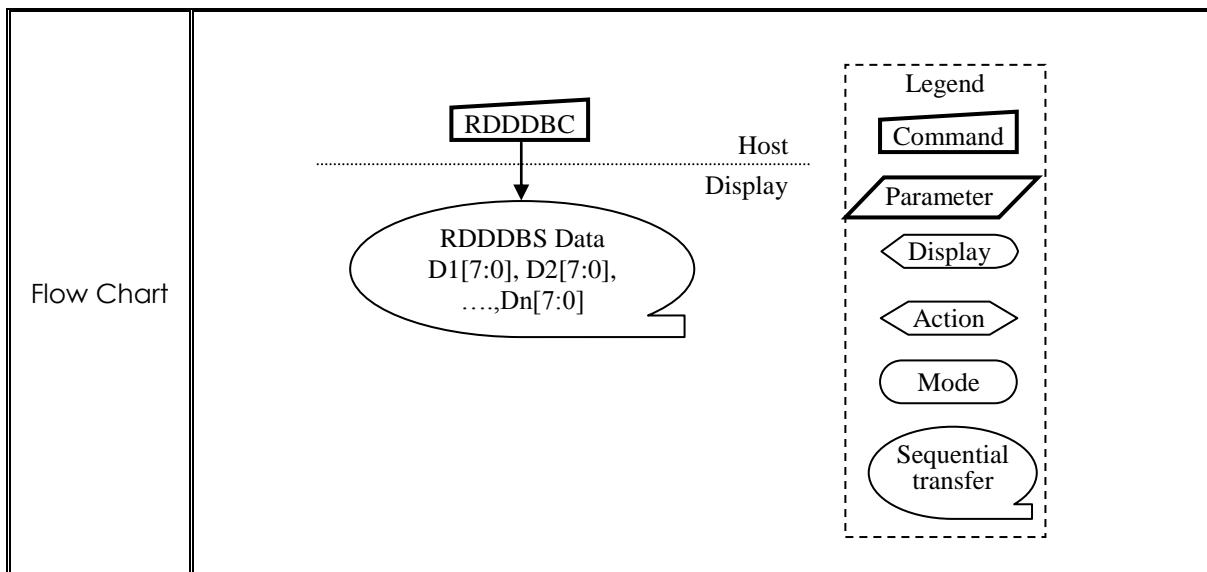
9.2.53 Read DDB Start (A1h)

A1H		RDDDBS (Read DDB Start)																					
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	Write	1	0	1	0	0	0	0	1	A1													
1 st Parameter	Read	S 7	S 6	S 5	S 4	S 3	S 2	S 1	S 0	0000 .. FFFF													
2 nd Parameter	Read	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8	0000 .. FFFF													
3 rd Parameter	Read	MR 7	MR 6	Mr 5	MR 4	MR 3	MR 2	MR 1	MR 0	0000 .. FFFF													
4 th Parameter	Read	MR 15	MR 14	MR 13	MR 12	MR 11	MR 10	MR 9	MR 8	0000 .. FFFF													
5 th Parameter	Read	1	1	1	1	1	1	1	1	FF													
Description	<p>This command returns supplier identification and display module model/revision information.</p> <p>Note: This information is not the same what "9.2.57 Read ID1 (DAh)", "9.2.58 Read ID2 (DBh)" and "9.2.59 Read ID3 (DCh)" commands are returning.</p> <p>This read sequence can be interrupted by any command and it can be continued by "9.2.54 Read DDB Continue (A8h)" command when the first parameter, what has been transferred, is the parameter, which has not been sent e.g. RDDDBS => 1st parameter has been sent => 2nd Parameter has been sent => interrupt => RDDDBC => 3rd parameter of the RDDDBS has been sent.</p> <p>Parameter Value Note 1st S[7:0] 01h 2nd S[15:8] 0Bh 3rd MR[7:0] xxh Display module version 4th MR[15:8] 80h Display module</p>																						
Restriction																							
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Status	Default Value								
Power On Sequence	XX _{HEX}								
SW Reset	XX _{HEX}								
HW Reset	XX _{HEX}								
<p>Flow Chart</p>  <pre>graph TD; RDDDBS[RDDDBS] --> Send1[/Send 1st Parameter/]; Send1 --> Send2[/Send 2nd Parameter/]; Send2 --> Send3[/Send 3rd Parameter/]; Send3 --> Send4[/Send 4th Parameter/]; Send4 --> Send5[/Send 5th Parameter/];</pre> <p>Legend</p> <ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer									

9.2.54 Read DDB Continue (A8h)

A8H		RDDDBC (Read DDB Continue)																				
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	Write	1	0	1	0	1	0	0	0	A8												
1 st Parameter	Read	D1 7	D1 6	D1 5	D1 4	D1 3	D1 2	D1 1	D1 0	00 .. FF												
:	Read	Dx 7	Dx 6	Dx 5	Dx 4	Dx 3	Dx 2	Dx 1	Dx 0	00 .. FF												
(n+1) th Parameter	Read	Dn 7	Dn 6	Dn 5	Dn 4	Dn 3	Dn 2	Dn 1	Dn 0	00 .. FF												
Description	This command returns supplier's identification and display module model/revision information from the point where RDDDBS command was interrupted by an other command e.g. RDDDBS was interrupted after 3 rd parameter (S[15:8]). The first parameter (D1[7:0]), what RDDDBC is returning, is S[7:0]. See also section "9.2.53 Read DDB Start (A1h)".																					
Restriction																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																					
Power On Sequence	XX _{HEX}																					
SW Reset	XX _{HEX}																					
HW Reset	XX _{HEX}																					



9.2.55 Read First Checksum (AAh)

AAH		RDFCS (Read First Checksum)																				
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	Write	1	0	1	0	1	0	1	0	AA												
Parameter	Read	FCS 7	FCS 6	FCS 5	FCS 4	FCS 3	FCS 2	FCS 1	FCS 0	xx												
Description	This command returns the first checksum what has been calculated from Nokia's area registers and the frame memory after the write access to those registers and/or frame memory has been done.																					
Restriction	It will be necessary to wait 150ms after there is the last write access on Nokia area registers before there can read this checksum value.																					
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																					
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Flow Chart	<p>The flow chart illustrates the interaction between the Host and the Display. A rectangular box labeled "RDFCS" is positioned above a dashed horizontal line. Below this line, a trapezoidal shape represents the "Display". An arrow points from the "RDFCS" box down to the "Display" trapezoid, with the text "Send FCS[7:0]" written below the arrow. To the right of the flow chart is a legend enclosed in a dashed box:</p> <ul style="list-style-type: none"> Command (represented by a rectangle) Parameter (represented by a parallelogram) Display (represented by a trapezoid) Action (represented by a diamond) Mode (represented by an oval) Sequential transfer (represented by an oval with a curved arrow) 																					

May 18th, 2012

9.2.56 Read Continue Checksum (AFh)

AFH	RDCCS (Read Continue Checksum)																					
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	Write	1	0	1	0	1	1	1	1	AF												
Parameter	Read	CCS 7	CCS 6	CCS 5	CCS 4	CCS 3	CCS 2	CCS 1	CCS 0	xx												
Description	This command returns the continue checksum what has been calculated continuously after the first checksum has calculated from Nokia's area registers and the frame memory after the write access to those registers and/or frame memory has been done.																					
Restriction	It will be necessary to wait 300ms after there is the last write access on Nokia area registers before there can read this checksum value in the first time.																					
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																					
Power On Sequence	00 _{HEX}																					
SW Reset	00 _{HEX}																					
HW Reset	00 _{HEX}																					
Flow Chart	<p>The flow chart illustrates the RDCCS command sequence. It starts with a rectangular box labeled "RDCCS". An arrow points from this box down to a trapezoidal box labeled "Send CCS[7:0]". To the right of the flow chart is a legend enclosed in a dashed box, defining six symbols: <ul style="list-style-type: none"> Command: represented by a rectangle. Parameter: represented by a rectangle. Display: represented by a left-pointing triangle. Action: represented by a right-pointing triangle. Mode: represented by an oval. Sequential transfer: represented by an oval containing a diagonal line. </p>																					

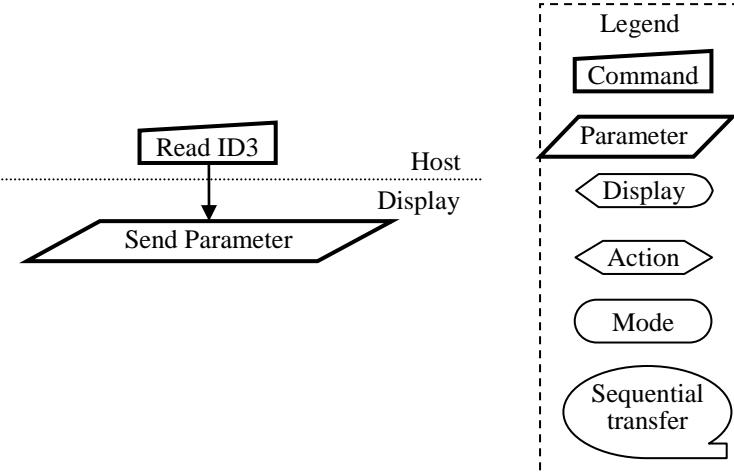
9.2.57 Read ID1 (DAh)

DAH	RDID1 (Read ID1)																					
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	Write	1	1	0	1	1	0	1	0	DA												
Parameter	Read	xx																				
Description	This read byte identifies the display module's manufacturer which is FEhex																					
Restriction																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																					
Power On Sequence	XX _{HEX}																					
SW Reset	XX _{HEX}																					
HW Reset	XX _{HEX}																					
Flow Chart	<p>The flowchart illustrates the interaction between the Host and the Display. It starts with a 'Read ID1' command from the Host, which triggers a 'Send Parameter' action from the Display. The legend on the right defines the symbols used in the flowchart.</p> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																					

9.2.58 Read ID2 (DBh)

DBH	RDID2 (Read ID2)																								
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
Command	Write	1	1	0	1	1	0	1	1	DB															
Parameter	Read	1	V6	V5	V4	V3	V2	V1	V0	80 ... FF															
Description	<p>This read byte is used to track the display module/driver version. It is defined by display supplier (with Nokia's agreement) and changes each time a revision is made to the display, material or construction specifications. See Table:</p> <table border="1"> <thead> <tr> <th>ID Byte Value V[6...0]</th> <th>Version</th> <th>Changes</th> </tr> </thead> <tbody> <tr> <td>80h</td> <td></td> <td></td> </tr> <tr> <td>81h</td> <td></td> <td></td> </tr> <tr> <td></td> <td></td> <td></td> </tr> <tr> <td></td> <td></td> <td></td> </tr> </tbody> </table>										ID Byte Value V[6...0]	Version	Changes	80h			81h								
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Status	Default Value																								
Power On Sequence	See Description																								
SW Reset	See Description																								
HW Reset	See Description																								
Flow Chart	<pre> graph TD Host[Host] -- "Read ID2" --> Display[Display] Display -- "Send Parameter" --> Host </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																								

9.2.59 Read ID3 (DCh)

DCH	RDID3 (Read ID3)																					
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	Write	1	1	0	1	1	1	0	0	DC												
Parameter	Read	xx																				
Description	This read byte identifies the display module/driver. It is specified by Nokia and for this display module project module is defined as 86 _{HEX} .																					
Restriction																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																					
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SW Reset	XX _{HEX}																					
HW Reset	XX _{HEX}																					
Flow Chart	 <p>The flowchart illustrates the interaction between the Host and the Display. The Host initiates a 'Read ID3' command, which is received by the Display. In response, the Display sends a 'Send Parameter' message back to the Host. A legend on the right side of the chart provides a key for the symbols used in the flowchart.</p>																					

10 Display Module Default Position

The default position (display driver, glass, filter order, etc.) of the display module is always as follow, when MADCTL's (36h) parameter is 00h. The colour filter order is always RGB (if colour filters are used).

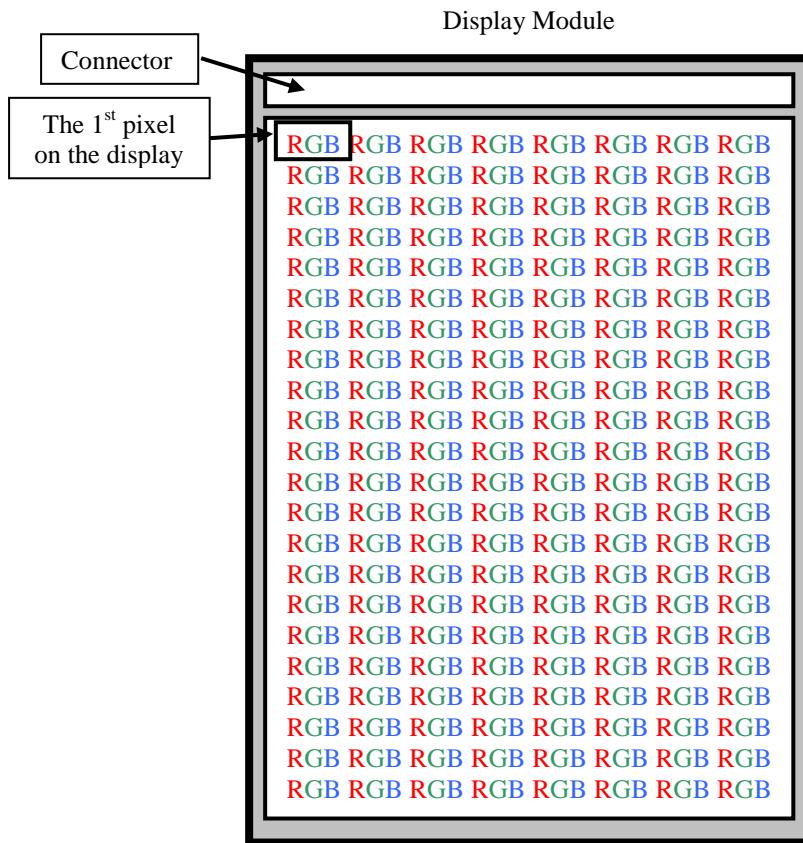


Figure 138: Display Module Default Position

10.1.1.1 Example display power on script

Following example pseudo code minimum script can be used to power on the panel.

- Enable Vddi
- Enable VPNL
- Issue Reset (> 10us pulse) or release reset from low to high
- SLPOUT
- wait 120ms
- Write register 51h , parameter EA h (100% brightness)
- Write register 53h, param 2C h (FFh works also)
- Issue DISPON command
- Send image data to panel