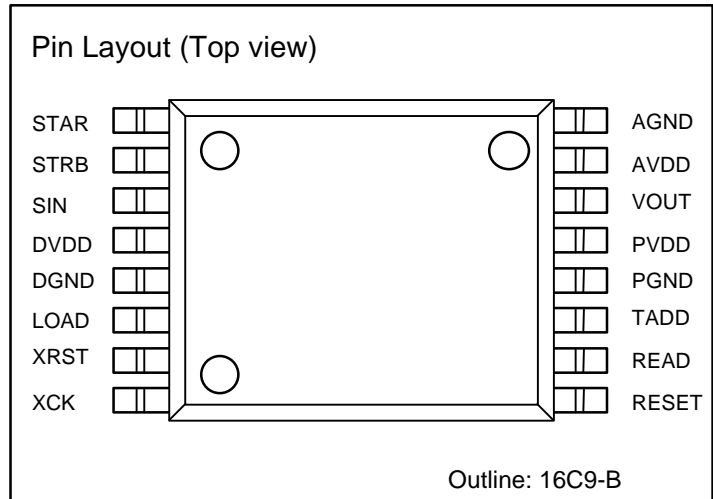## 1. Overview

M64283FP is a CMOS image sensor of 128 × 128 pixels, which supports an image-processing function and an analog signal calibration, a device that allows information compression and parallel processing like human retina. M64283FP can achieve high performance, a compact system and low power consumption for an image-processing apparatus.

Pin Layout (Top view)

STAR	AGND
STRB	AVDD
SIN	VOUT
DVDD	PVDD
DGND	PGND
LOAD	TADD
XRST	READ
XCK	RESET

Outline: 16C9-B

2. Features

◆ Single 5.0 V supply voltage

◆ Low power consumption (Typically 15 mw)

◆ Positive/Negative image output modes

◆ Edge enhancement and edge extraction output modes

◆ Vertical/Horizontal projection modes

◆ Random access mode

◆ Gain level adjustment mode

3. Application

Image capture devices, game machine interface devices, PC peripherals and any other consumer electronics devices

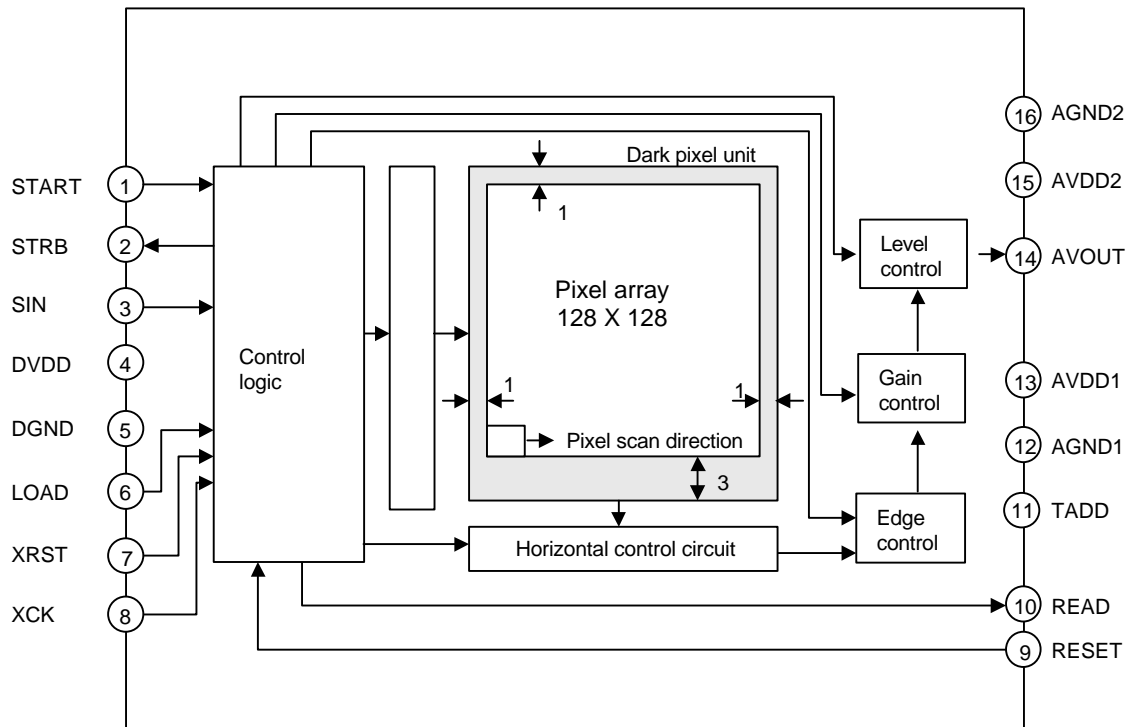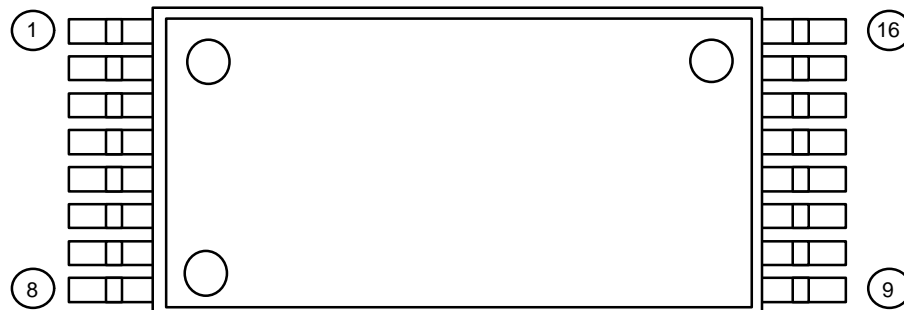Specifications and information in this document are subject to change without notice.
Ver. 2. 2. 3

4. Block Diagram

Figure 1. Block Diagram

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Ver. 2. 2. 3

5. PINOUT

Pin No.	Name	Pin function	Description
1	START	Start	Digital Input Image capture start signal Pulled down internally by 50 kΩ
2	STRB	Strobe	Digital Output Strobe signal for data output
3	SIN	Data input	Digital Input Register data input Pulled down internally by 50 kΩ
4	DVDD	Digital power supply	Power supply for control logic unit 5 V
5	DGND	Digital ground	Ground for control logic unit
6	LOAD	Data set	Digital Input Validate register data input Pulled down internally by 50 kΩ
7	XRST	Logic reset	Digital Input Reset of control logic unit Pull up by 50 kΩ Low active
8	XCK	System clock	Digital Input System clock Pulled down internally by 50 kΩ
9	RESET	Register reset	Digital Input Register reset Pulled up internally by 50 kΩ Low active
10	READ	Data output timing	Digital Output Indicate data output timing
11	TADD	Test Enable /Register address	Digital Input Test mode enable and Register address MSB Pulled up internally by 50 kΩ
12	AGND1	Analog ground	Analog ground of pixel analog unit
13	AVDD1	Analog power supply	Analog power supply of pixel analog unit 5 V
14	VOUT	Data output	Analog Output Image signal data output
15	AVDD2	Amplifier power supply	Analog power supply of analog unit 5 V
16	AGND2	Amplifier ground	Analog ground of analog unit

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6. Image Format

Parameter	Specifications
Optical size	1/4 "
Number of valid pixels	128(H) $\times$ 128(V)
Number of total pixels	130(H) $\times$ 132(V)
Image area	3.07 mm $\times$ 3.07 mm
Pixel size	24 μm $\times$ 24 μm
Optical black	Horizontal (H) - 1 pixel at the back.
	Vertical (V) - 3 pixels at the front and 1 pixel at the back

7. Absolute Maximum Rating

Symbol	Parameter	Value	Unit
DVDD	Digital power supply	7	V
AVDD1	Analog power supply for pixel unit	7	V
AVDD2	Analog power supply for amplifier	7	V
V_I	Logic input voltage*	-0.3 to VDD	V
T_{opt}	Ambient operating temperature	-10 to +55	$^\circ$C
T_{stg}	Storage temperature	-20 to +80	$^\circ$C

* The digital input pins are START, SIN, LOAD, XRST, XCK, RESET and TADD.

8. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
T_{opt}	Ambient operating temperature	0	25	45	$^\circ$C
DVDD	Digital Power supply	4.5	5.0	5.5	V
AVDD1	Analog power supply for pixel unit	4.5	5.0	5.5	V
AVDD2	Analog power supply for amplifier	4.5	5.0	5.5	V
V_{IH}	"H" logic input voltage*	2.2		DVDD	V
V_{IL}	"L" logic input voltage*	0		0.8	V
f_{xck}	System clock	50	500	1000	kHz

* The digital input pins are START, SIN, LOAD, XRST, XCK, RESET and TADD.

Ver. 2. 2. 3

9. D.C. Electrical Characteristics

Symbol	Parameter		Minimum	Typical	Maximum	Unit
V_{OH}	"H" digital output voltage*		4.5		DVDD	V
V_{OL}	"L" digital output voltage*		0		0.5	V
I_{out}	Analog output current rating**		-100		100	µA
R_o	Analog output resistance**			100		Ω
DI_{DD}	Digital circuit current			0.5		mA
AI_{DD}	Analog circuit current	Front view image			2.5	mA
		Two-dimensional edge (50%)			3	mA
		Vertical/Horizontal projection			4	mA

 * The digital output pins are READ and STRB
** The analog output pin is VOUT

10. Electro-optical Characteristics(Ta = 25°C)

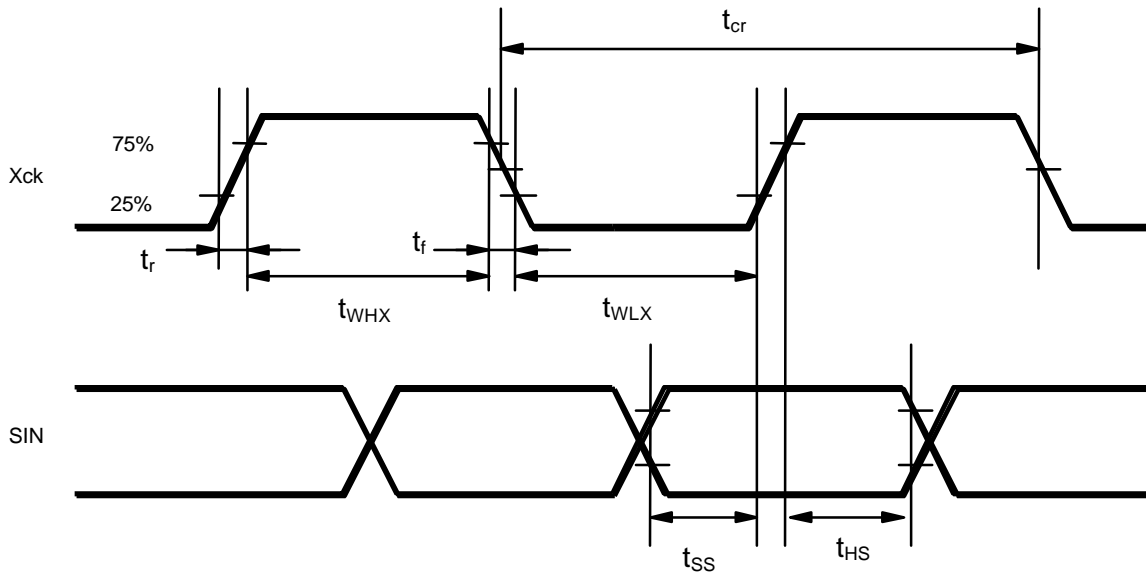| Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
	Image capture illumination (at image capture face)		1		5000	lx
	Variable range of exposure time		16 µ		1	sec
	Frame rate*		1		30	fps
S	Sensitivity	Condition 1		10		mV/lx msec
V_{sat}	Saturation power voltage		1000			mV
V_o	Average Typical power			(TBD)		mV
V_{drk}	Dark signal			(TBD)		mV
SHV_o	Light shading			(TBD)		%
SHV_{drk}	Dark shading			(TBD)		%
Smr	Smear			(TBD)		%

Condition 1. Halogen light source is used. Infrared filter is not used. Gain setting is 04H (ten times).
* 1fps is for exposure time up to 1 sec. 30fps is for exposure time 1msec or less.
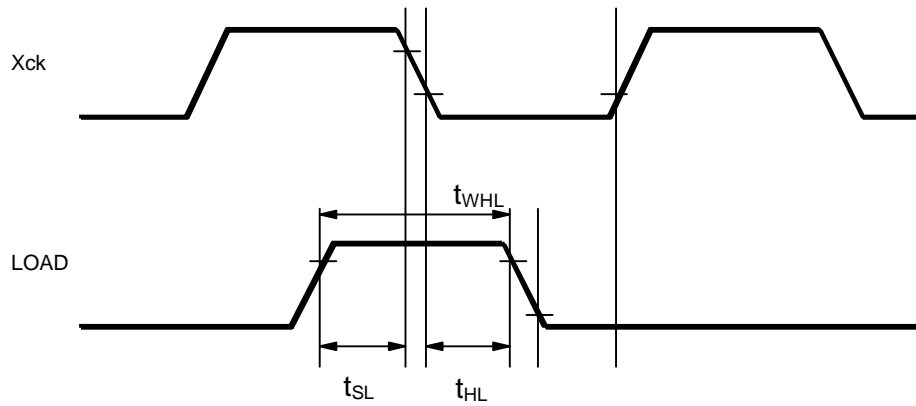
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11. A.C. Electrical Characteristics

Symbol	Parameter	Target value			Unit
		Minimum	Typical	Maximum	
t_{cr}	XCK cycle time	2	-	-	μsec
t_{WHX}	XCK pulse width ("H" level)	0.8	-	-	μsec
t_{WLX}	XCK pulse width ("L" level)	0.8	-	-	μsec
t_r	XCK rise time	-	-	0.2	μsec
t_f	XCK fall time	-	-	0.2	μsec
t_{SS}	SIN setup time	0.4	-	-	μsec
t_{HS}	SIN hold time	0.4	-	-	μsec
t_{SL}	LOAD setup time	0.4	-	-	μsec
t_{HL}	LOAD hold time	0.4	-	t_{WLX}-0.4	μsec
t_{WHL}	LOAD pulse width ("H" level)	0.8	-	-	μsec
t_{SXR}	XRST setup time	0.4	-	-	μsec
t_{HXR}	XRST hold time	0.4	-	-	μsec
t_{SR}	RESET setup time	0.4	-	-	μsec
t_{HR}	RESET hold time	0.4	-	-	μsec

(A) XCK/SIN timing

6/35

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Ver. 2. 2. 3

(B) XCK/LOAD timing

Xck

LOAD

t_{WHL}

t_{SL} t_{HL}

(C) XCK/XRST/RESET timing

Xck

Xrst

t_{SXR} t_{HXR}

RESET

t_{SR} t_{HR}

(D) XCK/START timing

Xck

START

t_{SST} t_{HST}

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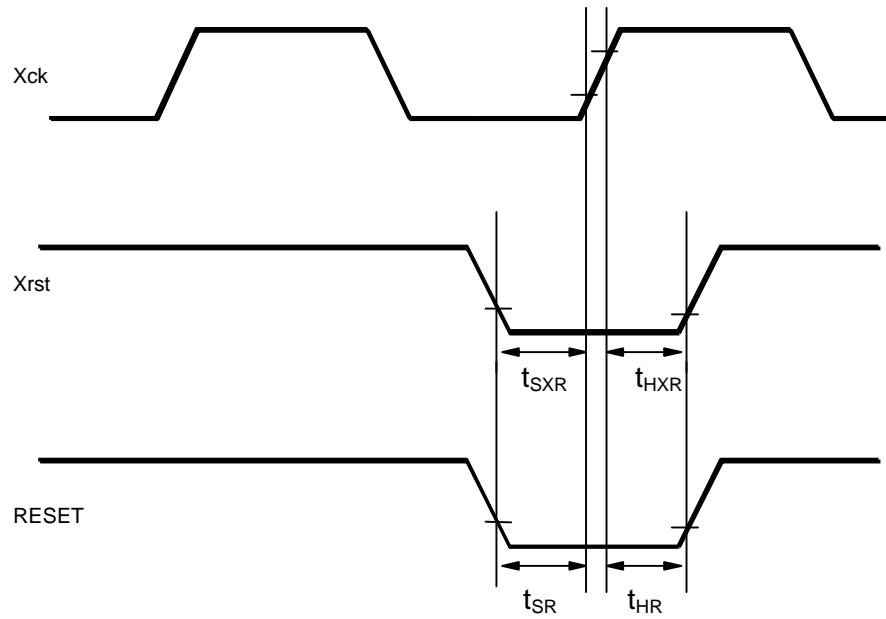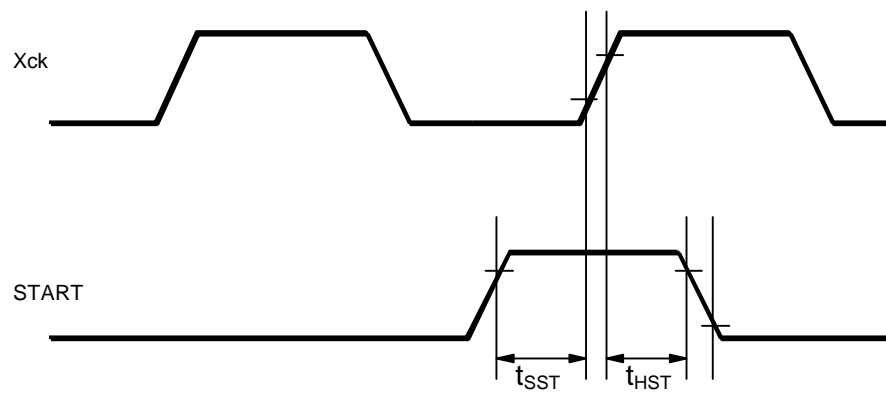
12. Description of Function

12.1. Image Capture Procedure
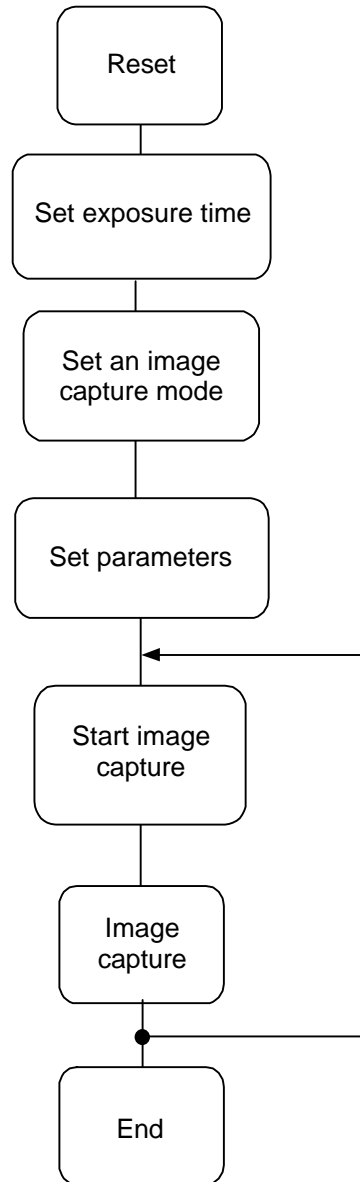
Figure 2. Operation Flow Chart

Image capture is executed according to the procedure in Fig. 2. First, reset all the registers of the chip, and then program the registers. To reset the chip, set both XRST and RESET to "L". There are10 sets of registers, each 8 bit. Input data format is supposed to be 11 bits (x 10 sets), the first 3 bits are for address and the last 8 bits are for data. Each input data bit is fetched on the rising edge of XCK. The contents of a register, address from 0 to 7, become valid on the falling edge of XCK when both LOAD and TADD are

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"H", and those, address 8 and 9, become valid on the same edge when LOAD is "H" and TADD is "L".

After all the registers have been written, image capture starts when START is input on the rising edge of XCK. Two modes are available for image capture, i.e., one is an accumulation mode, which accumulates the input image signal (optical signal), and an image output mode which converts the optical signal into electrical signal and output the results. When the exposure time specified by the registers C_0 and C_1 has passed, an analog image signal is output in serial. READ becomes "H" when analog image signal is output. At this moment, all the registers can be rewritten because the exposure time and the image capture mode are stored in the internal control registers of the chip.

When image capture has started, the image signal is supposed to be output until the chip is reset.

12.2. The programming model

Parameter and Function	Symbol	Number of bits	Description
Image capture mode	P,M,X	4bit×3	Allows to select positive, negative, and edge image capture modes manually
Exposure time	C_0,C_1	8bit×2	Program exposure time
Gain	G	5bit	Program gain of output amplifier.
Output pin voltage (V_{ref})	V	3bit	Program bias voltage of output pin.
Enable edge enhancement/extraction mode	N	1bit	Enable the edge enhancement/extraction mode forcibly "H" active
Vertical/Horizontal edge extraction	VH	2bit	Allows to select vertical edge and horizontal edge modes
Edge enhancement mode	E	4bit	Set the degree of edge enhancement
Output inversion mode	I	1bit	Allows to select an inversion mode "H" active
Enable automatic black level* calibration	AZ	1bit	Enable automatic black level calibration with unfixed bias voltage "H" active.
Enable black level calibration	Z	2bit	Black level calibration with fixed bias voltage.
Enable dark pixel line output	OB	1bit	Enable to output optical black level of dark pixel line "L" active
Offset voltage	O	6bit	Allows to change offset voltage of output signal with positive/negative bias
Enable clamp circuit	CL	1bit	Enable clamp circuit operation "L" active
Enable sample hold circuit	SH	1bit	Enable sample & hold circuit operation "L" active
Enable projection	PX,PY	2bit	Enable Vertical/Horizontal projection mode "H" active
Projection output control	MV	5bit	Allows to adjust projection signal amplitude
Random access start address	ST	4bit×2	Specify random access start address by (x, y)
Random access stop address	END	4bit×2	Specify random access stop address by (x', y')

* Black level shall be defined as output voltage from pixel in shading condition.

12.3. Register Mapping

Register No.	TADD	Address	7	6	5	4	3	2	1	0
0	1	000	Z_1	Z_0	O_5	O_4	O_3	O_2	O_1	O_0
1	1	001	N	VH_1	VH_0	G_4	G_3	G_2	G_1	G_0
2	1	010	C_{17}	C_{16}	C_{15}	C_{14}	C_{13}	C_{12}	C_{11}	C_{10}
3	1	011	C_{07}	C_{06}	C_{05}	C_{04}	C_{03}	C_{02}	C_{01}	C_{00}
4	1	100	SH	AZ	CL		P_3	P_2	P_1	P_0
5	1	101	PX	PY	MV_4	OB	M_3	M_2	M_1	M_0
6	1	110	MV_3	MV_2	MV_1	MV_0	X_3	X_2	X_1	X_0
7	1	111	E_3	E_2	E_1	E_0	I	V_2	V_1	V_0
8	0	001	ST_7	ST_6	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0
9	0	010	END_7	END_6	END_5	END_4	END_3	END_2	END_1	END_0

* Note. If TADD is "0", any address except 001 or 010 is prohibited.

12.4. Image Capture Mode Register

12.4.1. Image Capture mode

Image capture modes set by P, M, and X registers are as follows:

(a)	Positive image mode	Set with the P register
(b)	Negative image mode	Set with the M register
(c)	Edge image	Set with the P and M registers

12.4.2. Image Capture Mode Register

Users can select the sensing mode from positive, negative, and vertical edge image (one-dimensional direction) capture modes by modifying P, M, and X registers manually. Each image capture mode is set by lower 4 bits of the P, M and X registers. However, for the X register, only one mode, X0 = 1 and X1 = X2 = X3 = 0, is effective. 4×1 filter can be configured by combination of either P or M register bits and X register. Figure 3 shows some configurations of P, M and X registers and filters provided by the registers. As shown in Figure 3, these filters can scan the entire screen with P, M, and X registers. The P and M registers perform vertical setting of filter and the X register performs the horizontal setting. The P and M registers allow an output image signal to have the positive and negative polarities. A line selected by the P register multiplies an image signal by a coefficient of +1 and a line selected by the M register multiplies an image signal by a coefficient of -1. Various image processing, positive, negative, and edge images, can be achieved by the combinations of P, M, and X registers.
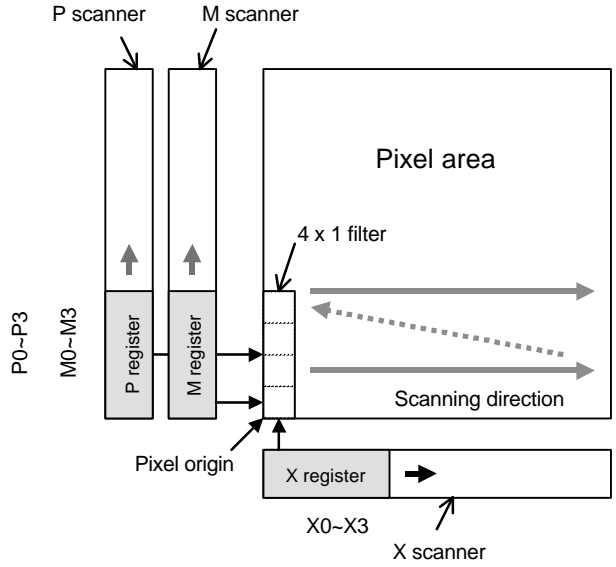
Figure 3. Filter Configuration with P, M and X registers

Figure 4 shows an example of filter setting. To output a positive image from an origin of an image area, set 1 to the least significant bit P0 of the P register as shown in Figure 4 (a). To output an edge image, set 1 to the least significant bit M0 of the M register as shown Figure 4 (b). Figure 5 (a), (b) and (c) show the examples of setting P, M, and X registers to output an edge image.
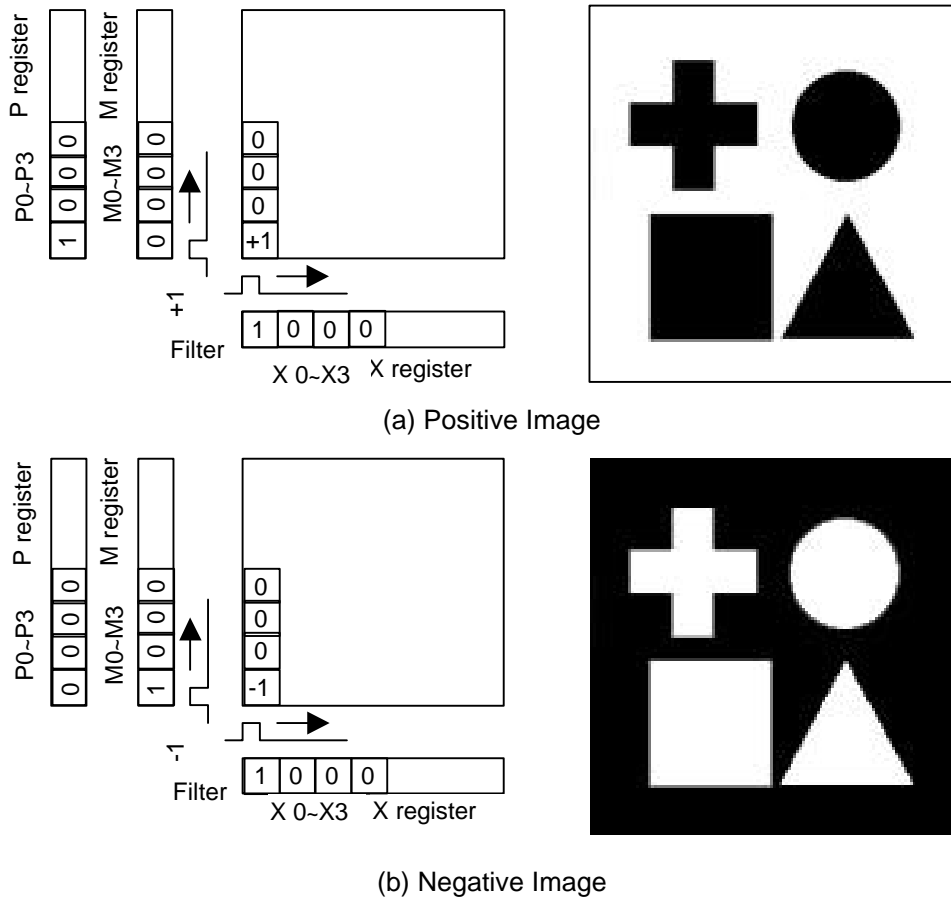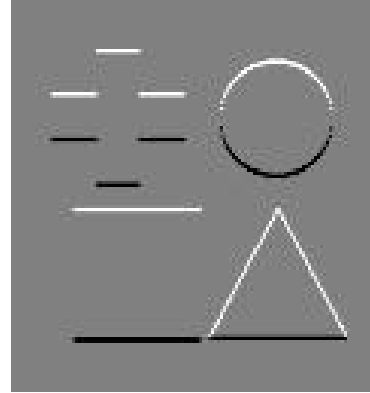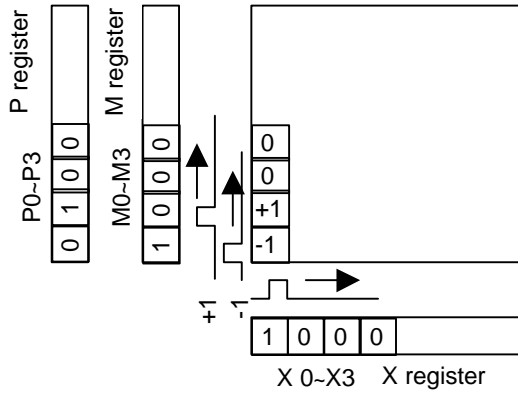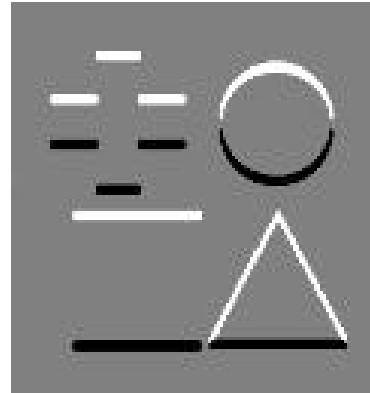

(a) Positive Image

(b) Negative Image

Figure 4. Example of Positive and Negative Image

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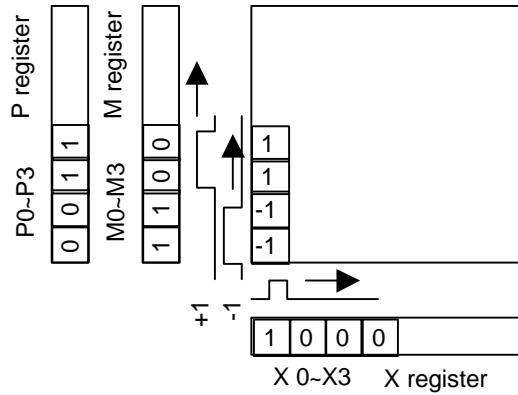
(a) Edge Image 1

(b) Edge Image 2
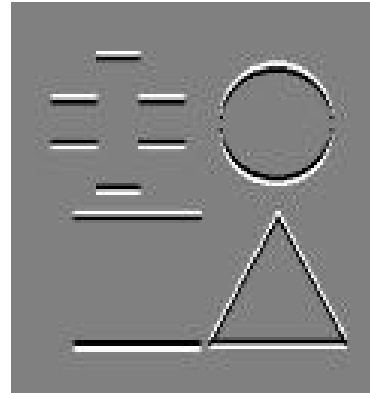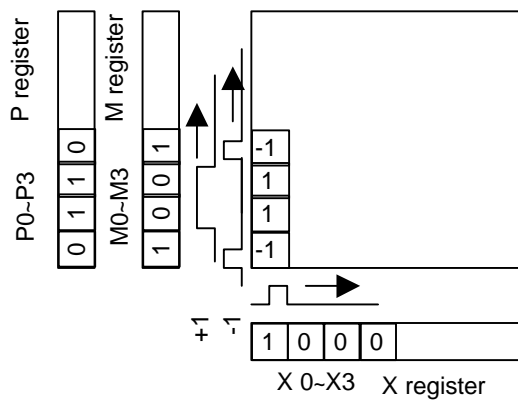
(c) Edge Image 3

Figure 5. Examples of Edge Image

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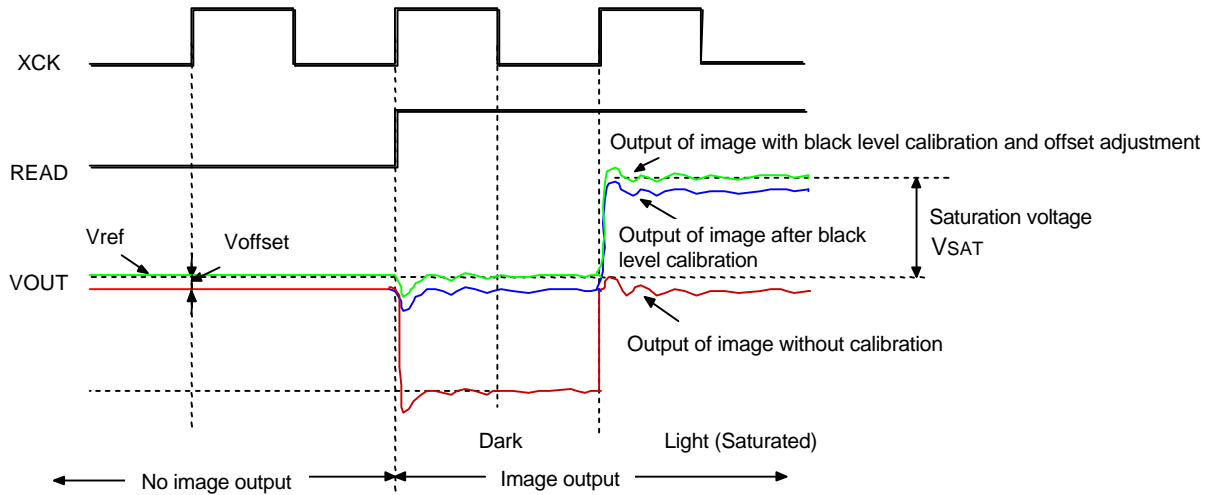Ver. 2. 2. 3

Figure 6. Waveform Chart of Analog Image Signal VOUT (Positive Image Output)

12.5. Analog Image Signal Control

The analog image signal VOUT is output on the rising edge of the system clock XCK. READ becomes "H" when VOUT is output. Figure 6 shows the waveforms of READ, XCK and VOUT. The output level of VOUT is controlled by output pin voltage specified by V register, automatic black level calibration register AZ (or black level calibration register Z), and offset adjustment register O.

12.5.1. Output Pin Voltage - V Register (3 bits)

This register sets the output pin voltage Vref. The output pin voltage is the voltage value measured on the VOUT pin when an analog image signal is not output. The table shown below mentions the output pin voltage Vref set by the V register. Note: $V_2 = V_1 = V_0 = 0$ is not allowed.

Register setting			Vref Voltage (V)
V_2	V_1	V_0	
0	0	1	0.5
0	1	0	1.0
0	1	1	1.5
1	0	0	2.0
1	0	1	2.5
1	1	0	3.0
1	1	1	3.5

12.5.2. Automatic Black Level Calibration Register - AZ (1 bit)

As shown in Figure 6, the output voltage VOUT (amplitude) becomes minimum (maximum) in the dark state: the incident light is 0lx (black level). On the other hand, the output voltage VOUT becomes the same as Vref in the light state: the incident light is very strong and the pixels are saturated (saturation level). The black level is calibrated so that the output amplitude is in proportion to the incident light intensity (the output amplitude becomes large as the incident light increases). As shown in Figure 6, the output voltage VOUT, in which black level has been calibrated by biasing the saturation voltage Vsat, becomes Vref in the dark state, and its amplitude becomes maximum in the light state. Figure 7 shows a scheme of automatic black level calibration. In this scheme, the difference voltage between the effective pixel and the dark pixel is put out. By using this circuit, shift of the saturation voltage Vsat attributed to exposure time can be calibrated automatically. The automatic black level calibration is enabled in any image capture mode and works when the AZ register is "H" (an initial value of AZ: L).
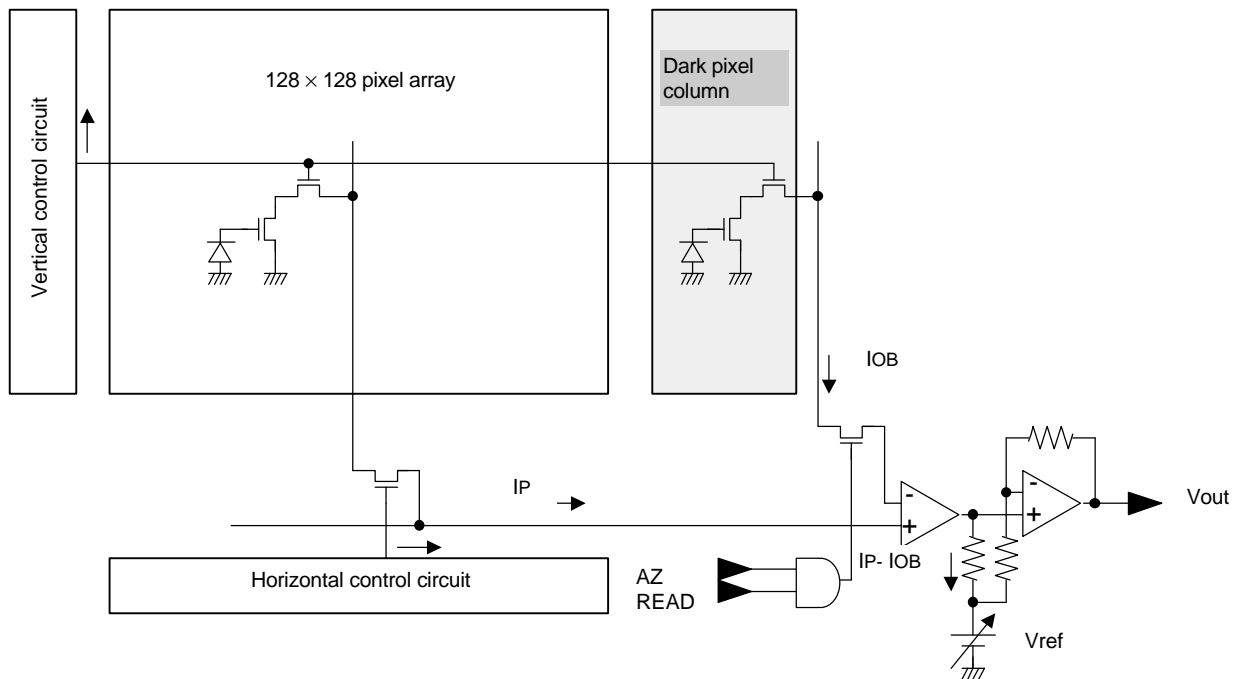
Figure 7. Structure of Automatic Black Level calibration Circuit

Parameter	Automatic black level control
A Z	
0	Disable
1	Enable

12.5.3. Black Level Calibration Register - Z (2 bits)

The black level calibration enabled by the Z register achieves the effect equivalent to the automatic black level calibration. However, the calibration bias voltage is the saturation voltage Vsat at the minimum exposure time of the positive image mode. Therefore, the black level is slightly shifted when the exposure time or image capture mode has changed. Nothing can be set when the AZ register is "H" and when the automatic black level control is being executed.

Parameter		Zero point calibration
Z_1	Z_0	
0	0	No adjustment
1	0	Positive image reading calibration
0	1	Negative image reading calibration

12.5.4. Automatic Black Level Calibration Register - CL (Clamp Circuit)

As shown in Figure 6, the black level of the output voltage VOUT in the dark state does not equal to the Vref value, even after automatic black level calibration. This is caused by offset voltage of an output amplifier, non-uniformity in the internal arithmetic circuit, etc. A value of Voffset varies depending on an image capture mode and setting of amplifier gain. However, by using the circuit shown in Figure 8, the offset value Voffset of black level can be kept to a certain fixed value. The automatic black level calibration using the clamp circuit is enabled at every image capture mode (except the random access projection output) and it works when the CL register is "L" (initial value of CL: L). To activate the clamp circuit, use both SH register (sample hold circuit) and OB register (black level output) by setting "L" simultaneously.
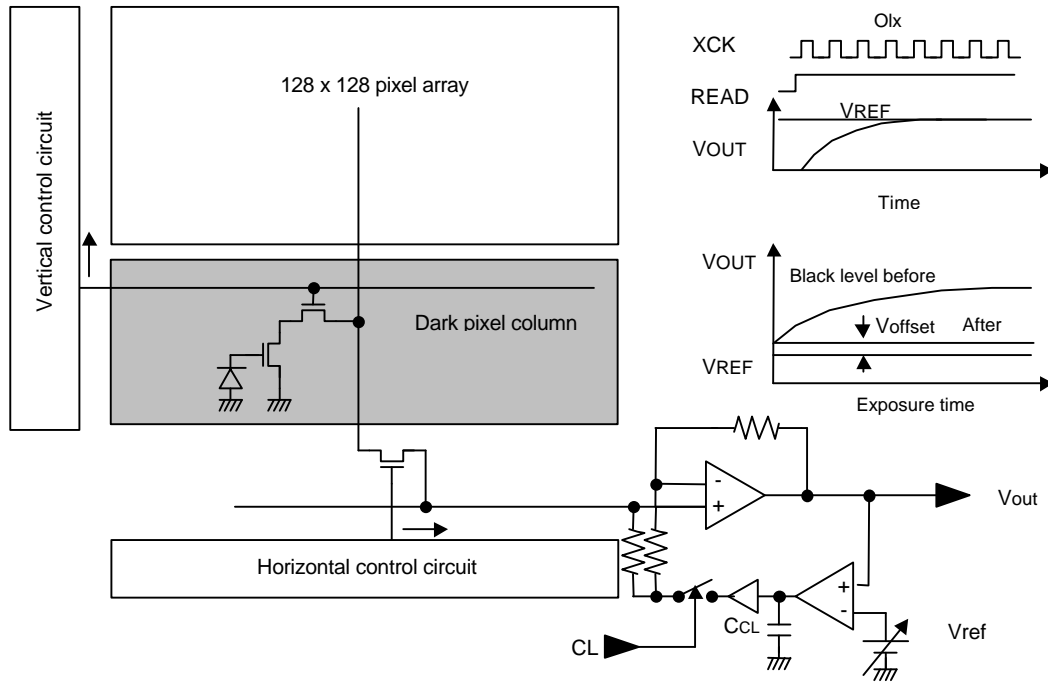
Figure 8. Automatic Black Level calibration Circuit with Clamp Circuit

Parameter			Automatic black level control
A Z	SH	OB	
0	0	0	Enable
1	1	1	Disable

12.5.5. Offset Adjustment O Register (6 bits)

This register calibrates Voffset, the offset voltage from the output pin voltage Vref. The most significant bit O_5 is a sign bit. It can be adjusted in the positive direction and the negative direction if the most significant bit is set to "H" and "L" respectively. A maximum value shall be 0.5 V. The amplitude is controlled by 5-bit resolution.

O_5	Register setting range	Offset voltage (V)	Step (mV)	Number of steps
H	H 20 to H 3F	0 to 0.5	16	32
L	H 00 to H 1F	0 to -0.5	16	32

12.5.6. Dark Pixel Line Output OB (1 bit)

When an image is output with the OB register being "L", the first line of the image frame becomes the output signal from 128 dark pixels. Adjust the O register so that this dark pixel output (optical black) level
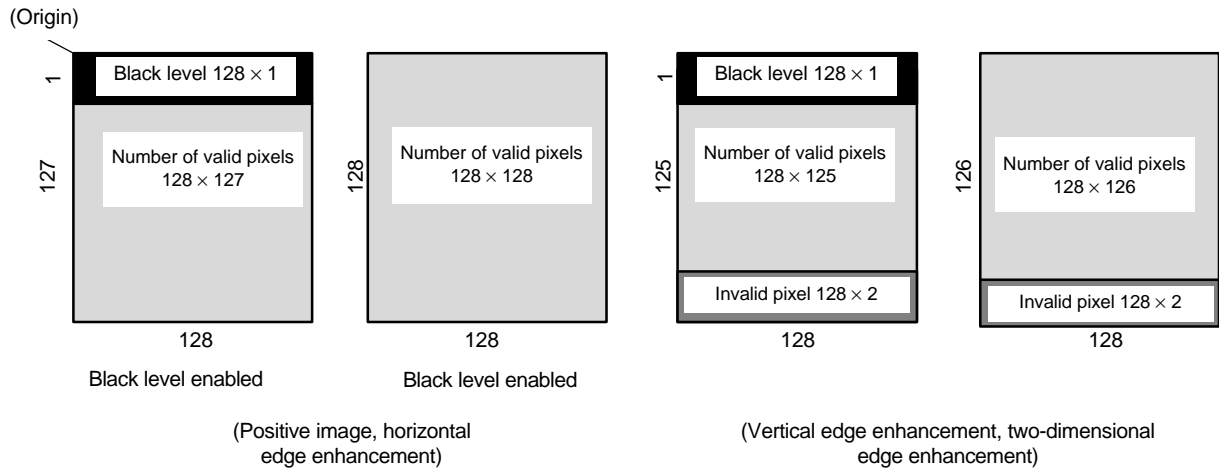
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becomes the Vref value.

Figure 9. Relation between Number of Valid Pixels and Dark Pixel Line

Parameter	Execution of dark pixel output
O B	
0	Enable
1	Disable

12.6. Output Inversion Register - I (1 bit)

This register selects an inversion mode when "H" is selected and a non-inversion mode when "L" is selected.

12.7. Exposure time Setting Registers - C_0 and C_1 (8 bits $\times$ 2)

This register sets exposure time. Total of exposure time set by both C_0 and C_1 register is the actual exposure time.

C_0 register (8 bits)

Register setting range	Exposure time (msec)	Step (μsec)	Number of steps
H 00 to H FF	0 to 4.08	16	256

C_1 register (8 bits)

Register setting range	Exposure time (msec)	Step (msec)	Number of steps
H 00 to H FF	0 to 1044.5	4.096	256

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Available exposure time

Image capture mode	Minimum exposure time (μsec)	Maximum exposure time (sec)
Positive image/Negative image	16 (C_0=01,C_0=00)	1 (C_0=FF,C_0=FF)
Horizontal edge/ Horizontal edge enhancement	16 (C_0=01,C_0=00)	1 (C_0=FF,C_0=FF)
Vertical edge/ Vertical edge enhancement	528 (C_0=11,C_0=00)	1 (C_0=FF,C_0=FF)
Two-dimensional edge/ Two-dimensional edge enhancement	528 (C_0=11,C_0=00)	1 (C_0=FF,C_0=FF)

Note. When C_1 = 00h and C_0 = 00h are set, reading image pixels is done (read-only mode) without resetting every image capture mode. In this case, the clamp circuit cannot be used.

12.8. Edge and Edge Enhancement Image Capture Mode
12.8.1. Image Capture Mode

In addition to setting P, M and X registers individually, an edge image and edge enhancement image can be output according to N, VH and E registers. The edge enhancement image is an image that adds an original image and an edge image multiplied by a certain coefficient. Horizontal edge, horizontal edge enhancement, vertical edge, vertical edge enhancement, two-dimensional edge, and two-dimensional edge enhancement modes are available.

(a) Horizontal edge   (b) Horizontal edge enhancement
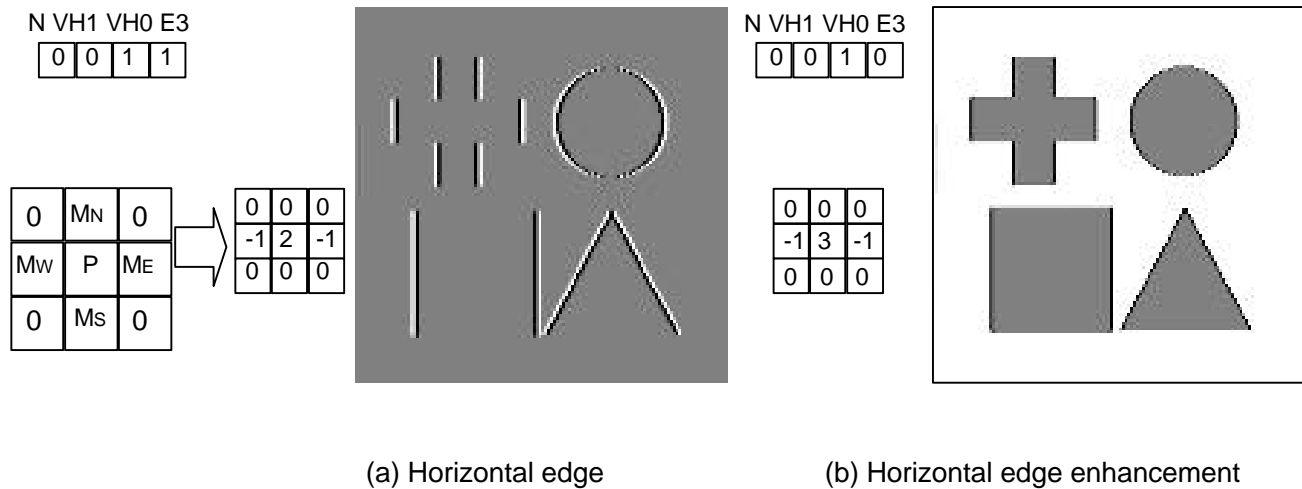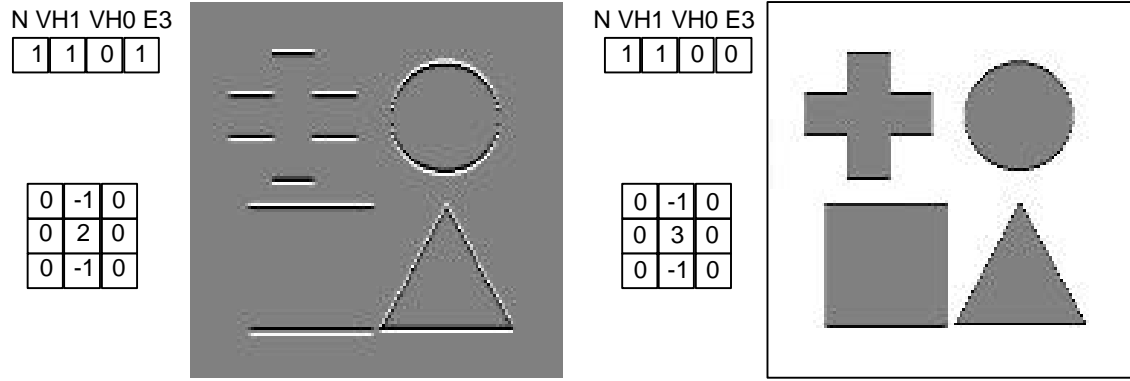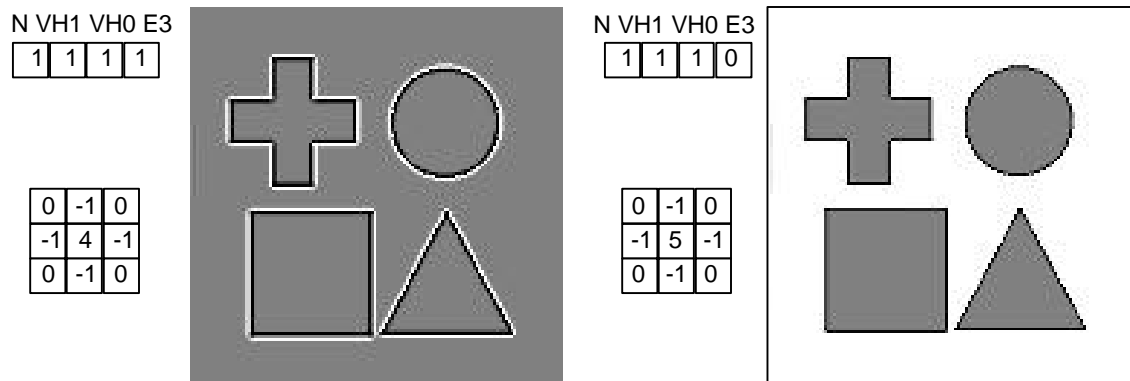
Figure 10. Example of Edge Enhancement 1 (Horizontal edge: Original image is the same as Figure 4)

(a) Vertical edge   (b) Vertical edge enhancement

Figure 11. Example of Edge Enhancement 2 (Vertical edge)

(a) Two-dimensional edge   (b) Two-dimensional edge enhancement

Figure 12. Example of Edge Enhancement 3 (Two-dimensional edge)

Using N, VH and E registers, a convolution of 3 x 3 size can be achieved as shown in Figure 10, Figure 11 and Figure 12. An edge image can be obtained by taking the difference between the center pixel P and the neighbor Mn, Ms, Mw and Me.

Edge mode	Output signal	Number of output pixels	Number of valid pixels
Vertical edge image	$\{(P-MN)+ (P-MS)\}\times\alpha$	128(H)$\times$128(V)	128(H)$\times$126(V)
Horizontal edge image	$\{(P-Mw)+(P-ME)\}\times\alpha$	128(H)$\times$128(V)	128(H)$\times$128(V)
Two-dimensional edge image	$\{(P-MN)+(P-MS)+(P-ME)+(P-MW)\}\times\alpha$	128(H)$\times$128(V)	128(H)$\times$126(V)
Vertical edge enhancement image	$P +\{(P-MN)+(P-MS)\}\times\alpha$	128(H)$\times$128(V)	128(H)$\times$126(V)

Horizontal edge enhancement image	$P +\{(P-Mw)+(P-ME)\}\times\alpha$	128(H)×128(V)	128(H)×128(V)
Two-dimensional edge enhancement image	$P+\{(P-MN)+(P-MS)+(P-ME)+(P-MW)\}\times\alpha$	128(H)×128(V)	128(H)×126(V)

α: Edge enhancement ratio

In the above-mentioned table, both P and M shows the intensity of output signal from the pixel. The relation between the output pixel and valid pixel is shown below:
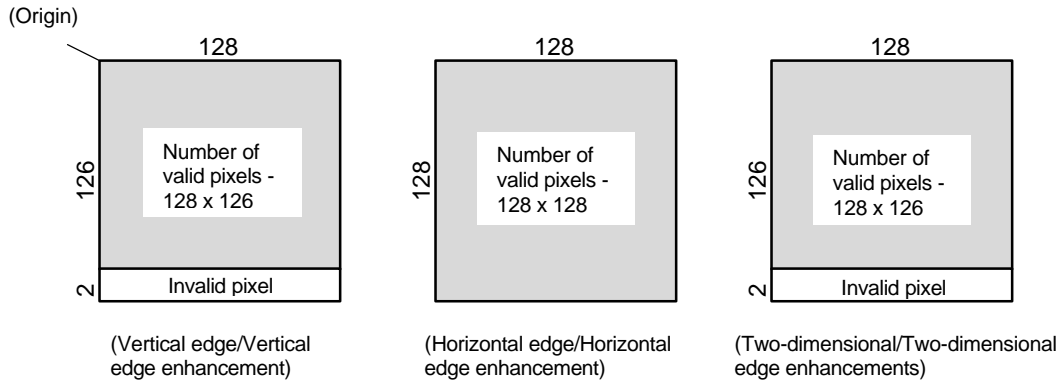

Figure 13. Relation between Number of Output Pixels and Number of Valid Pixels

12.8.2. N Register (1 bit)

If this register is set, the P and M registers are set for the vertical edge enhancement mode. When "H" is written, the P and M register are set automatically to "H02" and "H05" respectively. In this case, writing to both P and M registers is disabled.

12.8.3. VH Register (2 bit)

Using this register, users can select the image capture mode from the vertical edge, horizontal edge, or two-dimensional edge modes. The edge enhancement mode uses the same edge configuration modes.

Parameter			Edge mode
N	VH_1	VH_0	
0	0	0	No edge output
0	0	1	Horizontal edge mode
1	1	0	Vertical edge mode
1	1	1	Two-dimensional edge mode

12.8.4. E Register (4 bits)

This register sets the ratio of edge enhancement (in the table   above). The most significant bit E_3 switches between the edge enhancement and edge mode. "H" selects the edge mode and "L" selects the

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Ver. 2. 2. 3

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edge enhancement mode. However, "L" should be set for the output of positive and negative image. E register sets the ratio of edge enhancement as follows:

Parameter			Ratio of edge enhancement
E_2	E_1	E_0	
0	0	0	0%
0	0	1	12.5%
0	1	0	25.0%
0	1	1	37.5%
1	0	0	50.0%
1	0	1	62.5%
1	1	0	75.0%
1	1	1	87.5%

12.9. Projection Setting
12.9.1. Projection Function
The artificial retina chip can execute the projection of input image. The projection executes addition of all pixels along either vertical or horizontal direction. As shown in Figure 14, size and center position of an input image can be obtained by projecting the input image vertically and horizontally. Figure 15 shows the circuit diagram of the artificial retina chip to achieve the projection. In the case of the horizontal projection, the P scanner becomes active simultaneously, and X scanner reads out the result. In the case of the vertical projection, the role of P scanner and that of the X scanner are exchanged. When projection mode is active, make the automatic black level calibration register AZ "H".

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Ver. 2. 2. 3
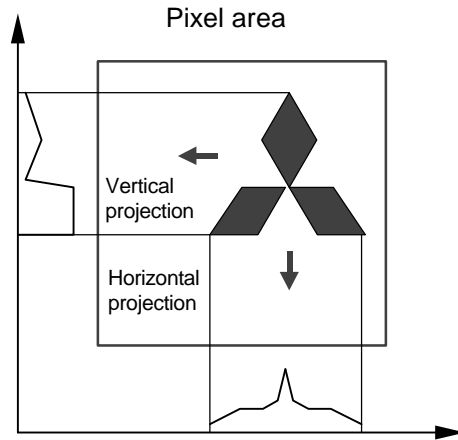
Figure 14. Principle of Projection Function
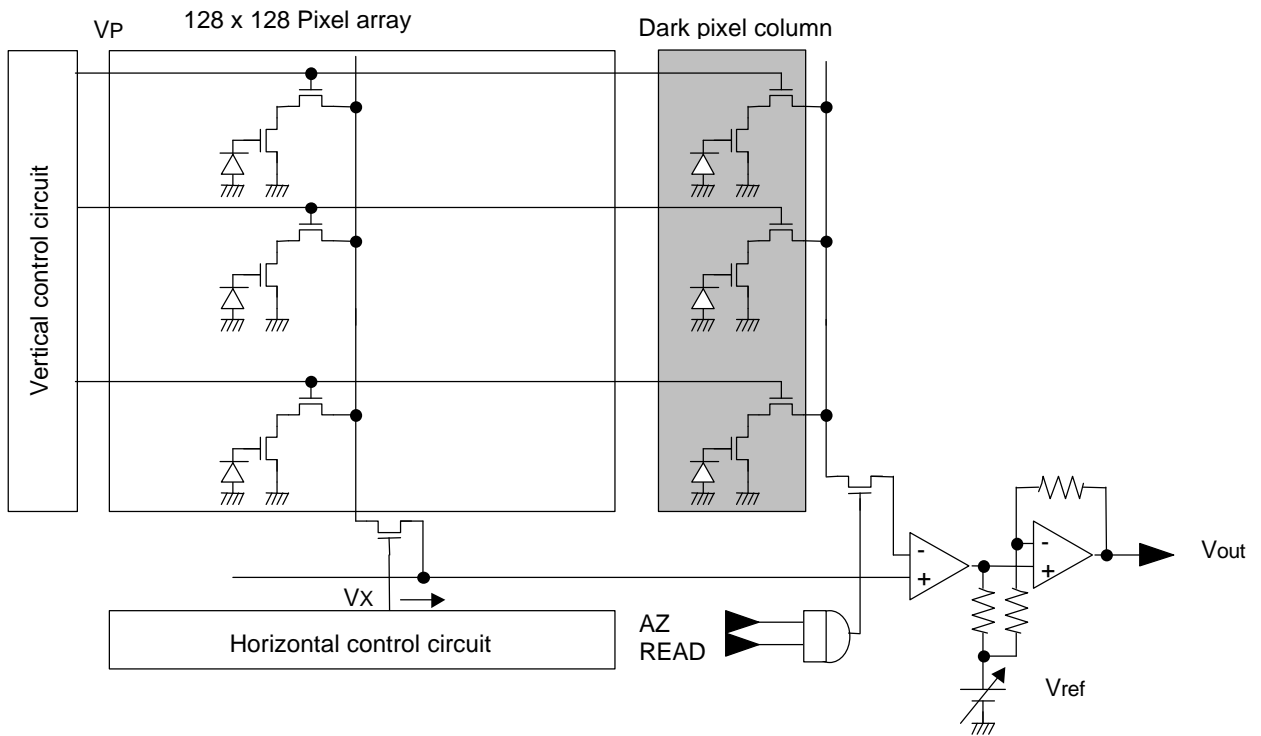
Figure 15. Diagram of Horizontal Projection Circuit

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Ver. 2. 2. 3
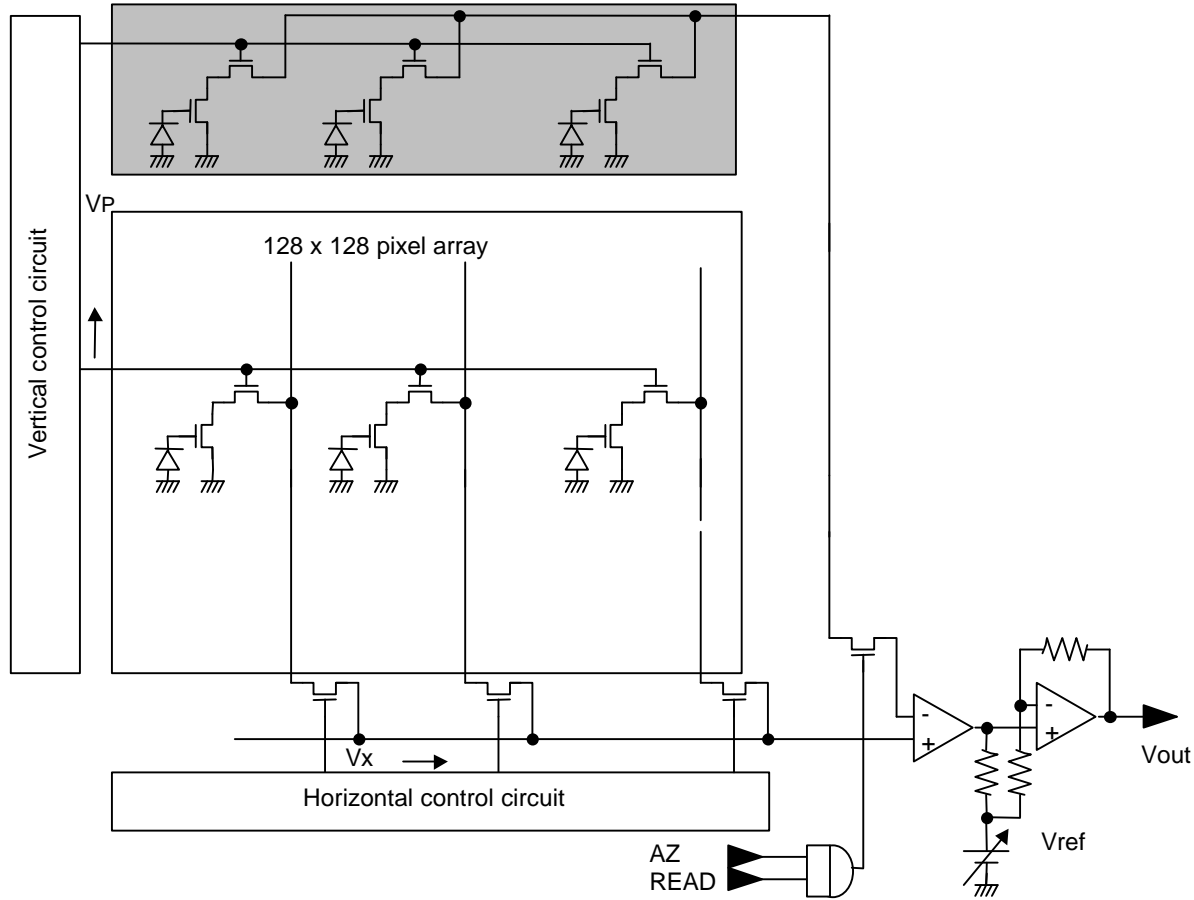
Figure 16. Diagram of Vertical Projection Circuit

12.9.2. Projection Registers - PX/PY

Parameter		Projection mode
P X	P Y	
0	0	No projection
1	0	Execution of horizontal projection
0	1	Execution of vertical projection

12.9.3. Projection Output Offset Register - MV (5 bits)

Output voltage amplitude of the projection can be modified. The output voltage amplitude can be modified +/- 50% by adjusting the offset voltage by +/- 0.11 V/8 mV.

Specifying MV_4 as sign binary digit, users can modify the amplitude in a positive and negative direction when MV_4 is "H" and "L" respectively.

MV4	Register setting range	Offset voltage (V)	Step (mV)	Number of steps
H	H 0 to H F	0 to 0.12	8	16
L	H 0 to H F	0 to -0.12	8	16

12.9.4. G Register (5 bits)

This register set output amplifier gain. When the most significant bit G_4 is "H", the gain increases 6 dB.

Parameter				Total gain (dB)	
G_3	G_2	G_1	G_0	G_4	
				0	1
0	0	0	0	14.0	20.0
0	0	0	1	15.5	21.5
0	0	1	0	17.0	23.0
0	0	1	1	18.5	24.5
0	1	0	0	20.0	26.0
0	1	0	1	21.5	27.5
0	1	1	0	23.0	29.0
0	1	1	1	24.5	30.5
1	0	0	0	26.0	32.0
1	0	0	1	29.0	35.0
1	0	1	0	32.0	38.0

Ver. 2. 2. 3

12.10. Random Access Function

12.10.1. Random Access

The whole image is divided into 16 x 16 block areas in which minimum block consists of 8 x 8 pixels, a start block position (x, y) can be specified by the ST register (8 bits) and an end block position (x', y') by the END register (8 bits). The access area is specified when coordinate data has been set to both ST and END registers. To execute the random access, users can choose either positive image or projection mode. Although the automatic black level calibration is available, clamp circuit is not available in this mode. Therefore, the CL register must be set to "H". When the random access is executed, both READ and STRB are also output.

12.10.2. Block Diagram

Figure 17 shows the block diagram of the chip. The lower 4 bits of the ST register indicate the x coordinate of a start block, and the higher 4 bits indicate the y coordinate of the start block (x = ST [3:0], y = ST [7:4]). Similarly, the lower 4 bits of the END register indicate the x coordinate of an end block, and the higher 4 bits indicate the y coordinate of the end block (x' = END [3:0], y' = END [7:4]). An initial value of ST and END register is 00Hex when the random access starts. In this case, all the pixels are accessed ((x, y) = (0, 0), (x', y') = (16, 16)). The end block coordinate must be greater than the start block coordinate (x'>x or y'>y). If this condition is not satisfied, the end block coordinate becomes 16.
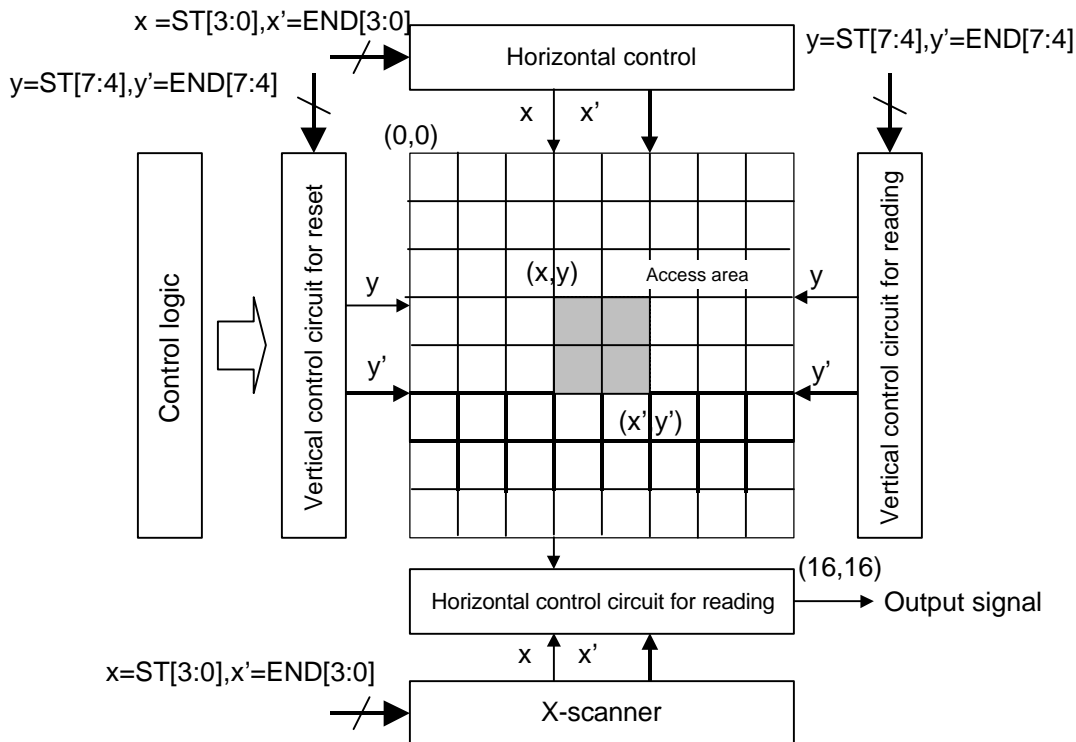
Figure 17. Random Access Diagram

12.10.3. Examples of Area Setting

Accessed area is specified according to parameters for the random access mode. The start point pixel coordinate set by the ST register is (8*x, 8*y) and the end point pixel coordinate is (8*x'-1, 8*y'-1). The table below shows the image area corresponding to various register settings:

Parameter		Start block	End block	Start pixel coordinate	End pixel coordinate
ST	END	(x,y)	(x',y')	(X,Y) X=8*x,Y=8*y	(X',Y') X=8*x-1,Y=8*y-1
00h	00h	(0,0)	(16,16)	(0,0)	(127,127)
00h	11h	(0,0)	(1,1)	(0,0)	(7,7)
00h	10h	(0,0)	(16,1)	(0,0)	(127,7)
00h	01h	(0,0)	(1,16)	(0,0)	(7,127)
10h	20h	(0,1)	(16,2)	(0,8)	(127,15)
01h	02h	(1,0)	(2,16)	(8,0)	(15,127)
F0h	00h	(0,15)	(16,16)	(0,120)	(127,127)
0Fh	00h	(15,0)	(16,16)	(120,0)	(127,127)
55h	66H	(5,5)	(6,6)	(40,40)	(47,47)

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Ver. 2. 2. 3

13. Examples of Image Capture Modes

Image capture mode	000	001	010	011	100	101	110	111
Positive image (with dark pixel output)	80h	04h	0001h to FFFFh (Exposure time C1C0)		01h	00h	01h	03h
Positive image (without dark pixel output)	80h	04h	0001h to FFFFh		A1h	10h	01h	03h
Horizontal edge (with dark pixel output)	80h	24h	0001h to FFFFh		41h	00h	01h	C3h
Horizontal edge (without dark pixel output)	80h	24h	0001h to FFFFh		E1h	10h	01h	C3h
Horizontal edge enhancement (with dark pixel output)	80h	24h	0001h to FFFFh		01h	00h	01h	43h
Horizontal edge enhancement (without dark pixel output)	80h	24h	0001h to FFFFh		A1h	10h	01h	43h
Vertical edge (with dark pixel output)	80h	C4h	0021h to FFFFh		41h	00h	01h	C3h
Vertical edge (without dark pixel output)	80h	C4h	0021h to FFFFh		E1h	10h	01h	C3h
Vertical edge enhancement (with dark pixel output)	80h	C4h	0021h to FFFFh		01h	00h	01h	43h
Vertical edge enhancement (without dark pixel output)	80h	C4h	0021h to FFFFh		A1h	10h	01h	43h
Two-dimensional edge (with dark pixel output)	80h	E4h	0021h to FFFFh		41h	00h	01h	43h
Two-dimensional edge (without dark pixel output)	80h	E4h	0021h to FFFFh		E1h	10h	01h	43h
Two-dimensional edge enhancement (with dark pixel output)	80h	E4h	0021h to FFFFh		01h	00h	01h	43h
Two-dimensional edge enhancement (without dark pixel output)	80h	E4h	0021h to FFFFh		A1h	10h	01h	43h
X projection	00h	04h	0001h to FFFFh		A1h	90h	01h	03h
Y projection (with dark pixel output)	00h	04h	0001h to FFFFh		A1h	40h	01h	03h
Y projection (without dark pixel output)	00h	04h	0001h to FFFFh		A1h	50h	01h	03h
Read-only (with dark pixel output)	80h	04h	0000h		01h	00h	01h	03h
Read-only (without dark pixel output)	80h	04h	0000h		A1h	10h	01h	03h

Gain 10 times. Pin voltage Vref set to 1.5 V. Edge enhancement ratio 50%.

Exposure time set by both C1 and C0 shall be set according to lighting condition.

The read-only mode is for only data output without reset.

If dark pixel output is not used, a clamp circuit shall be turned off.

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Ver. 2. 2. 3

14. Operation Timing

The operation timing of this chip below is described in the subsequent pages.

(1) Chip reset

Shows the timing of initial reset of logic controller. Reset is executed on the rising edge of clock XCK.

(2) Data input

Exposure time of image capture, initial values of scanners, Vref value, and gain parameters are fetched into the register. The data (8 bits x 10) are fetched on the rising edge of system clock XCK and become valid on the falling edge of XCK when LOAD is "H".

(3) Timing of image reading

Operation timing of reading an image out is shown. Either P or M scanner selects the line. Pixel data are output in serial from the column selected by the X scanner.
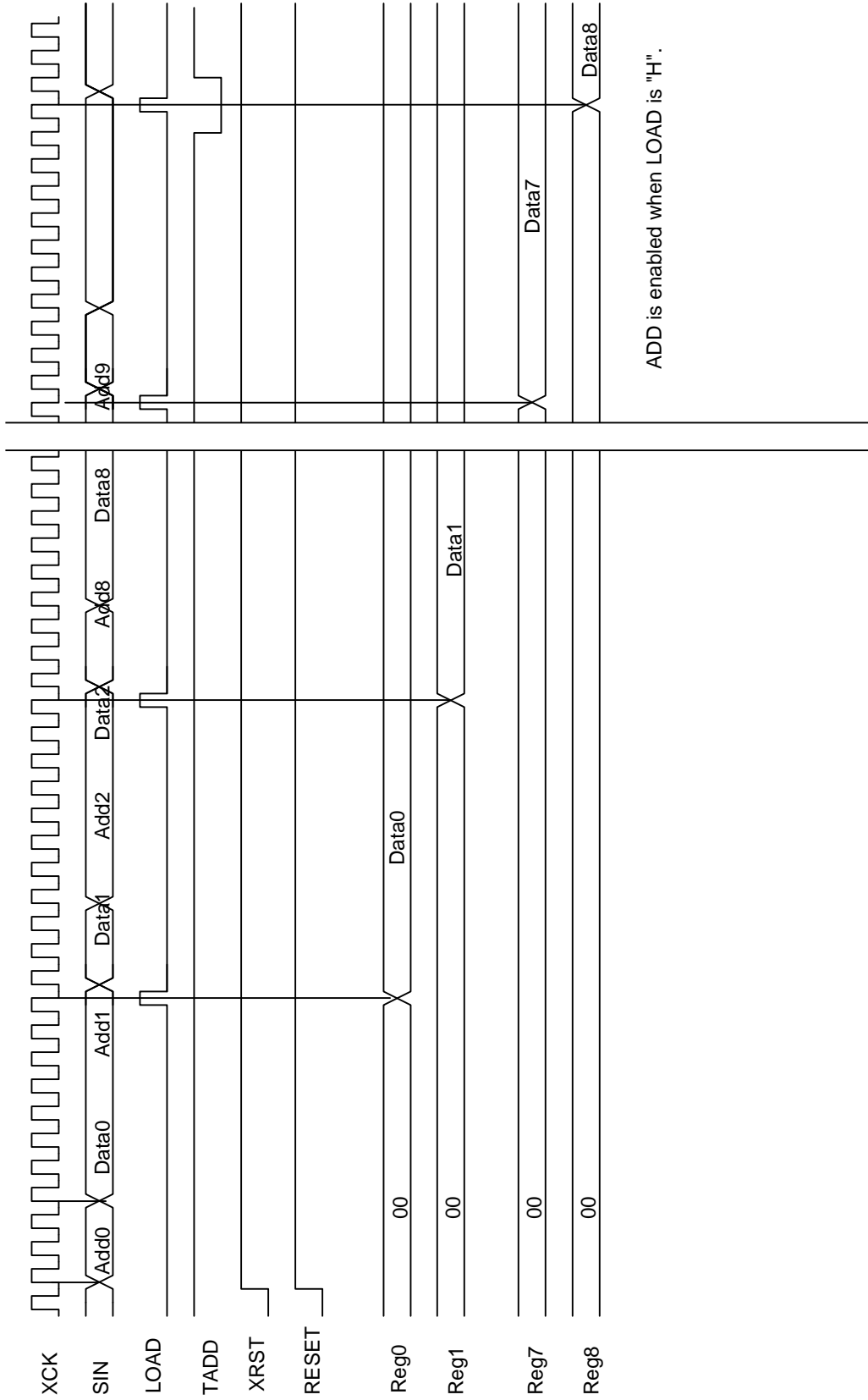

(4) Timing of projection reading

Timing of reading horizontal and vertical projection results is shown.

(5) Timing for read-only mode

Reading is executed without setting exposure time.

Drive Timing Chart (Data Set)

ADD is enabled when LOAD is "H".

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Ver. 2. 2. 3

Drive Timing Chart (Image Accumulation)

XCK

START

READ

VOUT

Exposure time

Start of accumulation of 1 frame.
The accumulation of 1 frame starts at 2 clock cycles after START has been input.

Start of output of 1 frame image

Start of accumulation of 2 frames.
The START signal is generated at 5 clock cycles after READ has been "L".
(The START signal after the second frame is generated automatically by internal logic.)

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Ver. 2. 2. 3

Drive Timing Chart (Positive Image Reading)

XCK

VP0
VP1
VP126
VP127

P-scanner output

VX0
VX1
VX2
VX3
VX4
VX5
VX6
VX7
VX125
VX126
VX127

X-scanner output
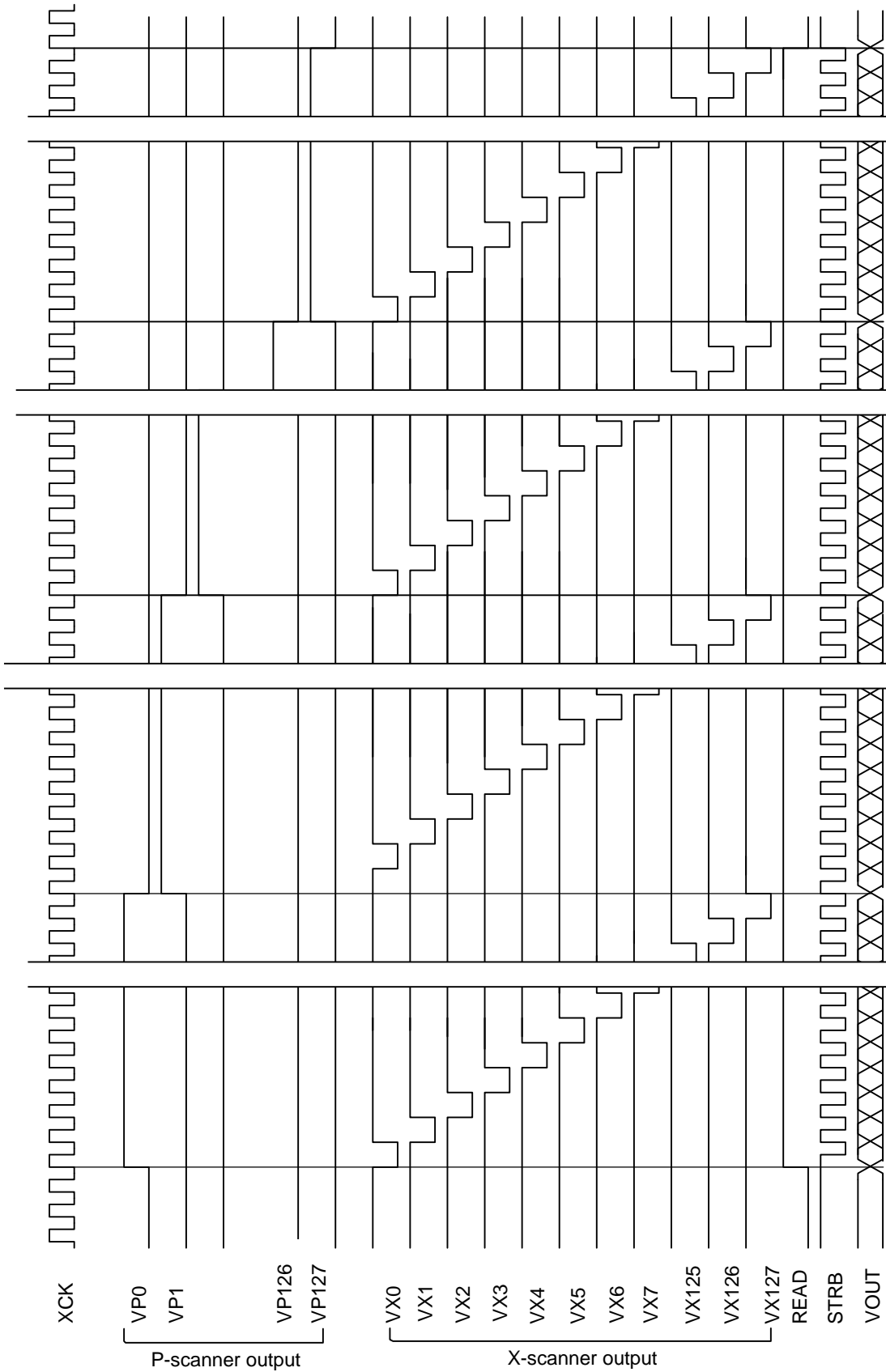
READ
STRB
VOUT

Drive Timing Chart (Two-dimensional edge enhancement Image Reading)

XCK
VP0
VP1
VP2
VP3
VP126
VP127
VM0
VM1
VM2
VM3
VM126
VM127
VX0
VX1
VX2
VX3
VX125
VX126
VX127
READ
STRB
VOUT

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Ver. 2. 2. 3
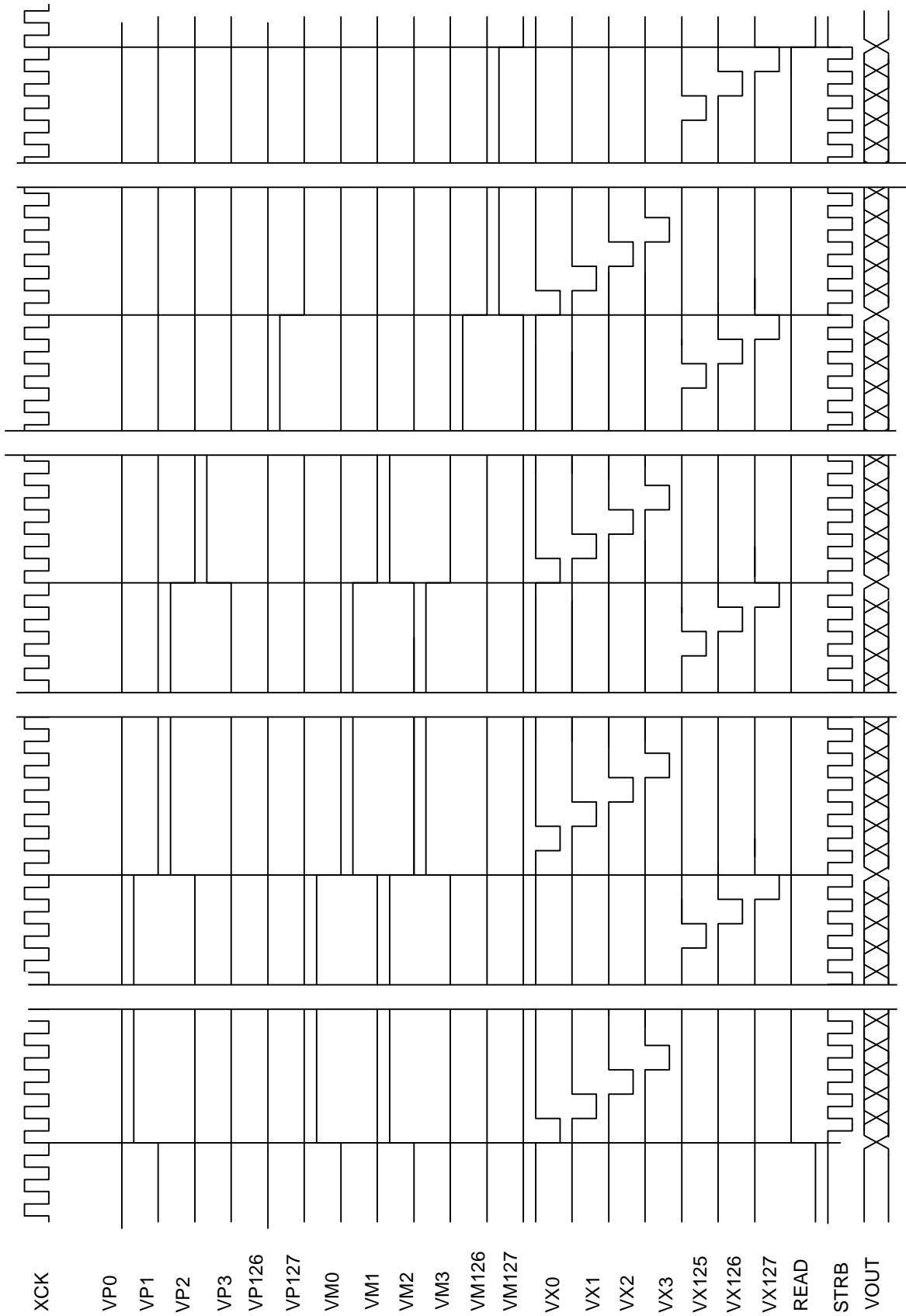
Drive Timing Chart (X Projection)

XCK
START
VC[127:0]
VXC0
VXC2
VXC3
VXC125
VXC127
VP[127:0]
VX0
VX1
VX2
VX3
VX124
VX125
VX126
VX127
READ
STRB
VOUT

Exposure time

FFFF
0000000
00000000
000000000
0000000000
FFFFF
FFFFFFFF
FFFFFFFFF
FFFFFFFF
00000000
0000000
FFFFFFFF
FFFFFF
00000000
00000000

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Ver. 2. 2. 3
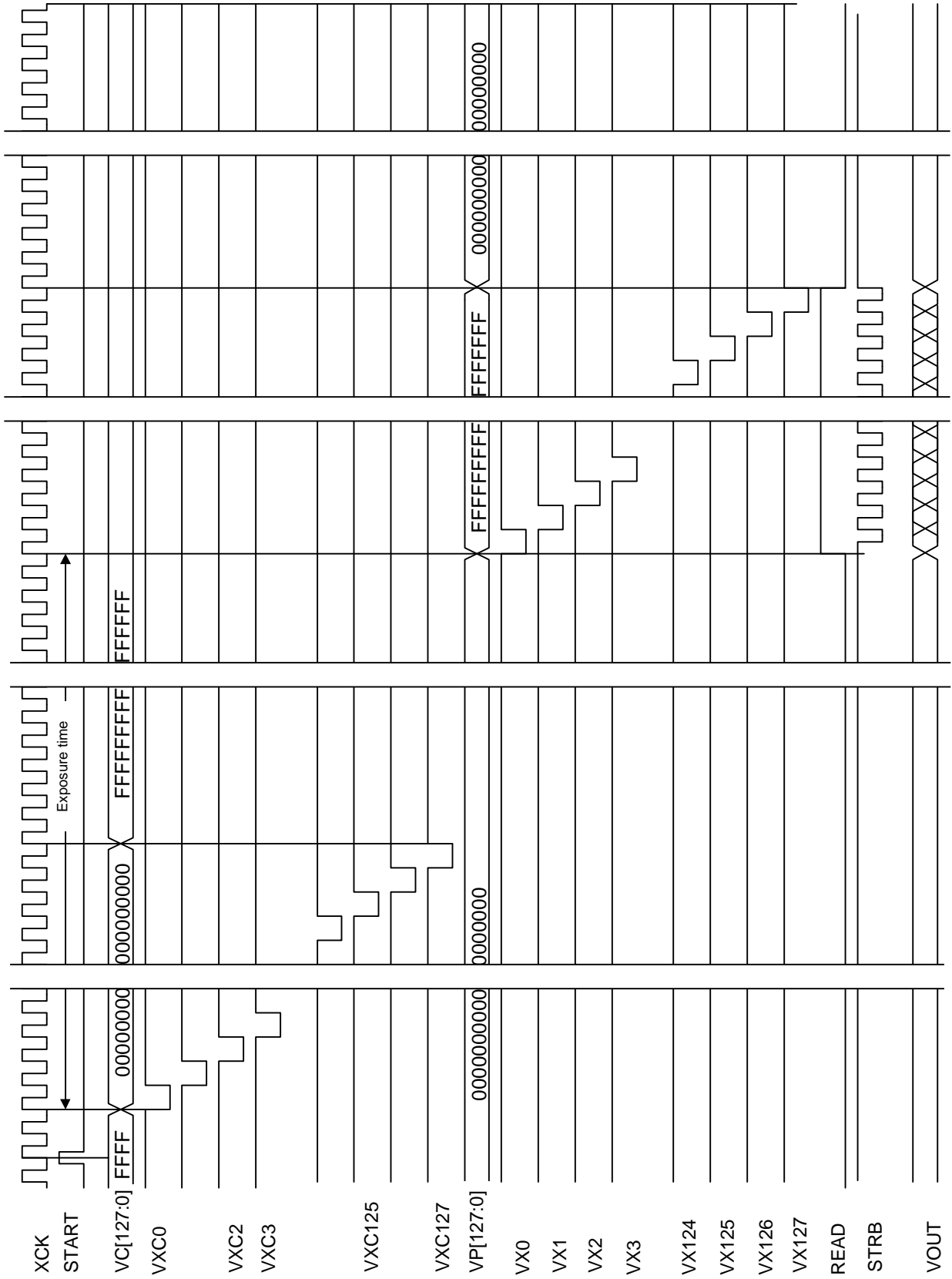
Drive Timing Chart (Y Projection)

| XCK |
| START |
| VXC[127:0] |
| VC0 |
| VC1 |
| VC2 |
| VC3 |
| VC125 |
| VX[127:0] |
| VP0 |
| VP1 |
| VP2 |
| VP3 |
| VP124 |
| VP125 |
| VP126 |
| VP127 |
| READ |
| STRB |
| VOUT |

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Ver. 2. 2. 3
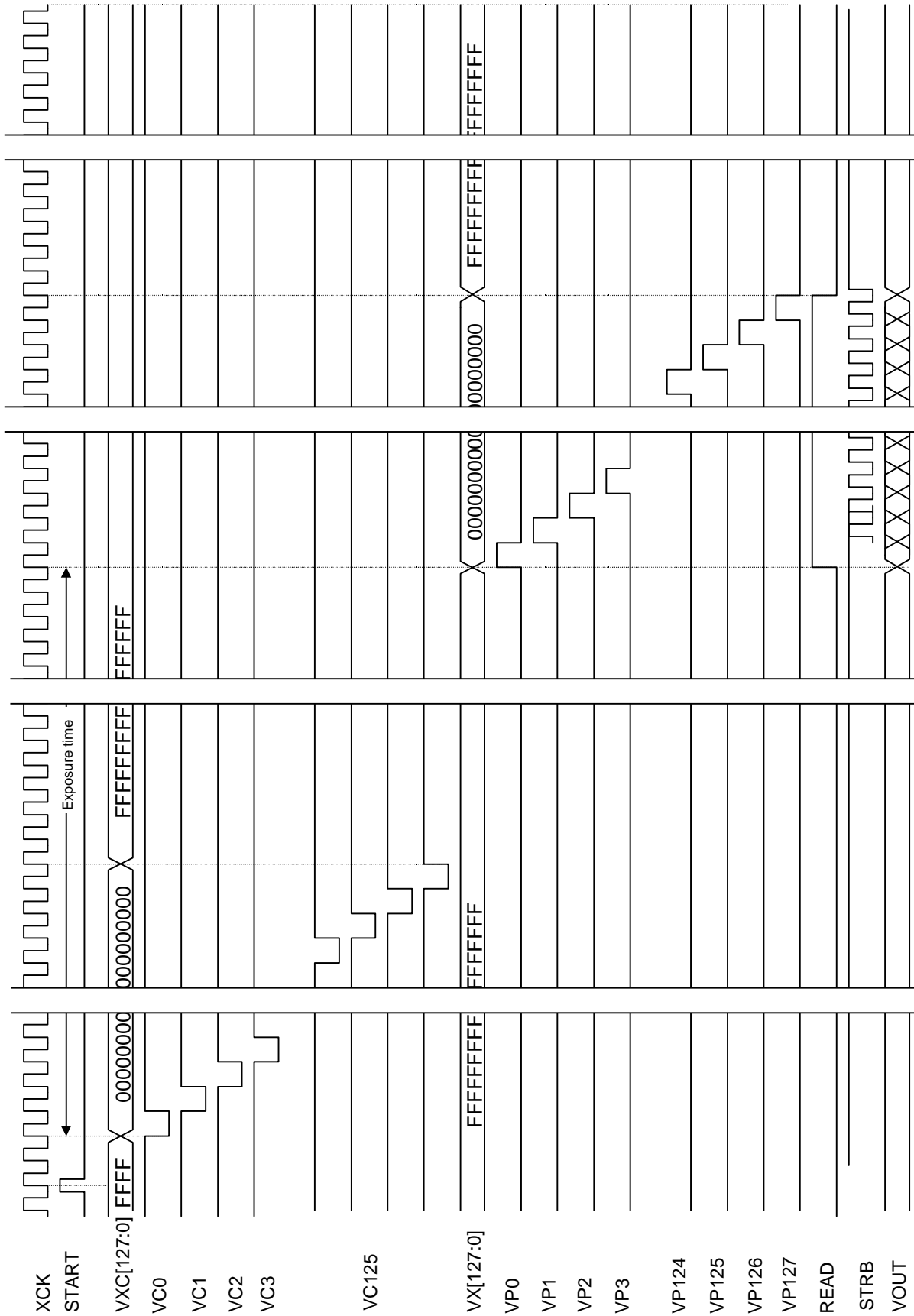
Drive Timing Chart (Read-only Mode)

XCK

START

READ

VOUT

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Ver. 2. 2. 3
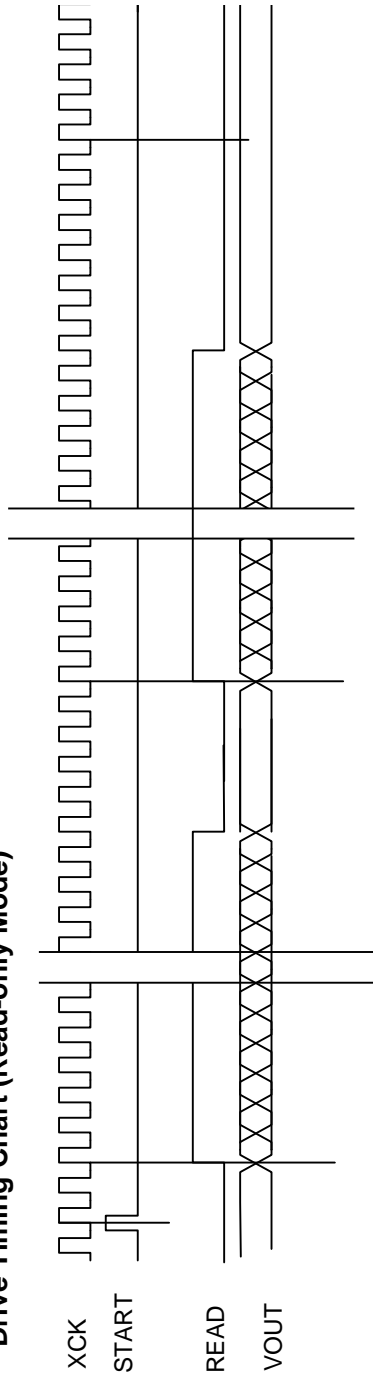
Details of revision

07/22/1998

Place of revision	Details of revision		

Table at page 5	Typical value changed.	AI$_{DD}$ circuit current
		  Positive image mode 2 mA → 3 mA
		  Two-dimensional edge enhancement 50% mode
		  3 mA → 3.5 mA
		  Projection mode 3 mA → 4 mA	

7th line at page 8	Document corrected.	Register (× 8) → Register (× 10)	
Description after 7th line at page 8	Document added.	If TADD is "H" ... If TADD is "L"	
Table at page 9	Document corrected.	Automatic black level calibration, "L" active → Automatic black level calibration, "H" active	
11th line at page 14	Document corrected.	When the AZ register is "L"→ When the AZ register is "H"	
Table at page 14	Description modified.	Enable → Disable Disable → Enable	
Figure 7 at page 14	Logical symbol modified.	AZ input Negative logic → Positive logic	
5th line at page 15	Document corrected.	The AZ register is "L" and → The AZ register is "H" and	
27th line at page 17	Document added.	In this case, a clamp circuit cannot be used.	
32th line at page 20	Document added.	Upon executing the projection, the automatic black level calibration AZ register ...	
Figure 15 at page 21	Logical symbol modified.	AZ input Negative logic → Positive logic	
Figure 16 at page 22	Logical symbol modified.	AZ input Negative logic → Positive logic	
Figure 16 at page 22	Description modified.	DZ AZ	

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Ver. 2. 2. 3