

DIGITAL LOGIC & MICROPROCESSOR

[AExE02]

2.1 DIGITAL LOGIC

Number System: A number system is a writing system for expressing numbers. There are several different number systems, including the following:

Number system is a basis for counting various items. On hearing word ‘number’, all of us immediately think of the familiar decimal number system with its 10 digits: 0, 1, 2, 3, 4, 5, 6, 7, 8 and 9.

Number system refers to the digits, its arrangements, positional value and base of number system.

Introduction to positional and non-positional number system

In positional number system, each digit of a number has its unique positional weight or place value. Examples of positional number system are decimal, binary, octal, hexadecimal etc. In non-positional number system, each digit/symbol of a number has no positional weight or place value. Example of non-positional number system is Roman Number System.

There are basically two number systems

1. Non-positional Number System
2. Positional Number system

1. Non-Positional Number System:

Non positional number systems were used in early days of human civilization. People used to count any things on fingers. When ten fingers were not adequate, stones, pebbles, or sticks were used to indicate the values. In this system the symbols such as

I for 1,	II for 2
III for 3	III for 4
IIII for 5 etc....	

2. Positional Number System:

The positional number system is one in which the position of a number represents different values depending upon the position they occupy in the number. There are only few symbols are used. And the value of each digit is determined by three considerations.

1. The digit itself
2. The position of the digit in the number
3. The base of the number system.

A number with radix r is represented by a string of digits as below: the general form of all number can be written as a general form:

$$\text{MSB} - (A_{n-1}) + A_{n-2} + A_{n-3} \dots + A_2 + A_1 + A_0 \cdot A_{-1} + A_{-2} \dots + A_{-m+1} + (A_{-m}) \rightarrow \text{LSB}$$

$$(\text{Number}) = \left(\sum_{i=0}^{i=n-1} A_i \right) + \left(\sum_{j=-m}^{j=-1} A_j \right)$$

(Integer Portion) + (Fraction Portion)

Where ($0 < A_i < r$) each symbol for a particular base system.

For $r = 10$ (decimal number system) A_i will be one of 0, 1, 2, 3, 4, 5, 6, 7, 8, 9. The subscript i gives the position of the coefficient and hence the weight r by which the coefficient must be multiplied.

- A_{n-1} is the MSD (Most Significant Digit)
- A_{-m} is the LSD (Least Significant Digit)

A digit/bit having maximum positional weight is called Most Significant Digit (MSD)/Most Significant Bit (MSB) and a digit having minimum positional weight is called Least Significant Digit (LSD)/Least Significant Bit (LSB). In other words, the left most digit or bit is called MSD or MSB and the right most digit or bit is called LSD or LSB.

The characteristics of positional number systems are

- The value of the base determines the total number of different symbols or digits available in the number system and the first digit is always zero (0).
- The maximum value of a single digit is always equal to one less than the value of the base.

Types of Positional Number System

1. Decimal Number System
2. Binary Number System
3. Octal Number System
4. Hexadecimal Number System

1. Decimal Number System

A number system having base 10 is called decimal number system
Following are the characteristics of a decimal number system.

- Uses ten digits 0, 1, 2, 3, 4, 5, 6, 7, 8 and 9.
- Called base 10 number system.
- Radix (r) = 10
- Symbols = 0 through $r-1 = 0$ through $10-1 = \{0, 1, 2, \dots, 8, 9\}$
- Each position in a decimal number represents a 0 power of the base (10). Example: 10^0
- Last position in a decimal number represents an x power of the base (10).

2. Binary Number System

Binary number system is one whose base is 2. That means there is only two symbols or digits (0 and 1) are used.

A number system having base 2 is called binary number system

Following are the characteristics of a binary number system.

- Uses two digits, 0 and 1.
- Called base 2 number system
- Radix (r) = 2
- Symbols = 0 through $r-1$ = 0 through 2-1 = {0, 1}
- Each position in a binary number represents a 0 power of the base (2). Example: 2^0
- Last position in a binary number represents an x power of the base (2). Example: 2^x where x represents the last position - 1.
- Digits in a binary number are called bits (Binary digits).

3. Octal Number System

Octal number system is one whose base is 8. Eight symbols or digits (0, 1, 2, 3, 4, 5, 6 and 7) are used.

A number system having base 8 is called octal number system

Following are the characteristics of an octal number system.

- Uses eight digits 0,1,2,3,4,5,6 and 7.
- Called base 8 number system.
- Radix (r) = 8
- Symbols = 0 through $r-1$ = 0 through 8-1 = {0, 1, 2...6, 7}
- Each position in an octal number represents a 0 power of the base (8). Example: 8^0
- Last position in an octal number represents an x power of the base (8). Example: 8^x where x represents the last position - 1.

The decimal equivalent of an octal number 360 (written 360_8) is

4. Hexadecimal Number System

Hexadecimal number system is one with base is 16. That means there is 16 symbols or digits (0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E and F) are used. The first ten digits are decimal number and the remaining six digits are denoted by the symbol A, B, C, D, E and F representing the decimal values 10, 11, 12, 13, 14, and 15.

A number system having base 16 is called Hexa-Decimal number system

Following are the characteristics of a hexadecimal number system.

- Uses 10 digits and 6 letters, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E and F.
- Letters represents numbers starting from 10. A = 10, B = 11, C = 12, D = 13, E = 14, F = 15.
- Called base 16 number system.
- Radix (r) = 16

- Symbols = 0 through r-1 = 0 through 16-1 = {0, 1, 2...9, A, B, C, D, E, F}
- Each position in a hexadecimal number represents a 0 power of the base (16)
- Example – 16⁰
- Last position in a hexadecimal number represents an x power of the base (16)
- Example – 16^x where x represents the last position - 1

NUMBER BASE CONVERSION SYSTEM

Table: Four-bit Binary numbers with their Octal values, Decimal values and Hexadecimal values.

Decimal Number (base - 10)	Binary Number (base - 2)	Octal Number (base - 8)	Hexadecimal Number (base - 16)
0	0000	0	0
1	0001	1	1
2	0010	2	2
3	0011	3	3
4	0100	4	4
5	0101	5	5
6	0110	6	6
7	0111	7	7
8	1000	10	8
9	1001	11	9
10	1010	12	A
11	1011	13	B
12	1100	14	C
13	1101	15	D
14	1110	16	E
15	1111	17	F

CASE 1: Conversion from base-r system to decimal number system

The base r can be binary (r = 2) or octal (r = 8) or hexadecimal (r = 16) or any other. The general expression is:

$$(Number)_r = A_{n-1}r^{n-1} + A_{n-2}r^{n-2} + A_{n-3}r^{n-3} + \dots + A_1r^1 + A_0r^0 + A_{-1}r^{-1} + \dots + A_{-m}r^{-m}$$

$$(Number)_r = \left(\sum_{i=0}^{i=n-1} A_i r^i \right) + \left(\sum_{j=-1}^{j=-m} A_j r^j \right)$$

(Integer Portion) + (Fraction Portion)

CASE 2: Conversion from decimal to base-r system

The base r can be binary (r = 2) or octal (r = 8) or hexadecimal (r = 16) or any other.

1. Separate the number into integer part and fractional part
2. Divide “decimal integer part” by base r repeatedly until the quotient becomes zero and storing remainders at each step

3. Multiply "decimal fractional part" by r and accumulate the integer digits so obtained
4. Combined the accumulated results and parenthesis, the whole result with subscript r.

CASE 3: Binary to Octal & Hexadecimal and vice versa

A conversion from a binary number system to octal number system and hexadecimal number system plays an important in digital computers.

- a. Binary to octal and vice versa
 - b. Binary to hexadecimal and vice versa
- a. Binary to Octal and vice versa**

An octal number is represented by at least three bits of binary numbers. So, each digits of an octal number is represented by at least three bits of binary numbers. ($8 = 2^3$)

While converting a binary number to an octal number system a binary number are grouped into the multiple of three digits to represent its equivalent octal number. If there are integer part and a fractional part in the given binary number then the integer parts of a binary number is grouped into three bits from right side to left side and if the integer part of a binary number is not a multiple of three bits then '0' is append in-front of the number. The fractional part of a binary number is grouped from left side to right side and if it is not a multiple of three bits then '0' is append at the end of a fractional part. ($2^3 = 8$)

- b. Binary to Hexadecimal and vice versa**

A hexadecimal number is represented by at least four bits of binary numbers. So, each digits of a hexadecimal number is represented by at least four bits of binary numbers. ($16 = 2^4$)

While converting a binary number to a hexadecimal number system a binary number are grouped into the multiple of four digits to represent its equivalent hexadecimal number. If there are integer part and a fractional part in the given binary number then the integer parts of a binary number is grouped into four bits from right side to left side and if the integer part of a binary number is not a multiple of four bits then '0' is append in-front of the number. The fractional part of a binary number is grouped from left side to right side and if it is not a multiple of four bits then '0' is append at the end of a fractional part. ($2^4 = 16$)

COMPLEMENT

Complements are used in the digital computers in order to simplify the subtraction operation and for the logical manipulations. For each radix-r system (radix r represents base of number system) there are two types of complements. There are two types of complements for each base-r system.

1. The r's complement
2. The (r-1)'s complement

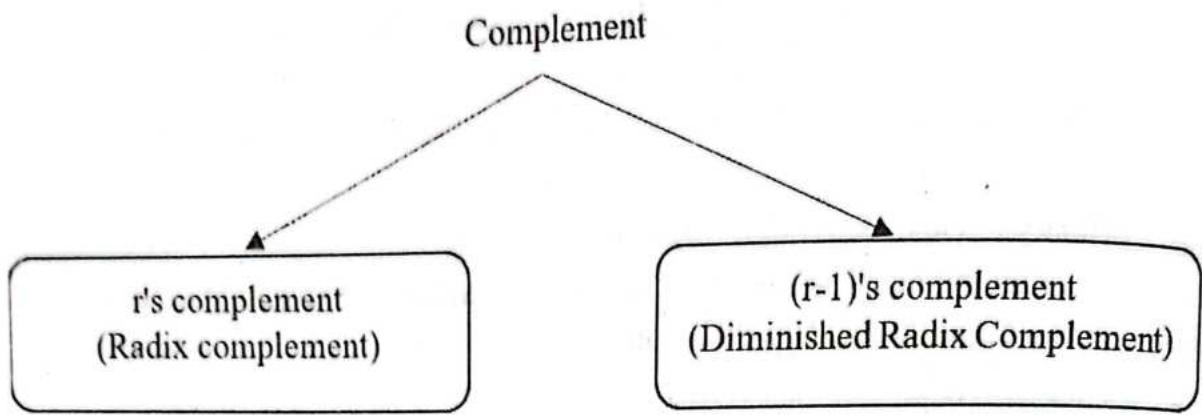


Figure: Complement

For decimal number system the complements are 10's and 9's complement. 2's and 1's complement for binary system. 8's and 7's complement for octal number system and so on.

Table: r's and (r-1)'s Complement

S.N.	Complement	Description
1	Radix Complement	The radix complement is referred to as the r's complement
2	Diminished Radix Complement	The diminished radix complement is referred to as the (r-1)'s complement

1. The r's complement

- Given the positive number N in base r with integer part of n digits, the r's complement of N is defined as $r^n - N$ for $N \neq 0$ and 0 for $N = 0$;
 - ❖ r's Complement (radix complement)
 - ❖ r's complement of a number N is defined as $r^n - N$

Where N is the given number

- ❖ r is the base of number system
- ❖ n is the number of digits in the given number
- To get the r's complement fast, add 1 to the low-order digit of its (r-1)'s complement.

Example:

- 10's complement of 835_{10} is $164_{10} + 1 = 165_{10}$
- 2's complement of 1010_2 is $0101_2 + 1 = 0110_2$

2. The (r-1)'s complement

- Given a positive number N in base r with an integer part of n digits and a fraction part of m digits, the (r-1)'s complement of N is defined as $(r^n - r^{-m} - N)$
- (r-1)'s Complement (diminished radix complement)
- (r-1)'s complement of a number N is defined as $(r^n - 1) - N$
 - ❖ Where N is the given number
 - ❖ r is the base of number system
 - ❖ n is the number of digits in the given number
- To get the (r-1)'s complement fast, subtract each digit of a number from (r-1).

Example:

- 9's complement of (835)₁₀ is (164)₁₀ (Rule: $(10^n - 1) - N$)
- 1's complement of (1010)₂ is (0101)₂ (bit by bit complement operation)

Subtraction with complements

When subtraction is implemented with digital hardware, this method is found to be less efficient than the method that uses complements. Complements are used in digital computers for simplifying the subtraction operation and for logical manipulation. Using complements, all the arithmetic operations can be performed in the form of addition. There are two types of compliments: $(r - 1)$'s complement and r 's complement where r is base of a number system. So, for binary number system, $r = 2$ hence, it has two complements- 1's complement and 2's complement. Likewise, for decimal number system, $r = 10$ hence it also has two complements-9's complement and 10's complement.

The subtraction of two n-digit unsigned numbers M - N in base-r can be done as follows:

1. Add the minuend M to the r 's complement of the subtrahend N. This performs

$$\begin{aligned} &= M + (r^n - N) \\ &= M - N + r^n. \end{aligned}$$

2. If $M \geq N$, the sum will produce an end carry, r^n , which is discarded; what is left is the result $M - N$.
3. If $M < N$, the sum does not produce an end carry and is equal to $r^n - (N - M)$, which is the r 's complement of $(N - M)$. To obtain the answer in a familiar form, take the r 's complement of the sum and place a negative sign in front it.

Things to Remember:

- A system which process a continuous time variant signal is called analog system and a system which process a discrete time variant signal is called digital system.
- The digital system contains devices such as logic gates, flip-flop, shift register and counters etc.
- A digital computer is an electronics device that read the data from the environment through an input device, store them in a memory, process them according to the command given by the user (programmer) and display the result or output to the environment through an output unit. A digital computer contains
 1. Input Unit
 2. Output Unit
 3. Storage Unit
 4. Central Processing Unit
- Number system is a basis for counting various items or data. The most popular and daily used number system is decimal number system. Number system is mainly classified in two type
 1. Non-Positional Number System

2. Positional Number System

- Non positional number system were used in early days of civilization. In positional number system the position of a number doesn't matter. For example, counting items on fingers, pebbles, marking a line on the wall etc.
- Positional number system is the most popular and daily used number system. In positional number system the position of a number represents different values depending upon the position they occupy in the number. Positional numbers are classified as follow:
 - Binary Number System
 - Octal Number System
 - Decimal Number System
 - Hexadecimal Number System
- Binary number system is one whose base is 2. i.e. only two symbols are used 0 and 1.
- Octal number system is one whose base is 8. i.e. only eight symbols are used 0, 1, 2, 3, 4, 5, 6 and 7.
- Decimal number system is one whose base is 10. i.e. only ten symbols are used 0, 1, 2, 3, 4, 5, 6, 7, 8 and 9.
- Hexadecimal number system is one whose base is 16. i.e. only sixteen symbols are used 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E and F.
- Note that the positional number system the symbols always begins with 0 and end with one less than the base system.
- A binary number is a weighted number in which the weight of each whole number digits is a positive power of two and the weight of each fractional digit is a negative power of two.
- Various system uses different number system, human being uses decimal number system in their day to day life. So, it is necessary to convert a number from one base system to another. While converting a number system following situations are occur".
 - Conversion from base-r system to decimal system
 - Conversion from decimal system to base-r system
 - Conversion from binary system to Octal system and Hexadecimal system and vice versa
- A binary number can be converted into decimal number by summing decimal values of the weights of all the 1s in the binary number.
- A decimal whole number can be converted to binary by using the sum-of-weights or the repeated division by -2 method.
- A decimal fraction can be converted to binary by using the sum-of- weights or the repeated multiplication-by-2-method.
- One hexadecimal digit represents a 4-bit binary number, and its primary usefulness is in simplifying bit patterns and making them easier to read.

- Complement in digital computer are used for subtraction operation. Binary subtraction can be accomplished with addition by using the 1's or 2's complement method.
- There are two types of complements for each base-r system
 - The r's complement
 - The $(r-1)$'s complement
- The 1's complement of a binary number is derived by changing 1s to 0s and 0s to 1s.
- The 2's complement of a binary number can be derived by adding 1 to the 1's complement.
- The basic rules for binary addition are as follows:
 - ❖ $0 + 0 = 0$
 - ❖ $0 + 1 = 1$
 - ❖ $1 + 0 = 1$
 - ❖ $1 + 1 = 10$
- The basic rules for binary subtraction are as follows:
 - ❖ $0 - 0 = 0$
 - ❖ $1 - 1 = 0$
 - ❖ $1 - 0 = 1$
 - ❖ $10 - 1 = 0 - 1$ with a borrow of 1.
- Positive binary number is represented by a 0-sign bit and A negative binary number is represented by a 1 sign bit.
- When numbers, alphabets or words are represented by a specific group of symbols, we can say that they are encoded. The group of symbols used to encode them is called codes. The codes are classified as follows
 1. Weighted Codes
 2. Non-weighted Codes
 3. Reflective Codes
 4. Sequential Codes
 5. Alphanumeric Codes
 6. Error detecting and correcting Codes
- In weighted codes, each digit position of the number represents a specific weight. For example, in decimal code,
- In this code each decimal digit is represented by a 4-bit binary number. BCD is a way to express each of the decimal digits with a binary code.
- Excess-3 code is a modified form of a BCD number. The excess-3 code can be derived from the natural BCD code by adding 3 to each coded number.
- Gray code is a non-weighted code and is a special case of unit-distance code.
- When the digital information in the binary form is transmitted from one circuit or system to another circuit or system an error may occur

- Error detection methods are parity checking, checksum error detection and cyclic redundancy check.
- A parity bit is used to detect an error in a code
 1. **Even Parity:** In even parity the added parity bit will make the total number of 1s an even amount.
 2. **Odd Parity:** In odd parity the added parity bit will make the total number of 1s an odd amount.
- The hamming code is the single bit error correction method using redundant bits.
- The CRC (Cyclic Redundancy Check) is based on polynomial division using modulo-2.
- Alphanumeric codes are called character codes and binary codes are used to represent alphanumeric data.
- ASCII (American Standard Code for Information Interchange) code is very popular code used in all personal computers and workstation. It is a standard binary code for alphanumeric character.
- Unicode typically uses 16 bits to store a character. This allows for the unique representation of characters in all languages and platforms.
- EBCDIC (Extended Binary Coded Decimal Interchange Code) is an eight bit character encoding used mainly on IBM mainframe and IBM mid-range computer operating systems.
- Integrated Circuit (IC) is a silicon chip contains the electrical components such as transistor, diodes, resistors and capacitor. On the basis of functions ICs are classified as
 1. Analog or Linear ICs
 2. Digital or Logic ICs
 3. Hybrid ICs
- In order to protect ICs from external environment and to provide mechanical protection, various forms of encapsulation are used for integrated circuit. On the basis of the packing of integrated circuits it is classified into two.
 1. Flat Package
 2. Dual in Line

In 1965 Gordon Moore, who was cofound Intel Corporation in 1968 said that the components fabricated into an Integrated Circuit (IC) is double in every 18 months.

Logic Levels

- In digital logic, a logic level refers to the specific voltage or current used to represent binary values of 0 and 1. In other words, it is the electrical representation of a binary digit (bit).
- The most commonly used logic levels in digital electronics are TTL (Transistor-Transistor Logic) and CMOS (Complementary Metal-Oxide-Semiconductor).
- In TTL logic, a high logic level is typically represented by a voltage of around 2-5 volts, while a low logic level is represented by a voltage of around 0 volts.

- In CMOS logic, a high logic level is typically represented by a voltage close to the power supply voltage (e.g., 5 volts), while a low logic level is represented by a voltage close to 0 volts.

Logic Gates

A logic gate is an elementary building block of a digital circuit. Most of the logic gates have two inputs and one output. Each input and outputs are represented by binary values (0 for “false” and 1 for “true”).

The electronic gate is a circuit that is able to operate on a number of binary inputs in order to perform a particular logical function

In most logic gates, the low state is approximately zero volts (0 V), while the high state is approximately five volts positive (+5 V).

Logic gates are the basic element that makes up a digital system. The types of gates available are the NOT, AND, OR, NAND, NOR, exclusive-OR, and the exclusive -NOR. Expect for the exclusive- NOR gate, are they available in monolithic integrated circuit form.

1. Basic Logic Gates

- a. OR Gate
- b. AND Gate
- c. NOT Gate

2. Universal Logic Gates

- a. NAND Gate
- b. NOR Gate

3. Derived Logic Gates/ Arithmetic Gate

- a. XOR Gate
- b. EX-Nor Gate

Basic Logic Gates

1. OR Gate

- The OR gate is a basic logic gate whose output is “true” or “high” if any one of the inputs are “true” or “high” otherwise the output is “false” or “low”. I.e. the output is “false” or “low” if all the inputs are “false” or “low”.

Things to Remember

For a 2-input OR gate, output Y is HIGH when either input A or input B is HIGH, or when both A and B are HIGH; Y is low only when both A and B are low.

- The OR gate performs logical addition, more commonly known as the OR function. An OR gate has two or more inputs and one output, as indicated by the standard logic symbol in Figure 2.20 where OR gates with two and four inputs are illustrated.

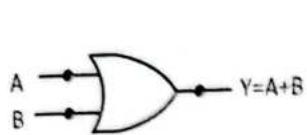


Figure (a) Two inputs OR gate

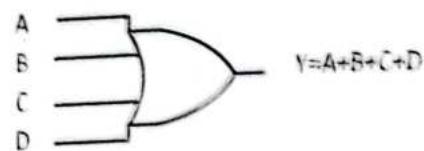


Figure (b) Four inputs OR gate

Table: Truth Table of OR gate

Inputs		Output
A	B	$Y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

2. AND Gate

- The AND gate is one of the basic gates that can be combined to form any logic function. An AND gate can have two or more inputs and performs what is known as logical multiplication.
- An AND gate produces a HIGH output only when all of the inputs are HIGH. When anyone of the input is LOW, the output is LOW.

For 2 input AND Gate, output Y is high only when inputs A and B are HIGH; Y is Low when either A or B is LOW, or when both A and B are LOW.

- The AND gate performs logical multiplication, more commonly known as the AND function. The AND gate may have two or more inputs and a single output, as indicated by the standard logic symbols shown in the Figure.

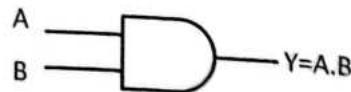


Figure: Two Input AND Gate

The Figure illustrates a two-input AND gate with all four possibilities of input combinations, and the resulting output for each.

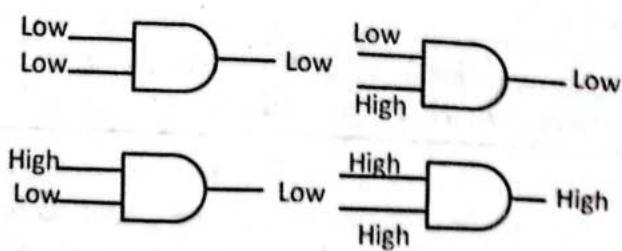


Figure: Four possible inputs for two input AND gate and resulting outputs

The total number of possible combinations of binary input to a gate is determined by the following formula:

$$N = 2^n$$

Where N is the number of possible input combination and n is the total number of input variables. To illustrate,

For 2 input variables, $N = 2^2=4$ Combinations

For 3 input variables, $N = 2^3=8$ Combinations

For 4 input variables, $N = 2^4=16$ Combinations

Table: Truth table for 2 input AND gate

Inputs		Output
A	B	$Y = A \cdot B$
0	0	0
0	1	0
1	0	0
1	1	1

3. NOT Gate/ Inverter

- The NOT gate or the inverter is a basic logic gate whose output is just inverse of the input. NOT gate have a single input and a single output. The output is “true” if the input is “false” and the output is “false” if the input is “true”.

When the input is LOW, the output is HIGH; when the input is HIGH, the output is LOW, thereby producing an inverted output pulse.

- The Figure 2.28 shows the symbol for the inverter.



The bubble [o] appearing on the output is the negation (inversion) indicator.

Figure: NOT Gate

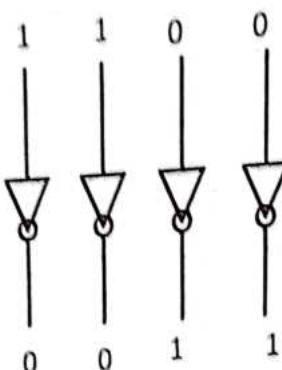
Table: Truth Table of NOT gate

Inputs		Outputs
A		$F = \bar{A}$
0		1
1		0

An Application:

Following Figure shows a circuit for producing the 1's complement of 4-bit binary number. The bits of the binary number are applied to the inverter inputs and the 1's complement of the number appears on the outputs.

Binary Number



1's Complement

Figure: Example of a 1's complement circuit using inverters

Universal Gate

- A universal gate is a gate which can implement any Boolean function without using any other types of gates. NAND and NOR gates are known as universal gates.
- Hence any Boolean function can be implemented using only NAND and NOR gate.
- NAND gate and NOR gates are the universal gates.
- The NAND gate and NOR gates are easier to fabricate and economical and can be used in all logic circuit.
- By connecting them together in various combinations the three basic gate types of AND, OR and NOT function can be formed using these gates.

NAND and NOR gates are called Universal Gate because all the other basic gates (NOT, AND and OR gate) can be constructed by using NOR gate only and by using NAND gate only.

1. NAND Gate

The NAND gate is a universal gate whose output is "true" if any one or all of the inputs to the gate is "false". The output of NAND gate is "false" if all the inputs to the gate is "true".

The Boolean function can be implemented using only NAND gates. By using NAND gate we can derive basic OR gate, AND gate and NOT gate.

Things to Remember

For a 2-input NAND gate, output F is LOW only when inputs A and B are HIGH: F is HIGH when either A or B is LOW, or when both A and B are LOW.



Figure 2-input NAND Gate

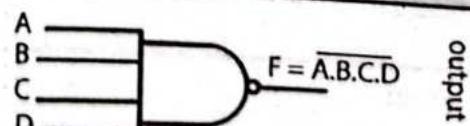


Figure: (b) 4-input NAND Gate

The NAND gate is the combination of two gates (One AND gate and an inverter). The inputs are first ANDed and then it is inverted as shown in below.

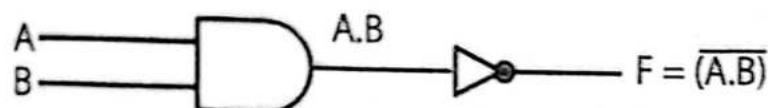


Table: Truth Table of NAND gate

Inputs		Outputs
A	B	Z = (A · B)
0	0	1
0	1	1
1	0	1
1	1	0

2. NOR Gate

For a 2-input NOR gate, output F is LOW when either input A or input B is HIGH, or when both A and B are HIGH: F is HIGH only when both A and B are LOW.

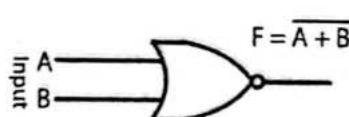


Figure: (a) 2-input NOR Gate

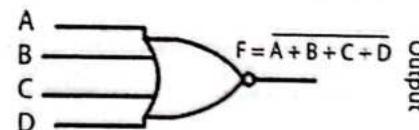


Figure: (b) 4-input NOR Gate

The NOR gate is the combination of two gates (One OR gate and an inverter). The inputs are first ORed and then it is inverted as shown in below.

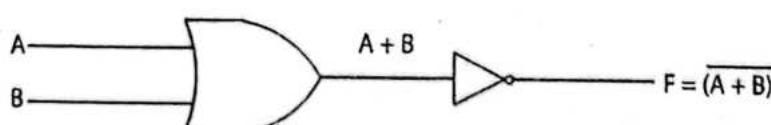


Figure: AND gate with Inverter

Table: Truth Table

Inputs		Output
A	B	F = (X + Y)̄
0	0	1
0	1	0
1	0	0
1	1	0

Derive Gate/ Arithmetic Gate/Exclusive Gate

1. XOR Gate
2. XNOR Gate

1. XOR Gate

The XOR gate is a derived gate in which the output is “true” if either, but not both, of the inputs are “true”. The output is “false” if both inputs are “false” or if both inputs are “true”.

For an exclusive -OR gate, output F is HIGH when input A is LOW and input B is HIGH, or when input a is HIGH and input B is LOW; F is LOW when A and B are both HIGH or both LOW.

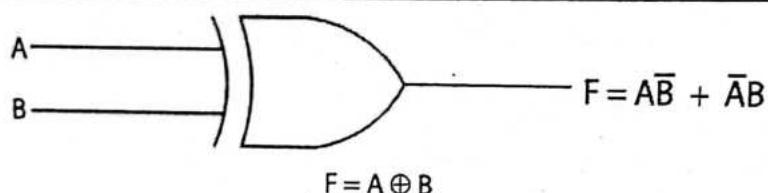


Figure: Logic symbol of 2 input Ex-OR Gate

Table: Truth Table of 2 input XOR gate

Inputs		Output
A	B	$F = A \overline{B} + \overline{A} B$
0	0	0
0	1	1
1	0	1
1	1	0

The Ex-OR gate can be constructed by using basic gates as shown in logic circuit below.

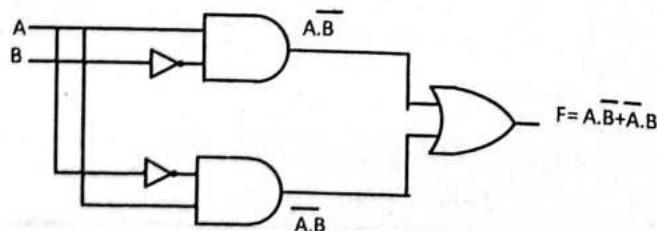


Figure: Circuit diagram of 2 input XOR

2. XNOR Gate

The XNOR gate is a combination of XOR gate followed by an inverter. Its output is “true” if the inputs are the same and “false” if the inputs are different.

For an exclusive-NOR gate, output F is LOW when input a is LOW and input B is HIGH, or when A is HIGH and B is LOW; F is HIGH when A and B are both HIGH or both LOW.



Figure: Logic Symbol of 2 input EXNOR gate

Table: Truth Table of XNOR gate

Inputs		Output
A	B	$F = AB + \overline{A} \overline{B}$
0	0	1
0	1	0
1	0	0
1	1	1

The Ex-NOR gate can be constructed by using the basic gates only as shown in logic circuit below.

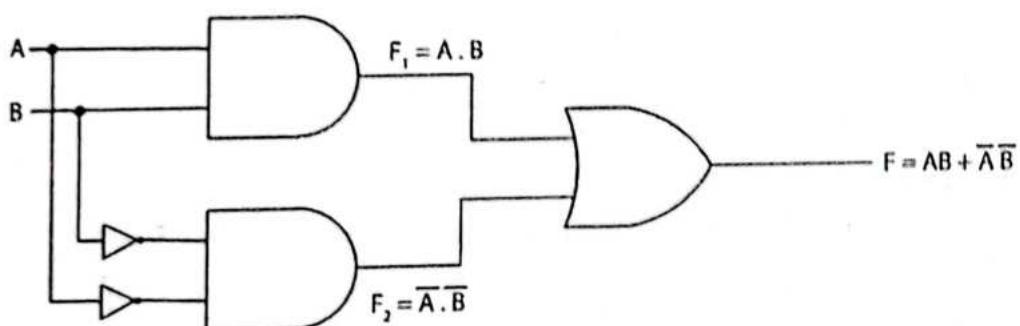


Figure: Circuit diagram of 2 input EXNOR gate

Boolean algebra:

Boolean Algebra is a mathematical system that uses binary variables (i.e., variables that can have only two values: 0 or 1) and logical operations (such as AND, OR, NOT, etc.) to describe and analyze logic circuits. It was invented by the mathematician George Boole in the 19th century and is used in many areas of computer science, including computer hardware design, digital electronics, and computer programming.

In Boolean Algebra, binary variables are used to represent logical values (e.g., true or false, on or off, etc.). The logical operations in Boolean Algebra are used to manipulate these binary variables and to build more complex expressions. The basic operations in Boolean Algebra are AND, OR, and NOT, which can be used to build more complex expressions using De Morgan's laws and other rules.

A Boolean function is an algebraic expression formed with Boolean variables (having values true or 1 and false or 0) and the logical operators (i.e. OR, AND, and NOT).

K-map is in fact a visual diagram of representing all possible ways a Boolean function may be expressed.

Boolean Functions: Terminology

$$F(a,b,c) = \bar{a}bc + ab\bar{c} + a\bar{b} + c$$

Variable

- Represents a value (0 or 1). Three variables are a, b and c.

Prime Implicant:

- A prime implicant is product or sum term obtain by combining the maximum possible number of adjacent squares (minterm/maxterm) in the map.

Essential Prime Implicant:

- If a minterm max term in a sequence is covered by only 1 prime implicant is said to be essential prime implicant.

Literal

- Appearance of variable either in complemented form or in an un complemented form
- Nine literals are; $\bar{a}, b, c, a, \bar{b}, \bar{c}, a, b, c$

Product Term:

- It is a term where literals are ANDed.
- Example: $\bar{a} \bar{b}$, $a c$, abc ,

Minterms:

- A Minterm is a special product (ANDing terms) of literals, in which each input variable appears exactly once. A function with n input variables has 2^n Minterms.
For example a three variable function like $F(X, Y, Z)$ has 8 Minterms ($2^3 = 8$). They are

$$\bar{A}\bar{B}\bar{C}, \bar{A}\bar{B}C, \bar{A}B\bar{C}, \bar{A}BC, A\bar{B}\bar{C}, AB\bar{C}, A\bar{B}C, ABC$$

And each minterm is true for exactly one combination of inputs

Sum Term:

- A term where literals are ORed.

$$\bar{x} + \bar{y}, x + z, x + y + z$$

Maxterms:

- A Maxterm is a special sum (ORing terms) of literals, in which each input variable appears exactly once. A function with n input variables has maximum of 2^n Maxterms.
For example, a three-variable function like $F(X, Y, Z)$ has 8 Maxterms ($2^3 = 8$). They are

$$\bar{A} + \bar{B} + \bar{C}, \bar{A} + \bar{B} + C, \bar{A} + B + \bar{C}, \bar{A} + \bar{B} + C, \bar{A} + B + C, A + \bar{B} + C, A + B + \bar{C}, A + B + C$$

And each maxterm is false for exactly one combination of inputs

Table: Minterms and Maxterms for 3 Binary variables with their symbolic shorthand

Inputs			Minterms		Maxterms	
A	B	C	Terms	Designation	Terms	Designation
0	0	0	$\overline{A} \overline{B} \overline{C}$	m_0	$A + B + C$	M_0
0	0	1	$\overline{A} \overline{B} C$	m_1	$A + B + \overline{C}$	M_1
0	1	0	$\overline{A} B \overline{C}$	m_2	$A + \overline{B} + C$	M_2
0	1	1	$\overline{A} BC$	m_3	$A + \overline{B} + \overline{C}$	M_3
1	0	0	$A \overline{B} \overline{C}$	m_4	$\overline{A} + B + C$	M_4
1	0	1	$A \overline{B} C$	m_5	$\overline{A} + B + \overline{C}$	M_5
1	1	0	$\overline{A} \overline{B} \overline{C}$	m_6	$\overline{A} + \overline{B} + C$	M_6
1	1	1	ABC	m_7	$\overline{A} + \overline{B} + \overline{C}$	M_7

Sum of Product/Sum of Minterms Method

Boolean functions can be expressed as a sum of Minterms or product of Maxterms and are said to be in canonical form. In canonical form every variable appears in every term. An arbitrary logic function can be expressed in following form.

1. Sum of Products (SOP)
2. Product of the Sums (POS)

Sum of Product (SOP)/Sum of Minterms

For n binary input variables there will be 2^n distinct Minterms. The Minterms whose sum defines the Boolean function are those that give the 1's of the function in a truth table. It is sometimes convenient to express the Boolean function in its Sum of Minterms form. If the terms are not in SOP form it can be made so by first expanding the expression into a sum of AND terms. Each term is then inspected to see if it contains all the variables. If any one of the variables is missed then it is ANDed with an expression such as $A + \overline{A}$, where A is one of the missing variables.

Truth Table to Karnaugh Map

A Karnaugh map (K-map) is a graphical tool used to simplify Boolean algebra expressions. It is used to minimize the number of logic gates required to implement a digital circuit, and to simplify the expression of a logical function. The K-map consists of a grid of cells, each representing a possible combination of inputs to a Boolean function. A truth table can be converted into a Karnaugh map (K-map) to simplify the Boolean expression for a logical function. The process of converting a truth table into a K-map involves the following steps:

- Draw the K-map grid
- Fill in the K-map cells

- Group adjacent cells with the same value
- Simplify the expression

Maurice Karnaugh developed Karnaugh maps which are used for minimizing Boolean expression for few variables. These maps are also known as Veitch diagram.

The Boolean expression can be minimized by two different ways:

1. Boolean algebra method
2. Map method

1. Boolean algebra Method

In Boolean algebra method we need better understanding of Boolean laws, rules and theorems. During the process of simplification, we have to predict each successive step. For these reasons, we can never be absolutely certain that an expression simplified by Boolean algebra alone is the simplest possible expression.

In Boolean algebra method we can use grouping, Multiplication by redundant variables and Application of De-Morgan's theorem as given by:

a. Grouping

$$\begin{aligned} &= A + AB + BC \\ &= A(1 + B) + BC \\ &= A + BC \quad [.: 1 + B = 1] \end{aligned}$$

b. Multiplication by redundant variables

Multiply by terms of the form $(A + \overline{A})$ doesn't alter the logic

Such multiplications by a variable missing from a term may enable minimization
 $AB + A\overline{C} + BC$

$$\begin{aligned} &= AB(C + \overline{C}) + A\overline{C} + BC \\ &= ABC + AB\overline{C} + A\overline{C} + BC \\ &= BC(A + 1) + A\overline{C}(B + 1) \\ &= BC + A\overline{C} \quad [.: A + 1 = 1] \end{aligned}$$

c. Application of De-Morgan's theorem

Expressions containing several inversions stacked one upon the other often are simplified by using De-Morgan's law which un-wraps multiple inversions:

$$\begin{aligned} &A\overline{B}\overline{C}((A\overline{B}\overline{C}) + (\overline{ACD}) + B\overline{C}) \\ &= ((\overline{A} + B + \overline{C}) + (\overline{A} + \overline{C} + \overline{D}) + B\overline{C}) \\ &= ((\overline{A} + B + \overline{C} + \overline{D}) + B\overline{C}) \\ &= \overline{AB}\overline{CD} \end{aligned}$$

2. Map method

The map method gives us the systematic approach for simplifying a Boolean expression. The map method, first proposed by Veitch and modified by Karnaugh, hence it is known as the Veitch diagram or the Karnaugh map. The map method is regarded as a pictorial form of a truth table.

Karnaugh Map is a graphical representation of the truth table of the given expression.

Karnaugh Map

a. For one variable and two variables

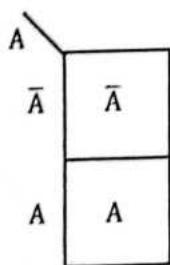
b. Three variables

c. Four variables

a. For one variable and two variables

The basic method is a graphical chart known as Karnaugh map (K-map). It contains boxes called cells. Each cell represents one of the 2^n possible products that can be formed from n variables. Thus a 1 variable map contains $2^1=2$, a 2 variables map contains $2^2 = 4$ cells, a 3 variables map contains $2^3 = 8$ cells, and a 4 variables map contains $2^4 = 16$ cells and so forth.

For One variable

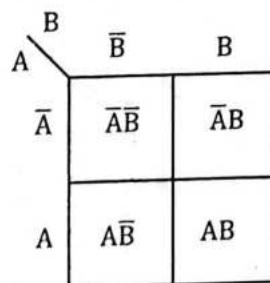


1-variable map is an array of two cells. The value of a binary variable is along the left side as shown in figure above.

(2 cells)

Figure (a): K-map for one variable

For Two Variables



2-variable map is an array of four cells. The value of binary variable A is along the left side and the value of binary variable B is at the top as shown in above figure.

(4 cells)

Figure (b): K-map for two variable

b. For Three Variables

The 3-variable Karnaugh map is an array of eight cells as shown below. Let A, B and C are three binary variables. The binary variable A is along left side and the binary variables B and C are along the top of the map. The cell in the upper left corner has a binary value of 000 and the cell in the lower right corner has a binary value of 110. The product terms that is represented by each cell in the Karnaugh map.

	BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
A	\bar{A}	$\bar{A}\bar{B}\bar{C}$	$\bar{A}\bar{B}C$	$\bar{A}BC$	$\bar{A}B\bar{C}$
A	A	A $\bar{B}\bar{C}$	A $\bar{B}C$	ABC	AB \bar{C}

3-variable map (8 cells)

Figure: K-map for three variable

c. For Four Variables

The 4-variable Karnaugh map is an array of sixteen cells as shown in figure below. Let A, B, C and D are four binary variables. The binary values of A and B are along left side and the values of C and D are across the top of the map. The value of a given cell is the binary values of A and B at the left in the same row combined with the binary values of C and D at the top in the same column. For example, the cell in the upper left corner has a binary value of 0000, the cell in the upper right corner has a binary value of 0010, and the cell in the lower right corner has a binary value of 1010 and so on.

	CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
AB	$\bar{A}\bar{B}$	$\bar{A}\bar{B}\bar{C}\bar{D}$	$\bar{A}\bar{B}\bar{C}D$	$\bar{A}\bar{B}CD$	$\bar{A}\bar{B}C\bar{D}$
$\bar{A}B$	$\bar{A}B\bar{C}\bar{D}$	$\bar{A}B\bar{C}D$	$\bar{A}BCD$	$\bar{A}B\bar{C}\bar{D}$	
AB	AB $\bar{C}\bar{D}$	AB $\bar{C}D$	ABC D	ABC \bar{D}	
$A\bar{B}$	A $\bar{B}\bar{C}\bar{D}$	A $\bar{B}\bar{C}D$	A $\bar{B}CD$	A $\bar{B}C\bar{D}$	

4-variable map (16 cells)

Figure: K-map for four variable

For One variable

A	\bar{A}	\bar{A}	0
A	A	A	1

1-variable map
(2 cells)

Figure (a): K-map for one variable

For Two Variables

B	\bar{B}	B
A	$\bar{A}\bar{B}$	$\bar{A}B$
A	A \bar{B}	AB

2-variable map
(4 cells)

Figure (b): K-map for two variables

For Three Variables

BC		$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
A		$\bar{A}\bar{B}\bar{C}$	$\bar{A}\bar{B}C$	$\bar{A}BC$	$\bar{A}B\bar{C}$
	0	1	3	2	
A	4	5	7	6	

3-variable map

(8 cells)

Figure. (c): K-map for three variable

For Four Variables

CD		$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
AB		$\bar{A}\bar{B}\bar{C}\bar{D}$	$\bar{A}\bar{B}\bar{C}D$	$\bar{A}\bar{B}C\bar{D}$	$\bar{A}\bar{B}CD$
	0	1	3	2	
$\bar{A}B$	4	5	7	6	
AB	12	13	15	14	
$A\bar{B}$	8	9	11	10	

4-variable map

(16 cells)

Figure (d): K-map for four variable

For One variable

A		0	1
	m ₀	0	
1	m ₁	1	

1-variable map

(2 cells)

Figure (a): K-map for one variable

For Two Variables

B		0	1
A		m ₀	m ₁
	m ₂	2	m ₃
1	m ₄	1	m ₅

2-variable map

(4 cells)

Figure (b): K-map for two variable

For Three Variables

BC		00	01	11	10
A		m ₀	m ₁	m ₃	m ₂
	m ₄	m ₅	m ₇	m ₆	
1					

3-variable map

(8 cells)

Figure (c): K-map for three variable

For Four Variables

CD		00	01	11	10
AB		m ₀	m ₁	m ₃	m ₂
	m ₄	m ₅	m ₇	m ₆	
Gray code sequence	00				
	01				
	11	m ₁₂	m ₁₃	m ₁₅	m ₁₄
	10	m ₈	m ₉	m ₁₁	m ₁₀

4-variable map

(16 cells)

Figure (d): K-map for four variable

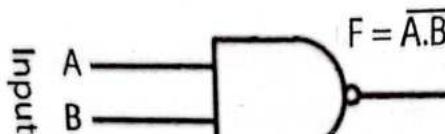
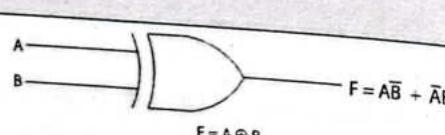
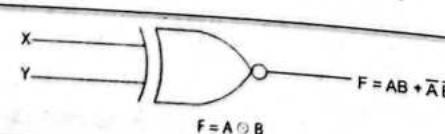
Things to Remember

- Boolean algebra was developed by the English mathematician George Boole. His work was based on the analysis of logic and is contained in his book named "An investigation of the laws of thought on which are founded the Mathematical Theories of Logic and Probabilities", published in 1854.
- Commutative law: $A + B = B + A$
 $AB = BA$
- Associative law: $A + (B + C) = (A + B) + C$
 $A(BC) = (AB)C$
- Distributive law: $A(B + C) = AB + AC$
- Boolean rules:

1. $A + 0 = A$	7. $A \cdot A = A$
2. $A + 1 = 1$	8. $A \cdot \overline{A} = 0$
3. $A \cdot 0 = 0$	9. $\overline{\overline{A}} = A$
4. $A \cdot 1 = A$	10. $A + AB = A$
5. $A + A = A$	11. $A + \overline{A}B = A + B$
6. $A + \overline{A} = 1$	12. $(A + B)(A + C) = A + BC$
- DeMorgan's theorems:
 1. The complement of a product is equal to the sum of the complements of the terms in the product.
$$\overline{XY} = \overline{X} + \overline{Y}$$
 2. The complement of a sum is equal to the product of the complements of the terms in the sum.
$$\overline{X + Y} = \overline{XY}$$
- According to Principle of Duality, dual of a Boolean expression can be obtained by replacing AND (\cdot) with OR ($+$) and vice versa, 1 with 0 and vice versa keeping variables and complements and variables are unchanged.
- Logic gates are one of the fundamental building blocks of digital systems.
- The inverter output is the complement of the input.
- When the input is LOW, the output is high; when the input is HIGH, the output is LOW, thereby producing an inverted output pulse.
- The AND gate output is HIGH only if all the inputs are HIGH.
- For a 2-input AND gate, output X is HIGH only when inputs A and B are HIGH; X is LOW when either A or B is LOW, or when both A and B are LOW.
- The OR gate output is HIGH if any of the input is HIGH.

- The NAND gate output is LOW only if all the inputs are HIGH.
- The NAND gate can be viewed as a negative-OR whose output is HIGH when any input is LOW.
- The NOR gate output is LOW if any of the inputs is HIGH.
- The NOR can be viewed as a negative-AND whose output is HIGH only if all the inputs are LOW.
- The exclusive-OR gate output is HIGH when the inputs are not the same.
- The exclusive-NOR gate is LOW when the inputs are not the same.
- The name, Graphic symbol, Algebraic function and Truth table of digital logic gates are given below:

Name	Graphic symbol	Algebraic function	Truth table	
AND		$Y = A \cdot B$	Inputs	
			A	B
			0	0
			0	1
			1	0
			1	1
OR		$Y = A + B$	Inputs	
			A	B
			0	0
			0	1
			1	0
			1	1
Inverter		$Y = \bar{A}$	Inputs	
			A	\bar{A}
			0	1
			1	0

Buffer		$F = A$	Inputs	Outputs
NAND		$F = \overline{A \cdot B}$	Inputs	Outputs
NOR		$F = \overline{A + B}$	Inputs	Output
Exclusive-OR (XOR)		$F = A \oplus B$	Inputs	Output
Exclusive-NOR Or equivalence		$F = A \odot B$	Inputs	Output

2.2 COMBINATIONAL AND ARITHMETIC CIRCUITS

A combinational logic is a circuit consisting of logic gates whose output at any time is determined by the present combinations of inputs. That means in combinational circuit the current output is not determined by the previous input and previous output, so there is no feedback and memory in a combinational circuit.

Combinational logic circuit consist of logic gate whose output at any instant of time are determined by the present combination of input. The basic building block of combinational logic circuit is gate.

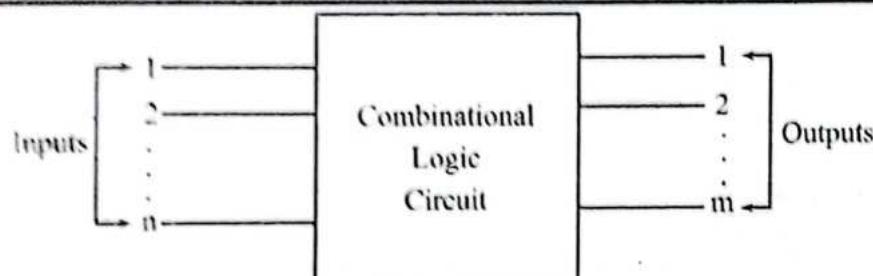


Figure: Block diagram of Combinational Circuit

Design of a Combinational Circuit

The design of a Combinational Circuit starts from the verbal communications and verbal outlines and ends with a logic circuit diagram. The procedure involves the following steps:

1. State the given problem completely and exactly
2. Interpret the problem and determine the available input variables and required output variables.
3. Assign a letter symbol to each input and output variables
4. Design the truth table, which defines the required relations between inputs and outputs.
5. Obtain the simplified Boolean expressions for each output
6. Draw the logic circuit diagram to implement the Boolean expression

The practical design method would have to consider such constraints as:

1. Minimum number of gates
2. Minimum number of inputs to a gate
3. Minimum propagation time of the signal through the circuit
4. Minimum number of interconnections
5. Limitations of the driving capabilities of each gate

Adder

The most common operation performed operation in a digital computer is arithmetic operation. The common arithmetic operation is addition of two binary digits. The simple addition of two digit 0 and 1 consists of:

$$0 + 0 = 0$$

$$0 + 1 = 1$$

$$1 + 0 = 1$$

$$1 + 1 = 10$$

The binary adder can be classified into two types

1. Half Adder
2. Full Adder
1. **Half Adder**

Half adder is a combinational circuit which is used to add two 1-bit numbers X and Y. the input variables designate the augends and addend bits and the output variables produce the sum and carry. The output variables are S for **Sum** and C for **Carry**.

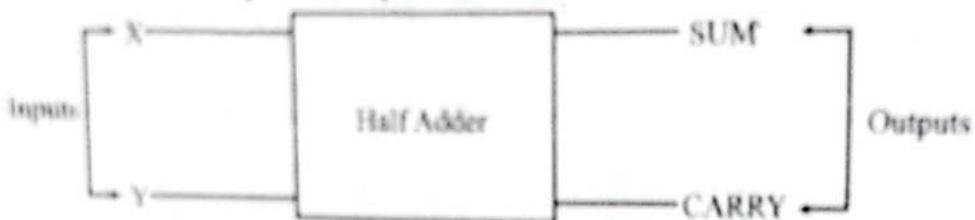


Figure: Block diagram of Half Adder

The half adder accepts two binary digits on its inputs and produces two binary digits on its outputs. – A **sum** bit and a **carry** bit.

The truth table for half adder is shown below.

Table: The truth table for Half Adder

Inputs		Outputs	
Input X	Input Y	Carry C	Sum S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

$$\text{Sum (S)} = \overline{X}Y + X\overline{Y}$$

$$= X \oplus Y$$

$$\text{Carry (C)} = XY$$

2. **Full Adder**

Full adder is a combinational circuit which is used to add three 1-bit numbers X, Y and Z. The full adder has three input lines and two output lines. The input variables are denoted by X, Y and Z similarly the output variables are denoted by S for SUM and C for CARRY.

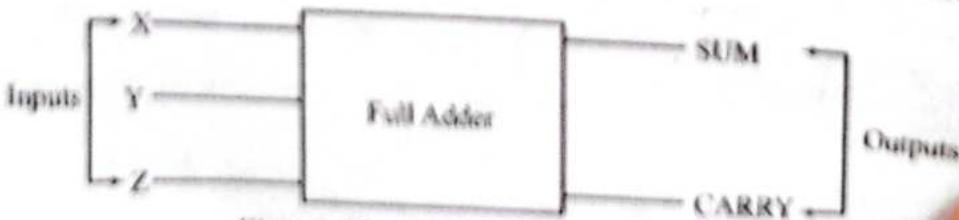


Figure: Block Diagram of Full Adder

The full adder accepts three binary digits on its inputs and produces two binary digits on its outputs. – A sum bit and a carry bit.

Table: The truth table for Full Adder

Inputs			Outputs	
Input X	Input Y	Input Z	Carry C	Sum S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

The Boolean function for full –adder from the about truth table is shown below.

$$\begin{aligned}
 \text{Sum (S)} &= X \bar{Y}Z + \bar{X}Y \bar{Z} + X \bar{Y} \bar{Z} + XYZ \\
 &= X \bar{Y}Z + XYZ + \bar{X}Y \bar{Z} + X \bar{Y} \bar{Z} \\
 &= Z(X \bar{Y} + XY) + \bar{Z}(\bar{X}Y + X \bar{Y}) \\
 &= Z(X \oplus Y) + \bar{Z}(X \oplus Y) \\
 &= Z(X \overline{\oplus} Y) + \bar{Z}(X \oplus Y)
 \end{aligned}$$

$$\begin{aligned}
 \text{Let, } P &= X \oplus Y \\
 &= Z \bar{P} + \bar{Z}P \\
 &= Z \oplus P
 \end{aligned}$$

Replacing the value of P we get:

$$\begin{aligned}
 \text{SUM (S)} &= Z \oplus X \oplus Y \\
 &= X \oplus Y \oplus Z \\
 \therefore \text{SUM (S)} &= X \oplus Y \oplus Z \\
 \text{Carry (C)} &= XY + XZ + YZ \\
 \text{Sum (S)} &= \bar{X} \bar{Y}Z + \bar{X}Y \bar{Z} + X \bar{Y} \bar{Z} + XYZ
 \end{aligned}$$

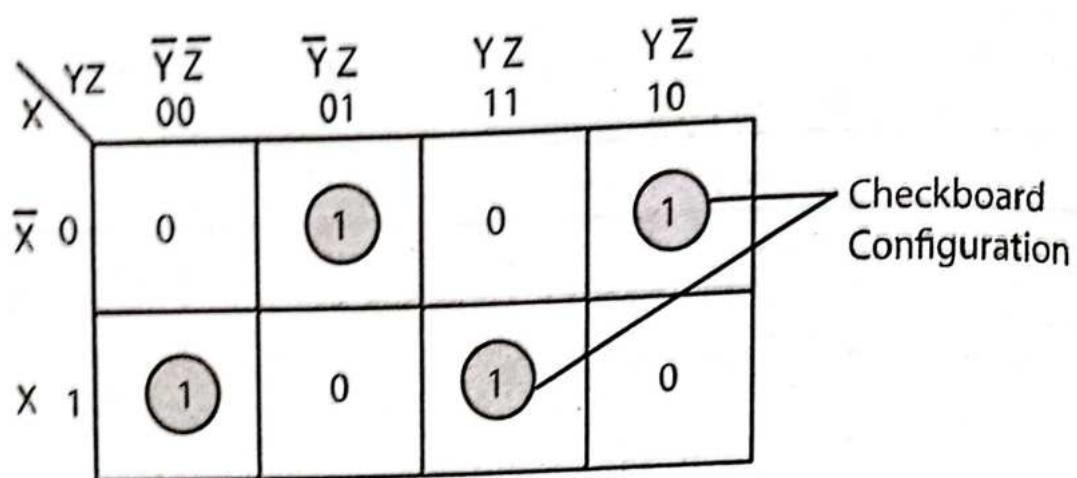


Figure (a): K map for Sum

$$\text{Carry (C)} = XY + XZ + YZ$$

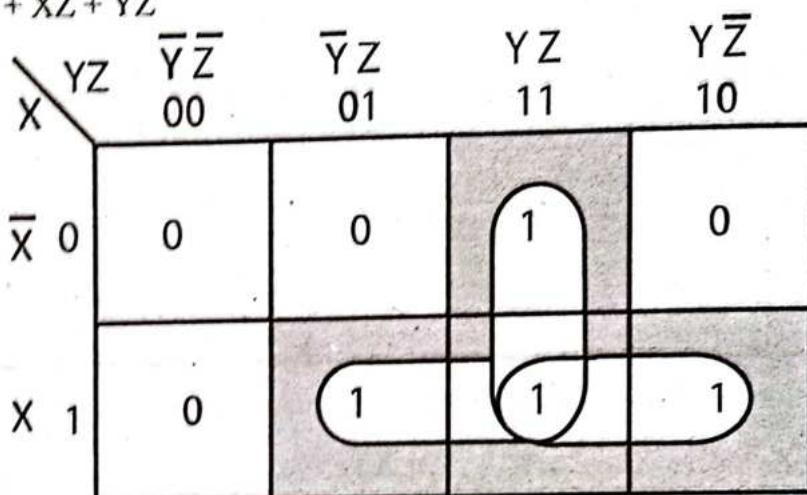


Figure (b): K map for carry

Figure: K map for Sum and Carry of Full Adder

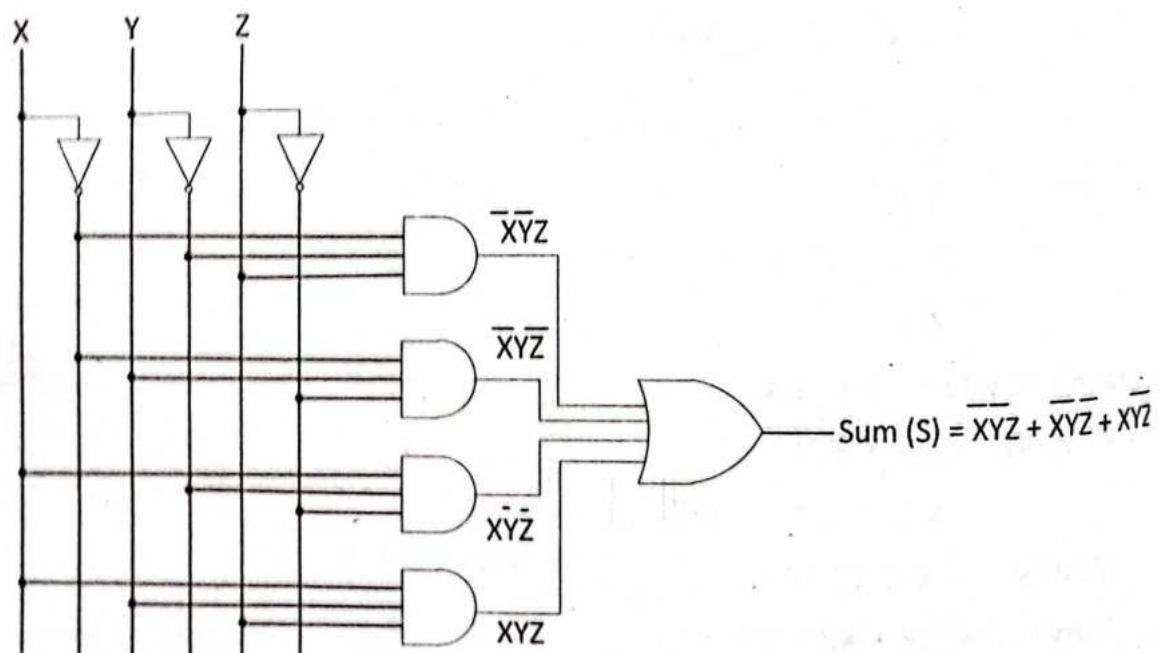


Figure (a): Logic Circuit diagram for Sum in Full Adder

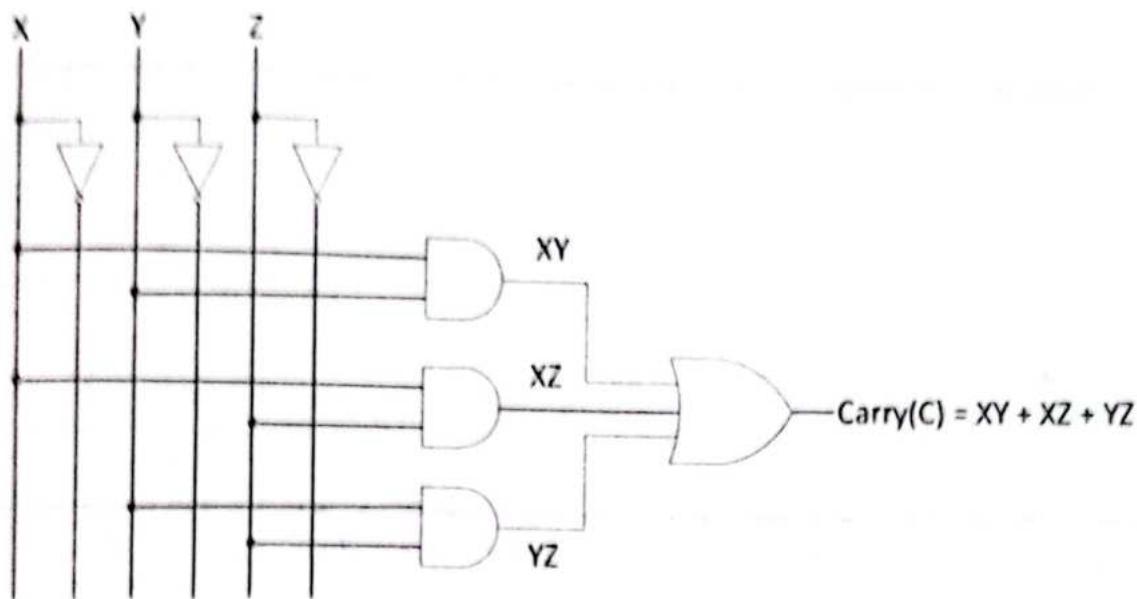


Figure (b): Logic Circuit diagram for Carry in Full Adder

Subtractor

The subtraction of two binary numbers is accomplished by taking the complement of the subtrahend and adding it to the minuend. If the minuend bit is smaller than the subtrahend bit, a bit is borrowed from the next higher significant position.

1. Half Subtractor

Half subtractor is a combinational logic circuit that subtracts two number of one bit and produces their difference. There are two input variable let say X and Y of a single bit and there will be two output variables B for borrow from higher significant bit and D for difference.

Let Y is subtracted from X. i.e. $X - Y$ then

$$0 - 0 = 0$$

$$0 - 1 = 1$$

$$1 - 0 = 1$$

$$1 - 1 = 0$$

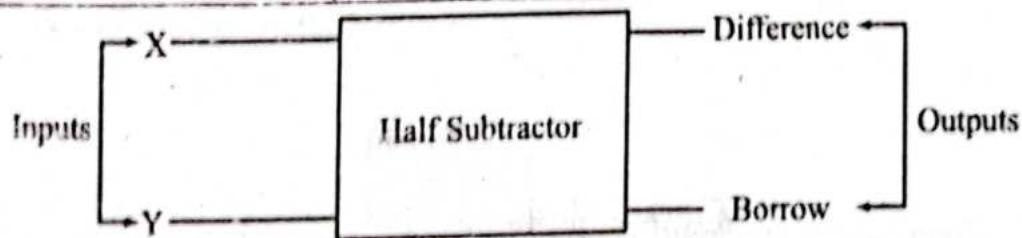


Figure: Block diagram of Half Subtractor

The half subtractor accepts two binary digits on its inputs and produces two binary digits on its outputs. – A difference bit and a borrow bit.

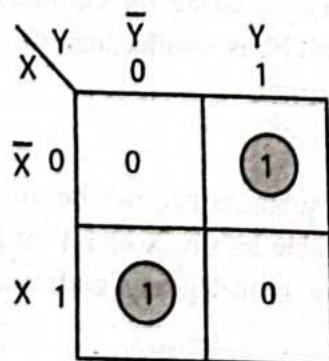
Table: The truth table for Half Subtractor

Inputs		Outputs	
Input X	Input Y	Borrow B	Difference D
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

The Boolean function from above truth table is written as follows.

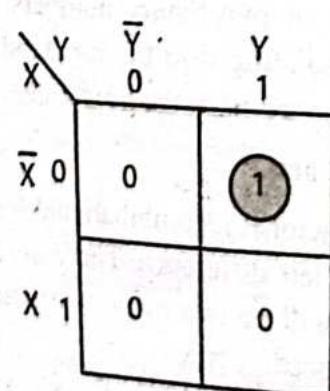
$$\begin{aligned}\text{Difference (D)} &= \overline{X}Y + X\overline{Y} \\ &= X \oplus Y\end{aligned}$$

$$\text{Borrow (B)} = \overline{X}Y$$



$$\text{Difference (D)} = \overline{X}Y + X\overline{Y}$$

Figure (a): K map for Difference



$$\text{Borrow (B)} = \overline{X}Y$$

Figure (b): K map for borrow

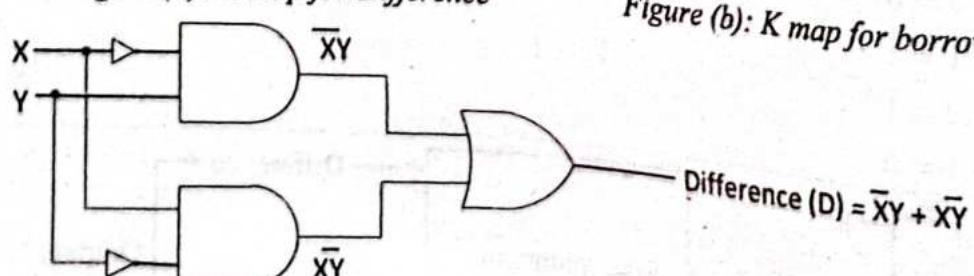


Figure (a): Logic circuit diagram for Difference of Half Subtractor

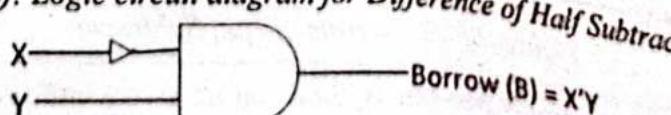


Figure (b): Logic circuit for Borrow of Half Subtractor

2. Full Subtractor

A full subtractor is a combinational logic circuit that performs a subtraction operation between three numbers of a single bit. Let say the input variables are X, Y and Z and the outputs are Difference (D) and Borrow (B).

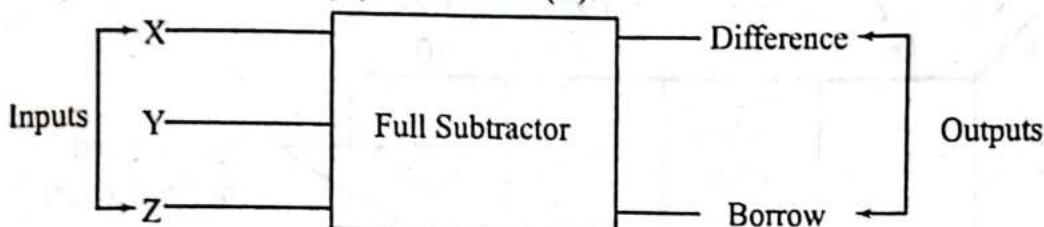


Figure: Block Diagram of Full Adder

The full subtractor accepts three binary digits on its inputs and produces two binary digits on its outputs. – A difference bit and a borrow bit.

Table: The truth table for Full Subtractor

Inputs			Outputs	
Input X	Input Y	Input Z	Borrow B	Difference D
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

The Boolean function from the above truth table is calculated as follows.

$$\text{Difference (D)} = \overline{X} \overline{Y} Z + \overline{X} Y \overline{Z} + X \overline{Y} \overline{Z} + XYZ$$

$$\begin{aligned} \therefore F_D &= X \overline{Y} \overline{Z} + XYZ + \overline{X} \overline{Y} Z + \overline{X} Y \overline{Z} \\ F_D &= X(\overline{Y} \overline{Z} + YZ) + \overline{X}(\overline{Z} + Y \overline{Z}) \\ &= X(Y \oplus Z) + \overline{X}(Y \oplus Z) \\ &= X(Y \oplus Z) + \overline{X}(Y \oplus Z) \end{aligned}$$

$$\begin{aligned} \text{Let } Y \oplus Z &= P \\ &= X \bar{P} + \bar{X}P \\ &= X \oplus P \end{aligned}$$

$$\text{Difference (D)} = X \oplus Y \oplus Z$$

$$\therefore F_D = X \oplus Y \oplus Z$$

$$\text{Borrow (B)} = \overline{X} Y + \overline{X} Z + YZ$$

$$\text{Difference (D)} = \overline{X} \overline{Y} Z + \overline{X} Y \overline{Z} + X \overline{Y} \overline{Z} + XYZ$$

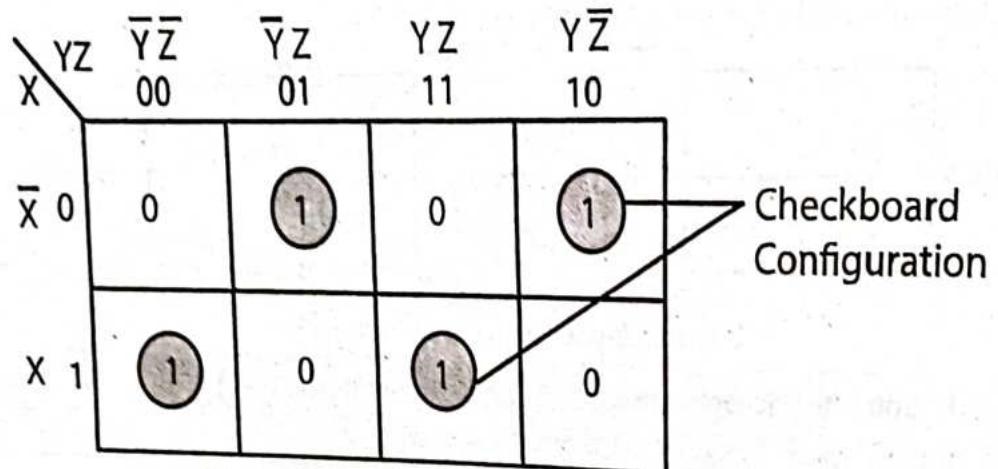


Figure: K map for Difference of Full Subtractor

$$\text{Borrow (B)} = \overline{X} Y + \overline{X} Z + YZ$$

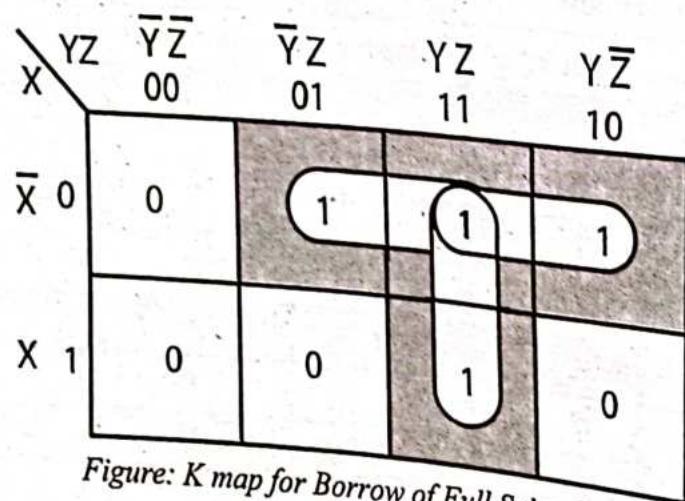


Figure: K map for Borrow of Full Subtractor

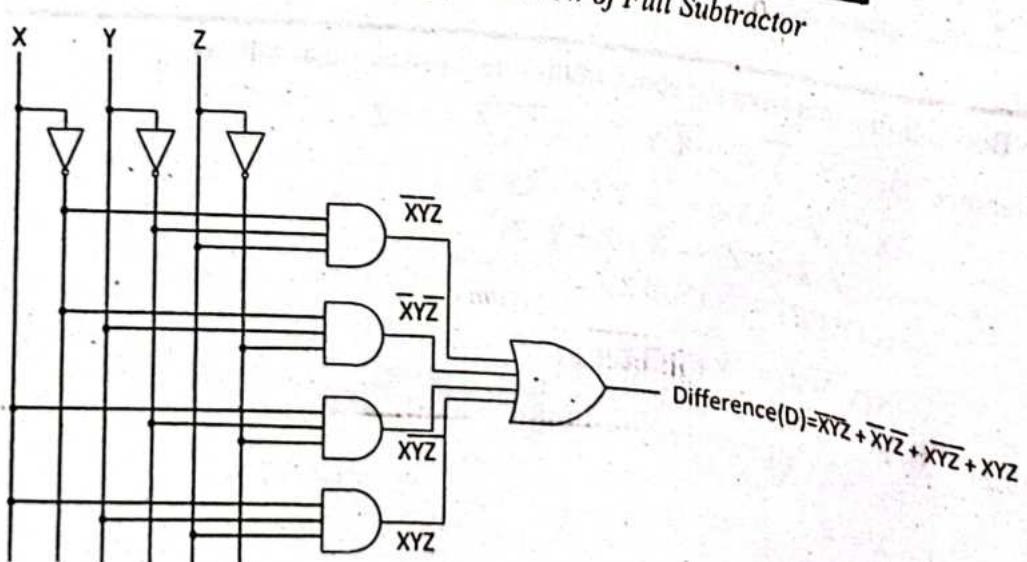


Figure: Logic Circuit diagram for Difference in Full Subtractor

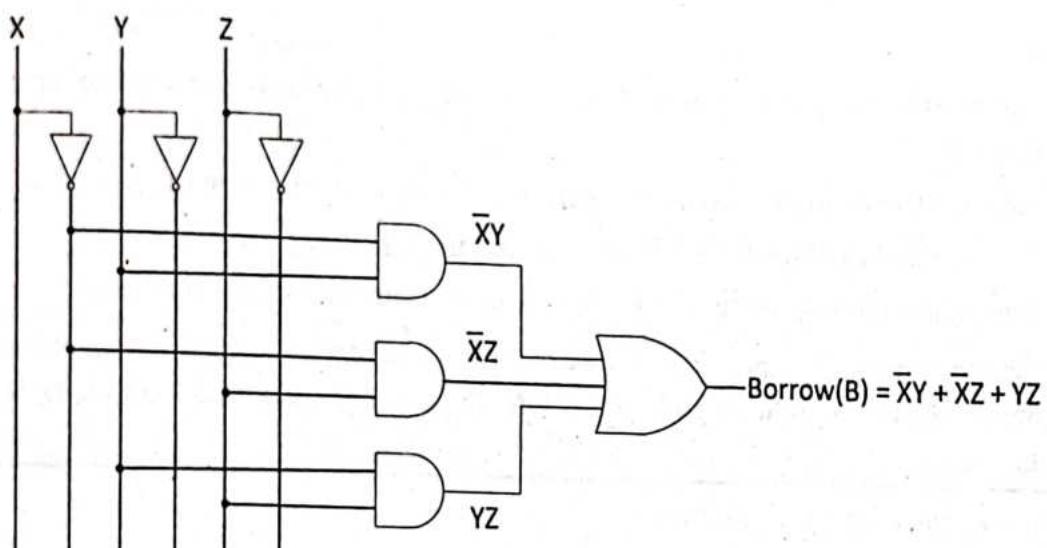


Figure: Logic Circuit diagram for Borrow in Full Subtractor

Decoder

A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines. If the n -bit coded information has unused combinations, the decoder may have fewer than 2^n outputs.

- It is a combinational circuit that converts binary coded information other codes (e.g., octal, decimal, hexadecimal, etc.)
- A decoder (with enable input) is exactly the same as DEMUX.
- Binary code of n bits can represent $\leq 2^n$ distinct elements of information.
- A decoder has n inputs and $\leq 2^n$ output.

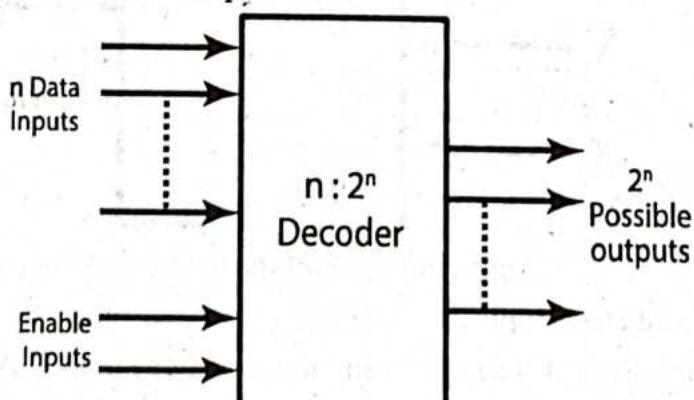


Figure: Block diagram of a decoder

A decoder is a combinational logic circuit that receives n number of inputs and produces 2^n number of outputs.

There are following types of decoder:

- 1) 2-to-4-line decoder
- 2) 3-to-8-line decoder
- 3) BCD-to-Decimal Decoder
- 4) 4×16 -line decoder by using two 3×8 decoders

Encoder

- An encoder is a combinational logic circuit that performs the reverse operation of a decoder.
- An encoder is a digital circuit that performs the inverse operation of a decoder.
- An encoder has 2^n (or fewer) input lines and n output lines.
- The output lines generate the binary code corresponding to the input value.

It has maximum 2^n input lines and n output lines, hence it encodes the information from 2^n inputs into an n -bit code. Therefore, the encoder encodes 2^n input lines with ' n ' bits.

There are following types of encoder:

- 1) 4-to-2 encoder
- 2) 8-to-3 encoder
- 3) Priority Encoder
- 4) Decimal to BCD
- 5) Hexadecimal to binary

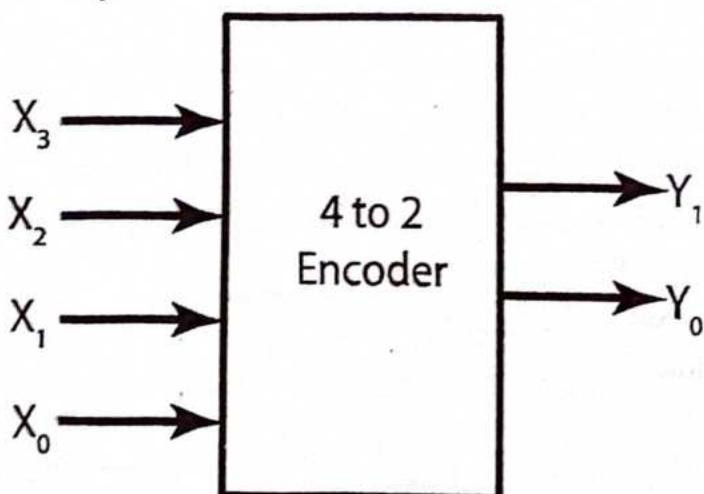


Figure: Block diagram of 4-to-2 encoder

Multiplexers and Demultiplexer

Multiplexer is a circuit that accepts many inputs but one output. A demultiplexer is a circuit that performs function exactly in the reverse of a multiplexer. Generally, multiplexer and demultiplexer are used together, because of the communication systems are bi-directional.

1. Multiplexer / Data Selector

A multiplexer is a circuit used to select and route any one of the several input signals to a single output.

It is a combinational logic circuit that select binary information from one of many lines and direct it to a single output line

For m input lines and n selection lines

$$2^n = m$$

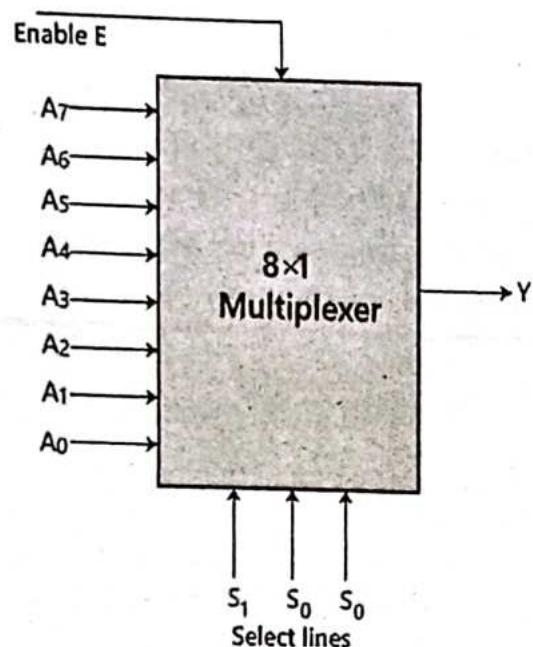


Figure: Block diagram of multiplexer (Source: <https://www.javatpoint.com/multiplexer-digital-electronics>)

Types of Multiplexer

Following are types of Multiplexer:

- 2 to 1 Multiplexer
- 4 to 1 Multiplexer
- 8 to 1 Multiplexer
- 16 to 1 Multiplexer

8-to-1 multiplexer

Step 1: Construction of block diagram of 8:1 Mux

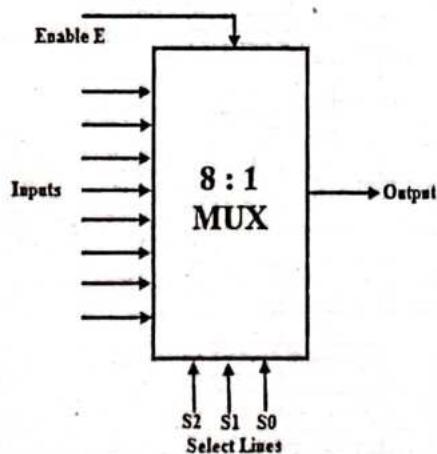


Figure: Block diagram of 8-to-1 multiplexer

Step 2: Calculating the number of select lines:

It has 8 data input line and 1 output lines

$$\text{Number of select lines (m)} = \log_2 n$$

Where n is number of input lines

$$\begin{aligned}
 (m) &= \log_2(8) \\
 &= \log_2(2^3) \\
 &= 3 \log_2(2) \\
 (m) &= 3 \times 1 = 3 [\because \log_a a = 1]
 \end{aligned}$$

Step 3: Construction of Truth table for 8 to 1 Multiplexer

Table: Function Table for 8-to-1 multiplexer

Inputs								Selectors			Outputs
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	S ₂	S ₁	S ₀	Y
-	-	-	-	-	-	-	D ₀	0	0	0	D ₀
-	-	-	-	-	-	D ₁	-	0	0	1	D ₁
-	-	-	-	-	D ₂	-	-	0	1	0	D ₂
-	-	-	-	D ₃	-	-	-	0	1	1	D ₃
-	-	-	D ₄	-	-	-	-	1	0	0	D ₄
-	-	D ₅	-	-	-	-	-	1	0	1	D ₅
-	D ₆	-	-	-	-	-	-	1	1	0	D ₆
D ₇	-	-	-	-	-	-	-	1	1	1	D ₇

$$\begin{aligned}
 Y &= S_2 \overline{S_1} \overline{S_0} \overline{D_0} + S_2 \overline{S_1} \overline{S_0} D_0 + S_2 \overline{S_1} S_0 D_0 + S_2 S_1 \overline{S_0} \overline{D_0} + S_2 S_1 D_0 + S_2 S_1 S_0 \overline{D_0} \\
 &+ S_2 S_1 S_0 D_0
 \end{aligned}$$

Step 4: Construction of Circuit diagram for 8 to 1 multiplexer

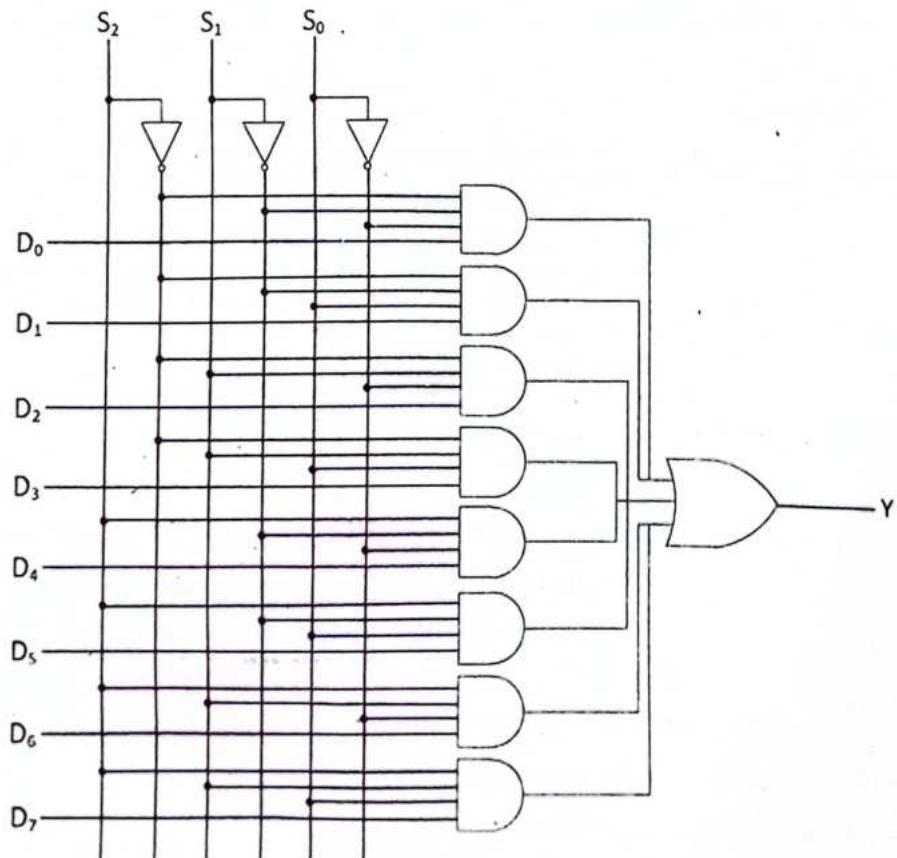


Figure: Construction of Circuit diagram for 8 to 1 multiplexer

Application of Multiplexer:

- Communication system
- Telephone network
- Computer memory
- Transmission from the computer system of a satellite.
- Multiplexers are used in various fields where multiple data need to be transmitted using a single line.
- An example of a 4-to-1 multiplexer is 1C 74153 in which output is same as the input.

Advantages of Multiplexer

- It reduces the number of wires.
- Reduces circuit complexity and cost.
- Implementation of various circuits in MUX.

2. Demultiplexer/Data Distributor

A demultiplexer is a circuit that receives information on a single input line and transmits information on one of 2^n possible output lines. The selection of a specific output line is controlled by the bit values of n selection lines. The demultiplexer works just inverse of the multiplexer.

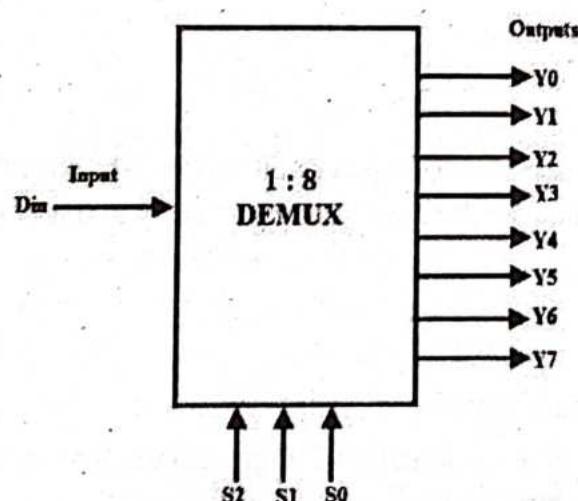


Figure: Demultiplexer

A decoder with enable input can function as a demultiplexer. It is also known as data distributor

Types of Demultiplexer

- a. 1-to-2 Demultiplexer
- b. 1-to-4 Demultiplexer
- c. 1-to-8 Demultiplexer
- d. 1-to-2 Demultiplexer

Things to Remember

- Combinational logic circuit is a circuit consisting of logic gates whose output at any time is determined by the combination of present inputs only. The output of combinational logic circuit is not affected by previous inputs as well as previous output.
- The design of a combinational circuit is very crucial task. The design process starts with a verbal communication and ends with logic circuit diagram. While designing a combinational logic circuit following things must be considered.
 1. Number of logic gates
 2. Number of inputs
 3. Propagation time
 4. Number of interconnections
 5. Driving capabilities.
- Binary adder is a combinational logic circuit that is used to add binary numbers. Binary adders are
 1. Half Adder
 2. Full Adder
- Half adder is a combinational logic circuit that is used for adding two single bit binary numbers. The output of half adder is sum and carry and it is given by following Boolean expression.

$$\text{Sum (S)} = X \oplus Y$$

$$\text{Carry (C)} = XY$$

Where X and Y are inputs

- Full adder is a combinational logic circuit that is used for adding three single bit binary numbers. The output of full adder is sum and carry and it is given by following Boolean expression...

$$\text{Sum (S)} = X \oplus Y \oplus Z$$

$$\text{Carry (C)} = XY + XZ + YZ$$

Where X, Y and Z are inputs

- Binary subtractor is a combinational logic circuit that is used for subtracting binary numbers. Binary subtractors are

1. Half Subtractor

2. Full Subtractor

- Half subtractor is a combinational logic circuit that is used to subtract two single bit binary numbers. The output of half subtractor is Difference and Borrow and it is given by following Boolean expression...

$$\text{Difference (D)} | \text{Borrow} = X \oplus Y$$

$$\text{Borrow (B)} = \overline{X} Y$$

Where X and Y are inputs

- Full Subtractor is a combinational logic circuit that is used for subtract three single bit binary numbers. The output of full subtractors is difference and borrow and it is given by following Boolean expression...

$$\text{Difference (D)} = X \oplus Y \oplus Z$$

$$\text{Borrow (B)} = \overline{X} Y + \overline{X} Z + YZ$$

Where X, Y and Z are inputs

- In digital system it is sometime necessary to convert a code from one form to another. A code converter is a combinational logic circuit for converting a code from one form to another.
- BCD to excess-3: there are ten numbers in BCD (from 0 to 9). So, to represent all numbers four binary bits are required. The number except 0 to 9 are represented by don't care condition. Excess-3 is three number excess to BCD number.

$$W = A + BC + BD = A + B(C + D)$$

$$X = \overline{B} C + \overline{B} D + B \overline{C} D$$

$$Y = CD + \overline{C} \overline{D}$$

$$Z = \overline{D}$$

Where A, B, C and D are BCD variables and W, X, Y and Z are excess-3 variables

Analysis process of a combinational logic circuit is somewhat reverse process of design.

Binary Arithmetic:

Everything that is stored in or manipulated by the computer is a number. The computer only understands the numbers 1 and 0. Therefore, every number has to be converted to binary (0s and 1s) digits. The basic arithmetic operations of the binary number system are addition and subtraction.

a. Binary Addition

Binary addition is a simple mathematical operation used to add two binary numbers together. The logical rules of this operation are implemented in every digital computer – through digital circuits known as adders. There are four rules of binary addition.

For addition, we have four simple rules to remember:

$$0 + 0 = 0,$$

$$0 + 1 = 1,$$

$$1 + 0 = 1, \text{ and}$$

$$1 + 1 = 0 \quad (10, 0 \text{ is the sum and the carry bit are added to the next column bit})$$

Table: Addition of Binary Number.

S.no	Input		Output	
	A	B	Sum(S)	Carry(C)
1	0	0	0	0
2	0	1	1	0
3	1	0	1	0
4	1	1	0	1

b. Binary Subtraction

Binary subtraction includes subtracting two binary numbers (comprising only two digits, 0 and 1). It is one of the four binary operations. The binary subtraction has two new terms involved – the difference and the borrow. We have four main rules to remember for the binary Subtraction:

- $0 - 0 = 0$,
- $0 - 1 = 1$, borrow/take 1 from the adjacent bit to the left
- $1 - 0 = 1$, and
- $1 - 1 = 0$

Table: Subtraction of binary numbers

S.No	Input		Output	
	A	B	Difference	Borrow
1	0	0	0	0
2	0	1	1	0
3	1	0	1	0
4	1	1	0	1

Operation on Unsigned and Signed Binary Number:

The operations performed on unsigned binary numbers are different from the operations performed on signed binary numbers. Unsigned binary numbers represent positive integers and are used to perform arithmetic operations such as addition, subtraction, multiplication, and division. On the other hand, signed binary numbers represent positive and negative integers and are used to perform arithmetic operations such as addition, subtraction, multiplication, and division, as well as comparisons.

Unsigned Binary Number:

An unsigned binary number is a binary number that represents positive integers only. It is used to perform arithmetic operations such as addition, subtraction, multiplication, and division.

In unsigned binary representation, each bit represents a power of 2, starting with 2^0 for the least significant bit (LSB) and $2^{(n-1)}$ for the most significant bit (MSB), where n is the number of bits in the representation.

Signed Binary Number:

A signed binary number is a binary number that represents positive and negative integers. It is used to perform arithmetic operations such as addition, subtraction, multiplication, and division, as well as comparisons.

There are two methods to represent signed binary numbers: sign-magnitude representation and two's complement representation.

- **Sign-magnitude representation:** In sign-magnitude representation, the most significant bit (MSB) is used to represent the sign of the number. A 0 in the MSB indicates a positive number, and a 1 in the MSB indicates a negative number. The remaining bits represent the magnitude of the number.
- **Two's complement representation:** In two's complement representation, a positive number is represented in binary form, and a negative number is represented by taking the binary representation of the positive number and inverting all the bits (changing 0s to 1s and 1s to 0s) and then adding 1.

2.3 Sequential Logic Circuit

- Sequential circuit is basic memory element of sequential logic system.
- The logic circuits whose output at any instant of time depend not only on the present inputs but also on the past outputs are called sequential circuits.
- A sequential circuit consists of a combinational circuit to which storage elements are connected to form a feedback path.
- Sequential circuit = Combinational logic + memory element

Sequential circuit also called regenerative circuit fall into three types:

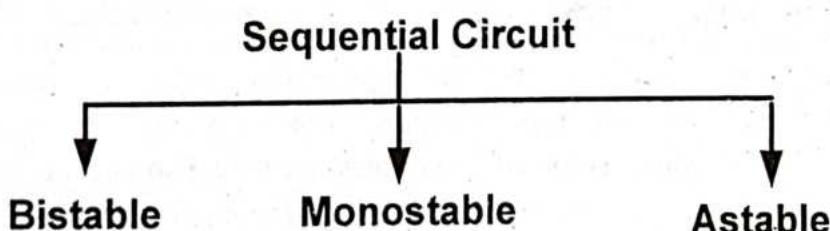


Figure: Types of sequential Circuit.

- Bistable: Two Stable operating point
- Monostable: Only one stable operating point
- Astable: It has no stable operating point

Basic building block of sequential circuit is flip flop. Flip flop is a storage device which store one bit of information. There is a memory element to form a feedback path.

A sequential circuit is specified by a time sequence of inputs, outputs and internal states. The block diagram of sequential circuit is given below:

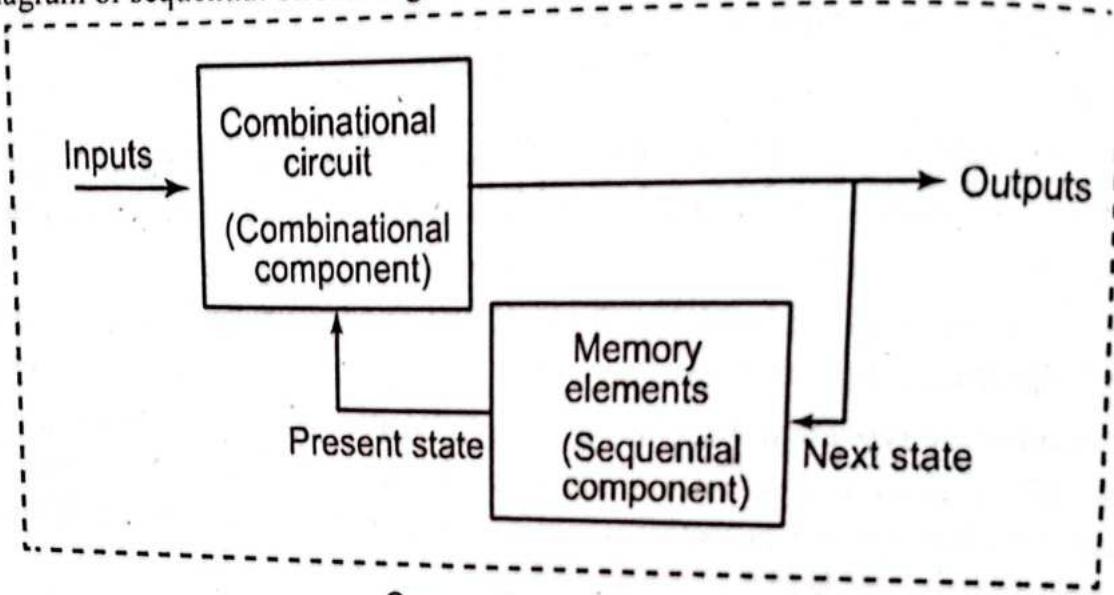


Figure: Block diagram of sequential circuit/ Finite state machine (FSM)

Sequential circuit is slower in operation than combinational circuit. It may or may not contain clock input.

There are two types of sequential circuits:

a. **Synchronous Sequential Circuit:**

It is a system whose behavior can be defined from the knowledge of its signals at discrete instant of time (i.e., by the clock signal parallelly driven by one clock signal).

b. **Asynchronous Sequential circuit:**

It is a system whose behavior depends in the order in which its input signals change and can be affected at any instant of time (one's output is given to clock of another). Comparison between Combinational and Sequential circuits

Table: Comparison between Combinational and Sequential circuits

S.No	Combinational circuits	Sequential circuits
1	In combinational circuits, the output variables are all times dependent on the combination of input variables.	In sequential circuits, the output variables depend not only on the present input variables but they also depend upon the past history of these input variables.
2	Memory unit is not required in combinational circuits	Memory unit is required to store the past history of input variables in the sequential circuit
3	Combinational circuits are faster in speed because the delay between input and output is due to propagation delay of gates.	Sequential circuits are slower than the combinational circuits

S.No	Combinational circuits	Sequential circuits
4	Combinational circuits are easy to design.	Sequential circuits are comparatively harder to design.
5	Parallel adder is a combinational circuit.	Serial adder is a sequential circuit.

Flip Flop:

- It is a memory device which can assume only two stable states, which has a pair of complementary outputs and one or more inputs that can cause output state to change. It is also called binary latch.
- A flip flop is a sequential circuit which is popularly known as a basic digital memory circuit. A flip flop stores 1 bit; therefore, it is called as 1-bit memory cell. It has two stable states: logic 1 and logic 0.
- The output of circuit (Q and \bar{Q}) will always be complementary. This means that if $Q=0$, then $\bar{Q}=1$ and vice versa. They will never be equal; $Q=\bar{Q}=0$ or 1 is an invalid state. If $Q=1$, $\bar{Q}=0$, it is called 1 state or SET state. If $Q=0$, $\bar{Q}=1$, it is called 0 state or RESET state.

Features of flip flop:

Binary Storage: Flip-flops can store one bit of binary data, either 0 or 1, and retain it until the next clock pulse.

Edge Triggered: Flip-flops change state only when there is a transition (i.e., a rising or falling edge) in the clock signal.

Synchronous Operation: Flip-flops operate in synchrony with the clock signal, which ensures stable and predictable operation.

Clocked Latches: Flip-flops are clocked latches, which means that the state of the flip-flop is controlled by the clock signal and can only change on the rising or falling edge of the clock.

Positive Feedback: Flip-flops use positive feedback, which means that the output of the flip-flop is connected back to its input, creating a feedback loop that is responsible for maintaining the state of the circuit.

Applications of Flip-Flop:

- As a memory element.
- In various types of register
- In counter/timer.
- As a delay time

Types of Flip-flop:

- SR Flip-Flop:
- D Flip flop (Delay or Data Flip Flop)

- JK Flip Flop
- T Flip Flop (Toggle Flip flop)
- Master Slave Flip-Flop

Introduction to S-R Flip-Flop

The SR flip-flop is a type of bistable latch circuit in digital electronics. It has two inputs: "set" (S) and "reset" (R), and two outputs: Q and its inverse, \bar{Q} .

SR stands for "Set-Reset". The reset input resets the flip-flop back to its original state with an output Q that will be either at a logic level "1" or logic "0" depending upon this set/reset condition.

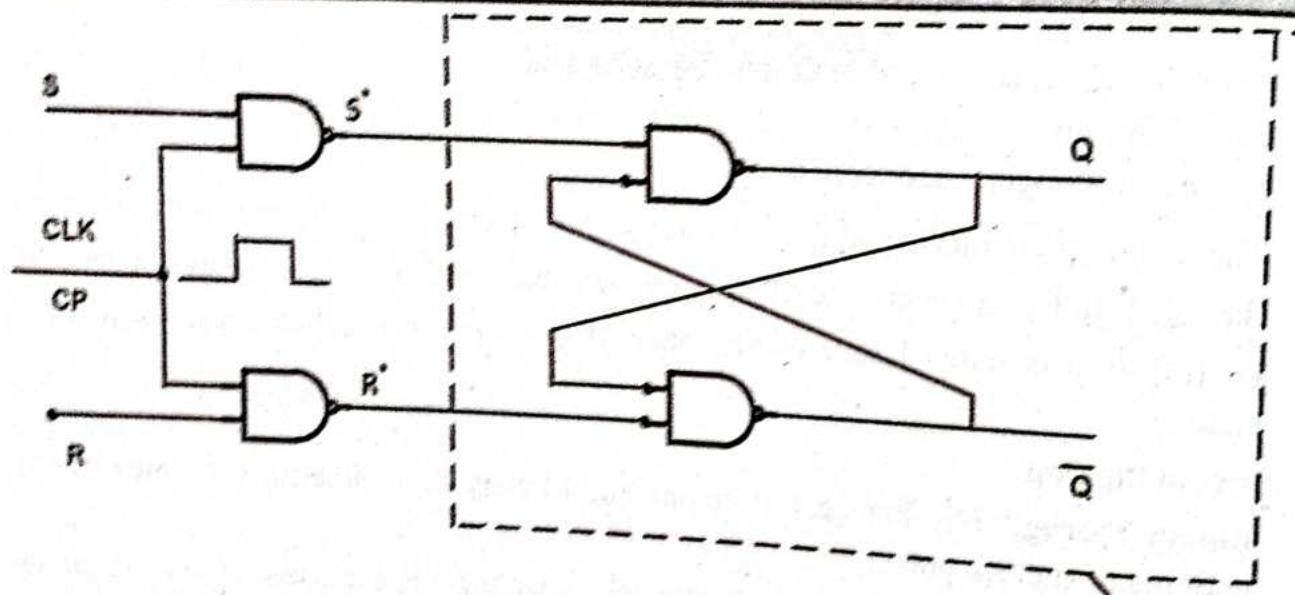


Figure: Logic Circuit diagram of SR Flip Flop

Table: Truth table for S-R NAND latch

S*	R*	Q	\bar{Q}
0	0	Not used	
0	1	1	0
1	0	0	1
1	1	Previous State (Memory)	

$$\therefore S^* = \bar{S} \cdot \bar{C}L\bar{K}$$

$$= \bar{S} + C\bar{L}K$$

$$\therefore R^* = \bar{R} \cdot \bar{C}L\bar{K}$$

$$\therefore R^* = R + C\bar{L}K$$

$$[A + \bar{B} = \bar{A} \cdot \bar{B} \text{ and } \bar{A} \cdot \bar{B} = \bar{A} + \bar{B}]$$

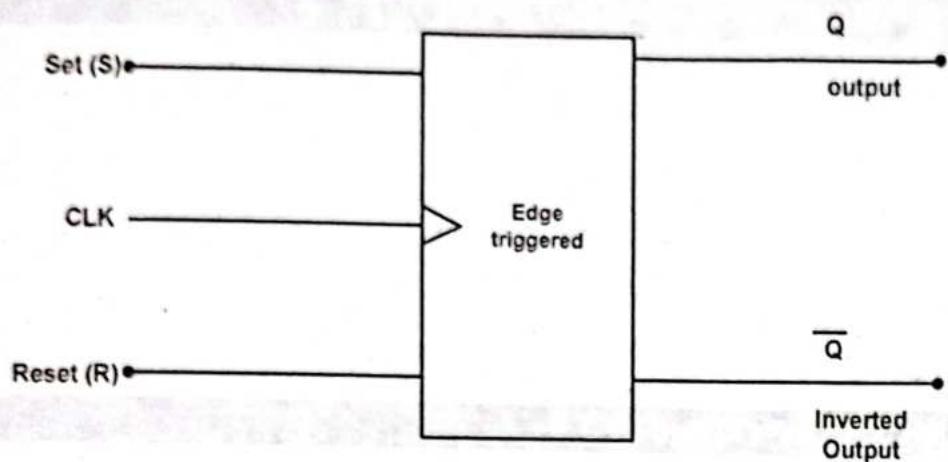


Figure: Graphics Symbol of SR Flip Flop

Table: Truth table for S-R flip flop

CLK	S	R	Q	\bar{Q}
0	X	X	Memory Q_n (Previous State)	
1	0	0	Memory Q_n (Previous State)	
1	0	1	0	1
1	1	0	1	0
1	1	1	Not used [Invalid]	

Case I: When CLK=1

When $CLK = 0$, $S^* = \bar{S} + CLK$

$$\therefore S^* = \bar{S} + \bar{0} = \bar{S} + 1 = 1 \dots \text{Equation (3)}$$

and $R^* = \bar{R} + \bar{C}\bar{L}\bar{K} = \bar{R} + \bar{0} = \bar{R} + 1 = 1$ Equation (4)

Whatever the value of \bar{S} and \bar{R} , it's not going to change the value of R^* and S^* .

Case 2:

When CLK = 1

$$S^* = \bar{S} + \overline{CLK} = \bar{S} + \bar{1} = \bar{S} + 0 = \bar{S}. \dots \text{Equation (5)}$$

$$R^* = \bar{R} + \overline{CLK} = \bar{R} + \bar{1} = \bar{R} + 0 = \bar{R} \dots \text{Equation (6)}$$

$$\therefore S^* = \overline{s}$$

$$\therefore R^* = \bar{R}$$

Case 2.1

When $\text{CLK} = 1, S=0, R=0$

$$\therefore S^* = \bar{S} = \bar{0} = 1$$

$$\therefore R^* = \bar{R} = \bar{O} = 1$$

Case 2.2 When CLK=1, S=0, R=1

$$S^* = \bar{S} + \bar{CLK} = \bar{0} + \bar{1} = 1 + 0 = 1$$

$$S^* = 1$$

$$R^* = \bar{R} + \bar{CLK}$$

$$= \bar{R} + \bar{1}$$

$$= \bar{R} + 0 = \bar{1} + 0 = 0$$

$$\therefore R^* = 0$$

Case 3: When CLK=1, S=1, R=0

$$\therefore R^* = \bar{R} + \bar{CLK} = \bar{0} + \bar{1} = 1 + 0 = 1$$

$$S^* = \bar{S} + \bar{CLK}$$

$$= \bar{S} + \bar{1} = \bar{1} + \bar{1} = 0 + 0 = 0$$

Case 4: When CLK=1, S=1, R=1

$$S^* = \bar{S} + \bar{CLK} = \bar{1} + \bar{1} = 0 + 0 = 0$$

$$R^* = \bar{R} + \bar{CLK} = \bar{1} + \bar{1} = 0 + 0 = 0$$

Table: Truth table for S-R flip flop

CLK	S	R	Q_{n+1} (Next State)
0	X	X	Q_n = Present State (Memory)
1	0	0	Q_n = Present State (Memory)
1	0	1	0
1	1	0	1
1	1	1	Invalid [Do not use this configuration]

Table: Characteristics table of S-R flip flop

Q_n	S_n	R_n	Q_{n+1}
0	0	0	$Q_n(0) = 0$
0	0	1	$0 = 0$
0	1	0	$1 = 1$
0	1	1	$X = X$ (Indeterminate)
1	0	0	$Q_n(1) = 1$
1	0	1	$0 = 0$
1	1	0	$1 = 1$
1	1	1	$X = X$ (Indeterminate)

Table: Excitation table for S-R flip flop

Q_n		Q_{n+1}	S	R
0		0	0	X
0		1	1	0
1		0	0	1
1		1	X	0

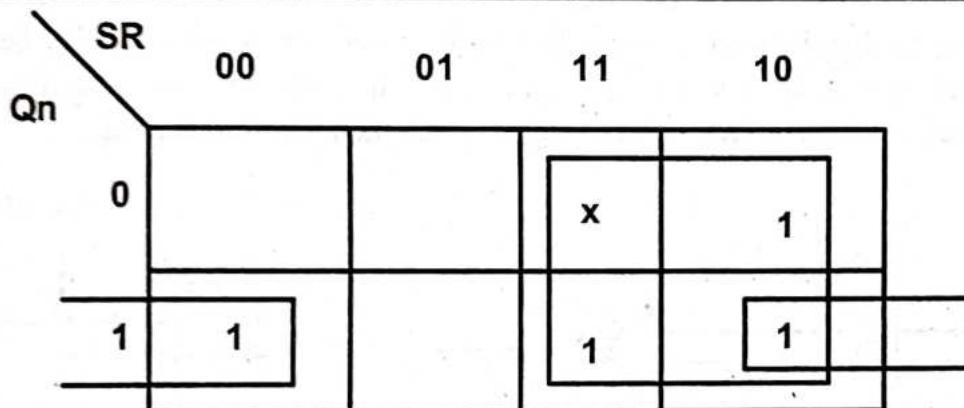


Table: K-map for Excitation table of S-R flip flop

The characteristic equation can be generated from the excitation table of SR flip flop. The characteristic equation is given by:

$$\therefore Q_{n+1} = Q_n \bar{R}_n + S_n$$

Next State = function of present state and input.

Gated Flip-Flops:

The addition of two AND gates at the R and S inputs will result in a flip flop that can be enabled or disabled. When the ENABLE input is HIGH, information at the R and S will be transmitted directly to the outputs. The latch is said to be enabled. When the ENABLE input is LOW, the AND gate outputs must be low and changes in neither R nor S will have any effect on the flip flop output Q. The latch is said to be disabled.

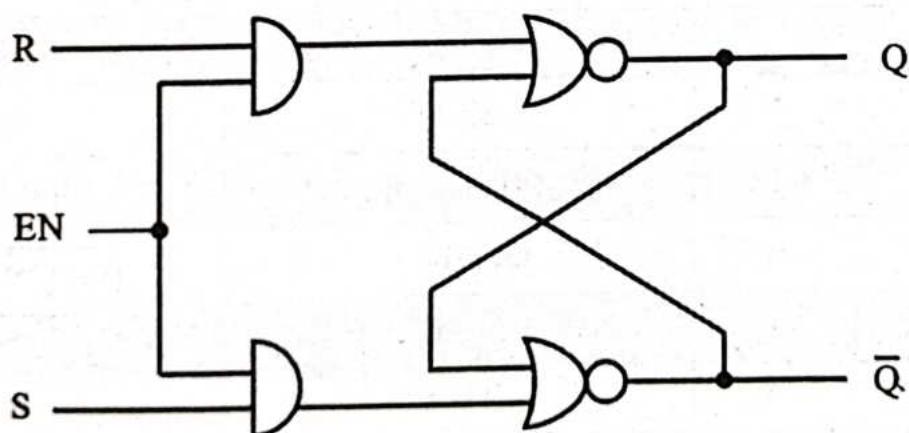


Figure: Gated R-S flip-flop (NOR)

Enable (EN)	S	R	Q_{n+1}
0	X	X	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	Invalid

Figure: Truth Table

When two inputs signal R and S are applied to the circuit, there is time delay between these signals, which may lead to a wrong output result. In order to overcome this problem of unequal propagation delay time of input signals, the gated flip flop is used.

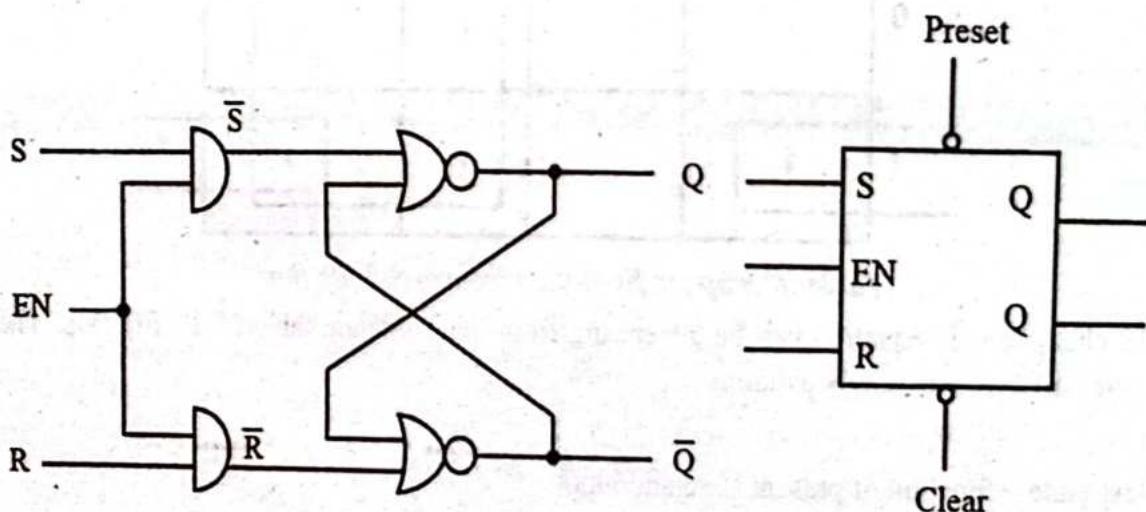


Figure: Gated RS flipflop (NAND)

Figure: Logic symbol

The characteristics table of gated RS Flip flop is given by:

Q_n	S_n	R_n	Q_{n+1}	Remark
0	0	0	$Q_n(0) = 0$	No change
0	0	1	$0 = 0$	Reset
0	1	0	$1 = 1$	set
0	1	1	$X = X$ (Indeterminate)	Invalid
1	0	0	$Q_n(1) = 1$	set.
1	0	1	$0 = 0$	Reset
1	1	0	$1 = 1$	set
1	1	1	$X = X$ (Indeterminate)	Invalid

SR

Q_n	00	01	11	10
0	0	0	x	1
1	1	0	x	1

$$Q_n + 1 = S + Q_n R$$

This is the characteristic equation

Gated D flip flop (Delay or Data Flip-flop)

The data flip flop has only one input called data (D) input and two output Q and \bar{Q} . It can be constructed from S-R flip flop by inserting an inverter between S and R and assigning the symbol D to S input. The output Q is same as D input.

The D flip flop is designed to overcome the problem of forbidden state and race conditions. It is a circuit that has single S input that is inverted using a NAND gate and given to the R input. Hence, two separate inputs are not required. The single S input is called the D-input. D-flip flop is the modification of the clock S-R flip-flop.

Table: Truth tables for S-R flip flop

CLK	S	R	$Q_n + 1 (N.S)$
0	X	X	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	Invalid X

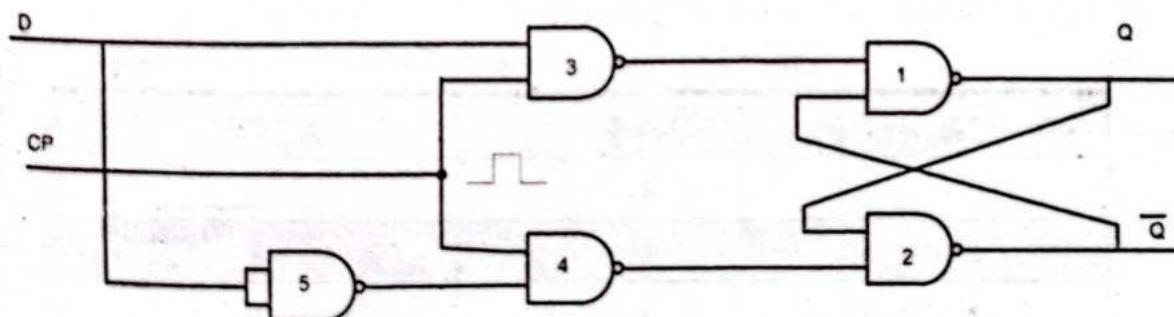


Figure: Logic Circuit Diagram of gated D Flip Flop using NAND gate

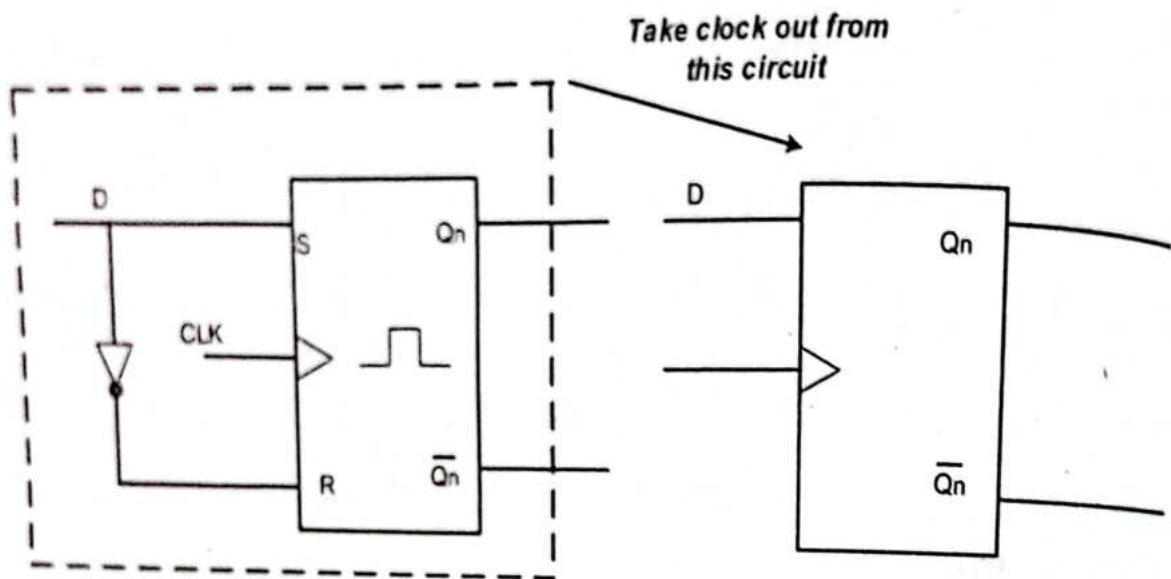


Figure: Graphics Symbol of D Flip Flop

Table: Truth table for D flip flop

CLK	D	Q_{n+1}	
0	X	Q_n (Previous i/p)	Whatever the value of D the o/p will not be affected.
1	0	0	
1	1	1	

The Characteristics table is derived from Truth Table

Table: Characteristics table for D flip flop

Q_n	D	Q_{n+1}	Remark	
0	0	0	Same as D	The next state will depend on the input and previous state.
0	1	1	Same as D	
1	0	0	Same as D	
1	1	1	Same as D	

The next state is same as Data input.

$$D = Q_n + 1$$

Excitation table is derived from characteristics table:

Table: Excitation table for D flip flop

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

$$D = Q_n + 1$$

-Map for characteristics equation

	D	0	1
Q _n	0	0	1
1	2	1	3

Table: K-map for Excitation table of D flip flop

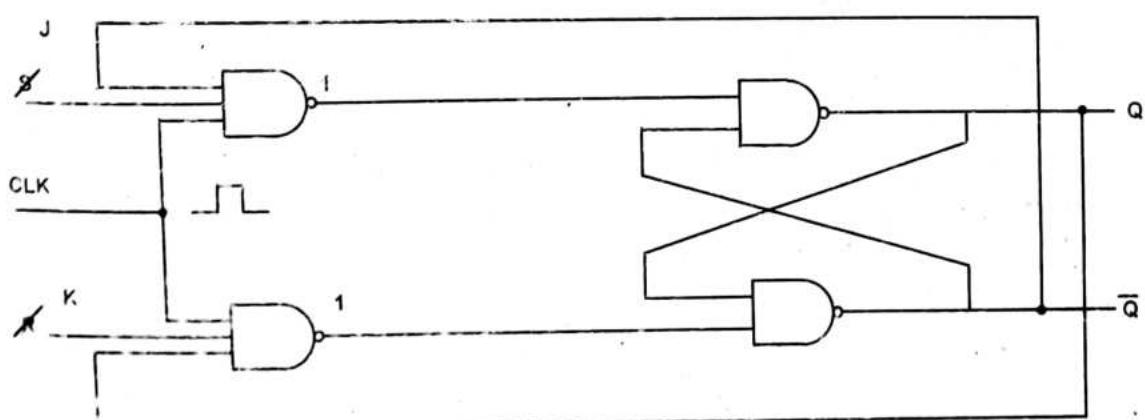
$$Q_{n+1} = D$$

Advantages of D flip flop over RS Flip flops:

In some events, both inputs become high in RS flip-flop which is undesirable condition. The drawback of RS flip flop is overcome in D flip flop. There is only one input that is D which drive the flip flop

Edge Triggered Flip-Flop:

- A J-K flip flop is basically a gated S-R flip flop with addition of clocked input circuit
- A JK flip-flop is a refinement of the S-R flip-flop in that the indeterminate state of SR type is defined in the JK types. Input J and K behave like inputs S and R to set and clear the flip flop (not that in a JK flip-flop, the letter J is for set and the letter K is for clear). When inputs are applied to both J and K simultaneously, the flip-flop switches to its complement state, that is, if Q=1, it switches to Q=0, and vice versa.
- Following Figure (a) shows the logic circuit diagram of J-K flip flop and figure (b) shows the logic circuit diagram of S-R latch using NAND gate



Figure(a): Logic Circuit Diagram of J-K Flip Flop

Table: Truth table for J-K flip flop

CLK	S (J)	R (K)	Q_{n+1}
0	X	X	Q_n (memory)
1	0	0	Q_n (memory)
1	0	1	0
1	1	0	1
1	1	1	Not used

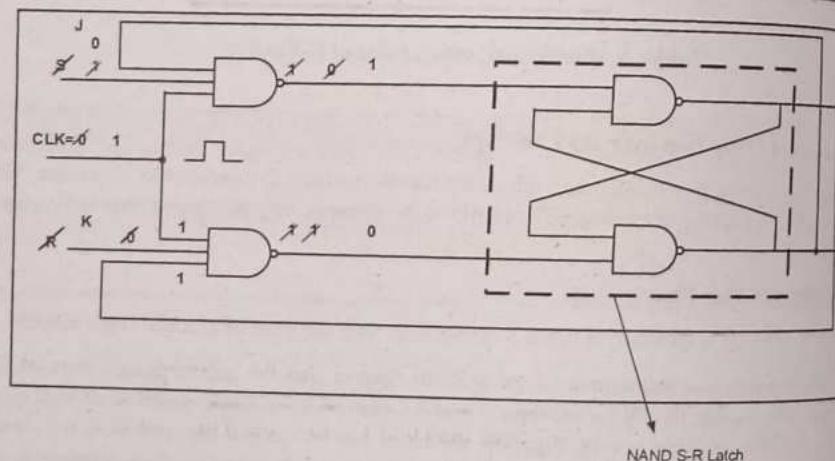


Figure (b): Logic Circuit Diagram of SR latch using NAND gate

Following Four condition are observed in JK flip-

- When Clock is low, $CLK=0$ and When the input to the NAND S-R Latch is 1,1 That is $CLK=0$, Memory (Q_n)
- When $CLK=1$, $J=1$, $K=0$ The value of $Q=1$ and $\bar{Q}=0$
- When $CLK=1$, $J=0$, $K=1$, $\bar{Q}=1$, and $Q=0$
- For $CLK=1$, $J=1$, $K=1$

Initially, assume $Q=0$ and $\bar{Q}=1$

$$Q = 0, 1, 0, 1$$

$$\text{And } \bar{Q} = 1, 0, 1, 0$$

This condition is called Racing.

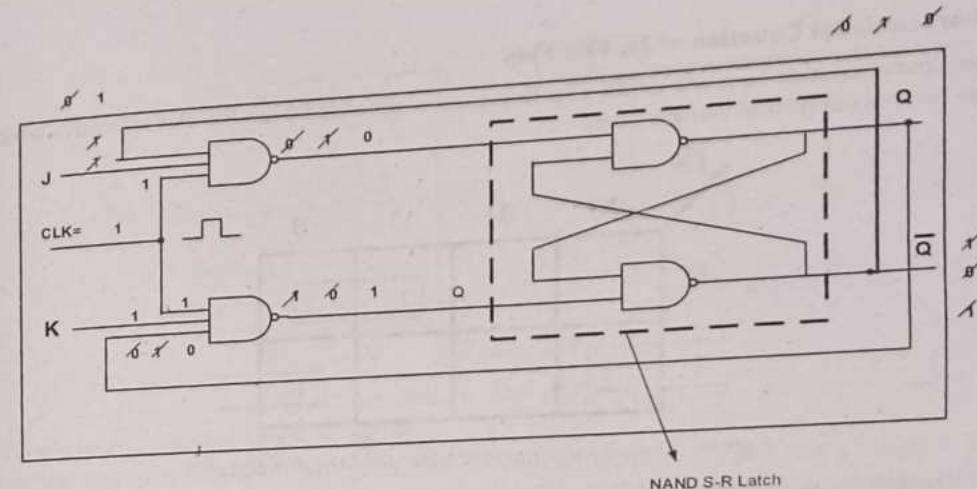


Figure: Logic Circuit Diagram of JK latch using NAND gate

Table: Truth table for J-K flip flop

CLK	S (J)	R (K)	Q_{n+1}
0	X	X	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	Q_n (Toggle)

Toggle means that output quickly changes from 0 to 1, 1 to 0, and 0 to 1 and so on.

Characteristics Table for J-K Flip Flop

Since, next state (Q_{n+1}) is dependent on the present input J and K and previous state.

Table: Characteristic table for J-K flip flop

Q_n	J	K	Q_{n+1}
0	0	0	$Q_n = 0$
0	0	1	0
0	1	0	1
0	1	1	$\bar{Q}_n = \bar{0} = 1$
1	0	0	$Q_n = 1$
1	0	1	0
1	1	0	1
1	1	1	$\bar{Q}_n = \bar{1} = 0$

Table: Truth table for J-K flip flop

CLK	S (J)	R (K)	Q_{n+1}
0	X	X	Q_n (memory)
1	0	0	Q_n (memory)
1	0	1	0
1	1	0	1
1	1	1	Not used

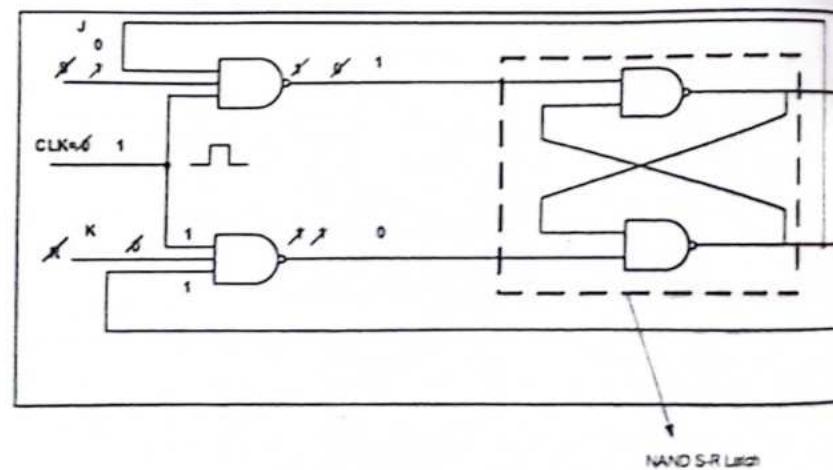


Figure (b): Logic Circuit Diagram of SR latch using NAND gate

Following Four condition are observed in JK flip-

- When Clock is low, CLK=0 and When the input to the NAND S-R Latch is 11 That is CLK=0, Memory (Q_n)
- When CLK= 1, J=1 , K=0 The value of Q= 1 and $\bar{Q}=0$
- When CLK= 1, J=0, K=1, $\bar{Q}=1$, and Q=0
- For CLK= 1, J=1, K=1

Initially, assume Q=0 and $\bar{Q}=1$

$$Q = 0, 1, 0, 1 \dots$$

And $\bar{Q} = 1, 0, 1, 0 \dots$

This condition is called Racing.

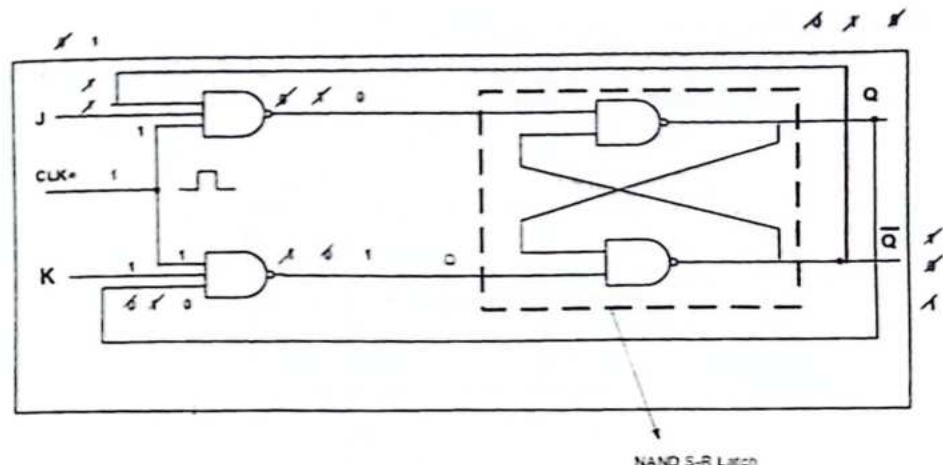


Figure: Logic Circuit Diagram of JK latch using NAND gate

Table: Truth table for J-K flip flop

CLK	S (J)	R (K)	Q_{n+1}
0	X	X	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	Q_n (Toggle)

Toggle means that output quickly changes from 0 to 1, 1 to 0, and 0 to 1 and so on.

Characteristics Table for J-K Flip Flop

Since, next state (Q_{n+1}) is dependent on the present input J and K and previous state.

Table: Characteristic table for J-K flip flop

Q_n	J	K	Q_{n+1}
0	0	0	$Q_n = 0$
0	0	1	0
0	1	0	1
0	1	1	$\bar{Q}_n = \bar{0} = 1$
1	0	0	$Q_n = 1$
1	0	1	0
1	1	0	1
1	1	1	$\bar{Q}_n = \bar{1} = 0$

Characteristics Equation of JK Flip Flop

The characteristics equation of JK flip flop can be generated from the characteristics table. The table is simplified using k map.

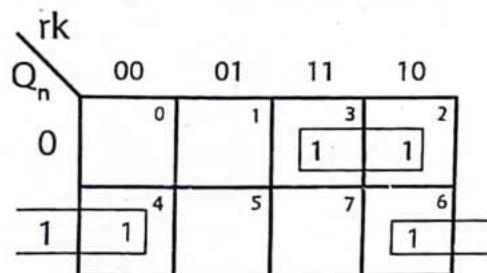


Figure: K-map for Characteristic table of J-K flip flop

Characteristics equation of JK FF

Therefore, $Q_{n+1} = Q_n \bar{K} + \bar{Q}_n J$ (This is the characteristics equation of JK FF)

Excitation Table:

Excitation table can be derived from the characteristics table.

Table: Excitation table for J-K flip flop

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

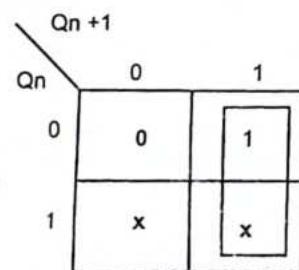


Figure: K-map for Excitation table of J-K flip flop

Therefore, $J = Q_{n+1}$

$$K = \overline{Q_{n+1}}$$

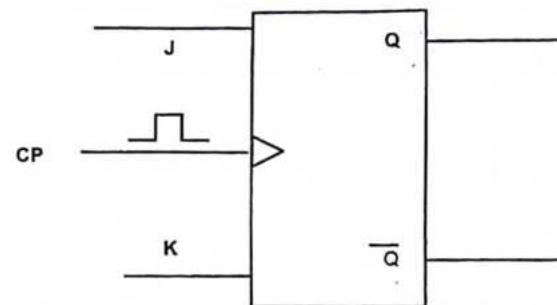


Figure: Graphics symbol of JK flip flop

Race around condition in JK Flip Flop

For J-K flip-flop, if $J=K=1$, and if $CLK=1$ for a long period of time, then Q output will toggle as long as CLK is high, which makes the output of the flip-flop unstable or uncertain. This problem is called race around condition in J-K flip-flop. This problem (Race around Condition) can be avoided by ensuring that the clock input is at logic "1" only for a very short time. This introduced the concept of Master Slave JK flip flop.

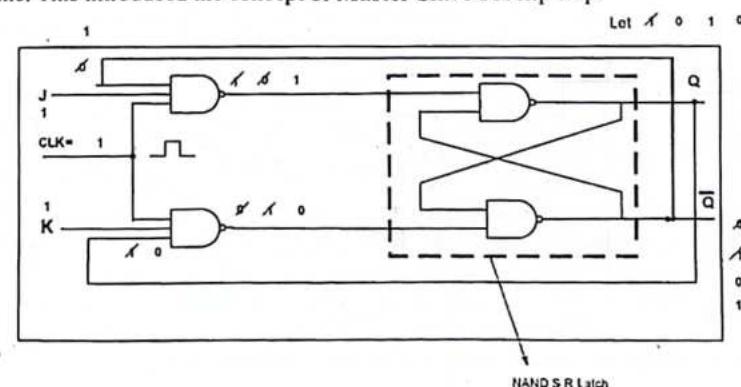


Figure: Race around condition in J-K Flip Flop

Master-Slave:

- The given Figure describes the concept of a Master-Slave Flip-Flop. This type of circuit is composed of two JK flip-flops that are connected in a series configuration, with one acting as the "master" and the other as the "slave." The output from the master flip-flop is connected to the inputs of the slave flip-flop, and the output from the slave is fed back to the inputs of the master. The circuit also includes an inverter that is connected to the clock pulse. The inverter inverts the clock pulse, so that the clock pulse for the slave flip-flop is the inverse of the clock pulse for the master. In other words, if the CP is 0 for the master flip-flop, it is 1 for the slave, and if the CP is 1 for the master, it is 0 for the slave.

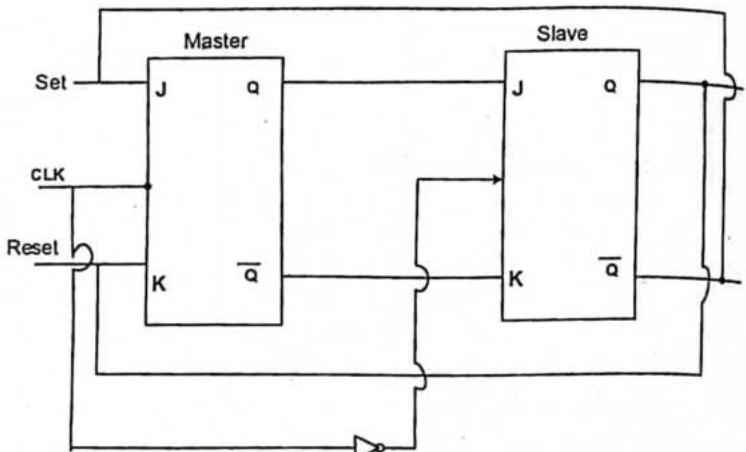


Figure: Logic diagram of Master Slave J-K flip flop

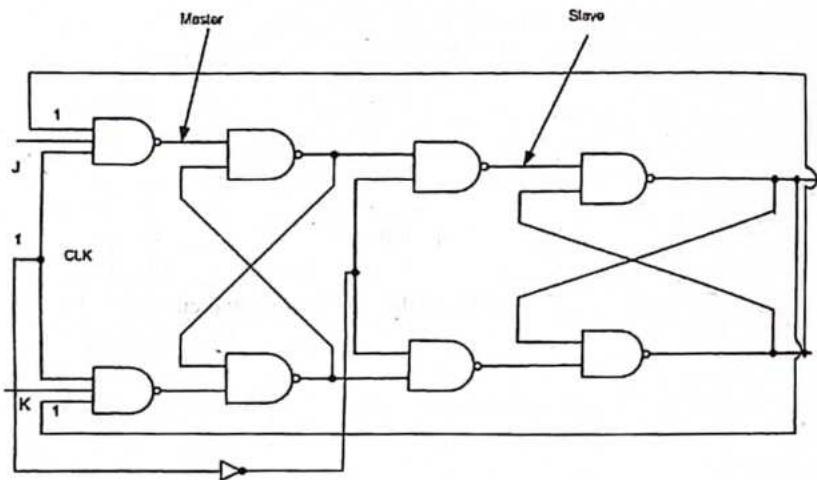


Figure: Working principle of Master Slave J-K Flip Flop

Table: Truth table for J-K flip flop

CLK	S (J)	R (K)	Q_{n+1}
0	X	X	Q_n (memory)
1	0	0	Q_n (memory)
1	0	1	0
1	1	0	1
1	1	1	Q_n (Toggle)

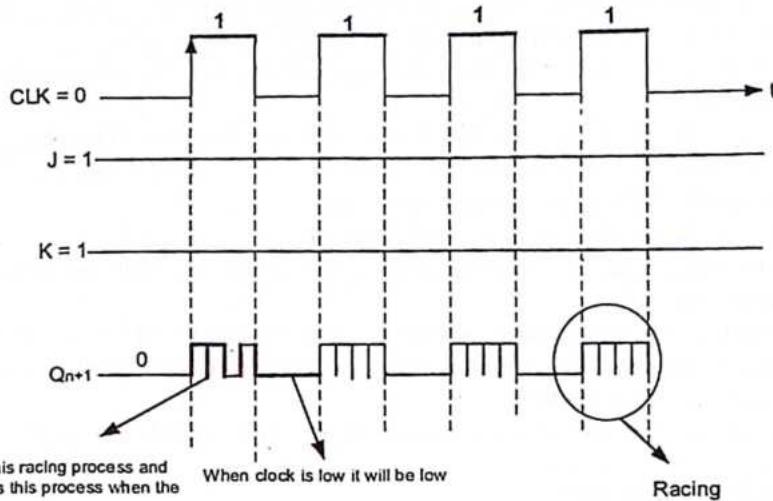


Figure: Timing diagram of Master Slave J-K flip flop

Conditions to overcome racing:

- $T/2 <$ propagation delay of Flip Flop
- Edge triggering
- Master slave (Negative edge triggered flip-flop)

Excitation Table of Flip-Flop

A flip-flop excitation table is a table used in the design of sequential circuits to determine the necessary input conditions that result in a desired change in state. This table provides a convenient way to determine the input conditions that will cause the required transition and is an essential tool in the design of flip-flop based sequential circuits.

SR Flip-flop				D Flip-flop		
Q(t)	Q(t+1)	S	R	Q(t)	Q(t+1)	DR
0	0	0	X	0	0	0
0	1	1	0	0	1	1
1	0	0	1	1	0	0
1	1	X	0	1	1	1

JK flip-flop				T flip-flop		
Q(t)	Q(t+1)	J	K	Q(t)	Q(t+1)	DR
0	0	0	x	0	0	0
0	1	1	x	0	1	1
1	0	x	1	1	0	1
1	1	x	0	1	1	0

Figure: Excitation table of different flip-flop

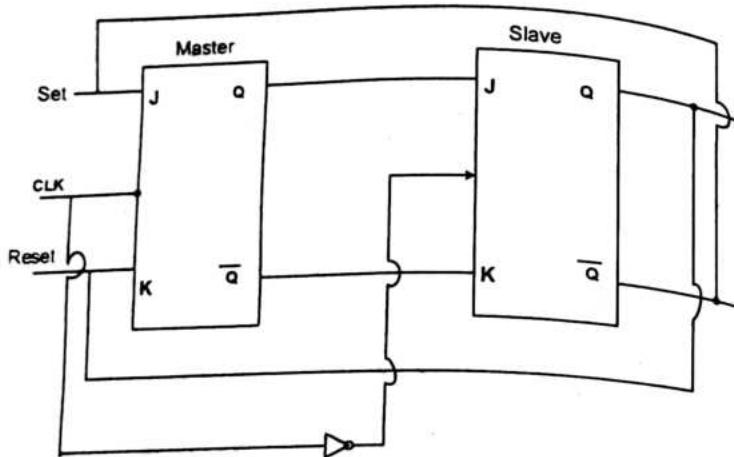


Figure: Logic diagram of Master Slave J-K flip flop

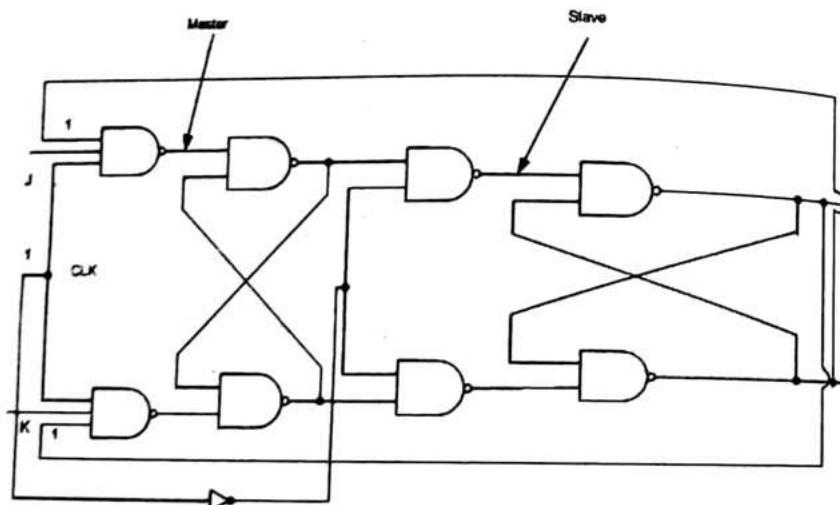


Figure: Working principle of Master Slave J-K Flip Flop

Table: Truth table for J-K flip flop

CLK	S (J)	R (K)	Q_{n+1}
0	X	X	Q_n (memory)
1	0	0	Q_n (memory)
1	0	1	0
1	1	0	1
1	1	1	Q_n (Toggle)

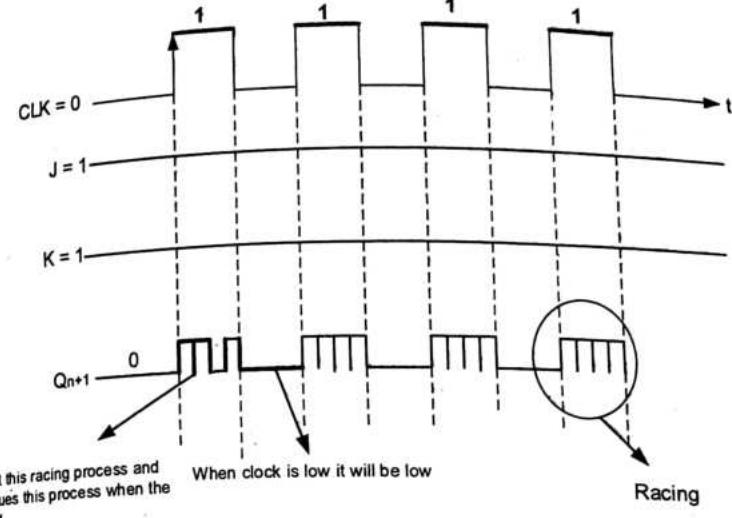


Figure: Timing diagram of Master Slave J-K flip flop

Conditions to overcome racing:

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Excitation Table of Flip-Flop

A flip-flop excitation table is a table used in the design of sequential circuits to determine the necessary input conditions that result in a desired change in state. This table provides a convenient way to determine the input conditions that will cause the required transition and is an essential tool in the design of flip-flop based sequential circuits.

SR Flip-flop			
$Q(t)$	$Q(t+1)$	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

D Flip-flop		
$Q(t)$	$Q(t+1)$	DR
0	0	0
0	1	1
1	0	0
1	1	1

JK flip-flop			
$Q(t)$	$Q(t+1)$	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

T flip-flop		
$Q(t)$	$Q(t+1)$	DR
0	0	0
0	1	1
1	0	1
1	1	0

Figure: Excitation table of different flip-flop

Things to Remember

- The output of the flip-flop changes more than once.
- It occurs when $J=K=1$ and propagation delay of flip-flop T_{PD} is less than clock pulse width T_{PW} .
- The overall circuit acts as a single flip-flop and stores one bit of information.
- The problem of race around condition is not present in M-S J-K flip-flop.
- The master is triggered when the clock goes to 1.
- The slave is triggered when the clock goes to 0.
- When clock is inactive, then the next state of the flip-flop is the previous state or no change in the state.
- D flip-flop behaves as a combinational circuit and the buffer behaves as a D flip-flop.
- If the output of the flip flop changes more than once in same clock period, then it is called race around condition.
- Race around condition can be eliminated by master slave flip flop or edge triggered flip flop.

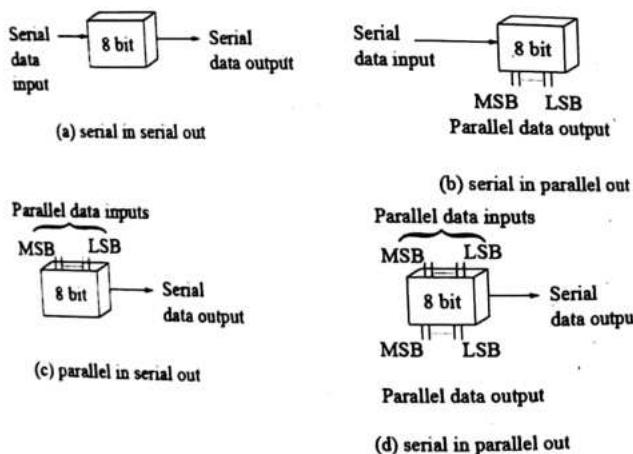
Introduction to Register

A register is the group of binary cells suitable for holding information.

- It is a group of flip flop sensitive to pulse transition.
- A register is a digital circuit with two basic functions: Data Storage and data movement.
- A register consists of one or more flip flop used to store and shift data.
- An 'n' bit register consists of a group of 'n' flip flop capable of storing n bits binary information. A register capable of shifting its binary information in one or more direction is called shift register.
- Registers are essential synchronous system.

Types of Register:

There are four types of Register:



- Serial In Serial Out (SISO):** SISO shift registers accept data serially i.e., one bit at a time and output taken from it is also in serial form.
- Serial In Parallel Out (SIPO):** Data are entered serially but output is taken parallelly. Once the data are stored, each bit appears on its respective output line, all at a time.
- Parallel In Serial Out (PISO):** A parallel-in serial-out (PISO) shift register is a type of digital circuit that takes a parallel input and converts it into a serial output. The input data is stored in parallel, meaning each data bit is stored in a separate flip-flop or storage element. The data is then shifted out in a serial fashion, with each bit being shifted out one after the other in sequence. PISO shift registers are useful for converting parallel data into a serial format for transmission or storage, as serial data is easier to transmit or store than parallel data. The circuit can be used for a variety of applications, including data storage, data transmission, and data manipulation.
- Parallel In Parallel Out (PIPO):** Data are entered simultaneously into their respective stage on parallel lines rather than on a bit by bit basis. Output is available simultaneously.

Applications of shift Register:

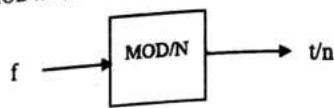
Shift registers have a variety of applications in digital circuits, some of the most common include:

- Data storage:** Shift registers can be used as a form of memory to store digital data. They are especially useful in situations where a small amount of data needs to be stored temporarily.
- Serial-to-parallel conversion:** Shift registers can be used to convert serial data into parallel data, making it easier to process.
- Parallel-to-serial conversion:** Shift registers can also be used to convert parallel data into serial data, which is useful for transmitting data over a single communication line.
- Data shifting:** Shift registers can be used to shift data from one register to another in a cyclic manner. This is useful in many applications, such as digital filtering, digital signal processing, and image processing.
- Pattern generation:** Shift registers can be used to generate various digital patterns, such as pseudo-random sequences, codes, and waveforms.
- Display interfaces:** Shift registers are commonly used in display interfaces to control the data flow to displays such as LEDs, LCDs, and OLEDs.
- Input/output expansion:** Shift registers can be used to expand the number of inputs and outputs in a digital circuit.
- As ring counter and Johnson counter

Synchronous and Asynchronous Counter:

The combination of flip flop that performs the counting operation are known as counter. A counter is probably one of the most useful and versatile subsystems in a digital system. It is a sequential circuit that passes through predefined number of states.

- Counter are basically used to count number of clock pulse applied. It can also be used for frequency divider, time measurement, frequency measurement, range measurement, pulse width and waveform generator.
- With n -FF, maximum possible stage in the counter is 2^n
- $N < 2^n$ or $n > \log_2 N$
Where, N =number of state
- $N =$
Counter are classified into two broad categories according to the way they are clocked:
 n = number of FF.
- Number of stages used in counter mean modulus of counter, i.e., if MOD is 5, then counter = 5 stages and if MOD is n , then counter = n stage.



- For example, a decade counter is applied with frequency of 10 MHz, then output frequency is:

$$f_{out} = \frac{t_{in}}{10} = 10 \text{ MHz}$$

a. Asynchronous (ripple or Serial) Counter:

- In this counter, the first flip flop is clocked by the external clock pulse and then each successive flip flop is clocked by the output of the preceding flip flop.
- Asynchronous counter is simple and straightforward in operation and its construction usually requires a minimum number of hardware.
- It does not have speed limitation.
- FFs are not clocked simultaneously
- It is very simple.
- The speed of operation is very slow
- The power consumption is less
- Minimum hardware is required
- The cost is less

b. Synchronous (Parallel) Counter:

- In synchronous counter, the clock input is connected to all of the flip flops so that they are clocked simultaneously.
- An increase in speed of operation can be achieved by use of synchronous counter.
- FFs are clocked simultaneously

- It is very complex
- The speed of operation is fast
- The power consumption is more
- It requires more hardware
- The cost is more.

Comparison between synchronous and asynchronous counter:

Asynchronous/Ripple/Serial	Synchronous/Ring/Parallel
Different FFs are applied with different clock	All FFs are applied with the same clock
It is slower	It is faster
There is a fixed count sequence that is: up or down.	Any count sequence is possible
Decoding error are present	No decoding error are present
These are also called ripple counter or serial counter	These are also called ring or parallel counter.
Time delay of all flip flop + time delay of combinational circuit.	Time delay of one flip flop + time delay of combinational circuit.

Up/down synchronous counters:

It is defined as a bidirectional counter that is capable of counting either up or down. An input (control) line $\overline{\text{up/down}}$ (or simply up) specifies the direction of counting.

$\overline{\text{up/down}} = 1 \rightarrow$ count upward

$\overline{\text{up/down}} = 0 \rightarrow$ count downward

BCD Counter:

- It is an MSI device which counts the BCD sequence.

Ring Counter:

- This counter counts a prescribed number of pulses and returns back to zero

Mod-n Counter

- This counter counts the pulses till $(n-1)$

14 MICROPROCESSOR: PROGRAMMING

Internal Architecture of Microprocessor

The 8085A (commonly known as 8085) is an 8-bit general purpose microprocessor capable of addressing 64K of memory.

The device has 40 pins, require a +5V single power supply and can operate with a 3-MHZ, single phase clock.

The Intel 8085 A is a complete 8-bit parallel central processing unit. The main components of 8085A are array of registers, the arithmetic logic unit, the encoder/decoder, and timing and control circuits linked by an internal data bus. The block diagram is shown in Figure.

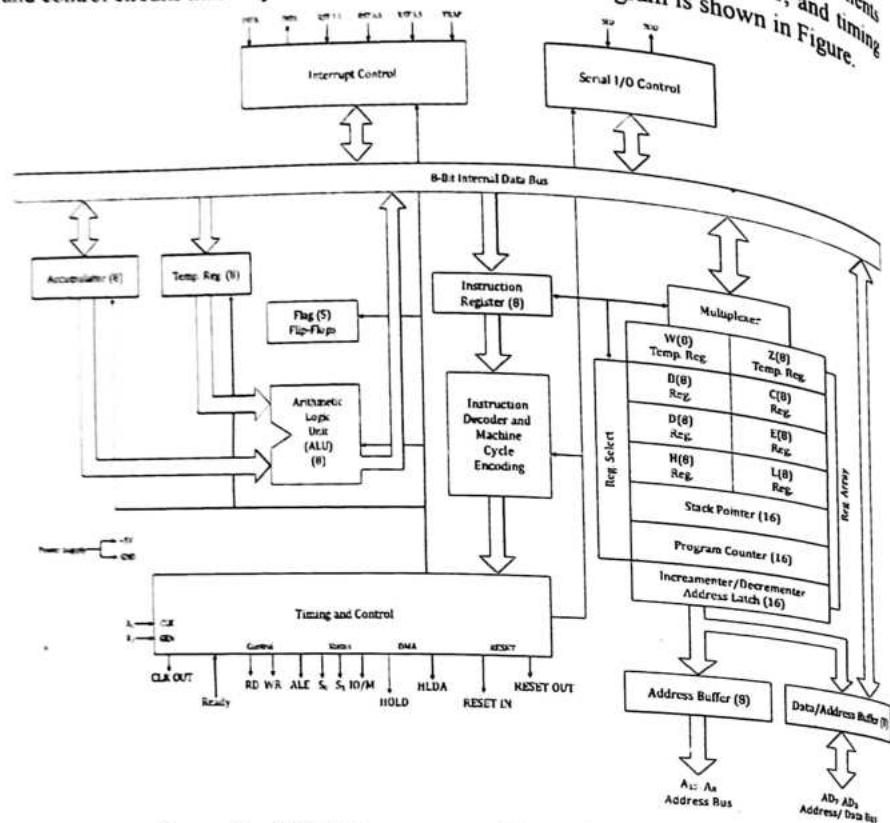


Figure: The 8085 A Microprocessor Functional Block Diagram

a) Arithmetical and Logic Unit (ALU)

The Arithmetic Logic Unit (ALU) is the central component of the computing system and performs various arithmetic and logic operations. The ALU comprises several components, including the accumulator, the temporary register, arithmetic and logic circuits, and five flags. The temporary register is used to temporarily store data during an arithmetic or logic operation, while the final result is stored in the accumulator. Additionally, the flags (which are flip-flops) are set or reset based on the outcome of the operation.

b) Accumulator (register A)

- It is one of the general-purpose registers of microprocessor also called as A register.
- The accumulator is an 8-bit register that is a part of arithmetic/logic unit (ALU).

This register is used to store 8-bit data and to perform arithmetic and logical operations.

The result of an operation is stored in the accumulator. The user can access this register by giving appropriate instructions (commands).

c) Temporary registers (W & Z)
It is also called as operand register (8 bit). It provides operands to ALU. ALU can store immediate result in temporary register. It is not accessible by user.

d) Instruction register (IR)

- It is an 8 bit register not accessible to the programmer.
- It receives the operation codes of instruction from internal data bus and passes to the instruction decoder which decodes so that microprocessor knows which type of operation is to be performed.

e) Register Array
(Scratch pad registers B, C, D, and E): It is an 8-bit register accessible to the programmers.

- Data can be stored upon it during program execution.
- These can be used individually as 8-bit registers or in pair BC, DE as 16-bit registers.
- The data can be directly added or transferred from one to another.
- Their contents may be incremented or decremented and combined logically with the content of the accumulator.

f) Register H & L

- They are 8-bit registers that can be used in same manner as scratch pad registers.

g) Stack Pointer (SP)

- It is a 16-bit register used as a memory pointer.
- A stack is nothing but the portion of RAM (Random access memory).
- It points to a memory location in R/W memory, called the stack.
- The beginning of the stack is defined by loading a 16-bit address in the stack pointer.
- The stack is usually accessed in Last in First out (LIFO) fashion.

h) Program Counter (PC)

- It contains the address of the next instruction to be fetched from Memory.
- Program counter is a special purpose register.

Flag
The Flag register is a Special Purpose Register. Depending upon the value of result after any arithmetic and logical operation the flag bits become set (1) or reset (0). In 8085 flags are described as:

D7	D6	D5	D4	D3	D2	D1	D0	CY
S	Z		AC		P			

a) Carry Flag/ Borrow Flag

- If the last operation generates a carry its status will 1 otherwise 0. It can handle the carry or Borrow from one word to another.
- Carry Flag is also known as Borrow Flag.
- During subtraction (A-B), if A>B it becomes reset and if (A<B) it becomes set. 1-carry out from MSB bit on addition or borrow into MSB bit on subtraction. 0-no carry out or borrow into MSB bit

b) Zero

- If the result of last operation is zero, its status will be 1 otherwise 0. It is often used in loop control and in searching for particular data value.
- After any arithmetical or logical operation if the result is 0 (00) H, the zero flag becomes set i.e. 1, otherwise it becomes reset i.e. 0. 00H zero flag is 1, from 0FH to FFH zero flag is 0
- 1- zero result, 0- non-zero result

c) Sign

- If the most significant bit (MSB) of the result of the last operation is 1 (negative), then its status will be 1 otherwise 0.
- After any operation if the MSB (B (7)) of the result is 1, it indicates the number is negative and the sign flag becomes set, i.e. 1. If the MSB is 0, it indicates the number is positive and the sign flag becomes reset i.e. 0. from 00H to 7F, sign flag is 0 from 80H to FF, sign flag is 1
- MSB is 1 (negative), 0- MSB is 0 (positive)

d) Parity

- If the result of the last operation has even number of 1's (even parity), its status will be 1 otherwise 0.
- If after any arithmetic or logical operation the result has even parity, an odd number of 1 bit, the parity register becomes set i.e. 1, otherwise it becomes reset i.e. 0.

e) Auxiliary carry

- If the last operation generates a carry from the lower half word (lower nibble), status will be 1 otherwise 0. Used for performing BCD arithmetic.

Timing and Control Unit

- It is used to generate timing and control signals which are necessary for the execution of instructions. It is used to control data flow between CPU and peripherals (including memory).

- It provides timing and control signals.
- Following are the timing and control signals:
- Control Signals: READY, RD', WR', ALL
- Status Signals: S0, S1, IO/M
- DMA Signals: HOLD, HLDA
- RESET Signals: RESET IN, RESET OUT

Interrupt Controls:

- The various interrupt controls signal (INTR, RST 5.5, RST 6.5, RST 7.5 and TRAP) are used to interrupt a microprocessor.

Serial I/O controls:

- It controls the serial data communication by using these two instructions: SID (Serial input data) and SOD (Serial output data).

Characteristics (Features) of 8085A Microprocessor and its Signals

The all the signals associated with 8085 can be classified into 6 groups:

BUS:

The 8085 has 16 signal lines that are used as the address bus; however, these lines are split into two segments A₁₅-A₈ and AD₇-AD₀. The eight signals A₁₅-A₈ are unidirectional and used as high order bus.

- a) Data Bus:** The signal lines AD₇-AD₀ are bidirectional, they serve a dual purpose. They are used the low order address bus as well as data bus.

- b) Control and status signals:** This group of signals includes two control signals (RD and WR), three status signals (IO/M, S1 and S0) to identify the nature of the operation, and one special signal (ALE) to indicate the beginning of the operation.

- c) ALE- Address Latch Enable:** This is a positive going pulse generated every time the 8085 begins an operation (Machine Cycle): It indicates that the bits AD₇-AD₀ are address bits. This signal is used primarily to latch the low-order address from the multiplexed bus and generate a separate set of eight address lines A₇-A₀.

- RD- Read:** this is a read control signal (active low). This signal indicates that the selected I/O or memory device is to be read and data are available on the data bus.

- WR Write:** This is a write control signal (active low). This signal indicates that the data on the data bus are to be written into a selected memory or I/O location.

- IO/M:** This is a status signal used to differentiate between I/O and memory operations. When it is high, it indicates an I/O operation; When it is low indicates a memory operation.

- Memory Operation:** This signal is combined with RD (Read) and WR (Write) to generate I/O and memory signals.

- S1 and S0:** These status signals, similar to IO/M, can identify various operations, but they are rarely used in small systems.

Supply and Clock Frequency:

- a) VCC: +5V power supply
- b) VSS: Ground reference
- c) X1 and X2: A crystal (RC or LC network) is connected at these two pins for frequency control. It can be used as the system clock for other devices.

Externally Initiated Signals:

- INTR (Input): interrupt request, used as a general-purpose interrupt.
- INTA (Output): This is used to acknowledge an Interrupt.
- RST 7.5, 6.5, 5.5 (Inputs): These are vectored interrupts that transfer the program control to specific memory locations. They have higher priorities than INTR interrupt. Among these three, the priority order is 7.5, 6.5, and 5.5.
- TRAP (input): This is a non-Maskable interrupt with highest priority.
- HOLD (input): This signal indicates that a peripheral such as a DMA (Direct Memory Access) controller is requesting use of Address and data bus.
- HLDA (output): Hold Acknowledge: This signal acknowledges the HOLD request.
- READY (Input): This signal is used to delay the microprocessor Read or Write cycle until a slow- responding peripheral is ready to send or accept data. When this signal goes low, the microprocessor waits for an integral number of clock cycles until it goes high.
- RESETIN: When the signal on this pin goes low, the program counter is set to zero, buses are tri-stated, and MPU is reset.
- RESET OUT: This signal indicates that the MPU is being reset. The signal can be used to reset other devices.

Serial I/O ports:

The 8085 has two signals to implement the serial transmission: SID (Serial Input Data) and SOD (Serial Output Data). In serial transmission, data bits are sent over a single line, one bit at a time, such as the transmission over telephone lines.

2.5 MICROPROCESSOR SYSTEM

Parallel Interface, Introduction to Programmable Peripheral Interface (PPI), Serial Interface, Synchronous and Asynchronous Transmission, Serial Interface Standards, Introduction to Direct Memory Access (DMA) and DMA Controllers. (AExE0205)

Parallel Interface:

The parallel interface is a method of communicating between a microprocessor and peripheral devices such as memory, input/output (I/O) devices, and other processors. In a parallel interface, multiple bits of data are transferred simultaneously on multiple parallel lines. This allows for a faster transfer of data compared to a serial interface, where data is transferred one bit at a time on a single line.

In a microprocessor-based system, the parallel interface is used to connect the microprocessor to external devices such as memory, I/O devices, and other processors. The microprocessor sends commands and data to these devices using the parallel interface, and it also receives data from these devices in the same manner.

Introduction to Programmable Peripheral Interface (PPI):

Programmable Peripheral Interface (PPI) is a digital interface standard used in programmable systems to communicate between peripheral devices and a microprocessor. It is a parallel interface, meaning that multiple bits of data are transferred simultaneously on multiple lines, allowing for faster data transfer compared to serial interfaces.

PPI is used to connect peripheral devices such as input/output (I/O) devices, memory, and other processors to the microprocessor. The microprocessor sends commands and data to these devices using the PPI, and it also receives data from these devices in the same manner.

Serial Interface:

A serial interface is a method of communicating between a microprocessor and peripheral devices such as memory, input/output (I/O) devices, and other processors. In a serial interface, data is transferred one bit at a time on a single line. This is in contrast to a parallel interface, where multiple bits of data are transferred simultaneously on multiple parallel lines.

In a microprocessor-based system, the serial interface is used to connect the microprocessor to external devices such as memory, I/O devices, and other processors. The microprocessor sends commands and data to these devices using the serial interface, and it also receives data from these devices in the same manner.

Synchronous and Asynchronous Transmission:

In microprocessor-based systems, synchronous and asynchronous transmission are used to communicate between the microprocessor and peripheral devices such as memory, input/output (I/O) devices, and other processors.

Synchronous transmission is used when a high data transfer rate is required and when a shared clock signal between the microprocessor and peripheral devices is available. This method is often used in applications where real-time communication is required, such as in industrial control systems, where the accurate timing of data is critical.

Asynchronous transmission is used when a shared clock signal is not available or when a simple and flexible communication solution is desired. This method is often used in applications where a fast data transfer rate is not a critical requirement, and where a simple and cost-effective communication solution is desired.

Serial Interface Standard:

There are several serial interface standards that are commonly used in microprocessor-based systems to communicate between the microprocessor and peripheral devices such as memory, input/output (I/O) devices, and other processors. Some of the most commonly used serial interface standards are:

Universal Asynchronous Receiver/Transmitter (UART): UART is a simple and widely used serial interface standard that is often used in embedded systems and other applications where a fast data transfer rate is not a critical requirement.

Inter-Integrated Circuit (I2C): I2C is a serial communication protocol that is used to connect peripheral devices to a microprocessor. It is widely used in embedded systems and other applications where multiple devices need to communicate with a single microprocessor.

Serial Peripheral Interface (SPI): SPI is a full-duplex serial communication protocol that is used to connect peripheral devices to a microprocessor. It is widely used in embedded systems and other applications where a fast data transfer rate is required.

RS-232: RS-232 is a standard for serial communication transmission of data. It is used to connect peripheral devices to a microprocessor and is widely used in industrial control systems, scientific instruments, and other applications where a fast data transfer rate is not a critical requirement.

RS-422 and RS-485: RS-422 and RS-485 are serial communication standards that are used to connect peripheral devices to a microprocessor. They are commonly used in industrial control systems, scientific instruments, and other applications where a fast data transfer rate is required and where the communication distance between devices is long.

Introduction to Direct Memory Access and DMA Controller:

Direct Memory Access (DMA) is a method used in microprocessor-based systems to transfer data directly between memory and peripheral devices without involving the microprocessor. This allows for faster data transfer and reduces the workload of the microprocessor, freeing it up to perform other tasks.

The DMA controller is responsible for managing the transfer of data between memory and peripheral devices. It communicates directly with the memory and peripheral devices, and also communicates with the microprocessor to set up the transfer and to obtain the necessary information about the transfer, such as the source and destination addresses, the size of the transfer, and the direction of the transfer.

2.6 INTERRUPT OPERATIONS

Interrupt:

In microprocessor architecture, an interrupt is a mechanism that allows a processor to temporarily stop executing its current task and attend to a high-priority request from another device, referred to as an interrupt request (IRQ).

Interrupts are a way for devices to communicate with the processor and request its attention, thereby allowing the processor to handle multiple tasks at the same time.

Interrupts can be triggered by a variety of events, such as the arrival of new data from a peripheral, a timer expiring, or an error occurring. When an interrupt is triggered, the processor stops its current task, saves its current state, and begins executing a special

interrupt service routine (ISR) associated with the interrupt. The ISR performs the necessary actions to service the interrupt, and when it is complete, the processor returns to the task it was previously executing, restoring its saved state.

Interrupt Service Routine (ISR):

Interrupt service routine (ISR) is actually a call back function (program) in case of software or device driver (I/O device) in case of hardware. When an interrupt is acknowledged by the processor, the routine or program which is running currently gets paused or interrupted, and the ISR program gets executed. An interrupt is a signal to the processor emitted by hardware or software indicating an event that needs immediate attention. Whenever an interrupt occurs, the controller completes the execution of the current instruction and starts the execution of an Interrupt Service Routine (ISR) or Interrupt Handler.

- An Interrupt Service Routine (ISR) is a piece of software code that is executed by the hardware in response to an interrupt.
- The ISR evaluates the interrupt and decides how to handle it. It performs the necessary actions to service the interrupt and then returns a logical value indicating the outcome.
- The main objective of an ISR is to process the interrupt and return control to the primary program. To prevent slowing down the device's performance and that of lower priority ISRs, an ISR must be executed quickly.
- Like procedures, the final instruction in an ISR should be a return statement.

A small program or a routine that when executed, services the corresponding interrupting source is called an ISR.

TRAP

It is a non-maskable interrupt, having the highest priority among all interrupts. By default, it is enabled until it gets acknowledged. In case of failure, it executes as ISR and sends the data to backup memory. This interrupt transfers the control to the location 0024H.

RST7.5

It is a maskable interrupt, having the second highest priority among all interrupts. When this interrupt is executed, the processor saves the content of the PC register into the stack and branches to 003CH address.

A Maskable Interrupt is an interrupt signal that has the second highest priority among all interrupts. When this interrupt is triggered, the microprocessor saves the current content of the Program Counter (PC) register onto the stack and branches to the address 003CH.

RST 6.5

It is a maskable interrupt, having the third highest priority among all interrupts. When this interrupt is executed, the processor saves the content of the PC register into the stack and branches to 0034H address.

RST 5.5

It is a maskable interrupt. When this interrupt is executed, the processor saves the content of the PC register into the stack and branches to 002CH address.

INTR

It is a maskable interrupt, having the lowest priority among all interrupts. It can be disabled by resetting the microprocessor.

When INTR signal goes high, the following events can occur –

- The microprocessor continuously checks the status of the INTR signal while executing each instruction.
- If the INTR signal is active (high), the microprocessor finishes the current instruction and sends a low-active Interrupt Acknowledge signal.
- After receiving the interrupt, the microprocessor saves the address of the next instruction to the stack and begins executing the received instruction.

Interrupt Processing

Interrupt processing refers to the process by which the microprocessor responds to an interrupt signal. When an interrupt is triggered, the microprocessor temporarily pauses its current task, saves the current state of the program and execution context, and begins executing the Interrupt Service Routine (ISR) associated with the interrupt. The ISR is responsible for processing the interrupt and determining the appropriate action to take. Once the ISR has completed its task, it returns control to the main program, and the microprocessor resumes its previous task. Interrupt processing is a crucial aspect of microprocessing, as it enables the microprocessor to handle external events and respond to them in a timely and efficient manner.

MULTIPLE CHOICE QUESTIONS

- Hexadecimal can express in one digit what is done by following binary number of binary digits
A. One B. Four
C. Two D. Eight
- NAND gates are preferred over others because these have lower fabrication area
A. Have lower fabrication area
B. Can be used to make any gate
C. Consume less electronic power
D. Provide maximum density in a chip
- According to Demorgan's theorem $A + B + C + D =$
A. $\bar{A}\bar{B}\bar{C}\bar{D}$ B. $AB + CD$
C. $A + BC + D$ D. $A + B + C + D$
- According to Demorgan's theorem $\bar{A}\bar{B}\bar{C}\bar{D} =$
A. $A + B + \bar{C} + \bar{D}$ B. $A + B + C + D$
C. $A + B + C + D$ D. $A + B + CD$
- The logic unit shown below is as the type
A. AND B. NAND
C. OR D. NOT
- The truth table shown below is for

Inputs		Outputs
a	b	
0	0	0
0	1	1
1	0	1
1	1	1

A. NAND B. OR
C. AND D. NOT
- Odd parity of word can be conveniently tested by
A. OR gate B. NOR gate
C. AND gate D. XOR gate
- A record at the end of file which contains control total is
A. Pointers B. Trunk
C. Trailer D. Trunkey
- Binary means
A. Three B. Ten
C. Four D. Two
- The digits used in a binary number system areand.....
A. 9 and 0 B. 1 and 2
C. 0 and 1 D. 3 and 4
- Names, numbers and other information needed to solve a problem are called
A. Program B. Data
C. Instruction D. Controls
- The is a sequence of instructions that tells the computer how to process the data
A. Data B. Controls
C. Program D. Instruction
- Computer ICs work reliably because they based on...design
A. Top-button B. Two-stage
C. System D. Two-status
- When a transistor is cut off or saturated, transistor.....have almost no effect
A. Wave B. Stage
C. Variations D. Circuits

15. A.....is group of devices that store digital data
 A. Circuits B. Variations
 C. Register D. Bit
16. is an abbreviation for binary digit
 A. 0 and 1 B. Base
 C. Binary D. Bit
17. A byte is a string of bits
 A. Two B. Eight
 C. Four D. Ten
18. The control and arithmetic-logic sections are called the,
 A. Block diagram
 B. Input/output unit
 C. Control unit
 D. Central Processing Unit
19. A microcomputer is a computer that uses afor its CPU
 A. Chips B. Microprocessor
 C. Registers D. Vacuum tube
20. The hexadecimal number system is widely used in analyzing and programming...
 A. Registers
 B. Microprocessors
 C. Chips
 D. Vacuum tube
21. The hexadecimal digits are 0 and 9 and A to...
 A. E B. G
 C. F D. D
22. The main advantage of hexadecimal numbers is the ease of conversion from hexadecimal toand vice versa
 A. Decimal B. ASCII
 C. Binary D. BCD

23. A typical microcomputer may have up to 65,536 registers in its memory. Each of these registers usually called a
 A. Address
 B. Chip
 C. Registers
 D. Memory location
24. Binary - Coded - decimal (BCD) numbers express each digit as a ...
 A. Bytes
 B. Bit
 C. Nibble
 D. All of the above
25. BCD numbers are useful whenever information is transferred into or out a digital system
 A. Decimal B. ASCII
 C. Binary D. Hexadecimal
26. The ASCII code is a 7-bit code for
 A. Letters
 B. Other symbols
 C. Numbers
 D. All of the above
27. The binary number 1100 0101 _{hu}bytes
 A. 1 B. 4
 C. 2 D. 8
28. How many bytes are there in 101 1001 0110 1110 numbers?
 A. 1 B. 4
 C. 2 D. 8
29. What is the base of F4C316 number?
 A. 2 B. 8
 C. 4 D. 16
30. What is the decimal equivalent of 2^{10} ?
 A. 4096 B. 1000
 C. 1024 D. 16
31. What does 4k represent?
 A. 4000 B. 40
 C. 4096 D. 400
32. Express 8192 in K units
 A. 8×10^3 K
 B. 8K
 C. 8.192K
 D. All of the above
33. Solve the following equation for X:
 $X_0 = 11001001_2$
 A. 201 B. 214
 C. 132 D. 64
34. A micro-processor has memory locations from 0000 to 3FFF. Each memory location stores 1 bytes. How bytes can the memory store? Express this in kilobytes
 A. 4095.4K B. 32740.32K C.
 16,38416K D. 46,04046K
35. If a microcomputer has 64K memory, what are the hexadecimal notations for the first and last memory location ?
 A. 0000, EEEE B. 0000, FFFF
 C. 0,64 D. 0000, 9999
36. How many nibbles are there in 1001 0000 0011 number
 A. Two B. One
 C. Three D. Eight
37. What is the ASCII code for T?
 A. 1010100 B. 1011100
 C. 1011010 D. 1011111
38. A gate is a logic circuit with one or more input signals but output signal
 A. Two B. One
 C. Double D. More than one

39. An inverter is a gate with only input; the output is always in the opposite state from the input
 A. One
 B. More than one
 C. Two
 D. All of the above
40. An inverter is also called agate
 A. NOT B. OR
 C. OR D. NAND
41. The OR gate has two or more input signals. If any input is the output is high
 A. Low
 B. 0
 C. High
 D. All of the above
42. The number of input words in a truth table always equals...., where n is the number of input bits
 A. 10^n B. 4^n
 C. 2^n D. 8^n
43. Thegate has two or more input signals. All inputs must be high to get a high output
 A. OR
 B. AND
 C. NAND
 D. NOR
44. In Boolean algebra, the over bar stands for the NOT operation, the plus sign stands for the operation
 A. AND B. NAND
 C. OR D. NOR
45. In Boolean algebra, the dot sign stands for the....operation
 A. AND B. NAND
 C. OR D. NOR

- 46.** The inverter OR gate and AND gate are called decision-making elements because they can recognize some input....while disregarding others. A gate recognizes a word when its output is.....
- Words, high
 - Bytes, high
 - Bytes, low
 - Character low
- 47.** How many inputs signals can a gate have?
- One
 - Two only
 - More than one
 - Both (A) and (B)
- 48.** How many output signals can a gate have?
- One
 - Two only
 - More than one
 - Both (A) and (B)
- 49.** The binary equivalent of the octal number 13.54 is
- 1011.1011
 - 1001.1110
 - 1101.1110
 - All of the above
- 50.** The octal equivalent of 111010 is
- 81
 - 71
 - 72
 - All of the above
- 51.** The octal equivalent of the number 11010.1011 is
- 32.15
 - 32.27
 - 63.51
 - All of the above
- 52.** The decimal equivalent of the binary number 11100001111 is
- 1806
 - 2806
 - 1807
 - All of the above
- 53.** The binary equivalent of the decimal number 135.75 is
- 1101.1
 - 3789.75
 - 1101.0111
 - All of the above
- 54.** The decimal equivalent of binary number 0.0111 is
- 4375
 - B. 0.5375
 - C. 0.4375
 - D. -0.4375
- 55.** The binary code of $(21, 115)_{10}$ is
- 10101.001
 - 10101.010
 - 10100.001
 - 10100.100
- 56.** Which of the following gate is two-level logic gate?
- OR gate
 - EXCLUSIVE OR gate
 - NAND gate
 - NOT gate
- 57.** The binary code of $(73)_{10}$ is
- 1010001
 - 1100101
 - 1000100
 - 1001001
- 58.** An AND gate will function as OR if
- All the inputs to the gates are "1"
 - All the inputs are "0"
 - Either of the inputs is "1"
 - All the inputs and outputs are complemented
- 59.** An OR gate has 6 inputs. How many input words are in its truth table?
- 64
 - 16
 - 32
 - 128
- 60.** An OR gate has 6 inputs. What is the only input word that produces a 0 output?
- 000000
 - 111000
 - 000111
 - 111111
- 61.** An AND gate has 7 inputs. How many input word are in its truth?
- 64
 - 16
 - 32
 - 128
- 62.** An AND gate has 7 inputs, what is the only input word that produces a 1 output?
- 0000000
 - 1110000
 - 0001111
 - 1111111
- 63.** A NOR gate has or more input signals. All inputs must be to get a high output
- Low
 - Some low some high
 - High
 - I's
- 64.** A NOR gate recognizes only the input word whose bits are....
- 0's and I's
 - 0's
 - I's
 - 0's or I's
- 65.** The NOR gate is logically equivalent to an OR gate followed by an ...
- AND
 - XOR
 - XAND
 - Inverter
- 66.** De Morgan's first theorem says that a NOR gate is equivalent to a bubbledgate
- AND
 - XOR
 - XAND
 - NOR
- 67.** A NAND gate is equivalent to an AND gate followed by an inverter. All inputs must be....to get a low output
- Low
 - Some low and some high
 - High
 - 0;s
- 68.** De Morgan's second theorem says that NAND gate is equivalent to a bubbledgate
- AND
 - XOR
 - XAND
 - OR
- 69.** An XOR gate recognizes only words with annumber of 1's
- Even
 - Different
 - Odd
 - All of the above
- 70.** The 2-input XOR gate has a high output only when the input bits are....
- Even
 - Low
 - Different
 - High
- 71.** The XOR gates are ideal for testing parity because even-parity words produce a Output and odd-parity words produce aoutput
- Low, high
 - Odd, even
 - High, low
 - Even, odd
- 72.** An odd-parity generator produces an odd-parity bit to go along with the data. The parity of the transmitted data is An XOR gate can test each received word for parity rejecting words with Parity
- Odd, even
 - Low, high
 - High, low
 - Even, odd
- 73.** The EXCLUSIVE-NOR gate is equivalent to angate followed by an inverter
- OR
 - NAND
 - AND
 - XOR
- 74.** Small-scale integration, abbreviated refers to fewer than 12 gates on the same chip. Medium-scale integration (MSD) means 12 to 100 gates per chip. And large-scale integration (LST) refers to more thangates per chip
- SSI, 75
 - SSI, 1000
 - SSI, 100
 - SSI, 10000

75. The two basic technologies for digital ICs are bipolar and MOS. Bipolar technology is preferred for and, whereas MOS technology is better suited to LSI
- SSI, MSI
 - SSI, LSI
 - MSI, LSI
 - ECL, DTL
76. What is 1's complement of 0000 1111 0010 1101 number?
- 1111 0000 0010 1101
 - 1111 0000 1101 0010
 - 1111 0000 0010 1101
 - 1111 1100 1010 1100
77.has become the most widely used bipolar family
- DTL
 - ECL
 - TTL
 - MOS
78.is the fastest logic family' it's used in high-speed applications
- DTL
 - ECL
 - TTL
 - MOS
79.dominates the LSI field andused extensively where lowest power consumption is necessary
- NMOS, PMOS
 - NMOS, CMOS
 - PMOS, CMOS
 - MOSFET, PMOS
80. The 7400 series, also called standard TTL, contains a variety of SSI and ... chips that allow us to build all kinds of digital circuits and systems
- LSI
 - MOS
 - MSI
 - MOSFET
81. Standard TTL has a multiple emitter input transistor and a output
- Totem-pole
 - Register
 - Bipolar
 - Transistor
82. The 7400-series devices are guaranteed to work reliably over a temperature range of 0 to and over a voltage range of 4.75 to 5.25V
- 80°C
 - 100°C
 - 70°C
 - 90°C
83. A ... TTL device can sink up to 16 mA and can source up to 400mA
- Low-power
 - Standard
 - High-power
 - Schottky
84. The maximum number of TTL loads that a TTL device can drive reliably over the specified temperature range is
- Fanout
 - Chip
 - Bipolar
 - Universal logic circuit
85. Digital design often starts by constructing a table?
- Standard
 - Truth
 - Two-Stage
 - Two-dimensional
86. A preliminary guide for comparing the simplicity of logic circuits is count the number of input.....leads
- Wires
 - Transistors
 - Gates
 - Registers
87. A bus is a group ofcarrying digital signals
- Wires
 - Transistors
 - Gates
 - Registers
88. One way to simplify the sum-products equation is to use Boolean algebra. Another way is themap
- De Morgan
 - Schottky
 - Standard
 - Karnaugh
89. What are the fundamental products for inputs words ABCD = 0010, ABCD = 1101 and ABCD = 1110?
- ABCD, ABCD, ABCD
 - ABCD, ABCD, ABCD
 - ABCD, ABCD, ABCD
 - ABCD, ABCD, ABCD
90. The ALU carries out arithmetic and numbers rather than decimal numbers
- Decimal
 - Binary
 - Hexadecimal
 - All of the above
91. A half-adder adds....bits
- 16
 - 19
 - 8
 - 2
92. A full-adder addsbits and producing a SUM and a....
- 8, SUBTRACTION
 - 3, CARRY
 - 16, DIVIDE
 - All of the above
93. A binary adder is a logic circuit that can add....binary numbers at a time
- Hundreds
 - One
 - Thousands
 - Two
94. The leading bit stands for theand the remaining bits for the, is known as signed binary numbers
- Sign, remainder
 - Value, sign
 - Sign, magnitude
 - Variable, value
95. Signed binary numbers requires too much hardware. This has led to the use of ... complements to represent negative numbers
- 1's
 - 3's
 - 2's
 - No
96. A 2's-complement adder-subtractor can add or subtract binary numbers. Sign-magnitude numbers represent....decimal numbers and 2's complements stands for Decimal numbers
- Hexa, sign
 - Positive, negative
 - Sign, hexa
 - Negative, positive
97. How many full and half-adders are required to add 16-bit numbers?
- 8 half-adders, 8 full-adders
 - 16 half-adders, no full-adders
 - 1half-adders, 15 full-adders
 - Half-adders, 12 full-address
98. Express-7 as 16-bits signed binary numbers
- 0000 0000 0000 0111
 - 0111 0000 0000 0000
 - 1000 0000 0000 0111
 - 0111 0000 0000 0000
99. Convert the 1000 0000 0000 1111 signed binary number to decimal number
- +15
 - 30
 - 15
 - +30
100. What is the 2's complement of 0011 0101 1001 1100 number?
- 1100 1001 1100 1011
 - 1100 1010 0110 0100
 - 1100 1010 0110 0011
 - 1100 1010 1111 1111
101. What is the 2's-complement presentation of -24 in a 16-bit microcomputer?
- 0000 0000 0001 1000
 - 1111 1111 1110 1000
 - 1111 1111 1110 0111
 - 0001 0001 1111 0011

- 102.** A flip-flop is aelement that stores a binary digit as a low or high voltage
 A. Chip B. I/O
 C. Bus D. Memory
- 103.** With an RS latch a high S and low R sets the output to; a low S and a high R....the output to low
 A. No change, set
 B. High, reset
 C. Race, high
 D. Set, Reset
- 104.** With a NAND latch a low R and a low S produce acondition
 A. Race B. Reset
 C. Set D. No change
- 105.** Computers use thousands of flip-flops. To coordinate the overall action, a common signal called theis sent to each flip-flop
 A. Latch B. Master
 C. Clock D. Slave
- 106.** With positive clocking the clock signal must be....for the flip-flop to respond
 A. High B. Set
 C. Low D. Race
- 107.** With a JK master-salve flip-flop the master is clocked when the clock is and the salve is triggered when the clock is.....
 A. Set, reset B. High, low
 C. Race, no change D. Set, race
- 108.** When the LOAD input of a buffer register is active, the input would word is stored on the next positive ...edge
 A. Clock B. Register
 C. Pulse D. Transistor

- 109.** A shift register moves the right. Serial loading means moving word in a shift register by one bit per clock pulse. With parallel broadside loading, it takes only Pulse to load the input word
 A. Eight, eight, clock
 C. Right, eight, clock
 B. Bits, one, register
 D. Bits, one, clock
- 110.** One flip-flop divides the frequency by a factor of in the n flip-flop divide by 2^n
 A. Two, $n+1$ B. $12, \frac{n+1}{2}$
 C. Four, $n+4$ D. $Two, \frac{n}{2}$
- 111.** Instead of counting with numbers, a ring counter uses that have a signal high.....
 A. Bytes B. GATE
 C. Bit D. Chip
- 112.** Theis ultraviolet-light and electrically programmable, allows the user to erase and until programs and data perfected
 A. EPROM B. PROM
 C. ROM D. RAM
- 113.** The memory cell of a dynamic is simple and smaller than memory cell of aRAM
 A. Volatile B. Semiconductor
 C. Static D. Bipolar
- 114.** How many memory locations can address bits access?
 A. 16,384 B. 4096
 C. 8,192 D. 14
- 115.** The 2764 is 65,536-bit EEPROM organized as 8,192 words of 8 bits each. How many address lines does it have?
 A. 12 B. 13
 C. 14 D. 8
- 116.** The 2732 is a 4096x8 EPROM. How many address lines does it have?
 A. 12 B. 13
 C. 14 D. 8
- 117.** Address 200H contains the byte 3FH. What is the decimal equivalent of 3FH
 A. 63 B. 16
 C. 32 D. 38
- 118.** What is the highest address in a 48k memory? Express in hexadecimal and decimal form
 A. 7FFFH, 64387 C. BFFFH, 49,151
 B. BFFFH, 49,152 D. 7FFFH, 64,386
- 119.** Flip-flop output are always
 A. Complimentary
 C. The same
 B. Independent of each other
 D. Same as inputs
- 120.** A combinational logic circuit which is used to send data coming from a single source to two or more separate destinations is called as
 A. Decoder B. Multiplexer
 C. Encoder D. Demultiplexer
- 121.** In which of the following adder circuits, the carry look ripple delay is eliminated?
 A. Half adder B. Full adder
 B. Parallel adder D. Carry-look-ahead adder

- 122.** Consider as RS flip-flop with both inputs set to 0. If a momentary '1' is applied at the input S, then the output
 A. Q will flip from 0 to 1
 C. Q will flip from 0 to 1
 B. Q will flip from 0 to 1 and then back to 0
 D. Q will flip from 0 to 1 and then back to 0
- 123.** How many full addresses are required to construct an m-bit parallel adder?
 A. $m/2$ B. m
 C. $m-1$ D. $m+1$
- 124.** The dynamic race hazard problem occurs in
 A. Combinational circuits only
 C. Both combinational and sequential circuits
 B. Sequential circuits only
 D. None of the above
- 125.** A shift register can be used for
 A. Parallel to serial conversion
 C. Serial to parallel conversion
 B. Digital delay line
 D. All of the above
- 126.** Which of the following flip-flops is free from race around problem?
 A. T flip-flop
 C. SR flip-flops
 B. Master slave JK flip-flop
 D. All of the above
- 127.** For an input pulse train of clock period T, the delay produced by an n stage shift register is
 A. $(n + 1)T$ B. $(n + 1)T$
 C. Nt D. $2nT$

- 128.** The master slave JK flip-flop is effectively a combination of
 A. An SR flip-flop and a T flip-flop
 C. A T flip-flop and a D flip-flop
 B. An SR flip-flop and a D flip-flop
 D. Two T flip-flops
- 129.** The functional difference between SR flip-flop and JK flip flop is faster than SR flip-flop
 A. JK flip-flop is faster than SR flip-flop
 C. JK flip-flop accepts both input 1
 B. JK flip-flop has a feedback path
 D. JK flip-flop does not require external clock
- 130.** The term sum-of-products in Boolean algebra means
 A. The AND function of several OR functions
 C. The OR function of several OR functions
 B. The OR function of several AND functions
 D. The AND function of several AND functions
- 131.** A positive AND gate is also a negative
 A. NAND gate B. AND gate
 C. NOR gate D. OR gate
- 132.** What table shows the electrical state of a digital circuit's output for every possible combination of electrical states in the inputs?
 A. Function table B. Routing table
 C. Truth table D. ASCII table
- 133.** How many bits are required to encode all twenty six letters, ten symbols, and ten numbers?
 A. 5 B. 2
 C. 6 D. 3

- 134.** The number of two-input NAND gates required to produce the two input OR function is
 A. 1 B. 3
 C. 2 D. 4
- 135.** What logic function is obtained by adding an inverter to the inputs of an AND gate?
 A. OR B. XOR
 C. NAND D. NOR
- 136.** Which of the following Boolean algebra expression is incorrect?
 A. $AB + A(B + C) + B(B + C) = B$
 B. $\overline{AB(C+BD)} + \overline{AB} C = B\overline{C}$
 C. $AB(\overline{C} + \overline{D}) = \overline{A} + B + \overline{CD}$
 D. $(A + C)(ABC + ACD) = ABC + ACD$
- 137.** Which gates is known as universal gate?
 A. NOT gate B. NAND gate
 C. AND gate D. XOR gate
- 138.** What logic function is produced by adding an inverter to the output of an AND gate?
 A. NAND B. XOR
 C. NOR D. OR
- 139.** An OR gate can be imagined as
 A. Switches connected in parallel
 B. MOS transistors connected in series
 C. Switches connected in parallel
 D. All of the above
- 140.** What logic function is produced by adding an inverter to each input and the output of an AND gate?
 A. NAND B. OR
 C. NOR D. XOR

- 141.** Which of the following algebra statements represent commutative law
 A. $(A + B) + CA + (B + C)$
 B. $A + B = B + A$
 C. $A \cdot (B + C) (A \cdot B) + (A \cdot C)$
 D. $A + AA$
- 142.** For what logic gate the output is complement of the input?
 A. NOT B. OR
 C. AND D. XOR
- 143.** ASCII and EBCDIC differ in
 A. Their efficiency in storing data
 B. The random and sequential access method
 C. The number of bytes used to store characters
 D. Their collecting sequences
- 144.** In which code the successive code characters differ in only one bit position?
 A. Gray code B. 8421 code
 C. Excess 3 code D. Algebraic code
- 145.** Cyclic codes are used in
 A. Data transfer
 B. Continuously varying signal
 C. Arithmetic and logical computation
 D. All of the above
- 146.** The 2's compliment of binary number 010111.1100 is
 A. 101001.1100 B. 010111.0011
 C. 101000.0100 D. 101000.0011
- 147.** The ASCII CODE
 A. Is a subset of 8-bit EBCDIC
 B. Is used only in Western Countries
 C. Is version II of the ASC Standard
 D. Has 128 characters, including 32 control characters

- 148.** The Gray code for decimal 7 is
 A. 0111 B. 0100
 C. 1011 D. 1010
- 149.** The octal equivalent of decimal 324.987 is
 A. 504.771 B. 815.234
 C. 640.781 D. 90.987
- 150.** Where an old number is converted into the binary number, the least significant digit (LSD) is
 A. 0
 B. 0 or 1
 C. 1
 D. All of the above
- 151.** Which of the following logic families use bipolar transistors?
 A. TTL B. NMOS
 C. GaAs D. CMOS
- 152.** Which of the following TTL subfamily is the fastest
 A. Standard TTL
 B. Schottky TTL
 C. High-speed TTL
 D. Low-speed TTL
- 153.** The output 0 and 1 levels for TTL logic family is approximately
 A. 0.1 and 5v
 B. 0.9 and 1.75
 C. 0.6 and 3.5 v
 D. -1.75 and -0.9v
- 154.** The functional capacity of SSI devices is
 A. 1 to 11 gates
 B. 100 to 10,000 gates
 C. 12 to 99 gates
 D. More than 10,000 gates

155. The functional capacity for LSI devices is

- A. 1 to 11 gates
- B. 100 to 10,000 gates
- C. 12 to 99 gates
- D. More than 10000 gates

156. The time required for a pulse to decrease from 90 to 10 percent of its maximum value is known as

- A. Rise time
- B. Binary level transition period
- C. Decay time
- D. Propagation delay

157. Which logic family dissipates the minimum power?

- A. DTL
- B. ECL
- C. TTL
- D. CMOS

158. Which TTL sub-family has maximum speed?

- A. Standard TTL
- B. High speed TTL
- C. Schottky-clamped TTL
- D. Low power TTL

159. Which of the following is the first integrated logic family?

- A. RTL
- B. TTL
- C. DTL
- D. MOS

160. Why are digital circuits easier to design than analog circuits?

- A. They do not control electricity precisely over a wide range
- B. They are made in the form of ICs
- C. All elements of digital circuit are from the same family
- D. They are smaller in size

161. Which of the following electronic component is not found in ordinary ICs?

- A. Diodes
- B. Transistors
- C. Resistors
- D. Inductors

162. The fan-out capability of a digital building block can be defined as

- A. The number of inputs that one output can transmit to
- B. The amount of cooling required for fanning the heat out
- C. The number of inputs that can transmit to one input
- D. The maximum power dissipation (heat generation) that the unit can stand

163. What is the main advantage of using MOSFET rather than bipolar transistor circuitry in ICs

- A. Much greater complexity (more components) than bipolar circuits
- B. Higher operating speed than bipolar circuits
- C. Fewer power supply connections are required with DOS ICs
- D. System designers are more familiar with MOS circuitry

164. FETs are used in linear ICs to

- A. Increase input resistance
- B. Increase device complexity
- C. Provide large resistance
- D. A and B above

165. Resistor Ratio design is used in linear ICs because

- A. Ratio increase input resistance
- B. Ratio increase amplifier gain
- C. Precise resistor values are not possible with IC processes
- D. All of the above

166. p-channel enhancement type MOSFET performs much the same function as a PNP transistor, except that

- A. It operates much faster
- B. It is considerably larger
- C. It is controlled by voltage rather than by current, so that it requires very little current at the control terminal
- D. It is controlled by current than voltage like a bipolar transistor

167. What advantages do ICs have over discrete-device circuits due to their greater complexity (i.e. more circuitry in less area)

- A. Smaller size
- B. Lower cost
- C. Higher reliability
- D. All of the above

168. The radix of the binary number is

- A. 3
- B. 2
- C. 1
- D. 10

169. The number of binary bits required to represent a hexadecimal digit is

- A. 3
- B. 6
- C. 4
- D. 8

170. $\bar{A} + \bar{B} - \bar{C} = D$ represents as:

- A. NAND gate
- B. EX-OR gate
- C. OR gate
- D. AND gate

171. The output of the following gate is 1 only if at least one of its inputs is 0

- A. AND gate
- B. NAND gate
- C. OR gate
- D. NOT gate

172. The 1's compliment of binary number 0.01011 is :

- A. 1.10100
- B. 0.0110
- C. 0.0010
- D. 1.1101

173. The 2's compliment of binary number 0.01010 is

- A. 1.10101
- B. 1.10100
- C. 0.10101
- D. 0.10100

174. A half-adder is also known as:

- A. AND circuit
- B. NOR circuit
- C. NAND circuit
- D. EX-OR circuit

175. The output of the following gate is 0 only if at least one of the inputs is 1:

- A. AND gate
- B. EX-OR gate
- C. OR gate
- D. NOR gate

176. Which of the following Boolean algebra rules is wrong?

- A. $0 + A = A$
- B. $A + A = A$
- C. $1 + A = 1$
- D. $1 \cdot x = 1$

177. The octal system has the radix of

- A. 2
- B. 8
- C. 4
- D. 10

178. The binary system has the radix of

- A. 0
- B. 2
- C. 1
- D. $\frac{1}{2}$

179. Octal number system uses fundamental digits 0 to 7. 124 (octal) in decimal equivalent is equal to

- A. 180
- B. 84
- C. 82
- D. 86

180. 92 (decimal) is octal number system is equivalent to

- A. 128₈
- B. 132₈
- C. 130₈
- D. 134₈

181. Four digit binary quantity 1001 is represented in the decimal system by?

- A. 7
- B. 1
- C. 9
- D. 13

182. Binary number 101101 is equivalent in decimal form to?

- A. 41
- B. 45
- C. 43
- D. 47

183. Number 37310 is equivalent in binary system to

- A. 101110101
- B. 101010101
- C. 100110101
- D. 101110011

184. According to Boolean algebra $A + A = A$

- A. A
- B. A/n
- C. NA
- D. 1

185. In Boolean algebra $A \cdot A = A$

- A. 5A
- B. A5
- C. A/5
- D. A

186. In Boolean algebra $A \cdot 0 = 0$

- A. 1
- B. A
- C. 0
- D. $1 + A$

187. The simplification of $AB + B\bar{C} + BC$ gives

- A. $AB \pm BC$
- B. $BC + BC$
- C. $AB + BC$
- D. B

188. Which of the following is not functionally a complete set?

- A. AND, OR
- B. NOR
- C. NAND
- D. AND, OR, NOT

189. Which of the following is not true?

- A. $0 \times 0 = 0$
- B. $1 \times 0 = 0$
- C. $0 \times 1 = 1$
- D. $1 \times 1 = 1$

190. The reduced form of the Boolean expression $(A + B)(A + C)$ is:

- A. $AB + AC$
- B. $AC + B$
- C. $A + B + C$
- D. $A + BC$

191. Which of the following is a universal gate?

- A. AND
- B. EX-OR
- C. OR
- D. NAND

192. Which function is equivalent to OR functions negative logic?

- A. NOT
- B. OR
- C. AND
- D. NOR

193. Which of the following expression is wrong?

- A. $1 + 0 = 1$
- B. $1 + 0 + 1 = 1$
- C. $1 + 1 = 0$
- D. $1 + 1 + 1 = 1$

194. The m-bit parallel adder consists of

- A. $(m + 1)$ full adders
- B. $m - 1$ full adder
- C. $m/2$ full adders
- D. m full adders

195. A flip flop can store

- A. 1 bits of data
- B. 3 bits of data
- C. 2 bits of data
- D. 4 bits of data

196. A shift register can be used for:

- A. Parallel to serial conversion
- B. Digital delay line
- C. Serial to parallel conversion
- D. All of the above

197. Semiconductor memory is:

- A. Somewhat larger than magnetic memory
- B. A volatile memory
- C. Somewhat larger than the magnetic core memory
- D. All of the above

198. The logic 1 in positive logic system is represented by:

- A. Zero voltage
- B. Higher voltage level
- C. Lower voltage level
- D. Negative voltage

199. A combinational logic circuit used when it is desired to send data from two or more source through a single transmission line is known as

- A. Encoder
- B. Multiplexer
- C. Decoder
- D. De-multiplexer

200. A logic circuit which is used to change a BCD number into an equivalent decimal number is

- A. Decoder
- B. Multiplexer
- C. Encoder
- D. Code converter

201. A combinational logic circuit which generates particular binary word or number is

- A. Decoder
- B. Encoder
- C. Multiplexer
- D. De-multiplexer

202. Parallel adders are

- A. Combinational logic circuits
- B. Both of the above
- C. Sequential logic circuits
- D. All of the above

203. A de-multiplexer is also known as

- A. Data selector
- B. Multiplexer
- C. Data distributor
- D. Encoder

204. A multiplexer is known as

- A. Coder
- B. Data selector
- C. Decoder
- D. Encoder

205. A flip-flop can store

- A. One bit of data
- B. Three bits of data
- C. Two bits of data
- D. Any number of bits of data

206. Which of the following input combination is not allowed in an SR flip-flop?

- A. S = 0, R = 0
- B. S = 1, R = 0
- C. S = 0, R = 1
- D. S = 1, R = 1

A. JK flip-flop
B. T flip-flop
C. D flip-flop
D. Master slave k flip-flop

207. The clock signals are used in sequential logic circuits

A. To tell the time of the day
B. To tell how much time has elapsed since the system was turned on
C. To carry serial data signals
D. To synchronize events in various parts of a system

208. What logic function is obtained by adding an inverter to the output of an AND gate?

- A. OR
- B. XOR
- C. NAND
- D. NOR

209. The simplified form of the Boolean expression $(X + Y + XY)(X + Z)$ is

- A. $X + Y + Z$
- B. $X + YZ$
- C. $XY + YZ$
- D. $XZ + Y$

210. The maximum count which a 6-bit binary word can represent is

- A. 36
- B. 63
- C. 64
- D. 65

211. The highest decimal number that can be represented with 10 binary digits is

- A. 1023
- B. 512
- C. 1024
- D. All of the above

212. What is the hexadecimal equivalent of a binary number 10101111

- A. AF
- B. 8C
- C. 9F
- D. All of the above

214. Which of the following logic families has the highest noise immunity?
 A. RTL B. TTL
 C. DTL D. HTL
215. Pick up wrong logical expression
 A. $1 + 0 = 0 + 1 = 1$ B. $X + Y = X \cdot Y$
 C. $0 + 0 = 1 \cdot 1 = 0$ D. $X + 0 = X$
216. In a four input NAND gate all but one inputs are 1, the output is
 A. 4 B. 1
 C. $\frac{1}{4}$ D. 0
217. In a four input AND gate all but one inputs are 1, the output is
 A. 0 B. 1
 C. $\frac{1}{4}$ D. 4
218. According to Indempotent law, $X + X$
 A. 1 B. X
 C. 0 D. $X \cdot X$
219. According to Indempotent law, $X \cdot X =$
 A. 1 B. X
 C. 0 D. $X + X$
220. The output will be one in case any input is one in the case of
 A. OR gate B. NAND gate
 C. AND gate D. NOT gate
221. Which of the following circuit is known as half adder?
 A. EXCLUSIVE AND circuit
 C. Flip-flop circuit
 B. INCLUSIVE OR circuit
 D. EXCLUSIVE OR circuit
222. Which of the following function is referred as the complementary?
 A. OR function
 B. NAND function
 C. NOT function
 D. AND function

223. Which of the following illustrates of the distribution law?
 A. $(A+) + C = A + (B + C) = A + B + C$
 B. $(AB)C = A(BC) = ABC$
 C. $A + B = B + A$
 D. $A(B + C) = (AB) + (AC)$
224. Which of the following is termed as minimum error code?
 A. Binary code B. Excess 3-code
 C. Gray code D. Octal code
225. For which of the following flip-flop combinations of two inputs?
 A. D-type flip-flop B. JK flip-flop
 C. R-S flip-flop D. T flip-flop
226. A 4-bit shift register can be made by using
 A. 3 JK flip-flop B. 5 JK flip-flop
 C. 4 JK flip-flop D. 8 JK flip-flop
227. Which of the following statements is false
 A. $AB = A + B$ B. $AB = AB$
 C. $A + B = AB$ D. $A + A = A$
228. The minimum form of the expression $(A + B)(A + B + C)$ will be
 A. $A + CB$ B. $AC + B$
 C. $A + BC$ D. $A + BC$
229. One's complement of 1011.01 is
 A. 0100.10 B. 1011.10
 C. 0100.11 D. 0100.01
230. The NAND gate output will be low if the two inputs are
 A. 00 B. 10
 C. 01 D. 11
231. What is the binary equivalent of the decimal number 368
 A. 101110000 B. 111010000
 C. 110110000 D. 111100000

241. The minimum power required for a logic gate is
 A. TTL B. DTL
 C. RTL D. CMOS
242. The output of a logic gate is 1 when all its inputs are at logic 0. The gate is either
 A. A NAND or an EX - OR
 B. An AND or an EX - OR
 C. An OR or an EX - NOR
 D. A NOR or an EX - NOR
243. Data can be changed from special code to temporal code by using
 A. Shift registers
 B. Combinational circuit
 C. Counters
 D. A/D converters
244. A ring counter consisting of five Flip-flops will have
 A. 5 states B. 32 states
 C. 10 states D. Infinite states
245. The speed of conversion is maximum in
 A. Successive - approximation A/D converter
 B. Parallel - comparative A/D converter
 C. Counter ramp A/D converter
 D. Dual-slope A/D converter
246. The 2's complement of the number 1101101 is
 A. 0101110 B. 0110010
 C. 0111110 D. 0010011
247. The correction to be applied in decimal adder to the generated sum is
 A. 00101 B. 01101
 C. 00110 D. 01010

248. When simplified with Boolean Algebra $(x+y)(x+z)$ simplifies to
 A. X B. $x(1+yz)$
 C. $x+x(y+z)$ D. $x+yz$
249. The gates required to build a half adder are
 A. EX-OR gate and NOR gate
 B. EX-OR gate and AND gate
 C. EX-OR gate OR gate
 D. Four NAND gates
250. The code where all successive numbers differ from their preceding number by single bit is
 A. Binary code B. Excess - 3
 C. BCD D. Gray
251. Which of the following is the faster logic
 A. TTL B. CMOS
 C. ECL D. LSI
252. If the input to T - flip flop is 100 Hz signal, the final output of the three T - flip-flop in cascade is
 A. 1000Hz B. 333Hz
 C. 500Hz D. 12.5 Hz
253. Which of the memory is volatile memory
 A. ROM B. PROM
 C. RAM D. EEPROM
254. -8 is equal to signed binary number
 A. 10001000 B. 10000000
 C. 00001000 D. 10000000
255. De-Morgan's first theorem shows the equivalence of
 A. OR gate and Exclusive OR gate
 B. NOR gate and Bubbled AND gate
 C. NOR gate and NAND gate
 D. NAND gate and NOT gate
256. The digital logic family with lowest propagation delay which has
 A. ECL B. CMOS
 C. TTL D. PMOS
257. The device which changes serial data to parallel data is
 A. COUNTER B. DEMULTIPLEXER
 C. MULTIPLEXER D. FLIP-FLOP
258. A device which converts BCD Seven Segment is called
 A. Encoder B. Multiplex
 C. Decoder D. De-multiplex
259. In a JK Flip-Flop, toggle means
 A. Set Q = 1 and $\bar{Q} = 0$
 B. Set Q = 0 and $\bar{Q} = 1$
 C. Change the output to the opposite state
 D. No change in output
260. The access time of ROM with bipolar transistors is about
 A. 1 sec B. 1 μ sec
 C. 1 msec D. nsec
261. The A/D converter whose conversion time is independent of the number of bits is
 A. Dual slope
 B. Parallel conversion
 C. Counter type
 D. Successive approximation
262. When signed numbers are used in binary arithmetic, then which of the following notations would be unique representation for zero
 A. Sign-magnitude B. 2's complement
 C. 1's complement D. 9's complement
- LSV output. This
 A. Improve the speed of the system
 B. Reduce the maximum quantization error
 C. Increase the number of bits at the output
 D. Increases the range of input voltage that can be converted to digital equivalent of Binary
270. The decimal equivalent of Binary number 11010 is
 A. 26 B. 16
 C. 36 D. 23
271. 1's complement representation of decimal number of -17 by using 8 bit representation is
 A. 1110 1110
 B. 1100 1100
 C. 1101 1101
 D. 0001 0001
272. The excess 3 code of decimal number 26 is
 A. 0100 1001 B. 1000 1001
 C. 0101 1001 D. 01001 101
273. How many AND gates are required to realize $Y = CD + EF + G$
 A. 4 B. 3
 C. 5 D. 2
274. How many select lines will a 16 to 1 multiplexer have
 A. 4 B. 5
 C. 3 D. 1
275. How many flip flops are required to construct a decade counter
 A. 10 B. 4
 C. 3 D. 2

276. Which TTL logic gate is used for wired ANDing A. Open collector output B. Tri state output C. Totem Pole D. ECL gates	284. CMOS circuits are extensively used for ON-chip computers because of their extremely low power dissipation A. Low power dissipation B. Large packing density C. High noise immunity D. Low cost	291. The NOR gate output is high if the two inputs are A. 00 B. 10 C. 01 D. 11 291. Which of the following is the fastest logic? A. ECL B. CMOS C. TTL D. LSI	292. How many flip-flop are required to construct mod 30 counter A. 5 B. 4 C. 6 D. 8 293. How many address bits are required to represent a 32 K memory A. 10 bits B. 14 bits C. 12 bits D. 16 bits 294. The number of control lines for 16 to 1 multiplexer is A. 2 B. 3 C. 4 D. 5 295. Which following requires refreshing? A. SRAM B. ROM C. DRAM D. EPROM	296. Shifting a register content to left by one bit position is equivalent to A. Division by two B. Multiplication by two C. Addition by two D. Subtraction by two 297. For JK flip-flop with J=1, K=0, the output after clock pulse will be A. 0 B. High impedance C. 1 D. No change 298. Convert decimal 153 to octal. Equivalent in octal will be A. (231) ₈ B. (431) ₈ C. (331) ₈ D. None of these
277. CMOS circuits consume power A. Equal to TTL B. Twice of TTL C. Less than TTL D. Thrice of TTL	285. The MSI chip 7474 is A. Dual edge triggered JK flip-flop (TTL) B. Dual edge triggered D flip-flop (CMOS) C. Dual edge triggered D flip-flop (TTL) D. Dual edge triggered JK flip-flop (CMOS)	299. The number of address bits required to represent a 32 K memory A. 10 bits B. 14 bits C. 12 bits D. 16 bits 300. The number of control lines for 16 to 1 multiplexer is A. 2 B. 3 C. 4 D. 5 301. The output of SR flip-flop is R = 0 is A. 1 B. No change C. 0 D. High impedance	302. The number of flip-flops contained in IC 7490 is A. 2 B. 4 C. 3 D. 10 303. The number of control lines for 32 to 1 multiplexer is A. 4 B. 16 C. 5 D. 6	304. How many two-input AND & OR gates are required to realize Y = CD + EF + G A. 2,2 B. 33 C. 23 D. None of these
278. In a RAM, information can be stored A. By the user, number of times B. By the user, only once C. By the manufacturer, a number of times D. By the manufacturer only once	286. Which of the following memory stores the most number of bits A. A 5M×8 memory B. A 5M×4 memory C. A 1M×16 memory D. A 1M×12 memory	305. Which of the following cannot be accessed randomly A. DRAM B. ROM C. SRAM D. Magnetic tape	306. The excess-3 code of decimal 7 is represented by A. 1100 B. 1011 C. 1001 D. 1010	307. When an input signal A = 11001 is applied to a NOT gate serially, its output signal is A. 00111 B. 10101 C. 00110 D. 11001
279. The hexadecimal number for (95.5) ₁₀ is A. (5F.8) ₁₆ B. (2E.F) ₁₆ C. (9A.B) ₁₆ D. (5A.4) ₁₆	287. The process of entering data into ROM is called A. Burning in the ROM B. Changing the ROM C. Programming the ROM D. Charging the ROM	308. For JK flip-flop with J=1, K=0, the output after clock pulse will be A. 0 B. High impedance C. 1 D. No change	309. The output of SR flip-flop is R = 0 is A. 1 B. No change C. 0 D. High impedance	310. The output of SR flip-flop is R = 0 is A. 1 B. No change C. 0 D. High impedance
280. The octal equivalent of (247) ₁₀ is A. (252) ₈ B. (367) ₈ C. (350) ₈ D. (400) ₈	288. When the set of input data to parity generator is 0111, the output will be A. 1 B. Unpredictable C. 0 D. Depends on the previous input	311. The number 140 in octal is equivalent to A. (96) ₁₀ B. (90) ₁₀ C. (86) ₁₀ D. None of these	312. The number of flip-flops contained in IC 7490 is A. 2 B. 4 C. 3 D. 10 313. The number of control lines for 32 to 1 multiplexer is A. 4 B. 16 C. 5 D. 6	314. How many two-input AND & OR gates are required to realize Y = CD + EF + G A. 2,2 B. 33 C. 23 D. None of these
281. The chief reason why digital computers use complemented subtraction is that it A. Simplifies the circuitry B. is a very simple process C. Can handle negative numbers easily D. Avoids direct subtraction	289. The number 140 in octal is equivalent to A. (96) ₁₀ B. (90) ₁₀ C. (86) ₁₀ D. None of these	315. The output of SR flip-flop is R = 0 is A. 1 B. No change C. 0 D. High impedance	316. The output of SR flip-flop is R = 0 is A. 1 B. No change C. 0 D. High impedance	317. The output of SR flip-flop is R = 0 is A. 1 B. No change C. 0 D. High impedance

308. The result of adding hexadecimal number A6 to 3A is A. DD B. F0 C. E0 D. EF	314. The output of a JK flip-flop with asynchronous preset and clear inputs is '1'. The output can be changed to '0' with one of the following conditions A. By applying J = 0, K = 0 and using a clock B. By applying J = 1, K = 0, and using the clock C. By applying J = 1, K = 1 and using the clock D. By applying a synchronous preset input	319. The decimal equivalent of the number 10101 is A. 21 B. 26 C. 31 D. 28	320. How many two input AND gates and two input OR gates are required to realize $Y = BD + CE + AB$ A. 1, 1 B. 3, 2 C. 4, 2 D. 2, 3	321. How many select lines will a 32:1 multiplexer will have A. 5 B. 9 C. 8 D. 11
309. A universal logic gate is one, which can be used to generate any logic function. Which of the following is a universal logic gate? A. OR B. XOR C. AND D. NAND	315. The information in ROM is stored A. By the user any number of times B. By the manufacturer during fabrication of the device C. By the user using ultraviolet light D. By the user once and only once	322. How many address bits are required to represent 4K memory A. 5 bits B. 8 bits C. 12 bits D. 10 bits	323. For JK flip-flop J = 0, K = 1, the output after clock pulse will be A. 1 B. 0 C. No change D. High impedance	324. According to commutative law of addition A. AB = BA B. A + (B+C) = (A+B) + C C. A = A+A D. A+B = B+A
310. The logic 0 level of a CMOS logic device is approximately A. 1.2 volts B. 5 volts C. 0.4 volts D. 0 volts	316. The conversation speed of an analog to digital converter is maximum with the following technique A. Dual slope AD converter B. Serial comparator AD converter C. Successive approximation AD converter D. Parallel comparator AD converter	325. Which of following are known as universal gates A. NAND and NOR B. XOR and OR C. AND and OR D. None	326. According to the associative law of multiplication A. B = BB B. A+B = B+A C. A(BC) = (AB)C D. B + B(B+0)	327. According to the distributive law: A. A(B+C) = AB+AC B. A(A+1) = A C. A(BC) = (AB) = ABC D. A + AB = A
311. Karnaugh map is used for the purpose of A. Reducing the electronic circuits used B. To map the given Boolean logic function C. To minimize the terms in a Boolean expression D. To maximize the terms of a given a Boolean expression	317. A weighted resistor digital to analog converter using N bits required a total of A. N precision resistors B. N+1 precision resistors C. 2N precision resistors D. N-1 precision resistors	328. The Boolean expression A. A sum term B. A product term C. A literal term D. A complement term	329. The Boolean expression A. A sum term B. A literal C. A product term D. Always 1	330. The domain of the expression AB'CD + AB' + C'D + B is... A. A and D B. A, B, C and D C. B only D. None of the above
312. A full adder logic circuit will have A. Two inputs and one output B. Three inputs and three outputs C. Two inputs and two outputs D. Three inputs and two outputs	318. The 2's complement of the number 1101110 is A. 0010001 B. 0010010 C. 0010001 D. None	331. According to the associative law of addition A. AB = BA B. A + (B+C) = (A+B) + C C. A = A+A D. A+B = B+A	332. According to the associative law of multiplication A. B = BB B. A+B = B+A C. A(BC) = (AB)C D. B + B(B+0)	333. According to the distributive law: A. A(B+C) = AB+AC B. A(A+1) = A C. A(BC) = (AB) = ABC D. A + AB = A
313. An eight stage ripple counter uses a flip-flop with propagation delay of 75 nanoseconds. The pulse width of the strobe is 50ns. Frequency of the input signal which can be used for proper operation of the counter is approximately A. 1 MHz B. 2 MHz C. 500MHz D. 4 MHz	334. Which one of the following is not a valid rule of Boolean algebra? A. A + 1 = 1 B. AA = A C. A = \bar{A} D. A + 0 = A	335. Which of the following consumes minimum power A. TTL B. DTL C. CMOS D. RTL	336. Safal's Computer/Software/Information Technology Engineering Licensure Examinations 147	

335. Which of the following rules states that if one input of an AND gate is always 1, the output is equal to the other input?

- A. $A + 1 = 1$
- B. $A \cdot A = A$
- C. $A + A = A$
- D. $A \cdot 1 = A$

336. According to De-Morgan's theorem, the following equality(s) are correct:

- A. $AB = A + B$
- B. $A + B + C = ABC$
- C. $X\bar{Y}Z = \bar{X} + \bar{Y} + Z$
- D. All of the other

337. The Boolean expression $X = AB + CD$ represents

- A. Two ORs ANDed together
- B. Two ANDs ORed together
- C. A 4-input AND gate
- D. An exclusive-OR

338. An example of a sum-of-products expression is

- A. $A + B(C + D)$
- B. $\bar{A}B + A\bar{C} + A\bar{B}\bar{C}$
- C. $\bar{A} + \bar{B} + C(\bar{A} + \bar{B} + C)$
- D. Both answers OR

339. An example of a sum-of-sums expression is

- A. $A(B + C) + AC$
- B. $\bar{A} + \bar{B} + BC$
- C. $(A + B)(\bar{A} + B + \bar{C})$
- D. Both answers A and B

340. An example of a standard SOP expression is

- A. $\bar{A}B + A\bar{B}C + ABD$
- B. $AB + \bar{A}B + AB$
- C. $A\bar{B}C + A\bar{C}D$
- D. $ABC\bar{D} + \bar{A}B + \bar{A}$

341. A 3-variable Karnaugh map has

- A. Eight cells
- B. Six cells
- C. Three cells
- D. Five cells

342. In a 4-variable Karnaugh map, a variable product term is produced

- A. A 2-cell group of 1_4
- B. A 4-cell group of 1_4
- C. An 8-cell group of 1_4
- D. A 4-cell group of 0_4

343. On a karnaugh map, a group of 0s produces

- A. A product-of-sums expression
- B. A "don't care" condition
- C. A sum-of-products expression
- D. AND-OR logic

344. A 5-variable Karnaugh map has

- A. Sixteen cells
- B. Sixty-four cells
- C. Thirty-two cells
- D. All of the above

345. The output expression for an AND-OR circuit having one AND gate with inputs A, B, C and D and one OR gate with inputs E and F is

- A. ABCDEF
- B. $(A + B + C + D)(E + F)$
- C. $A + B + C + D + E + F$
- D. $BCD + EF$

346. A logic circuit with an output $Z = ABC + AC$ consists of

- A. Two AND gates and one OR gate
- B. Two AND gates, one OR gate and two inverters
- C. Two OR gates, one AND gate and two inverters
- D. Two AND gates, one OR gate and one inverter

347. To implement the OR function $Z = \bar{A}CD + \bar{A}BC + \bar{B}CD + \bar{B}AC + \bar{C}AD + \bar{C}BD + \bar{D}AC + \bar{D}BC$, it takes

- A. Two AND gates and four inverters
- B. Two AND gates and three inverters
- C. Three AND gates and three inverters
- D. The expression $\bar{A}BCD + ABC\bar{D} + \bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{C}BD + \bar{A}\bar{C}B\bar{D} + \bar{B}\bar{C}AD + \bar{B}\bar{C}A\bar{D}$

348. The expression $\bar{A}BCD + ABC\bar{D} + \bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{C}BD + \bar{A}\bar{C}B\bar{D} + \bar{B}\bar{C}AD + \bar{B}\bar{C}A\bar{D}$

- A. Cannot be simplified
- B. Can be simplified to $\bar{A}BC - \bar{A}\bar{B}\bar{C}$
- C. Can be simplified to $\bar{A}BC - \bar{A}\bar{B}$
- D. None of these answers is correct

349. The input expression for an AND-OR-invert circuit having one AND gate with inputs A, B, C and D and one AND gate with inputs E and F is

- A. $ABC - EF$
- B. $\bar{A} - \bar{B} - \bar{C} - \bar{D} - \bar{E} - \bar{F}$
- C. $\bar{A} - B - C + D)(E + F)$
- D. $\bar{A} - B - \bar{C} + \bar{D})(\bar{E} + \bar{F})$

350. The exclusive-OR function is expressed as

- A. $\bar{A}B + AB$
- B. $\bar{A} + B(A + \bar{B})$
- C. $AB + \bar{A}\bar{B}$
- D. $\bar{A} + \bar{B} + (A + B)$

351. The AND operation can be produced with

- A. Two AND gates
- B. One NOR gate
- C. Three NAND gates
- D. Three NOR gates

352. The OR operation can be produced with

- A. Two NOR gates
- B. Four NAND gates
- C. Three NAND gates
- D. Both answers A and B

353. The OR operation can be implemented with the following logic functions

- A. All Boolean expressions
- B. All AND gates only
- C. Combinations of AND and OR gates
- D. Any of these

354. All Boolean expressions

- A. All AND gates only
- B. All NOR gates only
- C. Combinations of AND and OR gates
- D. Any of these

355. The device used to convert a binary number to a 7-segment display format is

- A. Multiplexer
- B. Decoder
- C. Encoder
- D. Register

356. An example of data storage device is

- A. Two inputs and two outputs
- B. Two inputs and three outputs
- C. Three inputs and two outputs
- D. Two inputs and one output

357. Full-adder is characterized by

- A. Two inputs and two outputs
- B. Two inputs and three outputs
- C. Three inputs and two outputs
- D. Two inputs and one output

358. The inputs to a full-adder are $A = 1$,

$B = 1$, $C_{in} = 0$. The outputs are

- A. $Z = 1$, $C_{out} = 1$
- B. $Z = 0$, $C_{out} = 1$
- C. $Z = 1$, $C_{out} = 0$
- D. $Z = 0$, $C_{out} = 0$

359. A 4-bit parallel adder can add

- A. Two 4-bit binary numbers
- B. Four bits at a time
- C. Two 2-bit binary number
- D. Four bits in sequence

360. The 74LS83A is an example of a 4-bits parallel adder. To expand this device to an 8-bit adder, you must
 A. Use four adders with no interconnections
 B. Use two adders and connect the sum outputs of one to the bit inputs of the other
 C. Use eight adders with no interconnections
 D. Use two adders with the carry output of one connected to the carry input of the other
361. If a 74HC85 magnitude comparator has $A = 1011$ and $B = 1001$ on its inputs, the outputs are
 A. $A > B = 0, A < B = 1, A = B = 0$
 B. $A > B = 1, A < B = A, A = B = 0$
 C. $A > B = 1, A < B = 0, A = B = 0$
 D. $A > B = 0, A < B = 0, A = B = A$
362. If a 1-of-16 decoder with active-LOW outputs exhibits a LOW on the decimal 12 output, what are the inputs?
 A. $A_3A_2A_1A_0 = 1010$
 B. $A_3A_2A_1A_0 = 1100$
 C. $A_3A_2A_1A_0 = 1110$
 D. $A_3A_2A_1A_0 = 0100$
363. A BCD-to-7 segment decoder has 0100 on its inputs. The active outputs are
 A. a, c, f, g B. b, c, e, f
 C. b, c, f, g D. b, d, e, g
364. If an octal-to-binary priority encoder has its 0, 2, 5, and 6 inputs at the active level, the active-HIGH binary output is
 A. 110 B. 10
 C. 010 D. 000

365. In general, a multiplexer has
 A. One data input, several data and selection inputs
 B. One data input, one data output and one selection input
 C. Several data inputs, several data outputs, and selection inputs
 D. Several data inputs, one data output and selection inputs
366. Data selectors are basically the same as
 A. Decoders B. Multiplexers
 C. De-multiplexers D. Encoders
367. Which of the following codes exhibit even parity?
 A. 10011000
 B. 11111111
 C. 01111000
 D. Both answer (A) and (B)
368. If an S-R latch has a 1 on the Set input and a 0 on the R input and then the input goes to 0, the latch will be
 A. Set B. Invalid
 C. Reset D. Clear
369. The invalid state of an S-R latch occurs when
 A. $S = 1, R = 0$ B. $S = 1, R = 1$
 C. $S = 0, R = 1$ D. $S = 0, R = 0$
370. For a gated D latch, the Q output always equals the D input
 A. Before the enable pulse
 B. Immediately after the enable pulse
 C. During the enable pulse
 D. Answers (B) and (C)
371. Like the latch, the flip-flop belongs to a category of logic circuits known as
 A. Monostable multivibrators
 B. Astable multivibrators
 C. Bistable multivibrators
 D. One-shot

372. The purpose of the clock edge is to
 A. Set the device
 B. Reset the device
 C. Cause the output to change states
 D. Cause the output to assume a state dependent on the controlling (S-R, J-K or D) inputs
373. For an edge-triggered D flip-flop,
 A. A change in the state of the flip-flop can occur only at a clock pulse edge
 B. The state that the flip-flop goes to depends on the D input
 C. The output follows the input at each clock pulse
 D. All of these answers
374. A feature that distinguishes the J-K flip-flop from the S-R flip-flop is the
 A. Toggle condition
 B. Type of clock
 C. Preset input
 D. Clear input
375. A flip-flop is in the toggle condition when
 A. $J = 1, K = 0$ B. $J = 0, K = 0C$.
 C. $J = 1, K = 1$ D. $J = 0, K = 1$
376. A J-K flip-flop with $J = 1$ and $K = 1$ has a 10 kHz clock input. The Q output is
 A. Constantly HIGH
 B. A 10 kHz square wave
 C. Constantly LOW
 D. A 5 kHz square wave
377. Asynchronous counters are known as
 A. Ripple counters
 B. Decade counters
 C. Multiple clock counters
 D. Modulus counters
378. D. The value of the counter
 A. The modulus of the counter
 B. The number of flip-flops
 C. The actual number of times it recycles in a second
 D. The maximum possible number of states
379. D. The modulus of the counter has a maximum modulus of
 A. 3 B. 8
 C. 6 D. 16
380. A 3-bit binary counter has a maximum modulus of
 A. 16 B. 8
 C. 32 D. 4
381. A 4-bit binary counter has a maximum modulus of
 A. 16 B. 8
 C. 32 D. 4
382. A modulus-12 counter must have
 A. 12 flip-flop
 B. 4 flip-flop
 C. 3 flip-flop
 D. Synchronous clocking
383. Which one of the following is an example of counter with a truncated modulus?
 A. Modulus 8 B. Modulus 16
 C. Modulus 14 D. Modulus 32
384. A 4-bit ripple counter consists of flip-flop that each have propagation delay from clock to Q output of 12 ns. For the counter to recycle from 1111 to 0000, it takes a total of
 A. 12ns B. 48ns
 C. 24ns D. 36ns

385. A BCD counter is an example of
A. A full-modulus counters
B. A truncated-modulus
C. A decade counter
D. Answers (A) and (C)

386. Which of the following is an invalid state in an 8421 BCD counter?
A. 1100 B. 0101
C. 0010 D. 1000

387. Three cascaded modulus-10 counters have an overall modulus of
A. 30 B. 1000
C. 100 D. 10,000

388. A 10 MHz clock frequency is applied to a cascaded counter consisting of a modulus-5 counter, a modulus-8 counter, and two modulus-10 counters. The lowest output frequency possible is
A. 10 kHz B. 5 kHz
C. 2.5 kHz D. 25 kHz

389. A 4-bit binary up/down counter is in the binary state of zero. The next state in the DOWN mode is
A. 0001 B. 1000
C. 1111 D. 1110

390. The terminal count of a modulus-13 binary counter is
A. 0000 B. 1101
C. 1111 D. 1100

391. A stage in a shift register consists of
A. A latch
B. A byte of storage
C. A flip-flop
D. Four bits of storage

392. To serially shift a byte of data into a shift register, there must be
A. One clock pulse
C. One load pulse
B. Eight clock pulses
D. One clock pulse for each 1 in the data

393. To parallel load a byte of data into a shift register with a synchronous load, there must be
A. One clock pulse
C. One clock pulse for each 1 in the data
B. Eight clock pulses
D. One clock pulse for each 0 in the data

394. The group of bits 10110110 is serially shifted (right-most bit first) into an 8-bit parallel output register with an initial state of 11100100. After two clock pulses, the register contains.
A. 01011110
B. 1111001
C. 10110101
D. 00101101

395. With a 1 MHz clock frequency, 8 bits can be serially entered into a shift register in
A. 80 μ s B. 80 ms
C. 8 μ s D. 10 μ s

396. With a 1 MHz clock frequency, 8 bits can be parallel entered into a shift register
A. In 80 μ s
B. In the propagation delay time of eight flip-flops
C. In 1 μ s
D. In the propagation delay time of one flip-flop

397. A modulus-10 Johnson counter requires
A. Ten flip-flop
B. Five flip-flop
C. Four flip-flop

406. A byte-oriented memory has
A. 1 data output
C. 4 data output
D. 16 data output

407. The storage cell in a SRAM is
A. A flip-flop
B. A fuse
C. A capacitor
D. A magnetic domain

408. A DRAM must be
A. Replaced periodically
C. Refreshed periodically
B. Always enabled
D. Programmed before each use

409. A flash memory is
A. Nonvolatile
B. A read/write memory
C. A read-only memory
D. Answers (A) and (B)

410. Hard disk, floppy disk, Zip disk, and Jaz disk are all
A. Magneto-optical storage devices
B. Magnetic storage devices
C. Semiconductor storage devices
D. Optical storage devices

411. Optical storage devices employ
A. Ultraviolet light
B. Optical couplers
C. Electromagnetic field
D. Lasers

412. A fixed-function IC package containing four AND gates in an example of
A. A ROM
B. A RAM
C. A ROM
D. A SRAM

413. An LSI device has a circuit complexity of

- A. 12 to 99 equivalent gates
- B. 2000 to 5000 equivalent gates
- C. 100 to 9999 equivalent gates
- D. 10,000 to 99,000 equivalent gates

414. A positive-going pulse is applied to an inverter. The time interval from the leading edge of the input to the leading edge of the output is 7 ns. This parameter is

- A. Speed-power product
- B. Propagation delay t_{PLH}
- C. Propagation delay, t_{PLH}
- D. Pulse width

415. The CMOS family with the fastest switching speed is

- A. AC
- B. ACT
- C. HC
- D. ALVC

416. If power were the major criterion in the design of a digital system, the logic family that you would probably use is

- A. HCL
- B. LV
- C. ALVC
- D. LVC

417. When the frequency of the input signal to a CMOS gate is increased, the average power dissipation

- A. Decreases
- B. Does not change
- C. Increases
- D. Decreases exponentially

418. CMOS operates more reliably than TTL in a high-noise environment because of its

- A. Lower noise margin
- B. Higher noise margin
- C. Input capacitance
- D. Smaller power dissipation

419. Proper handling of a CMOS device is necessary because of its

- A. Fragile construction
- B. High-noise immunity
- C. Susceptibility to discharge
- D. Low power dissipation

420. Which of the following is not a TTL circuit?

- A. 74F00
- B. 74HC00
- C. 74AS00
- D. 74ALS00

421. An open TTL NOR gate input

- A. Acts as a LOW
- B. Should be grounded
- C. Acts as a HIGH
- D. Answers (B) and (C)

422. An LS TTL gate can drive a maximum of

- A. 20 unit loads
- B. 40 unit loads
- C. 10 unit loads
- D. Unlimited unit loads

423. If two unused inputs of a LS TTL gate are connected to an input being driven by another LS TTL gate, the total number of remaining unit load that can be driven by this gate is

- A. Seven
- B. Seventeen
- C. Eight
- D. Unlimited

424. The main advantage of ECL over TTL or CMOS is

- A. ECL is less expensive
- B. ECL consumes less power
- C. ECL is available in a greater variety of circuit type
- D. ECL is faster

425. ECL cannot be used in

- A. High-noise environments
- B. High-frequency applications
- C. Damp environments
- D. ECL is less expensive

426. The basic mechanism for storing a data bit in an E²CMOS cell is

- A. Control gate
- B. Floating gate
- C. Floating drain
- D. Cell current

427. A CPLD is a

- A. CMOS programmable logic device
- B. Capacitive programmable logic device
- C. Complex programmable logic device
- D. Complementary process latching device

428. VHDL is a

- A. Logic device
- B. Computer language
- C. PLD programming language
- D. Very high density logic

429. The types of SPLDs do not include

- A. GAL
- B. RAM
- C. PROM
- D. PAL

430. A GAL has

- A. A reprogrammable AND array, a fixed OR array, and programmable output logic
- B. A fixed AND array and a programmable OR array
- C. One-time programmable AND and OR array
- D. Reprogrammable AND and OR array

431. An SPLD that has a programmable AND array and a fixed OR array is a

- A. PROM
- B. PAL
- C. PLA
- D. GAL

432. A connection between a row and column in a PAL array is made by

- A. Blowing a fusible link
- B. Leaving a fusible link intact
- C. Connecting an input variable to the input line
- D. Connecting an input variable to the product term line

433. The device number PAL14H4 indicates

- A. A PAL with fourteen active-HIGH outputs and four inputs
- B. A PAL that implements fourteen AND gates and four OR gates
- C. A PAL with implements and four active-HIGH outputs
- D. Who the manufacturer is

434. A GAL is different from a PAL because

- A. A GAL has more inputs and outputs
- B. A GAL is implemented with a different technology
- C. A GAL can replace several different PALs
- D. All except answer (A)

435. The reprogrammable cells in a GAL array are

- A. TTL
- B. ECL
- C. E²CMOS
- D. Bipolar fuses

436. OLMC is an acronym for

- A. Output Logic Main Cell
- B. Output Logic Macrocell
- C. Optimum Logic Multiple Channel
- D. Odd-parity Logic Master Check

437. Two ways in which a GAL output can be configured are

- A. Combinational and I/O
- B. Fixed and variable
- C. Simple and complex
- D. Combinational and registered

438. The device number GAL22V10 means that

- A. The device has 22 dedicated inputs and 10 dedicated outputs
- B. The device has 22 inputs including dedicated inputs and I/Os and 10 outputs either dedicated or I/Os
- C. The device has a variable number of inputs form a maximum of 22 to a minimum of 10
- D. The device has 24 inputs including dedicated inputs and I/Os and 14 outputs either dedicated or I/Os

- 439. To conventionally program an SPLD, you need a**
- Special fixture
 - Special fixture and a master PLD that has been preprogrammed at the factory
 - Computer, a programmer, and HDL software
 - Computer, a programmer, and BASIC software
- 440. ISP stands for**
- In-System Programmable
 - Integrated Silicon Program
 - Integrated System Program
 - In-System Integrated Programming
- 441. The GAL22V10 has**
- 10 inputs and 22 outputs
 - 22 dedicated inputs and 10 outputs
 - 12 dedicated inputs and 10 dedicated outputs
 - 12 dedicated inputs and 10 outputs, any of which can be an input
- 442. The GAL22V10 operates on a dc supply voltage of**
- 5V
 - 3.3V
 - 10V
 - 1.2V
- 443. OLMC stand for**
- Output logic modular circuit
 - Output logic macrocell
 - Output latch memory cell
 - Overall logic matrix circuit
- 444. The three states of a tri-state output buffer are**
- HIGH, LOW, high impedance
 - HIGH, LOW, ground
 - HIGH, LOW, in between
 - Right, left, centre

- 445. The OLMC of the GAL22V10 contains**
- One OR gate, one flip-flop, multiplexers
 - One OR gate, one flip-flop, multiplexer
 - One AND gate, one latch, multiplexers
 - One OR gate, one flip-flop, decoders
- 446. The GAL16V8 has**
- 16 dedicated inputs and 8 outputs
 - 8 dedicated inputs and 8 outputs
 - 8 inputs and 16 outputs
 - 16 input/outputs and 8 outputs
- 447. A typical OLMC consists of**
- Gates, multiplexers, and a flip-flop
 - Gates, and a shift register
 - A Gray code counter
 - A fixed logic array
- 448. A CPLD is a**
- CMOS PLD
 - Complementary PLD
 - Complex PLD
 - A fixed logic array
- 449. A CPLD contains**
- Shift registers
 - Logic arrays
 - Programmable interconnects
 - Answers (B) and (C)
- 450. FPGA stands for**
- Fast propagation gate array
 - Field programmable gate array
 - Field presentable gate array
 - File programmable gate array
- 451. $2 \times 10^1 + 8 \times 10^0$ equal to**
- 10
 - 28
 - 280
 - 28
- 452. The binary number 1101 is equal to the decimal number**
- 13
 - 11
 - 49
 - 3
- 453. The binary number 11011101 is equal to the decimal number**
- 121
 - 441
 - 221
 - 256
- 454. The decimal number 17 is equal to the binary number**
- 10010
 - 10001
 - 11000
 - 01001
- 455. The decimal number 175 is equal to the binary number**
- 11001111
 - 10101111
 - 10101110
 - 11101111
- 456. The sum of $11010 + 01111$ equals**
- 101001
 - 110101
 - 101010
 - 101000
- 457. The difference of $110 - 010$ equals**
- 001
 - 101
 - 010
 - 100
- 458. The 1's complement of 10111001 is**
- 01000111
 - 11000110
 - 01000110
 - 10101010
- 459. The 2's complement of 11001000 is**
- 00110111
 - 01001000
 - 00110001
 - 00111000
- 460. The decimal number -34 is expressed in the 2's complement form as**
- 10101110
 - 11011110
 - 10100010
 - 01011101
- 461. The decimal number +122 is expressed in the 2's complement form as**
- 01111010
 - 01000101
 - 11111010
 - 10000101

470. A 7-bit Hamming code (even parity) 001001 for a BCD digit is known to have single error the encoded BCD digit is

- A. 9
- B. 3
- C. 5
- D. 0

471. When the input to an inverter is HIGH (1), the output is
A. HIGH or 1 B. HIGH or 0
C. LOW or 1 D. LOW or 0

472. An inverter performs an operation known as
A. Complementation
B. Inversion
C. Assertion
D. Both answers (A) and (B)

473. The output of an AND gate with inputs A, B, and C is a 1 (HIGH) when

- A. A = 1, B = 1, C = 1
- C. A = 1, B = 0, C = 1
- B. A = 0, B = 0, C = 0
- D. Only answers (A) and (C)

474. A pulse is applied to each input of a 2-input NAND gate. One pulse goes HIGH at t = 0 and goes back LOW at t = 1ms. The other pulse goes HIGH at t = 0.8 ms and goes back LOW at t = 3ms. The output pulse can be described as follows:

- A. It goes LOW at t = 0 and back HIGH at t = 3ms
- B. It goes LOW at t = 0.8 ms and back HIGH at t = 3 ms
- C. It goes LOW at t = 0.8 ms and back HIGH at t = 1 ms
- D. It goes LOW at t = 0.8 ms and back LOW at t = 1 ms

475. A pulse is applied to each input of a 2-input NOR gate, one pulse goes HIGH at t = 0 and goes back LOW at t = 1ms. The other pulse goes HIGH at t = 0.8 ms and goes back LOW at t = 3 ms. The output pulse can be described as follows:

- A. It goes LOW at t = 0 and back HIGH at t = 3 ms.
- B. It goes LOW at t = 0.8 ms and back HIGH at t = 3ms
- C. It goes LOW at t = 0.8 ms and back HIGH at t = 1 ms
- D. It goes HIGH at t = 0.8 ms and back LOW at t = 1 ms

476. A pulse is applied to each input of a exclusive-OR gate. One pulse goes HIGH at t = 0 and goes back LOW at t = 1 ms. The other pulse goes HIGH at t = 0.8 ms and goes back LOW at t = 3 ms. The output pulse can be described as follows:

- A. It goes HIGH at t = 0 and back LOW at t = 3 ms
- B. It goes HIGH at t = 0 and back LOW at t = 0.8ms
- C. It goes HIGH at t = 1 ms and back LOW at t = 3ms
- D. Both answers (B) and (C)

477. For and AND gate

- A. All LOW input produce a HIGH output
- B. Output is HIGH if and only if inputs are HIGH
- C. Output is LOW if and only if inputs are HIGH
- D. Output is LOW if and only if inputs are LOW

478. The output of a gate is LOW when atleast one of its inputs is HIGH. This is true for

- A. AND
- B. OR
- C. NAND
- D. NOR

479. The output of a gate is LOW when atleast one of its inputs is LOW. It is true for

- A. AND
- B. NAND
- C. OR
- D. NOR

480. The output of a gate is HIGH when atleast one of its inputs is LOW. It is true for

- A. XOR
- B. NOR
- C. NAND
- D. OR

481. The output of a gate is HIGH when atleast one of its inputs is HIGH. It is true for

- A. NAND
- B. OR
- C. AND
- D. XOR

482. The output of a gate is HIGH if and only if all its inputs are HIGH. It is true for

- A. XOR
- B. OR
- C. AND
- D. NAND

483. The output of a gate is LOW if and only if all its inputs are HIGH. It is true for

- A. AND
- B. NOR
- C. XNOR
- D. NAND

484. The output of a gate is HIGH if and only if all its inputs are LOW. It is true for

- A. NOR
- B. NAND
- C. XOR
- D. XNOR

485. The output of a gate is LOW if and only if all its inputs are LOW. It is true for

- A. XOR
- B. OR
- C. AND
- D. NOR

486. The output of a 2-input gates is 1 if and only if its inputs are unequal. It is true for

- A. OR
- B. XNOR
- C. XOR
- D. NOR

487. The output of a 2-input gates is 0 if and only if its inputs are unequal. It is true for

- A. XNOR
- B. NOR
- C. AND
- D. NAND

488. The output of a 2-input gates is 1 if and only if its inputs are equal. It is true for

- A. AND
- B. OR
- C. XOR
- D. XNOR

489. The output of a 2-input gates is 0 if and only if its inputs are unequal. It is true for

- A. AND
- B. OR
- C. XOR
- D. NOR

490. The most suitable gate for comparing two bits is

- A. AND
- B. NAND
- C. OR
- D. XOR

491. Which of the following gates can be used as an inverter?

- A. AND
- B. XOR
- C. OR
- D. None of the above

492. Which of the following gates cannot be used as an inverter?

- A. NAND
- B. NOR
- C. AND
- D. XNOR

493. The maximum number of 3-inputs gates in a 16-pin IC will be

- A. 2
- B. 4
- C. 3
- D. 5

- 494.** A quality having continuous values is
 A. A digital quantity
 B. A binary quantity
 C. An analog quantity
 D. A natural quantity
- 495.** The term bit means
 A. A small amount of data
 B. Binary digit
 C. A 1 or a 0
 D. Both answers (B) and (C)
- 496.** The time interval on the leading edge of a pulse between 10% and 90% of the amplitude is the
 A. Rise time B. Pulse width
 C. Fall time D. Period
- 497.** A pulse in a certain waveform occurs every 10 ms. The frequency is
 A. 1 kHz B. 100Hz
 C. 1 Hz D. 10 Hz
- 498.** In a certain digital waveform, the period is twice the pulse width. The duty cycle is
 A. 100% B. 50%
 C. 200% D. 150%
- 499.** An inverter
 A. Performs the NOT operation
 B. Changes a LOW to a HIGH
 C. Changes a HIGH to a LOW
 D. Does all of the above
- 500.** The output of an AND gate is HIGH when
 A. Any input is HIGH
 B. No inputs are HIGH
 C. All inputs are HIGH
 D. Both answers (A) and (C)
- 501.** The output of an OR gate is HIGH when
 A. Any input is HIGH
 B. No inputs are HIGH
 C. All inputs are HIGH
 D. Both answers (A) and (C)

- 502.** How many 3 lines to 8 line decoder are required for a 1 of 32 decoder?
 A. 1 B. 4
 C. 8 D. 16
- 503.** Convert BCD $0001\ 0010\ 0110$ to binary
 A. 1111110
 B. 1111101
 C. 1111000
 D. 1111111
- 504.** How many data select lines are required for selecting eight inputs?
 A. 1 B. 2
 C. 3 D. 4
- 505.** How many 1-of-16 decoders are required for decoding a 7 bit binary number?
 A. 5 B. 6
 C. 7 D. 8
- 506.** The implementation of simplified sum-of-products expressions may be easily implemented into actual logic circuits using all universal gates with little or no increased circuit complexity.
 A. AND/OR B. NAND
 C. NOR D. OR/AND
- 507.** Which of the following combinations cannot be combined into k-map groups?
 A. Corners in the same row
 B. Corners in the same column
 C. Diagonal corners
 D. Overlapping combinations
- 508.** Which gate is best used as a basic comparator?
 A. NOR B. OR
 C. XOR D. AND

- 509.** The binary numbers $A = 1100$ and $B = 1001$ are applied to the inputs of a comparator. What are the output levels?
 A. $A > B = 1, A < B = 0, A \neq B = 1$
 B. $A > B = 0, A < B = 1, A = B = 0$
 C. $A > B = 1, A < B = 0, A = B = 0$
 D. $A > B = 1, A < B = 0, A = B = 1$
- 510.** A logic probe is placed on the output of a gate and the display indicator is dim. A pulser is used on each of the input terminals, but the output indication does not change. What is wrong?
 A. The output of the gate appears to be open
 B. The dim indication on the logic probe indicates that the supply voltage is probably low
 C. The dim indication is a result of a bad ground connection on the logic probe
 D. The gate may be a tri state logic.
- 511.** Two 4-bit binary numbers (1011 and 1111) are applied to a 4-bit parallel adder. The carry input is 1. What are the values for the sum and carry output?
 A. $\Sigma_1 \Sigma_2 \Sigma_3 = 0111, C_{out} = 0$
 B. $\Sigma_1 \Sigma_2 \Sigma_3 = 1111, C_{out} = 1$
 C. $\Sigma_1 \Sigma_2 \Sigma_3 = 1011, C_{out} = 1$
 D. $\Sigma_1 \Sigma_2 \Sigma_3 = 1100, C_{out} = 1$
- 512.** Each "1" entry in a K-map square represents:
 A. A HIGH for each input truth table condition that produces a HIGH output.
 B. A HIGH output on the truth table for all LOW input combinations.
 C. A LOW output for all possible HIGH input conditions.
 D. A DON'T CARE condition for all possible input truth table combinations.
- 513.** Looping on a k-map always results in the elimination of:
 A. Variables within the loop that appear only in their complemented form
 B. Variables that remain unchanged within the loop
 C. Variables within the loop that appear in both complemented and uncomplemented form
 D. Variables within a loop that appear only in their uncomplemented form
- 514.** The carry output of a half-adder circuit can be expressed as.....
 A. $C_{out} = AB$
 B. $C_{out} = A + B$
 C. $C_{out} = A \oplus B$
 D. None of the above
- 515.** What is the major difference between half-adders and full-adders?
 A. Nothing basically; full-adders are made up of two half-adders.
 B. Full adders can handle double-digit numbers.
 C. Full adders have a carry input capability.
 D. Half adders can handle only single-digit numbers.
- 516.** Manipulation of individual bits of a word is often referred to as
 A. Bit twiddling
 B. Bit swapping
 C. Micro operation
 D. None of the above
- 517.** The ASCII code for letter A is
 A. 1100011 B. 100000
 C. 1111111 D. 0010011
- 518.** Which gate can be used as anti-coincidence detector?
 A. X-NOR B. NAND
 C. X-OR D. NOR

519. Which of the following is a self-complementing code?
 A. 8421 code B. 5211 code
 C. Gray code D. Binary code
520. Excess 3 code is also known as:
 A. Weighted code
 B. Self-complementing code
 C. Cyclic redundancy code
 D. Algebraic code
521. Binary equivalent of gray code number 101 is
 A. 101 B. 110
 C. 100 D. 111
522. Which of the following expression is in the product-of-sums form?
 A. $(A + B)(C + D)$ B. $(AB)(CD)$
 C. $AB(CD)$ D. $B + CD$
523. Which of the following expressions is in the sum-of-products form?
 A. $(A + B)(C + D)$ B. $(AB)(CD)$
 C. $AB(CD)$ D. $AB + CD$
524. Which statement below best describes a Karnaugh map?
 A. A Karnaugh map can be used to replace Boolean rules.
 B. The Karnaugh map eliminates the need for using NAND and NOR gates.
 C. Variable complements can be eliminated by using Karnaugh maps.
 D. Karnaugh maps provide a visual approach to simplifying Boolean expressions.
525. A decoder can be used as a demultiplexer by
 A. tying all enable pins LOW
 B. tying all data-select lines LOW
 C. tying all data-select lines HIGH
 D. using the input lines for data selection and an enable line for data input

526. How many 4-bit parallel adders would be required to add two binary numbers each representing decimal numbers up through 300_{10} ?
 A. 1 B. 2
 C. 3 D. 4
527. A certain BCD-to-decimal decoder has active-HIGH inputs and active-LOW outputs. Which output goes LOW when the inputs are 1001?
 A. 0 B. 3
 C. 9 D. None of the above
528. A full-adder has a $Cin = 0$. What are the sum (Σ) and the carry (C_{out}) when $A = 1$ and $B = 1$?
 A. $\Sigma = 0, C_{out} = 0$ B. $\Sigma = 0, C_{out} = 1$
 C. $\Sigma = 1, C_{out} = 0$ D. $\Sigma = 1, C_{out} = 1$
529. Which of the following gates is a series circuit gate?
 A. AND GATE
 B. OR GATE
 C. XOR GATE
 D. None of the above
530. $A+B$ can be implemented by
 A. NAND gate alone
 B. Both (A) and (B)
 C. NOR gate alone
 D. None of the above
531. Which of the following logic expression is incorrect?
 A. $1 \oplus 0 = 1$ B. $\oplus 1 \oplus 0 = 1$
 C. $1 \oplus 1 \oplus 1 = 1$ D. $1 \oplus 1 = 0$
532. Let x and y be the input and z be the output of NAND gate. The value of z is given by:
 A. $x \cdot y$
 B. $x + y$
 C. $x \cdot y$
 D. None of the above
533. $(NOR)(XOR)(NAND) =$
 A. NOR B. XOR
 C. NAND D. XNOR
534. The total number of Boolean functions which can be realized with four variables is
 A. 4 B. 256
 C. 17 D. 65,536
535. The Boolean function $A + BC$ is reduced form of...
 A. $AB + BC$ B. $A B + ABC$
 C. $(A+B)(A+C)$ D. $(A + C) B$
536. The logical expression $y = A + A B$ is equivalent to...
 A. $Y = AB$ B. $Y = A + B$
 C. $Y = A+B$ D. $Y = A B$
537. What is the maximum number of different Boolean functions involving n Boolean variables?
 A. n^2 B. 2^{2^n}
 C. 2^n D. 2^{n^2}
538. With three variables maximum possible logical expression is:
 A. 6 B. 512
 C. 256 D. 65536
539. In n variables maximum possible dual expression is:
 A. n^2 B. $2^{2^{n-1}}$
 C. 2^n D. 2^{n^2}
540. Which of the following expression is not equivalent to x ?
 A. $X \text{NAND } x$ B. $X \text{NAND } 1$
 C. $X \text{NOR } X$ D. $X \text{NOR } 1$
541. The address bus width of a memory of size 1024×8 bits is
 A. 8 bits B. 13 bits
 C. 10 bits D. 15 bits

542. The final step in designing the combinational circuit is
 A. To determine the input and output variables
 B. To draw the truth table
 C. To minimize the Boolean function for each output obtained
 D. To draw the minimized logic diagram
543. The fetching, decoding and executing of an instruction is broken down into several time intervals. Each of these intervals, involving one or more clock period is called
 A. Instruction cycle
 B. Machine cycle
 C. Process cycle
 D. None of the above
544. A combinational circuit consists of
 A. Logic gate and memory elements
 B. Logic gates only
 C. Memory elements only
 D. None of the above
545. Full adder circuit can be implemented by
 A. Multiplexer
 B. AND and OR gates
 C. Half adders
 D. Decoders
546. How many full adders are required to construct an m -bit parallel adder?
 A. m
 B. $m/2$
 C. $m-1$
 D. $m+1$

547 select the statement that best describes the parity method of error detection:

- A. Parity checking is best suited for detecting double-bit errors that occur during the transmission of codes from one location to another.
- B. Parity checking is not suitable for detecting single-bit errors in transmitted codes.
- C. Parity checking is best suited for detecting single-bit errors in transmitted codes.
- D. Parity checking is not suitable for detecting single-bit errors in transmitted codes.

548 A logic circuit that provides a HIGH output for both inputs HIGH or both inputs LOW is a(n)

- A. EX-NOR gate
- B. OR gate
- C. EX-OR gate
- D. NAND gate

549 A logic circuit that provides a HIGH output if one input or the other input, but not both, is HIGH, is a(n):

- A. EX-NOR gate
- B. OR gate
- C. EX-OR gate
- D. NAND gate

550 Identify the type of gate below from the equation $X = A \oplus B = \bar{A}B + A\bar{B}$

- A. OR GATE
- B. NOR GATE
- C. EX-OR GATE
- D. NAND GATE

551 Parity systems are defined as either _____ or _____ and will add an extra _____ to the digital information being transmitted.

- A. Positive, negative, byte
- C. Upper, lower, digit
- B. Odd, even, bit
- D. On, off, decimal

552 Which type of gate can be used to add two bits?

- A. EX-OR
- B. EX-NOR
- C. EX-NAND
- D. None of the above

553 Why is an exclusive-NOR gate sometimes called an equality gate?

- A. The output is false if the inputs are equal.
- B. The output is true if the inputs are opposite.
- C. The output is true if the inputs are equal.
- D. None of the above

554 Show from the truth table how an exclusive-OR gate can be used to invert the data on one input if the other input is a special control function.

- A. Using A as the control, where 0, X is the same as B. Where 1, X is the same as B.
- B. Using A as the control, where 0, X is the same as B. Where 1, X is the inverse of B.
- C. Using A as the control, where 0, X is the inverse of B. Where 1, X is the same as B
- D. Using A as the control, where 0, X is the inverse of B. Where 1, X is the inverse of B.

555 Determine odd parity for each of the following data words:

- | | | |
|------------------------|----------|----------|
| 1011101 | 11110111 | 10011010 |
| A. P = 1, P = 1, P = 0 | | |
| B. P = 0, P = 0, P = 0 | | |
| C. P = 1, P = 1, P = 1 | | |
| D. P = 0, P = 0, P = 1 | | |

556 The Ex-NOR is sometimes called the _____.

- A. Parity gate
- B. Equality gate
- C. Inverted gate
- D. Parity gate or the equality gate

557 Determine the values of A, B, C, and D that make the sum term $\bar{A} + B + \bar{C} + D$ equal to zero.

- A. A = 1, B = 0, C = 0, D = 0
- B. A = 1, B = 0, C = 1, D = 0
- C. A = 0, B = 1, C = 0, D = 0
- D. A = 1, B = 0, C = 1, D = 1

558 An AND gate with schematic "bubbles" on its inputs performs the same function as a(n) _____ gate.

- A. NOT
- B. OR
- C. NOR
- D. NAND

559 For the SOP expression, how many 1s are in the truth table's output column

- A. 1
- B. 2
- C. 3
- D. 4

560 A truth table for the SOP expression has how many input combinations?

- A. 1
- B. 2
- C. 4
- D. 8

561 How many gates would be required to implement the following Boolean expression before simplification? $XY + X(Y+Z) + Y(X+Z) + B'C$ is:

- A. 1
- B. 2
- C. 3
- D. 5

562 In canonical SOP form, the number of min terms in logical expression, $A + B'C$ is:

- A. 4
- B. 5
- C. 6
- D. 7

563 How many gates would be required to implement the following Boolean expression after simplification? $XY + X(Y+Z) + Y(X+Z)$

- A. 1
- B. 2
- C. 3
- D. 5

564 Which Boolean algebra property allows us to group operands in an expression in any order without affecting the results of the operation [for example, $A + B = B + A$]?

- A. Associative
- B. Commutative
- C. Boolean
- D. Distributive

565 Applying DeMorgan's theorem to the expression $(X + Y) + \bar{Z}$, we get _____

- A. $(X + Y)Z$
- B. $(X' + Y')Z$
- C. $(X + Y)Z'$
- D. $(X' + Y')Z'$

566 Use Boolean algebra to find the most simplified SOP expression for $F = ABD + CD + ACD + ABC + A'BCD$.

- A. $F = ABD + ABC + CD$
- B. $F = CD + AD$
- C. $F = BC + AB$
- D. $F = AC + AD$

567 In a sequential circuit the next state is determinedand.....

- A. State variable, current state
- B. Current state, flip-flop output
- C. Current state and external input
- D. Input and clock signal applied

568 The divide-by-60 counter in digital clock is implemented by using two cascading counters:

- A. Mod -6, Mod-10
- B. Mod -50, Mod -10
- C. Mod 10, Mod-50
- D. Mod- 50 , Mod -6

569. The minimum time for which the input signal has to be maintained at the input of flip-flop is called ____ of the flip-flop.

- A. Set-up time
- B. Hold time
- C. Pulse interval time
- D. Pulse stability time (PST)

570. ____ is said to occur when multiple internal variables change due to change in one input variable

- A. Race condition
- B. Hold delay
- C. Hold and wait
- D. Clock skew

571. A decade counter is.....

- A. Mode-3 counter
- B. Mod- 5 counter
- C. Mod -8 counter
- D. Mod-10 counter

572. A nibble consist of.....bits

- A. 2
- B. 4
- C. 8
- D. 16

573. Excess- 8 code assigns to “-8”

- A. 1110
- B. 1100
- C. 1000
- D. 0000

574. The three fundamentals gates are:

- A. AND, NAND, NOR
- B. NOT, NOR, XOR
- C. NOT, OR, AND
- D. NOT, NOR XOR

575. The amount of memory that is supported by any digital system depends upon.....

- A. The organization of memory
- B. The structure of memory
- C. The size of decoding unit
- D. The size of the address bus of the microprocessor

576. Stack is an acronym for....

- A. LIFO memory
- B. FIFO memory
- C. Flash memory
- D. Bust flash memory

577. Addition of two octal numbers “36” and “71” results....

- A. 213
- B. 123
- C. 127
- D. 345

578. Addition of two octal numbers “567” and “243” results

- A. 2013
- B. 1023
- C. 1027
- D. 1032

579.is one of the examples of synchronous inputs.

- A. J-K input
- B. EN input
- C. Preset input (PRE)
- D. Clear Input (CLR)

580.occurs when the same clock signal arrives at different times at different clock input due to propagation delay.

- A. Race condition
- B. Ripple effect
- C. Clockskew
- D. None of the above

581. In a state diagram, the transition from a current state to the next state is determined by....

- A. Current state and the input
- B. Previous state and inputs
- C. Current state and output
- D. Previous state and output

582. Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)

- A. 1100
- B. 0011
- C. 0000
- D. 1111

ANSWERSSHEET

1.B	2.C	3.A	4.A	5.A	6.B	7.D	8.C	9.D	10.C
11.B	12.C	13.D	14.C	15.C	16.D	17.B	18.D	19.B	20.B
21.C	22.C	23.D	24.C	25.A	26.D	27.A	28.C	29.D	30.C
31.C	32.B	33.A	34.C	35.B	36.C	37.A	38.B	39.A	40.A
41.C	42.C	43.B	44.C	45.A	46.A	47.D	48.A	49.A	50.C
51.A	52.C	53.A	54.C	55.A	56.B	57.D	58.D	59.A	60.A
61.D	62.D	63.A	64.B	65.D	66.A	67.C	68.D	69.C	70.C
71.A	72.A	73.D	74.C	75.A	76.B	77.C	78.B	79.B	80.C
81.A	82.C	83.B	84.A	85.B	86.B	87.A	88.D	89.C	90.B
91.D	92.C	93.D	94.C	95.C	96.B	97.C	98.C	99.C	100.B
101.B	102.D	103.B	104.A	105.C	106.A	107.B	108.A	109.D	110.A
111.C	112.A	113.C	114.A	115.B	116.A	117.A	118.C	119.A	120.D
121.D	122.A	123.B	124.D	125.D	126.B	127.A	128.A	129.C	130.B
131.D	132.A	133.C	134.B	135.D	136.B	137.B	138.A	139.C	140.B
141.B	142.A	143.D	144.A	145.B	146.C	147.D	148.B	149.A	150.C
151.A	152.B	153.C	154.A	155.B	156.C	157.D	158.C	159.A	160.A
161.D	162.A	163.A	164.D	165.C	166.C	167.D	168.B	169.C	170.A

171.B	172.A	173.B	174.D	175.D	176.D	177.B	178.B	179.B	180.D
181.C	182.B	183.A	184.A	185.D	186.C	187.D	188.A	189.C	190.D
191.D	192.C	193.B	194.D	195.A	196.D	197.B	198.B	199.B	200.A
201.C	202.A	203.C	204.B	205.A	206.D	207.C	208.D	209.C	210.B
211.B	212.A	213.A	214.D	215.C	216.D	217.A	218.B	219.B	220.A
221.D	222.C	223.D	224.C	225.B	226.C	227.B	228.D	229.A	230.D
231.A	232.C	233.D	234.C	235.C	236.D	237.A	238.D	239.B	240.A
241.D	242.D	243.A	244.A	245.B	246.D	247.C	248.D	249.B	250.D
251.C	252.D	253.C	254.A	255.B	256.A	257.B	258.C	259.C	260.B
261.B	262.A	263.D	264.A	265.A	266.B	267.A	268.D	269.B	270.A
271.A	272.C	273.D	274.A	275.B	276.A	277.C	278.A	279.A	280.B
281.C	282.C	283.C	284.B	285.C	286.A	287.C	288.C	289.A	290.A
291.A	292.A	293.D	294.C	295.C	296.B	297.C	298.A	299.A	300.C
301.A	302.A	303.C	304.A	305.D	306.D	307.C	308.C	309.D	310.D
311.C	312.D	313.A	314.C	315.B	316.D	317.A	318.B	319.A	320.B
321.A	322.C	323.B	324.A	325.B	326.C	327.D	328.A	329.C	330.B
331.D	332.C	333.A	334.C	335.D	336.D	337.B	338.B	339.C	340.B
341.A	342.B	343.A	344.C	345.D	346.B	347.B	348.A	349.D	350.C
351.A	352.D	353.D	354.D	355.B	356.A	357.C	358.B	359.A	360.D
361.C	362.B	363.C	364.A	365.D	366.B	367.D	368.A	369.B	370.D
371.D	372.D	373.D	374.A	375.C	376.D	377.A	378.C	379.B	380.D
381.B	382.B	383.C	384.B	385.D	386.A	387.B	388.C	389.C	390.D
391.C	392.B	393.A	394.B	395.A	396.D	397.B	398.A	399.C	400.D
401.B	402.B	403.D	404.A	405.D	406.B	407.A	408.C	409.D	410.B
411.D	412.D	413.D	414.C	415.D	416.D	417.C	418.B	419.C	420.B
421.D	422.A	423.B	424.D	425.A	426.B	427.C	428.C	429.B	430.A

431.B	432.B	433.C	434.D	435.C	436.B	437.D	438.B	439.C	440.A
441.D	442.B	443.C	444.A	445.A	446.B	447.A	448.C	449.D	450.B
451.D	452.A	453.C	454.B	455.B	456.A	457.D	458.C	459.D	460.B
461.A	462.D	463.D	464.C	465.B	466.A	467.B	468.A	469.D	470.A
471.D	472.D	473.D	474.C	475.A	476.D	477.B	478.D	479.A	480.C
481.B	482.C	483.D	484.A	485.B	486.C	487.A	488.D	489.C	490.D
491.B	492.C	493.C	494.C	495.D	496.A	497.B	498.B	499.D	500.C
501.D	502.B	503.A	504.C	505.D	506.B	507.C	508.C	509.C	510.A
511.C	512.A	513.C	514.C	515.C	516.A	517.B	518.C	519.A	520.B
521.B	522.A	523.D	524.D	525.D	526.C	527.C	528.B	529.A	530.B
531.B	532.A	533.B	534.D	535.C	536.C	537.B	538.C	539.B	540.D
541.C	542.D	543.B	544.B	545.A	546.A	547.C	548.A	549.C	550.C
551.B	552.A	553.C	554.B	555.D	556.B	557.B	558.C	559.C	560.D
561.D	562.B	563.B	564.B	565.A	566.A	567.C	568.A	569.B	570.A
571.D	572.B	573.D	574.C	575.D	576.A	577.C	578.D	579.D	580.B
581.A	582.C								