Fabrication and Characterization of PERL Silicon Solar-Cell

Muqtadir Hussain* [a),1], Efosa Imasekha [b),1] and Jingqi Sun [b)]
[1)]McMaster University, 1280 Main Street West, Hamilton, ON, L8S 4L8, Canada.

(Dated: November 29, 2024)

This report details the fabrication and characterization of Passivated Emitter and Rear Locally Diffused (PERL)-based silicon solar cells, with the objective of understanding the influence of material processing and device engineering on photovoltaic performance. The fabrication process included surface cleaning, texturing, doping, oxide growth, and contact metallization, designed to emulate the features of high-efficiency commercial silicon solar cells. Characterization was performed through IV measurements under dark and illuminated conditions, resistance analysis, and complementary observations from SEM imaging and carrier lifetime mapping. The results revealed a maximum efficiency of 0.70%, achieved by the rough-textured middle row with wide grid spacing, significantly below the benchmark efficiencies of commercial silicon solar cells. Performance was limited by non-uniform doping, surface defects, and elevated resistive losses, particularly in edge-dominated regions of the wafer. The discussion highlights the critical impact of process variability on device performance and proposes improvements, including uniform doping techniques, optimized texturing, and advanced contact fabrication. This study underscores the complexities of achieving commercial-grade efficiencies in a laboratory setting and offers insights into potential pathways for enhancing the performance of future solar cells.

I. INTRODUCTION

Silicon solar cells have long been the cornerstone of photovoltaic technology, providing a reliable and efficient means of converting sunlight into electricity. At their core, silicon solar cells rely on the photovoltaic effect, wherein photons with energies exceeding the bandgap of silicon (1.12 eV) generate electron-hole pairs. These charge carriers are then separated by the built-in electric field of the pn-junction, allowing for the generation of an electric current when connected to an external circuit. Key performance parameters such as open-circuit voltage (V_{OC}), short-circuit current (I_{SC}), fill factor (FF), and efficiency (η) collectively determine the effectiveness of a solar cell. However, achieving high efficiency requires optimizing both the material properties and the device architecture to minimize optical and electrical losses.

The solar cell fabricated in this experiment is loosely based on the Passivated Emitter and Rear Locally Diffused (PERL) silicon solar cell, a design that set a world record for single-junction silicon cell efficiency at 25% in 1994. While the PERL architecture is far too complex for undergraduate laboratory fabrication, the cell processed in this experiment incorporates several critical features inspired by the PERL design. These include a thermally grown silicon dioxide layer on the front surface for passivation and anti-reflective properties, a back-surface field (BSF) to minimize rear-side carrier recombination, and inverted pyramid structures to enhance light trapping and photon absorption.

The fundamental operating principle of a solar cell is based on the generation of electron-hole pairs through photon absorption. When photons strike a direct-bandgap semiconductor, as illustrated in Fig. 1, their energy ($E = h\nu$) is transferred to electrons in the valence band. If this energy exceeds or equals the bandgap of the material, the electrons are excited into the conduction band, enabling electrical conduction.

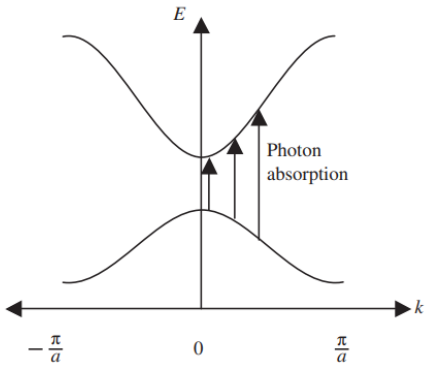

FIG. 1. Photon absorption exciting an electron between valence and conducting bands in a direct-gap semiconductor. (1)

Silicon-based solar cells utilize key semiconductor manufacturing techniques to achieve the structure depicted in Fig. 2. The typical design includes several critical components:

- A thin n+ doped silicon layer on the light-facing side of the cell. The n-type silicon enhances performance due to its superior electron mobility and conductivity.
- A metal grid and back metal contacts that serve as ohmic contacts for current collection. The front metal grid is made as narrow and thin as possible to minimize shadowing effects and maximize light reaching the active area of the cell.
- An anti-reflective coating that reduces photon loss by reflection, thereby increasing the efficiency of photon absorption.
- A p-type silicon region, creating a pn-junction positioned close to the incident light. The thickness of the n+ layer determines the proximity of the pn-junction to the light source, ensuring optimal photon interaction(1).

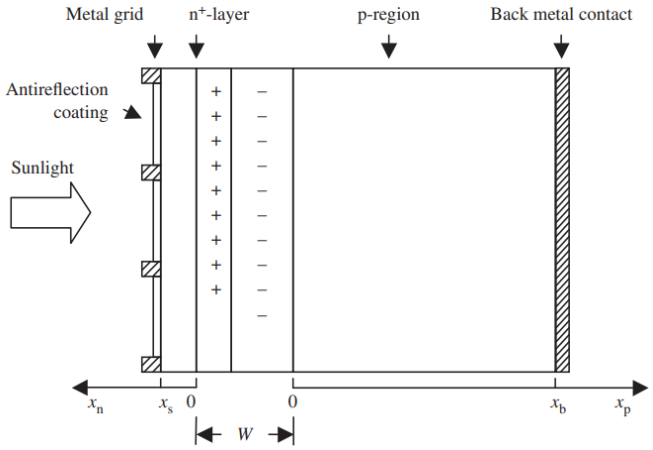

FIG. 2. Typical layout of silicon-based p-n junction solar cell. (1)

In this configuration, incident light passes through the spaces between the metal grid lines, penetrates the n+ silicon layer, and excites electrons at the pn-junction. The result is illustrated in Fig. 3: electrons transition into the conduction band, becoming free carriers that generate current. The flow of these electrons between the ohmic contacts creates the voltage and current required to produce power.

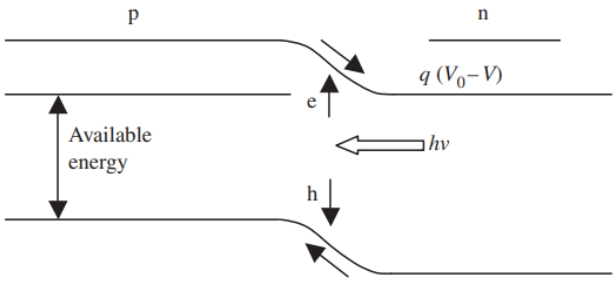

FIG. 3. Band diagram of solar cell undergoing excitation from light source. (1)

II. EXPERIMENTAL PROCESS

To fabricate our solar cell and achieve the experimental objectives, we meticulously followed a series of precise steps, ensuring precision at each stage while accommodating necessary adjustments. The fabrication process of the silicon solar cell began with a p-type silicon wafer, with a diameter of 5.09 cm, a thickness of 279 ± 25 μm oriented <1-0-0> with a resistance of 1 - 10 Ω-cm. A 120 nm layer of wet oxide was grown to produce Silicon dioxide on the surface to be used as the n-type contact region. The process started with the preparation of silicon wafers to establish a clean, defect-free substrate. We started by immersing the wafers in acetone for five minutes to remove organic contaminants. This was followed by rinsing with isopropanol (IPA) for three minutes to dissolve any residual acetone. Finally, the wafers were rinsed with deionized (DI) water for two minutes to remove ionic impurities. To prevent contamination from drying residues, we used a nitrogen gas jet to dry the wafers. Native silicon dioxide, which naturally forms on the wafer surface upon air exposure, was removed using a 10% hydrofluoric acid (HF) dip for 30 seconds. This critical step ensured the silicon surface was exposed for subsequent processes. We verified the removal of the oxide by observing the hydrophobicity of the wafer surface, as bare silicon becomes hydrophobic while oxidized silicon is hydrophilic. This preparation provided a pristine starting point for the rest of the fabrication.

After cleaning, we proceeded with surface texturing to enhance light trapping. This process targeted rows requiring specific surface textures, such as smooth, rough, and inverted pyramid structures. We employed photolithography to define patterns for surface modification. The wafers were spin-coated with a positive photoresist (S1813) at 4000 rpm for 45 seconds to ensure a uniform coating. This was followed by a soft bake at 115°C for 90 seconds to solidify the photoresist. The wafers were then exposed to UV light through a patterned quartz mask using a dose of 150 mJ/cm², which transferred the desired pattern onto the photoresist. After exposure, the wafers were developed in an MIF 319 developer solution for 60 seconds, removing the unexposed photoresist areas. The patterned wafers were then immersed in a 20% potassium hydroxide (KOH) solution at 80°C for 15 minutes. This anisotropic etching exploited the crystallographic properties of silicon, specifically the difference in etch rates between the (100) and (111) planes. KOH etches the (100) planes significantly faster than the (111) planes, enabling the formation of uniform inverted pyramid structures. Isopropanol was added to the etching solution to reduce surface tension, preventing bubble formation that could lead to etching defects. This step was essential for reducing surface reflectance and increasing the photon path length within the silicon.

Next, we doped the silicon to create the pn-junction, the active region of the solar cell. Using a spin-on dopant (P509), we deposited a phosphorus-rich liquid layer on the polished silicon surface by spinning the wafer at 3000 rpm for 30 seconds. The dopant layer was then baked at 200°C for five minutes to solidify it. The wafers were annealed at 950°C for 30 minutes in a nitrogen atmosphere to activate the phosphorus dopants and drive them into the silicon substrate, forming a thin n-type layer over the p-type wafer. This step was critical for creating the electric field required for photovoltaic operation. Following diffusion, the residual spin-on glass was removed using a 10% HF dip for 30 seconds. Lifetime and resistivity mapping were performed using a microwave photoconductivity decay (MDP) system, which revealed that the center of the wafer exhibited higher carrier lifetimes and lower resistivity than the edges. This discrepancy was attributed to non-uniform dopant distribution caused by centrifugal forces during the spin-coating process.

In the next stage, we optimized the anti-reflective coating (ARC) to minimize light reflectance. A thermally grown silicon dioxide layer, initially measured at 161 nm, was etched to a target thickness of 84.7 nm using HF. The optimal thickness was calculated using the quarter-wavelength formula, $d = \lambda/4n$ where $\lambda = 490$ nm (wavelength of visible light) and $n = 1.45704$ (refractive index of silicon dioxide). The first etch of 38 seconds reduced the oxide thickness to 118 nm, and a second etch of 28 seconds brought it to the final thickness. Ellipsometry measurements were conducted after each etching step to ensure precision. Achieving this thickness optimized the destructive interference of reflected light at 490 nm, enhancing the solar cell's optical performance.

To establish electrical connections, we fabricated the front and back contacts. For the front grid, photolithography was used to pattern fingers with varying spacings: narrow (200 µm), medium (450 µm), and wide (950 µm). The wafer was spin-coated with S1813 photoresist at 4000 rpm for 45 seconds, soft-baked at 115°C for 90 seconds, and exposed to UV light with a dose of 150 mJ/cm² through the grid-patterned mask. After development in MIF 319 for 60 seconds, the exposed oxide was etched using a 10% HF dip for 30 seconds, exposing the underlying silicon. A thin layer of titanium (10 nm) was sputtered as an adhesion layer, followed by a thicker layer of silver (200 nm) for conductivity. The lift-off process was performed in acetone with 5-minute sonication cycles to remove unwanted metal, leaving the grid intact. For the back contact, aluminum (500 nm) was sputtered across the rear surface of the wafer, forming a back-surface field (BSF) to reduce carrier recombination.

Once fabrication was complete, we characterized the solar cell to evaluate its performance. IV measurements under dark conditions were performed by sweeping the voltage from -0.2 V to 1.0 V in 0.03 V increments using a source meter, recording the corresponding current at each step. These measurements assessed diode behavior, including reverse leakage current and forward conduction. Illuminated IV measurements were conducted using a solar simulator calibrated to AM1.5G illumination (100 mW/cm2). From these data, we extracted key metrics such as open circuit voltage (VOC) short circuit current (ISC), maximum power point (MPP), fill factor (FF), and efficiency (η).

Finally, we measured the contact resistance using side pads designed for this purpose. Resistance values were plotted against pad spacing, allowing us to extrapolate specific contact resistivity. This analysis confirmed high conductivity for the aluminum back contact and revealed slight variability in the silver front contact based on finger spacing. Each step in the fabrication and characterization process was critical for optimizing the solar cell's performance, providing insights into how surface texture, doping profiles, and contact design influenced the device's efficiency.

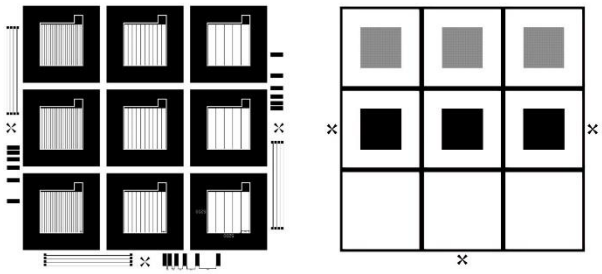

FIG. 4. Post-photolithography wafer and cell orientation

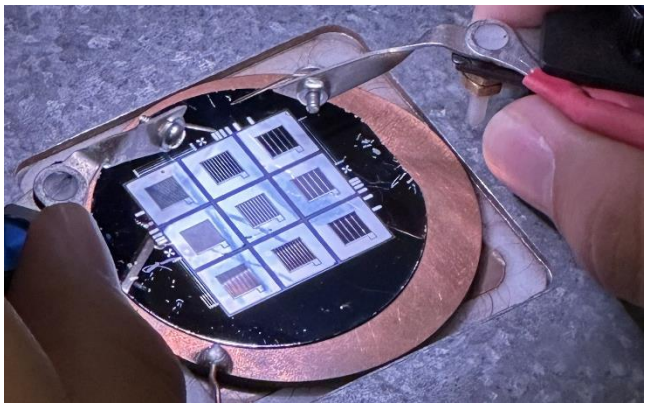

FIG. 5. Final wafer containing 9 individual solar cells with ohmic contacts.

III. RESULTS

The results of the fabricated Passivated Emitter and Rear Locally Diffused (PERL) silicon solar cell were obtained through comprehensive characterization and analysis. The characterization involved IV measurements under both dark and illuminated conditions, resistance measurements, and key performance metrics extraction. The objective was to evaluate the impact of surface texture (Flat, Rough, and Inverted Pyramids) and grid finger spacing (Narrow, Medium, and Wide) on cell performance. This section presents the processed data, representative metrics, and associated observations in detail.

A. IV Characteristics

The IV measurements provided insight into the diode characteristics in dark conditions and the photovoltaic performance under standard illumination (AM1.5G sunlight at 100 mW/cm²). IV measurements under dark conditions revealed the diode rectification behavior, including reverse leakage current and forward exponential growth. Under illumination, the photovoltaic response was characterized, and key performance metrics were extracted from corrected IV and power plots. From these curves, the open-circuit voltage (V_{OC}) short-circuit current (I_{SC}), maximum power point (MPP), fill factor (FF), and efficiency (η) were extracted. Additional parameters such as shunt resistance (R_{SH}) and series resistance (R_S) were determined from the IV data to understand the resistive losses and leakage pathways in the cells.

The open-circuit voltage (V_{OC}) was identified as the voltage at which the current becomes zero. For each configuration, V_{OC} was directly interpolated from the IV data. Similarly, the short-circuit current (I_{SC}) was the current at zero voltage, extracted directly from the data. The maximum power point (MPP) was calculated from the IV curve as the product of the voltage and current values where the power reached its peak. The extracted key metrics for all configurations are summarized in Table 1. The calculations were conducted using corrected IV and power plots with inverted current polarities, ensuring reliable results. For efficiency calculations, the input power (P_{in}) was determined as the product of the solar intensity (100 mW/cm^2) and the active cell area (0.2704 cm^2), giving P_{in} = 27.04 mW. Efficiency (η) was computed using the formula:

$$\eta = \frac{P_{MPP}}{P_{in}} \times 100$$

For example the cell in the Rough Row (Wide Spacing) configuration had P_{MPP} = 0.000189 W. Converting P_{MPP} to mW (0.189 mW) and applying the formula:

$$\eta = \frac{0.189}{27.04} \times 100 = 0.70\%$$

Similarly, fill factor (FF) was calculated as:

$$FF = \frac{P_{MP}}{V_{OC} I_{SC}}$$

TABLE I. Key Metrics for All Fabricated Solar Cell Configurations

Row	Grid Spacing	VOC (V)	ISC (A)	PMPP (W)	FF	Efficiency (%)	Rsh (Ω)	Rs (Ω)
Flat	Narrow	0.476	0.00128	0.0001766	0.289	0.65	1955.81	287.66
Flat	Medium	0.421	0.000502	0.0000532	0.252	0.2	734.01	581.58
Flat	Wide	0.472	0.00000233	0.000000147	0.134	0.00054	74036.75	1207307.36
Rough	Narrow	0.496	0.00000254	0.00000016	0.127	0.00059	106831.24	566392.53
Rough	Medium	0.457	0.000276	0.0000171	0.136	0.06	661.88	4807.5
Rough	Wide	0.308	0.00221	0.000189	0.277	0.7	176.79	95.17
Inverted Pyramids	Narrow	0.452	0.00000371	0.000000181	0.108	0.00067	37090.59	300724.54
Inverted Pyramids	Medium	0.501	0.0000134	0.00000114	0.17	0.0042	58292.9	869022.86
Inverted Pyramids	Wide	0.752	0.000281	0.0000336	0.159	0.12	10385.9	216576.02

To illustrate the photovoltaic performance, representative IV curves under dark and illuminated conditions were selected from the Rough Row (Wide Spacing) configuration, which exhibited the highest efficiency (0.70%). The dark IV curve shows the diode rectification behavior, including reverse leakage and forward conduction characteristics. The illuminated IV curve highlights the operating range for P_{MPP}.

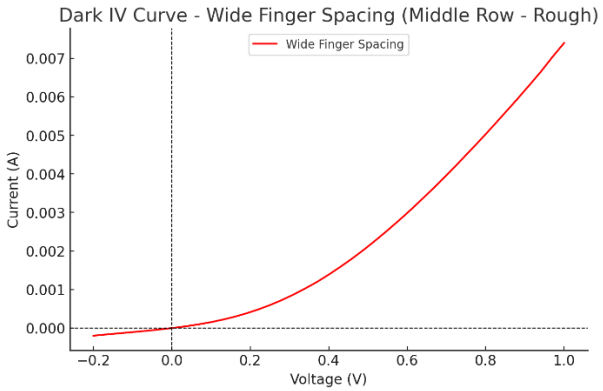

FIG. 6. Dark I-V Curve – Rough Row -Wide finger Spacing

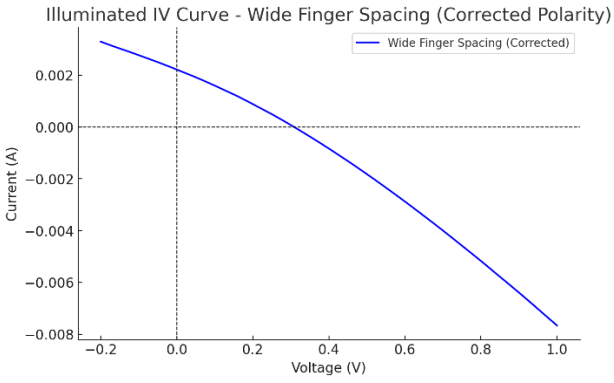

FIG. 7. Illuminated I-V Curve – Rough Row -Wide finger Spacing

The dark IV curve demonstrates the rectification behavior of the diode, while the illuminated IV curve and Power curve highlights the photovoltaic performance, including the operating range for V_{MP} and I_{MP}.The analysis confirms the strong influence of surface texture and grid finger spacing on cell performance. The Middle Row, Wide Spacing configuration exhibited the optimal balance of resistive losses, shunt resistance, and light trapping, making it the benchmark configuration for this study.

IV. DISCUSSION

The performance of the fabricated Passivated Emitter and Rear Locally Diffused (PERL)-based silicon solar cells was evaluated through detailed characterization, encompassing IV measurements under both dark and illuminated conditions, resistance characterization, and analysis of key performance metrics. Complementary data, such as carrier lifetime and resistivity measurements, provided critical insights into material quality and doping uniformity, while observations from SEM imaging shed light on the effects of surface texturing. The results are compared to commercial silicon solar cells, with hypotheses offered to explain the discrepancies based on fabrication processes and experimental conditions.

A. SEM Imaging results

SEM images of the textured surfaces revealed well-defined inverted pyramid structures, crucial for reducing surface reflectance and enhancing light absorption. These structures increase the path length of photons within the silicon, theoretically improving light trapping and current generation. However, occasional defects, such as under-etched or uneven structures, were observed, particularly at the wafer edges. These defects likely arose from non-uniform KOH etching, caused by uneven surface tension or incomplete IPA dissipation during the etching process. Such imperfections increase surface recombination, reducing carrier lifetime and partially negating the advantages of the inverted pyramid design. These findings correlate with the suboptimal performance of the inverted pyramid configurations compared to rough and flat surfaces, highlighting the importance of precise control during texturing.

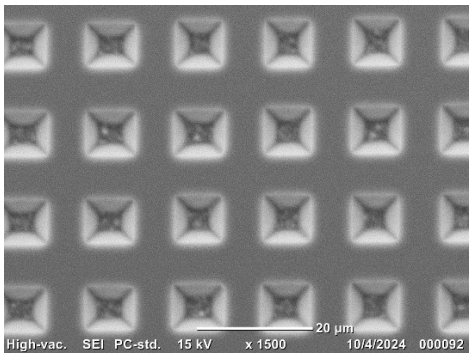

FIG. 8. A regular grid of inverted pyramids is visible, with well-defined edges and consistent size.

In the SEM images of the textured regions (Figure 8), we observed well-defined inverted pyramid structures. These features are indicative of successful KOH etching, leveraging the crystallographic anisotropy of silicon. Specifically, the (111) planes etch much slower than the (100) planes, leading to the triangular geometry characteristic of inverted pyramids. These structures enhance light absorption by increasing the path length of photons within the silicon, reducing reflectance and improving photon capture.

Some images (Figure 9) revealed under-etched areas where the inverted pyramid structures were either incomplete or irregular. These defects likely occurred due to insufficient KOH exposure or inadequate removal of the photoresist mask during the photolithography step. Such irregularities increase surface recombination by introducing non-uniform regions and act as traps for charge carriers, reducing the carrier lifetime and overall cell efficiency.

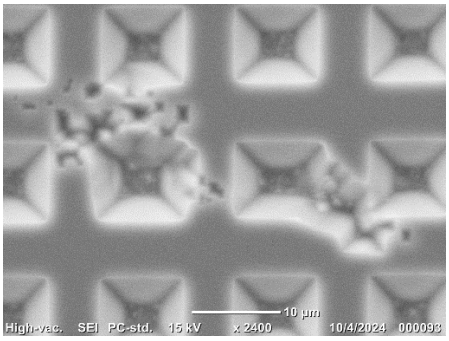

FIG. 9. Imperfect etching of inverted pyramid pattern leading to loss of effective light absorption.

In several images of the wafer edges, we observed more pronounced defects and uneven pyramid structures compared to the center. This observation aligns with the analysis of doping non-uniformity and resistivity data, as the edges are more susceptible to process-induced inconsistencies. During spin-coating of the dopant, centrifugal forces may have pushed the liquid outward, leading to thinner and uneven dopant layers at the edges. Similarly, edge turbulence during

KOH etching may have exacerbated the irregularities in texturing.

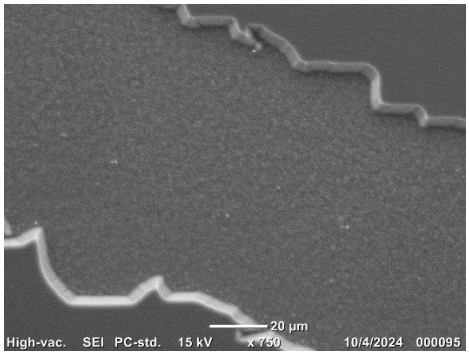

FIG. 10. A close-up of the wafer's edge, showing uneven etching and particulate contamination.

B. Carrier Lifetime and Resistivity Data

Carrier lifetime and resistivity are fundamental parameters that govern the performance of silicon solar cells, as they directly influence charge carrier generation, transport, and recombination within the device. The measured data from Minority Carrier Lifetime Profiling (MDP) and resistivity mapping revealed significant spatial non-uniformities across the wafer, which directly impacted the performance metrics obtained from IV characterization.

The carrier lifetime was found to be higher at the center of the wafer and significantly lower at the edges (Figure 11). This variation can be attributed to the spin-coating process used during the phosphorus doping step. During spin-coating, centrifugal forces drive the dopant solution outward, leading to a thicker dopant layer near the wafer edges. While this process ensures coverage across the wafer, the thicker dopant layer at the edges often suffers from incomplete diffusion and higher susceptibility to contamination during subsequent processing. The non-uniform spin-on layer likely introduced structural defects and contamination at the wafer edges, creating recombination centers that decreased carrier lifetime. This was exacerbated by edge-specific issues such as over-etching during KOH texturing and uneven oxide growth, which further degraded electrical properties at the edges.

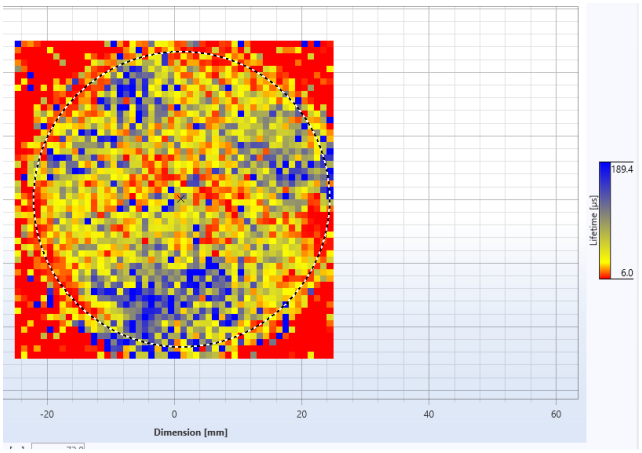

FIG. 11. Spatial variations in carrier lifetime across the wafer, measured in microseconds

The lower carrier lifetime at the edges resulted in increased recombination losses, where charge carriers generated by light were lost before contributing to the current. In contrast, the wafer center, where the dopant layer was thinner and more uniform, exhibited higher carrier lifetimes and better electrical properties. The uniform doping at the center likely facilitated better junction quality, reducing recombination and enhancing carrier transport efficiency. This explains the relatively higher performance observed in the middle regions of the fabricated cells, particularly in configurations with wide spacing, where resistive losses were minimized.

Resistivity measurements corroborated these findings, with higher resistivity values recorded at the edges compared to the center (Figure 12). Resistivity, which is inversely related to doping concentration, indicates the electrical conductivity of the silicon. The higher resistivity at the edges suggests incomplete activation of dopants during the thermal annealing process. In addition, structural imperfections and contamination at the edges likely contributed to increased resistivity, hindering charge transport and increasing series resistance in the affected regions.

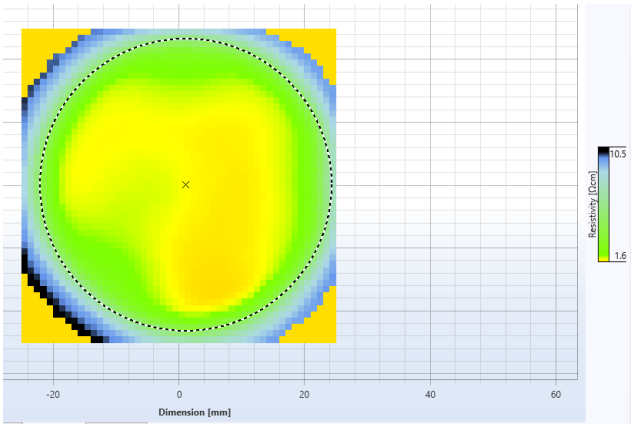

FIG. 12. Spatial distribution of resistivity (Ω·cm) across the wafer.

These spatial variations in carrier lifetime and resistivity are consistent with the trends observed in the IV performance metrics. Cells fabricated from regions with higher resistivity and lower carrier lifetime showed lower short-circuit current (I_{SC}) and higher series resistance (R_S), resulting in reduced efficiency. For instance, the flat row configurations, which likely relied more heavily on edge-dominated regions, exhibited both lower I_{SC} and higher R_S compared to the middle row (rough surface with wide spacing), where the center region's superior properties were more effectively utilized.

C. IV Measurements and Key Metrics

The IV measurements under dark conditions confirmed the expected diode rectification behavior, including exponential current growth in forward bias and minimal reverse leakage. Illuminated IV measurements provided critical photovoltaic performance metrics. Among the configurations, the middle row with wide spacing (rough surface) demonstrated the highest performance, achieving V_{OC} = 0.308 V, I_{SC} = 2.21 mA, and η = 0.70%. This superior performance can be attributed to the balance achieved between minimal shading losses due to wide grid spacing and enhanced light absorption from the rough surface texture. Although the inverted pyramid designs were expected to perform better theoretically due to superior light trapping, surface defects likely exacerbated recombination losses, undermining their efficiency. The flat rows, while free of recombination issues, suffered from higher reflectance and lower I_{SC}, as the lack of texturing failed to enhance photon capture.

D. Shunt and Series Resistance

Resistance characterization highlighted the critical impact of grid spacing and surface texture on the device's electrical properties. Narrow grid spacing improved shunt resistance by reducing leakage pathways but increased series resistance due to shading and longer current paths. Conversely, wide grid spacing minimized series resistance but introduced higher shunt leakage, especially in textured rows with more surface defects. The optimized middle row with wide spacing effectively balanced these trade-offs, resulting in superior overall performance.

E. Comparison to Reference Silicon Solar Cells

Commercial silicon solar cells typically achieve efficiencies exceeding 20%, V_{OC} values above 0.6 V and significantly higher I_{SC}. In comparison, the fabricated cells exhibited significantly lower values, with maximum efficiency reaching only 0.70%. These discrepancies stem from several factors:

- The lab-scale processes, including spin-on doping and thermal oxidation, lacked the precision of industrial techniques like ion implantation and chemical vapor deposition. Non-uniformities during doping and oxide growth introduced structural defects and recombination centers.
- Structural defects, contamination from handling, and uneven texturing introduced recombination centers that reduced carrier lifetime and I_{SC}
- Variability in the silver-silicon contacts due to inconsistencies in sputtering and photolithography alignment increased resistive losses.
- Photolithography-defined grids caused significant shading, particularly in narrow spacing configurations, reducing the effective light-absorbing area.

Each fabrication step played a crucial role in determining the final performance. The spin-coating process during doping dictated the uniformity of the pn-junction and, consequently, carrier mobility and lifetime. KOH anisotropic etching introduced light-trapping structures but also created surface defects that exacerbated recombination in textured rows. Optimization of the anti-reflective coating (ARC) thickness was vital for minimizing reflectance, but over-etching slightly degraded performance in some samples. Finally, photolithography and sputtering during contact fabrication defined electrical pathways. Misalignment and poor adhesion in these steps further impacted contact resistance and current flow.

The observed deviations can be explained by considering the interplay of processing imperfections and device physics. Lower V_{OC} in most configurations reflects increased recombination losses due to structural defects and incomplete doping. Reduced I_{SC} in flat rows underscores the importance of texturing for light trapping, while the underperformance of inverted pyramids highlights the detrimental effects of surface recombination. High series resistance in certain configurations points to poor contact quality, while low shunt resistance indicates leakage pathways from processing defects.

V. CONCLUSION

The fabrication and characterization of the PERL-based silicon solar cells provided valuable insights into the interplay of fabrication steps, material properties, and device performance. The results highlighted the importance of

precise process control and material uniformity in achieving high-performance solar cells. While the highest efficiency achieved in this study was 0.70% (Rough Row, Wide Spacing configuration), this value is significantly lower than the efficiencies of commercial silicon solar cells, which typically exceed 20%. The low efficiencies, combined with suboptimal V_{OC}, I_{SC}, and fill factor, emphasize the need to address several key limitations in the fabrication process.

Critical performance metrics, including shunt resistance (R_{SH})and series resistance (R_S) indicated significant resistive and recombination losses. These losses were primarily attributed to non-uniform doping, surface defects introduced during texturing, and inconsistencies in contact fabrication. The edge effects observed in carrier lifetime and resistivity measurements further demonstrated the impact of processing variability on device performance. Despite these challenges, the study successfully demonstrated the role of surface texturing, grid design, and anti-reflective coatings in influencing solar cell behavior.

To enhance the performance of future fabricated solar cells, several improvements can be implemented. Uniform doping techniques such as ion implantation or in-situ doping during chemical vapor deposition (CVD) can replace the spin-on doping process, providing better control over doping profiles and improving junction quality and carrier lifetime[(4)]. The anisotropic KOH etching process can be optimized to achieve more uniform inverted pyramid structures by carefully controlling surface tension and ensuring consistent IPA dissipation, thereby reducing defects and enhancing light trapping. Advanced contact fabrication methods, including sputtering with tighter controls and post-deposition annealing, can ensure uniform metal deposition, improved adhesion, and reduced contact resistance. The anti-reflective coating (ARC) can be further developed using plasma-enhanced chemical vapor deposition (PECVD) to achieve precise thickness control, minimizing reflectance and maximizing photon absorption[(5)]. Additionally, improved edge handling protocols, such as protective coatings and enhanced contamination control during processing, can mitigate the detrimental effects of structural defects and recombination at the wafer edges. Incorporating real-time process monitoring and automation would reduce variability during critical steps like doping, etching, and oxide growth, while in-situ metrology techniques could enhance consistency across wafers. Finally, the integration of advanced simulation tools can guide experimental work by optimizing cell design parameters, including grid spacing, surface texture, and ARC thickness, prior to fabrication. By addressing these areas, future iterations of this work can significantly improve solar cell performance and narrow the gap between lab-scale fabrication and commercial-grade efficiencies.

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[5] See Park, J., & Lee, H. H., Investigation of Anti-Reflective Coatings for Enhanced Photovoltaic Performance. *International Journal of Precision Engineering and Manufacturing-Green Technology*. Available at: https://link.springer.com/article/10.1007/s12541-020-00337-5. Accessed November 30, 2023.