Murad M. Qasaimeh

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Career Profile

- An accomplished computer engineer with excellent problem-solving and analytical thinking skills.
- Hands-on experience in RTL design/verification and SoC integration using VHDL, Verilog, and HLS.
- In-depth knowledge of designing microarchitecture to accelerate computationally intensive algorithms.
- Excellent programming skills in languages like C/C++ and Python.
- Excellent written and oral communication skills and ability to handle tasks efficiently with minimum supervision.
- Available for internships and full-time positions starting on December 2019.

Education

Iowa State University — Ames, Iowa
- PhD Candidate in Electrical and Computer Engineering, GPA: 3.85 — 2015 – Present

Thesis: Techniques for Efficient Processing of Computer Vision and Deep Learning on FPGAs

American University of Sharjah — Sharjah, UAE
- Master in Electrical and Computer Engineering, GPA: 3.82 — 2012 – 2014

Thesis: An FPGA-based Parallel Hardware Architecture for Real-time Image Classification

Jordan University of Science and Technology — Irbid, Jordan
- Bachelor of Science in Computer Engineering, GPA: 85.7/100 — 2006 – 2012

Senior Design Project: Indoor Mobile Robot Localization and Navigation

Experience

- **Xilinx Research Lab** — Longmont, Colorado
  Research Engineer Intern — Sept 2018 - Nov 2018
  - Mapped complete computer vision and deep learning pipeline using OpenCV on a Pynq enabled platform.
  - Contributed to deep learning and computer vision integration, and build working prototypes.
  - Explored the FPGA mapping of other recent compute efficient neural networks.

- **Xilinx Research Lab** — San Jose, California
  Research Engineer Intern — May 2018 - Aug 2018
  - Extended the supported xfOpenCV vision kernels in cmake-based sds++ cross compiliation design flow.
  - Evaluated the performance of Xilinx's XfOpenCV and NVIDIA's VisionWorks libraries for vision applications.
  - Mapped computer vision pipelines using OpenCV on a Pynq enabled platform.

- **Iowa State University** — Ames, Iowa
  Research and Teaching Assistant — Sept 2015 - Present
  - Designed and implemented hardware accelerators for computer vision algorithms in FPGAs, CPUs, and GPUs.
  - Designed hardware accelerators for tracking motor grader's blade position (project funded by John Deere).
  - Planed, designed, prototyped, and tested RTL and HLS designs.
  - Taught courses in embedded systems (CprE288), problem solving (CprE 185) labs in C.

Programming Skills

- **Programming Languages**: C, C++11, Python, Java, JavaScript, C#, Matlab.
- **Hardware Description Languages**: VHDL, Verilog, HLS
- **Machine Learning Frameworks**: TenserFlow, Keras, Caffe, Nvidia TensorRT, Xilinx DNNDK, OpenCV DNN.
- **Scripting Languages**: Python, TCL, Bash, Perl, Ruby.
- **Tools**: Matlab, Visual studio, Netbean, Weka, Ecllipse, MPLAB.
- **Hardware Platforms**: Xilinx Zynq-7000, Zynq UltraScale+ MPSoCs, Jetson TX1/TX2, Jetson AGX, Altera DE2.
- **Libraries**: OpenCV, Nvidia VisionWorks, Xilinx xFOpenCV.
- **Operating Systems**: Linux, Mac OS, Windows.

Selected Projects

- **Analyzing the Energy Efficiency of Vision Kernels on Embedded CPUs, GPUs and FPGAs. (Xilinx)**:
  Implemented an open source benchmarking flow to compare energy efficiency of 50+ vision kernels. **(xFOpenCV, OpenCV, VisionWorks)**
- **A Vision-Based Solution for tracking Motor Grader's Blade: (JOHN DEERE)**:
  Implemented hardware accelerator to detect and track the position of motor grader's blade in world coordinate using image processing algorithms running on ARM processor and FPGA fabric. The accelerator reached 60fps for 1600×1200 resolution with a blade localization error less than 2 cm. **(VHDL, OpenCV, C++, Python)**
- **FPGA-based real time Object Detection and Recognition System**:
  Designed parallel hardware architecture for real time object detection and recognition system, using SIFT feature detection and support vector machine (SVM) classifier. The hardware architecture achieved a speedup of ×55.06 in feature extraction and ×6.64 in classification. **(Verilog, Matlab).**
- **FPGA-based Depth Estimation from Stereo Images**:
  Implemented hardware accelerator to compute the disparity from a pair of images coming from stereo camera. The architecture reached 120fps for 1920×1080 resolution and disparity range of 256. **(VHDL, OpenCV, C++).**
- **Geo**:
  (Matlab, Python).

Selected Coursework

- **Hardware**: Reconfigurable Computing, Advanced Computer Architecture, Advanced Embedded Systems in Industrial Automation, Real-Time Systems.
- **Software**: Computer Graphics and Geometric Modeling, Data Mining Knowledge Discovery, Image and Video Processing, Advanced Computation Methods.

Selected Publications GOOGLE SCHOLAR

- M. Qasaimeh, P. Jones and J. Zambreno, **A Runtime Configurable Hardware Architecture for Computing Histogram based Feature Descriptors**, Proceedings of the International Symposium on Field-Programmable Logic and Applications (FPL), August, 2018.
- M. Qasaimeh, P. Jones and J. Zambreno, **A Modified Sliding Window Architecture for Efficient BRAM Resource Utilization**, Proceedings of the Reconfigurable Architectures Workshop (RAW), May, 2017.
- M. Qasaimeh and E. Salahat, **Real-Time Image and Video Processing Using High-Level Synthesis (HLS)**, Handbook of Research on Advanced Concepts in Real-Time Image and Video Processing, IGI Global, 2017.
- M. Qasaimeh, A. Sagahyroon and T. Shanableh, **FPGA-Based Parallel Hardware Architecture for Real-Time Image Classification**, in IEEE Transactions on Computational Imaging, pp. 56-70, March 2015.
- M. Qasaimeh, A. Sagahyroon and T. Shanableh, **A parallel hardware architecture for Scale Invariant Feature Transform (SIFT)**, 2014 International Conference on Multimedia Computing and Systems (ICMCS), Marrakech, 2014.