The TAL Instruction Set (cont.)		
Machine Code	Format	
0000 00ss ssst tttt dddd d000 0010 1010	slt R _d ,	$R_s, R_t \text{ if}([R_s] < [R_t]), \text{ then } R_d \leftarrow 0^{31} \parallel 1$
0010 10ss ssst tttt iiii iiii iiii iiii	slti R _t ,	else $R_d \leftarrow 0^{32}$ R_s , I $if[R_s]$) < ([I ₁₅] ¹⁶ [I] ₁₅₀), then $R_t \leftarrow 0^{31}$ 1 else $R_t \leftarrow 0^{32}$
0000 10ii iiii iiii iiii iiii iiii iiii	j	$PC \leftarrow [PC]_{3128} \parallel [I]_{250} \parallel 0^2$
0000 00ss sss0 0000 0000 0000 0000 1000	jr R _s	$PC \leftarrow [R_s]$
000 11ii iiii iiii iiii iiii iiii iiii	jal I	$R_{31} \leftarrow [PC] + 4; PC \leftarrow [PC]_{3128} \parallel [I]_{250} \parallel 0$
000 00ss sss0 0000 dddd d000 0000 1001		R_s $R_d \leftarrow [PC] + 4; PC \leftarrow [R_s]$
000 0000 0000 0000 0000 0000 0000 1100	syscall	PC ← ExceptionHandler
000 00xx xxxx xxxx xxxx 0xxx xx00 1101	break	PC ← ExceptionHandler
100 0010 0000 0000 0000 0000 0001 0000		restore state information
100 0000 000t tttt dddd d000 0000 0000		
100 0000 100t tttt dddd d000 0000 0000	mtc0 R _t ,	
100 0100 000t ttt dada d000 0000 0000	$mfc1$ R_t ,]	L13
100 0100 100t tttt dddd d000 0000 0000		L-u(CFI)

General Notes

- I specifies part of the instruction.
- M[i] is the value of the (aligned) word of memory beginning at location i.
- m[i] is the value of the byte of memory at location i.
- R_b, R_d, R_s, and R_t specify general registers. R₃₁ specifies register 31.
- C_d specifies a control register (co-processor 0).
- (6) F_d specifies a floating point register (co-processor 1). G_d and G_s specify a floating point register in single-precision floating point format. W_d and W_s specify a floating point register in two's complement format.
- || indicates concatenation of bit fields.
- Superscripts indicate repetitions of a binary value.
- Subscripts indicate bit positions (Little-Endian) of sub-field.
- Square brackets ([]) indicate "the contents of."