

# Tailoring Fault-Tolerance to Quantum Algorithms

Zhuangzhuang Chen and Narayanan Rengaswamy

**Abstract**—The standard approach to universal fault-tolerant quantum computing is to develop a general purpose quantum error correction mechanism that can implement a universal set of logical gates fault-tolerantly. Given such a scheme, any quantum algorithm can be realized fault-tolerantly by composing the relevant logical gates from this set. However, we know that quantum computers provide a significant quantum advantage only for specific quantum algorithms. Hence, a universal quantum computer can likely gain from compiling such specific algorithms using tailored quantum error correction schemes. In this work, we take the first steps towards such algorithm-tailored quantum fault-tolerance. We consider Trotter circuits in quantum simulation, which is an important application of quantum computing. We develop a solve-and-stitch algorithm to systematically synthesize physical realizations of Clifford Trotter circuits on the well-known  $[n, n - 2, 2]$  error-detecting code family. Our analysis shows that this family implements Trotter circuits with essentially optimal depth under reasonable assumptions, thereby serving as an illuminating example of tailored quantum error correction. We achieve fault-tolerance for these circuits using flag gadgets, which add minimal overhead. Importantly, the solve-and-stitch algorithm has the potential to scale beyond this specific example, as illustrated by a generalization to the four-qubit logical Clifford Trotter circuit on the  $[20, 4, 2]$  hypergraph product code, thereby providing a principled approach to tailored fault-tolerance in quantum computing.

**Index Terms**—Quantum error correction, fault-tolerance, Trotter circuits, quantum simulation, error-detecting code, Clifford gates, flag gadgets, logical Clifford synthesis (LCS)

## I. INTRODUCTION

QUANTUM error correction (QEC) is fundamental to the realization of scalable fault-tolerant quantum computers. In recent years, QEC has moved from theory to practice where there have been several demonstrations of small error corrected systems [2]–[5]. The next frontier is the development of *scalable* QEC schemes that enable significant quantum advantages for *specific* problem domains, when compared to the best classical supercomputers. The common approach is to pursue universal fault-tolerant quantum computing where a general-purpose QEC scheme is shown to fault-tolerantly realize a universal set of logical operations on the encoded information [6]–[8]. Given such a scheme, one can execute any quantum algorithm on the logical qubits by *composing* elements of this fault-tolerant universal set. In parallel,

Accepted to IEEE Journal on Selected Areas in Information Theory, vol. 6, pp. 311–324, 2025 (DOI: 10.1109/JSAIT.2025.3602446).

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Part of this work was presented at the 2024 IEEE International Conference on Quantum Computing and Engineering [1].

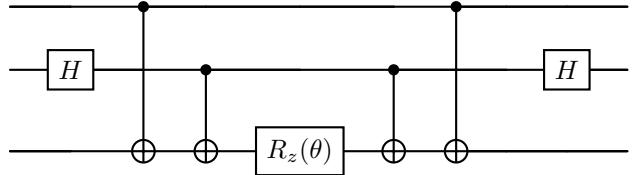


Fig. 1: Quantum Simulation Kernel (QSK) with 3 qubits.

quantum algorithms continue to be developed for various problems. However, it is widely expected that significant quantum advantage will be achieved only for some targeted problems and applications [9]–[11]. Hence, even in a universal fault-tolerant quantum computer, there are likely gains to be achieved by compiling such specific algorithms using *tailored* QEC mechanisms. More specifically, rather than composing *individual* gates from the universal set, it could be much more efficient to directly design fault-tolerant realizations of the *logical circuit as a whole*. Such exciting opportunities form the primary motivation for this work. To the best of our knowledge, this work constitutes the first such exploration.

At the outset, it is unclear how one can pose the goal of tailoring QEC schemes to logical algorithms as a systematic mathematical problem. When can we say that a QEC scheme is “well-matched” to execute an algorithm? In this paper, we work with the objective of achieving a depth-optimal fault-tolerant realization of a given logical circuit. Since quantum simulation is a key motivation and application of quantum computers, we pursue the goal of executing *Trotter circuits* fault-tolerantly with optimal depth [12], [13]. A Trotter circuit is also referred to as the *quantum simulation kernel* (*QSK*) [14], so we will use these terminologies interchangeably. An example QSK circuit for 3 qubits is shown in Fig. 1, where the *Z*-rotation angle  $\theta$  depends on the specifics of the simulation algorithm. For this work, we set  $\theta = \frac{\pi}{2}$  throughout, i.e., consider *Clifford* [15] QSK (C-QSK) circuits, to take the first steps towards the above goal. We develop a principled approach of deriving the physical realization of the logical C-QSK circuit on the well-known error-detecting family of  $[n, n - 2, 2]$  codes [16], [17]. The methods have the potential to generalize beyond this family, as we illuminate through a hypergraph product code, and also be amenable to optimization with respect to compilation constraints.

In prior work, we developed the *Logical Clifford Synthesis*

(LCS) algorithm [18]<sup>1</sup> that systematically constructs all physical Clifford circuits that realize a given logical Clifford circuit on any specified *stabilizer code* [16], [19]. The input logical Clifford circuit and stabilizer code are unrestricted, so the algorithm is very general. The LCS algorithm is computationally efficient because it leverages the  $2n \times 2n$  *binary symplectic matrix* representation of Clifford circuits [15], [20], rather than their  $2^n \times 2^n$  unitary matrix representation, and has complexity polynomial in  $n$ . Hence, this algorithm can be directly applied to obtain physical realizations of logical Clifford QSK circuits on the error-detecting code family. However, there are two key disadvantages of the LCS algorithm:

- 1) For an  $\llbracket n, k, d \rrbracket$  stabilizer code, the number of symplectic matrix solutions that realize a given logical Clifford circuit is  $2^{r(r+1)/2}$ , where  $r = n - k$ , ignoring stabilizer degrees of freedom. Hence, despite the computationally efficient nature of the algorithm, the search space grows super-exponentially in the dimension of the stabilizer group. For codes with constant rate [21]–[23], i.e.,  $k = \Theta(n)$ , the solution space is super-exponential in  $n$ . Currently, there is no known method to systematically obtain only “good” solutions from this space, although recent work has tailored solutions to the hardware [24].
- 2) The physical circuits output by the algorithm are neither necessarily fault-tolerant nor optimized for specific objectives such as depth or number of two-qubit gates. Guaranteeing fault-tolerance for a generic code while retaining the unitary nature of the solutions is hard. The linear algebraic approach of the algorithm does not enable one to track circuit properties, such as depth, through the steps of the algorithm.

Due to these drawbacks, we consider a *bottom-up* approach to synthesizing physical realizations of logical C-QSK circuits on the error-detecting code family. The key idea is to characterize the logical circuit via input-output Pauli tracking constraints (similar to the LCS algorithm), solve for separate small circuits to satisfy each of these constraints (the “solve” step), and then suitably merge these circuits to simultaneously satisfy all constraints (the “stitch” step), thereby realizing the logical circuit. We refer to this as the *solve-and-stitch* method. For this code family, we achieve fault-tolerance by adding flag gadgets [17] to the two-qubit gates in the solutions and proving that any single fault in the circuit remains detectable at the end. Most excitingly, by leveraging some properties of the code family, we prove that the depth of these fault-tolerant physical circuits only grows *linearly in the number of logical qubits*  $k$ . Since the logical QSK circuit itself has depth  $2k + 1$  (from  $2(k - 1)$  CNOTs, the  $Z$ -rotation, and two layers of single-qubit gates), the depth of these physical circuits is optimal. While  $k = n - 2$  for this family, which means that the depth is effectively linear in  $n$ , the proof involves calculations primarily in terms of the variable  $k$ . Therefore, the proof strategy has the potential to extend beyond this specific code family.

Overall, our results suggest that the error-detecting code family is indeed well-matched to efficiently realize logical C-QSK circuits fault-tolerantly. Obviously, the code doesn’t allow one to correct errors, so we will consider extending the solve-and-stitch approach to more non-trivial code families in future work. In such cases, decoders can also be tailored to these circuits since the error propagation has more structure.

The remainder of the paper is organized as follows. Section II provides necessary background to understand the details of this work. Section III explores transversal implementations of the logical C-QSK circuits and shows that this appears to be impossible using stabilizer codes. Section IV develops the solve-and-stitch method to physically realize logical C-QSK circuits on the error-detecting code family. Section V provides the depth analysis for the circuits produced in Section IV. Section VI provides several examples where the solve-and-stitch construction remains valid beyond the  $\llbracket n, n - 2, 2 \rrbracket$  code family. In particular, we highlight variations involving odd numbers of logical qubits, isolated logical gates, and a representative case on a hypergraph product code. Section VII designs flagged versions of the circuits from Section IV and establishes their fault-tolerance. Finally, Section VIII concludes the work and highlights opportunities for future work related to our results. Some additional details related to the results and further insights developed during this work are provided in the appendices.

## II. PRELIMINARIES

In Appendix I we review standard definitions related to the Pauli group, stabilizer codes, and the  $\llbracket n, n - 2, 2 \rrbracket$  code family.

### A. Quantum Simulation Kernel (QSK)

In quantum (Hamiltonian) simulation, a common strategy is to expand the Hamiltonian in the orthonormal basis of Hermitian Pauli operators  $E_j$  to write  $\mathbb{H} = \sum_j \alpha_j E_j$ , where  $\alpha_j \in \mathbb{R}$  [12]. The goal in simulation is to start with an initial state  $|\phi\rangle$  and compute the state at a future time instant  $t$  as  $|\phi(t)\rangle = \exp(-i\mathbb{H}t)|\phi\rangle$  (at least when  $\mathbb{H}$  is time-independent), where  $i := \sqrt{-1}$  and  $t \in \mathbb{R}$ . Since  $\{E_j\}$  may not mutually commute, one can leverage the *Trotter-Suzuki formula* [25] to approximate  $\exp(-i\mathbb{H}t)$  by repeated applications of  $\prod_j \exp(-i\alpha_j E_j t/T)$  for  $T$  (an integer) times. The circuit to implement such an exponentiated Pauli operator  $\exp(i\theta E)$  is called a *Trotter* circuit or a *quantum simulation kernel (QSK)* circuit. An example for 3 qubits is shown in Fig. 1, which corresponds to the case  $E_j = Z_1 X_2 Z_3$ . The structure generalizes for any  $k$ -qubit Pauli: start with single-qubit gates on those qubits that have a non- $Z$  component in  $E_j$  (Hadamard  $H$  for  $X$  or  $H_y := \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -i \\ i & 1 \end{bmatrix}$  for  $Y$ ), then perform CNOTs from the first  $(k - 1)$  qubits (control) to the  $k$ -th qubit (target), then perform a  $Z$ -rotation  $R_z(\theta)$  of the  $k$ -th qubit, and finally apply the gates before the rotation in the reverse order. The circuit depth is  $(2k + 1)$ , i.e., linear in  $k$ .

We only consider Clifford QSK (C-QSK) circuits, so we set  $\theta = \frac{\pi}{2}$  (i.e.,  $R_z(\theta) = P := \sqrt{Z}$ ). In this case the circuit is completely characterized by how it maps Pauli operators at its input to Pauli operators at its output using standard Pauli

<sup>1</sup>Implementations: <https://github.com/nrenga/symplectic-arxiv18a> (MATLAB), <https://github.com/AparnaGupta0301/Logical-Clifford-Synthesis> (Python)

conjugation relations for Clifford gates. For the  $k = 3$  circuit in Fig. 1, one can check the following input-output mappings:

$$\begin{aligned} X_1 &\mapsto Y_1 X_2 Z_3 , \quad Z_1 \mapsto Z_1 , \\ X_2 &\mapsto X_2 , \quad Z_2 \mapsto -Z_1 Y_2 Z_3 , \\ X_3 &\mapsto Z_1 X_2 Y_3 , \quad Z_3 \mapsto Z_3 . \end{aligned} \quad (1)$$

Hence, for any  $\llbracket n, k, d \rrbracket$  stabilizer code, the physical realization of the logical C-QSK circuit must satisfy the above relations for its  $k$  *logical* Pauli operators. Besides, the physical circuit must also preserve the stabilizer group  $\mathcal{S}$  under conjugation.

### B. Model for Circuit Depth

Throughout this work, we define *circuit depth* as the number of sequential layers of gates, where each layer may contain multiple gates acting on disjoint qubit subsets. In particular, each two-qubit gate contributes one unit of depth, and layers of single-qubit gates are either grouped into one depth unit if they act in parallel, or counted as separate units depending on gate structure. Our depth model is independent of hardware connectivity or scheduling constraints and thus reflects the logical circuit structure rather than physical layout. The primary goal is to analyze asymptotic scaling and structural optimizations in fault-tolerant circuit synthesis. Hardware-aware optimization, parallel gate scheduling, and mapping to physical architectures are beyond the scope of this work, but these may further improve our solutions.

## III. FAULT-TOLERANT QSK VIA TRANSVERSALITY

A natural fault-tolerant implementation of logical circuits is via a *transversal* physical operation, i.e., one that splits into a Kronecker product of single-qubit gates. Any fault in such a physical circuit does not propagate into other qubits. While the Eastin-Knill theorem [26] prevents an error-detecting stabilizer code from implementing a *universal* set of gates fault-tolerantly, there might exist a stabilizer code that realizes the specific logical C-QSK circuit transversally. In this section, we pursue this possibility and consider transversal  $H$  or  $P$  gates for implementing the logical C-QSK circuit.

**Theorem 1.** *There exists no stabilizer code where transversal Hadamard realizes the logical C-QSK circuit.*

*Proof:* See Appendix V-A for the proof. ■

**Theorem 2.** *There exists no stabilizer code where transversal Phase realizes the logical C-QSK circuit.*

*Proof:* See Appendix V-B for the proof. ■

In our proofs, we have refrained from specifying any particular code, leading us to the compelling conclusion that finding a stabilizer code capable of realizing the logical C-QSK circuits via transversal combinations of Hadamard and Phase gates *appears* inherently impossible. Note that this encompasses all transversal Clifford circuits since Hadamard and Phase gates generate the single-qubit Clifford group. Remarkably, based on the properties of C-QSK circuits, this conclusion can likely be extended to C-QSK circuits of arbitrary size and combinations of  $H$  and  $H_y$  gates. Our analysis suggests that leveraging stabilizer degrees of freedom

is unlikely to alter this conclusion. Of course, all this remains to be proven rigorously, hence we leave it as a conjecture.

**Conjecture 3.** *There exists no stabilizer code where transversal Clifford gates realize the logical C-QSK circuit for any non-trivial exponentiated Pauli operator.*

## IV. REALIZING C-QSK ON $\llbracket n, n-2, 2 \rrbracket$ CODE FAMILY

The discussion in Sec. III implies that transversal implementations of logical C-QSK circuits seem inherently impossible. Hence, we must incorporate two-qubit gates in the construction of physical circuits. This, however, raises a crucial question:

*Given specific input-output Pauli mapping rules dictated by the logical C-QSK circuit on a stabilizer code, what can we infer about the structure of the physical circuit satisfying these Pauli constraints, even without considering fault-tolerance?*

Our goal in this section is to address this question by developing a principled approach to circuit synthesis that allows us to track structural information during the synthesis. Naturally, such an approach provides a feasible solution that upper bounds depth, number of two-qubit gates etc.

The *Logical Clifford Synthesis (LCS)* algorithm [18] systematically synthesizes physical (Clifford) circuits satisfying Pauli constraints imposed by the logical (Clifford) circuit and code structure. This includes the constraints to ensure that the stabilizer group is preserved under conjugation by the physical Clifford circuit. The algorithm formulates the Pauli constraints as linear equations on a target binary symplectic matrix representing the desired physical Clifford circuit. Then it systematically solves for all feasible symplectic solutions by using symplectic transvections. Finally, it decomposes each solution into elementary Clifford gates. Despite its value, the LCS algorithm falls short of elucidating circuit properties and structure *during the construction of solutions*. This is because it directly finds the symplectic representation [15] of the circuit, which hides the circuit structure until it is decomposed into elementary gates. Therefore, one must determine all solutions before identifying the most desirable circuit. Unfortunately, since the number of solutions is  $2^{r(r+1)/2}$ , where  $r = n-k$ , the computational efficiency decreases super-exponentially with the dimension of the stabilizer group.

We circumvent these issues of the LCS algorithm by developing a *bottom-up* approach to synthesize physical circuits. The key idea is to “solve” for a small circuit satisfying one Pauli constraint by identifying a *root qubit*. Such a qubit is involved in both the input and output Pauli operator, but the Pauli acting on that qubit changes from input to output. Then these small circuits for different constraints are “stitched” together appropriately to satisfy all constraints simultaneously. By employing this approach for logical C-QSK circuits on  $\llbracket n, n-2, 2 \rrbracket$  codes, we can track circuit properties, such as depth, *during the construction of the circuit*. Notably, this method yields results comparable to the optimal circuits generated by LCS for this code family, *but without enumerating all solutions*. The following section illustrates such realization of logical C-QSK circuits under different scenarios.

### A. Circuit Synthesis via Solve-and-Stitch Approach

1) Even number of Hadamards for  $\llbracket 6, 4, 2 \rrbracket$  code: We introduced and described the procedure in detail in [1]. For completeness, we include it in Appendix III. In what follows, we will focus on the challenging cases of odd number of Hadamards and the presence of  $H_y$  gates, since these were not explained in [1].

2) Even number of Hadamards for  $\llbracket 8, 6, 2 \rrbracket$  code: See Appendix IV for details.

3) Odd number of Hadamards for  $\llbracket 6, 4, 2 \rrbracket$  code: In the case of logical C-QSK circuits with an odd number of Hadamard gates, we encounter some variations in the established pattern, necessitating the consideration of stabilizer effects during the physical circuit construction. While there are distinct differences, the fundamental idea of root qubits and the solve-and-stitch mechanism continues to prove valuable. In this example, we present the implementation of a 4-qubit C-QSK circuit with  $H$  applied to the first three qubits, as shown in Fig. 2.

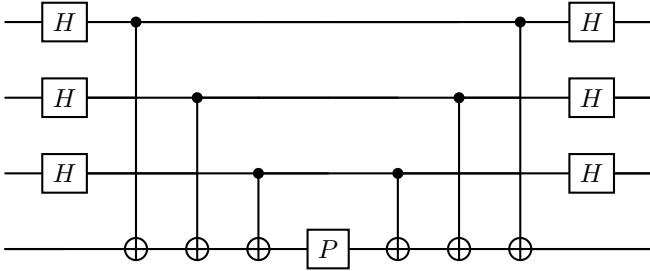


Fig. 2: C-QSK Circuit with odd number of Hadamard gates.

The mapping of each Pauli constraint is listed below:

$$\begin{aligned} X_1X_2 &\mapsto X_1X_2 & Z_2Z_6 &\mapsto -X_1Y_2X_3X_4Z_5, \\ X_1X_3 &\mapsto X_1X_3 & Z_3Z_6 &\mapsto -X_1X_2Y_3X_4Z_5, \\ X_1X_4 &\mapsto X_1X_4 & Z_4Z_6 &\mapsto -X_1X_2X_3Y_4Z_5, \\ X_1X_5 &\mapsto X_2X_3X_4Y_5Z_6 & Z_5Z_6 &\mapsto Z_5Z_6. \end{aligned} \quad (2)$$

In examining the logical- $X$  Pauli constraints, we observe that only the mapping of  $\overline{X_4}$  is non-trivial, necessitating the construction of only a single rooted circuit for the logical- $X$  component. For this particular Pauli constraint, we designate the fifth qubit as the root. Unlike the case of even number of Hadamards, observe that the output of this mapping results in the *disappearance* of  $X_1$ . To accommodate this, we first introduce  $\text{CNOT}_{5 \rightarrow 1}$  into the rooted circuit, as CNOT transforms  $XX$  to  $XI$ . For the remaining qubits, we once again apply CNOT or CZ gates based on the input-output Pauli relations. As always, we relocate the Phase gate to the end. Importantly, the mappings of  $\overline{X_1}$ ,  $\overline{X_2}$ , and  $\overline{X_3}$  in the logical- $X$  component are trivial and continue to be satisfied in the constructed rooted circuit, which is shown in Fig. 3.

In the logical- $Z$  components, the mappings of  $\overline{Z_1}$ ,  $\overline{Z_2}$ , and  $\overline{Z_3}$  are non-trivial. Notably, in each of these mappings, the gate  $X_1$  *emerges* while the gate  $Z_6$  *disappears* in the output configuration. To address this, first we designate the second, third, and fourth qubits as the root qubits, respectively. The disappearance of  $Z_6$  at the outputs introduces additional

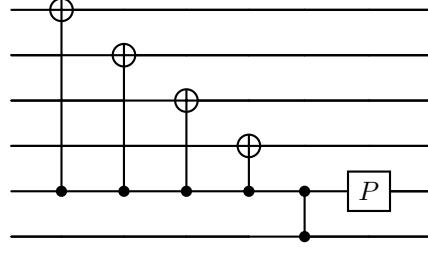
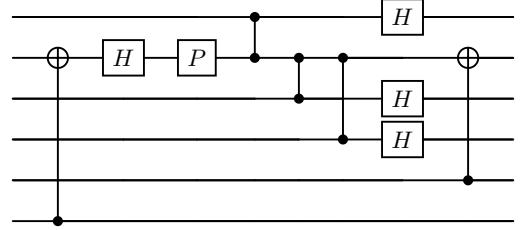
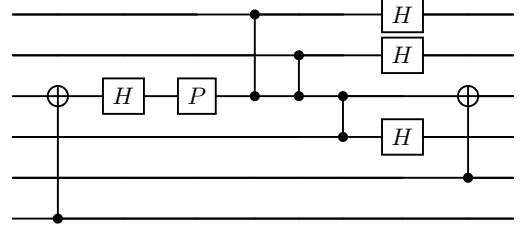


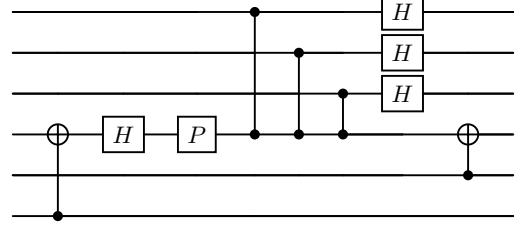
Fig. 3:  $X_1X_5 \mapsto X_2X_3X_4Y_5Z_6$



(a)  $Z_2Z_6 \mapsto X_1Y_2X_3X_4Z_5$  (ignoring sign)



(b)  $Z_3Z_6 \mapsto X_1X_2Y_3X_4Z_5$  (ignoring sign)



(c)  $Z_4Z_6 \mapsto X_1X_2X_3Y_4Z_5$  (ignoring sign)

Fig. 4: Rooted circuits for logical- $Z$  for odd number of Hadamards in C-QSK circuit on  $\llbracket 6, 4, 2 \rrbracket$  code.

processing in the rooted circuits. Therefore, in each rooted circuit shown in Fig. 4 we introduce CNOT gates at the beginning, specifically  $\text{CNOT}_{6 \rightarrow 2}$ ,  $\text{CNOT}_{6 \rightarrow 3}$ , and  $\text{CNOT}_{6 \rightarrow 4}$ , respectively. The designated root qubit serves as the target qubit for these additional CNOT gates because CNOTs transform  $ZZ$  into  $I\bar{Z}$ . Subsequently, these additional CNOT gates are followed by the  $H-P-\text{CZ}-H$  structure involving appropriate qubits. Observe that some CZ gates involve the first qubit due to the emergence of  $X_1$  in the output, a feature not observed in scenarios with an even number of Hadamard gates in the logical C-QSK circuit. To complete each rooted circuit, an additional CNOT gate is added at the end to produce  $Z_5$ , which is already present in the logical- $X$  rooted circuit.

The construction of the complete physical circuit in Fig. 5 closely mirrors the scenario with an even number of Hadamard gates on the logical circuit. The process involves stitch-

ing together individual rooted circuits, validating Pauli relations, and avoiding duplicated gates. Note that an additional Hadamard and Phase are introduced on the first qubit to retain  $X_1X_2$ ,  $X_1X_3$ , and  $X_1X_4$  unchanged. This also forms a symmetric  $H\text{-}P\text{-}CZ\text{-}H$  special structure on the first four qubits. However, while the logical constraints on the complete circuit are satisfied, the two stabilizers fail to be preserved.

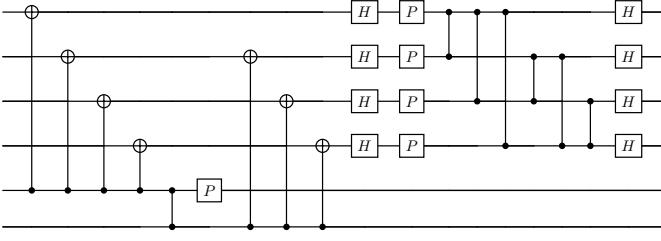


Fig. 5: Physical realization of Fig. 2 on the  $\llbracket 6, 4, 2 \rrbracket$  code produced by the solve-and-stitch approach using root qubits. But this does not preserve the two stabilizer generators.

To rectify this, additional gates  $P_6$  and  $\text{CNOT}_{6 \rightarrow 1}$  are incorporated into the circuit, which play a crucial role in preserving stabilizers without impacting the logical constraints on the full circuit. Together with  $H_1$  and  $P_1$ , these constitute non-trivial modifications not present in the rooted circuits.

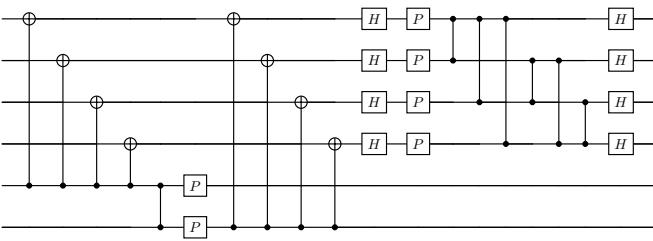


Fig. 6: Physical realization of Fig. 2 on the  $\llbracket 6, 4, 2 \rrbracket$  code produced by the solve-and-stitch approach using root qubits. Signs for  $\overline{Z}_i$  can be fixed with Pauli gates at the end.

4) *Mixed Hadamards and  $H_y$  gates on logical circuits:* We have already established the physical implementation of the Quantum Simulation Kernel (QSK) logical circuit for different parities of Hadamard gates positioned at the beginning and end of the circuit on the  $\llbracket n, n - 2, 2 \rrbracket$  code. This solve-and-stitch approach, however, is not limited to circuits with only Hadamard gates; it can also be extended to QSK circuits that incorporate a combination of Hadamard and  $H_y$  gates. The procedure begins by substituting all  $H_y$  gates with Hadamard gates in the QSK circuit and then applying Algorithm 1 to generate the corresponding physical circuit. Following this, specific modifications are made to the generated circuit to accommodate the varying parities of the Hadamard and  $H_y$  gates in the original QSK logical circuit. This ensures that all Pauli constraints are satisfied simultaneously, even when  $H_y$  gates are present. We illustrate this process using the simplest case—when both the number of Hadamard and  $H_y$  gates is even—as a representative example below.

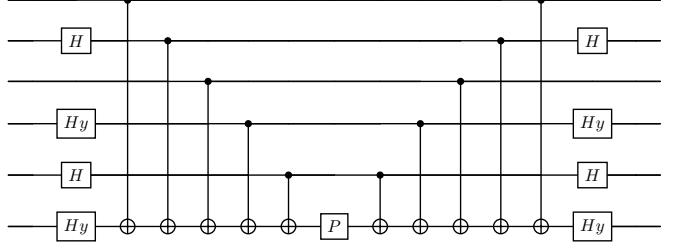


Fig. 7: C-QSK circuit with even number of Hadamard gates and even number of  $H_y$  gates.

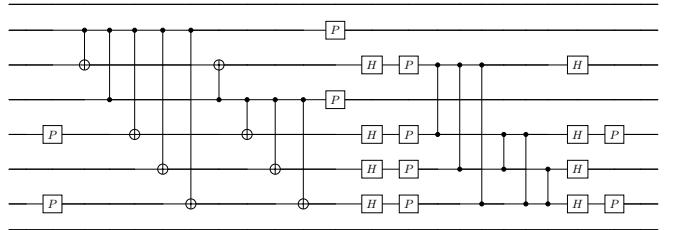


Fig. 8: Physical implementation of logical C-QSK circuit in Fig. 7.

The C-QSK circuit in Fig. 7 dictates the following input-output mappings of logical Pauli operators:

$$\begin{aligned} X_1 &\mapsto \overline{Y}_1 \overline{X}_2 \overline{Z}_3 \overline{Y}_4 \overline{X}_5 \overline{Y}_6 , & \overline{Z}_1 &\mapsto \overline{Z}_1 , \\ \overline{X}_2 &\mapsto \overline{X}_2 , & \overline{Z}_2 &\mapsto -\overline{Z}_1 \overline{Y}_2 \overline{Z}_3 \overline{Y}_4 \overline{X}_5 \overline{Y}_6 , \\ \overline{X}_3 &\mapsto \overline{Z}_1 \overline{X}_2 \overline{Y}_3 \overline{Y}_4 \overline{X}_5 \overline{Y}_6 , & \overline{Z}_3 &\mapsto \overline{Z}_3 , \\ \overline{X}_4 &\mapsto \overline{Z}_1 \overline{X}_2 \overline{Z}_3 \overline{Z}_4 \overline{X}_5 \overline{Y}_6 , & \overline{Z}_4 &\mapsto -\overline{Z}_1 \overline{X}_2 \overline{Z}_3 \overline{X}_4 \overline{X}_5 \overline{Y}_6 , \\ \overline{X}_5 &\mapsto \overline{X}_5 , & \overline{Z}_5 &\mapsto -\overline{Z}_1 \overline{X}_2 \overline{Z}_3 \overline{Y}_4 \overline{Y}_5 \overline{Y}_6 , \\ \overline{X}_6 &\mapsto -\overline{Z}_1 \overline{X}_2 \overline{Z}_3 \overline{Y}_4 \overline{X}_5 \overline{Z}_6 , & \overline{Z}_6 &\mapsto -\overline{Z}_1 \overline{X}_2 \overline{Z}_3 \overline{Y}_4 \overline{X}_5 \overline{X}_6 . \end{aligned}$$

Substituting for the logical operators of the  $\llbracket 8, 6, 2 \rrbracket$  code, we obtain the following mappings of physical Pauli operators:

$$\begin{aligned} X_1 X_2 &\mapsto X_1 Y_2 X_3 Z_4 Y_5 X_6 Y_7 , & Z_2 Z_8 &\mapsto Z_2 Z_8 , \\ X_1 X_3 &\mapsto X_1 X_3 , & Z_3 Z_8 &\mapsto Z_2 Y_3 Z_4 Y_5 X_6 Y_7 Z_8 , \\ X_1 X_4 &\mapsto X_1 Z_2 X_3 Y_4 Y_5 X_6 Y_7 , & Z_4 Z_8 &\mapsto Z_4 Z_8 , \\ X_1 X_5 &\mapsto X_1 Z_2 X_3 Z_4 Z_5 X_6 Y_7 , & Z_5 Z_8 &\mapsto Z_2 X_3 Z_4 X_5 X_6 Y_7 Z_8 , \\ X_1 X_6 &\mapsto X_1 X_6 , & Z_6 Z_8 &\mapsto Z_2 X_3 Z_4 Y_5 Y_6 Y_7 Z_8 , \\ X_1 X_7 &\mapsto X_1 Z_2 X_3 Z_4 Y_5 X_6 Z_7 , & Z_7 Z_8 &\mapsto Z_2 X_3 Z_4 Y_5 X_6 X_7 Z_8 . \end{aligned}$$

To obtain the physical circuit that satisfies all these Pauli constraints, replace the  $H_y$  gates with Hadamard gates in the logical circuit in Fig. 7, run Algorithm 1 to get the corresponding physical circuit, then add  $P_5$  and  $P_7$  at the beginning and at the end of this physical circuit. This new physical circuit is a valid solution and is shown in Fig. 8.

The remaining three parity combinations for  $H$  and  $H_y$  gates (even-odd, odd-even, odd-odd) are treated analogously using Algorithm 2, and their corresponding physical circuits are provided in Appendix VI. Although our depth analysis (in the next section) does not consider  $H_y$  gates for simplicity, this method highlights the versatility and robustness of the solve-and-stitch approach in constructing fault-tolerant quantum circuits under varying gate configurations.

### B. Solve-and-Stitch Approach on all $\llbracket n, n-2, 2 \rrbracket$ Codes

By delving into the constructions of physical circuits utilizing the root qubit idea in Sec. IV-A, we discerned both the similarities and differences in the patterns of these physical circuits. Our analysis indicates that these patterns are generalizable to all members of the  $\llbracket n, n-2, 2 \rrbracket$  family. We argue that the characteristics of these patterns stem from the inherent properties of the codes and the C-QSK circuits themselves. Hence, the solve-and-stitch algorithm constitutes a tailored design to realize C-QSK circuits on these codes.

In this section, we begin by establishing the logical Pauli mappings for C-QSK circuits with an arbitrary number of qubits. Note that a C-QSK circuit with odd number of qubits can be embedded into one with even number of qubits by introducing a qubit at the top which starts and ends in the  $|0\rangle$  state. Hence, we will restrict ourselves to C-QSK circuits with  $n-2$  qubits where  $n$  is even, as is necessary for the code family. Our results below will indicate the minimal overhead incurred by this assumption. Given the logical Pauli operators of the  $\llbracket n, n-2, 2 \rrbracket$  codes, we translate the logical Pauli mappings to physical Pauli constraints. Then we show that the stitching procedure always preserves all prior Pauli constraints. Finally, we provide the general algorithm to realize the logical C-QSK circuit on the  $\llbracket n, n-2, 2 \rrbracket$  code family.

Define the set  $[k] := \{1, 2, 3, \dots, k\}$ . Let  $i, j \in [k]$  index (logical) qubits of the C-QSK circuit. Let  $I_h \subseteq [k]$  be the index set of qubits where Hadamard gates appear in the C-QSK circuit. For Trotter circuits with  $H_y$  gates, let  $I_{hy}$  represent the index set of qubits where  $H_y$  gates appear in the QSK circuit. We also define  $I_e$  as the index set of qubits where neither Hadamard nor  $H_y$  gates are applied, i.e.,  $I_e = [k] \setminus (I_h \cup I_{hy})$ . It is worth mentioning that  $I_h$  and  $I_{hy}$  do not overlap, i.e.,  $I_h \cap I_{hy} = \emptyset$ . Unless otherwise specified, the following lemmas, theorems, corollaries, remarks pertain to the C-QSK circuit without  $H_y$  gates.

**Lemma 4.** *The logical Pauli mappings of the C-QSK circuit on  $k$  qubits can be expressed as follows:*

1) *If  $i \notin I_h$ , then*

$$\overline{X}_i \mapsto \overline{Y}_i \left( \prod_{j \in I_h} \overline{X}_j \right) \left( \prod_{j \in [k] \setminus (I_h \cup \{i\})} \overline{Z}_j \right), \quad (3)$$

$$\overline{Z}_i \mapsto \overline{Z}_i. \quad (4)$$

2) *If  $i \in I_h$ , then*

$$\overline{X}_i \mapsto \overline{X}_i, \quad (5)$$

$$\overline{Z}_i \mapsto -\overline{Y}_i \left( \prod_{j \in I_h \setminus \{i\}} \overline{X}_j \right) \left( \prod_{j \in [k] \setminus I_h} \overline{Z}_j \right). \quad (6)$$

*Proof:* See Appendix V-C for the proof.  $\blacksquare$

Let us now substitute for the logical Pauli operators in the above result. For the  $\llbracket n, n-2, 2 \rrbracket$  codes, logical Pauli operators are defined as  $\overline{X}_i = X_1 X_{i+1}$ ,  $\overline{Z}_i = Z_{i+1} Z_n$ , and

$$\overline{Y}_i = i \overline{X}_i \overline{Z}_i \quad (7)$$

$$= i X_1 X_{i+1} Z_{i+1} Z_n \quad (8)$$

$$= X_1 i (X_{i+1} Z_{i+1}) Z_n \quad (9)$$

$$= X_1 Y_{i+1} Z_n. \quad (10)$$

Given these physical operators, the physical Pauli mappings for logical C-QSK circuits on these codes are provided in Corollary 5 and Corollary 6, for the cases of even and odd number of Hadamards, respectively. The primary distinction lies in the parity of the number of elements in  $I_h$ , which governs the number of terms in the products in Lemma 4.

**Corollary 5.** *Any realization of the logical C-QSK circuit with even number of Hadamards on the  $\llbracket n, n-2, 2 \rrbracket$  codes must satisfy the following mappings of physical Pauli operators:*

1) *If  $i \notin I_h$ , then*

$$\begin{aligned} X_1 X_{i+1} \\ \mapsto X_1 Y_{i+1} \left( \prod_{j \in I_h} X_{j+1} \right) \left( \prod_{j \in [n-2] \setminus (I_h \cup \{i\})} Z_{j+1} \right), \end{aligned} \quad (11)$$

$$Z_{i+1} Z_n \mapsto Z_{i+1} Z_n. \quad (12)$$

2) *If  $i \in I_h$ , then*

$$X_1 X_{i+1} \mapsto X_1 X_{i+1}, \quad (13)$$

$$\begin{aligned} Z_{i+1} Z_n \\ \mapsto -Y_{i+1} \left( \prod_{j \in I_h \setminus \{i\}} X_{j+1} \right) \left( \prod_{j \in [n-2] \setminus I_h} Z_{j+1} \right) Z_n. \end{aligned} \quad (14)$$

**Corollary 6.** *Any realization of the logical C-QSK circuit with odd number of Hadamards on the  $\llbracket n, n-2, 2 \rrbracket$  codes must satisfy the following mappings of physical Pauli operators:*

1) *If  $i \notin I_h$ , then*

$$\begin{aligned} X_1 X_{i+1} \\ \mapsto Y_{i+1} \left( \prod_{j \in I_h} X_{j+1} \right) \left( \prod_{j \in [n-2] \setminus (I_h \cup \{i\})} Z_{j+1} \right) Z_n, \end{aligned} \quad (15)$$

$$Z_{i+1} Z_n \mapsto Z_{i+1} Z_n. \quad (16)$$

2) *If  $i \in I_h$ , then*

$$X_1 X_{i+1} \mapsto X_1 X_{i+1}, \quad (17)$$

$$\begin{aligned} Z_{i+1} Z_n \\ \mapsto -X_1 Y_{i+1} \left( \prod_{j \in I_h \setminus \{i\}} X_{j+1} \right) \left( \prod_{j \in [n-2] \setminus I_h} Z_{j+1} \right). \end{aligned} \quad (18)$$

From the above expressions, it is clear that for each mapping corresponding to  $\overline{X}_i$  or  $\overline{Z}_i$ , qubit  $i+1$  is always the root.

Armed with these general expressions for desired Pauli mappings, we can investigate the solve-and-stitch algorithm carefully. The “solve” phase of the algorithm solves for small rooted circuits, one for each mapping, by identifying root qubits. It is important to observe that each rooted circuit has controlled gates only with the root as the control (resp.

target) for logical- $X$  (resp. logical- $Z$ ) mappings. These are  $\text{CNOT}_{i+1 \rightarrow j+1}$  and  $\text{CZ}_{i+1,j+1}$ . Let us focus on the logical- $X$  mappings first and validate the stitching procedure.

**Lemma 7.** *The rooted circuits for logical- $X$  constraints in Lemma 4 can be stitched by concatenating them and dropping duplicate CZ gates. The stitched circuit satisfies all the logical- $X$  constraints simultaneously.*

*Proof:* See Appendix V-D for the proof.  $\blacksquare$

Next, consider the stitching of logical- $Z$  rooted circuits.

**Lemma 8.** *The rooted circuits for logical- $Z$  constraints in Lemma 4 can be stitched by concatenating them and dropping duplicate CZ gates. The stitched circuit satisfies all the logical- $Z$  constraints simultaneously.*

*Proof:* See Appendix V-E for the proof.  $\blacksquare$

**Remark 9.** *The  $\text{CNOT}_{j+1 \rightarrow i+1}$  gates to produce  $Z_{j+1}$  for  $j \notin I_h$  can as well be moved to the beginning of the rooted circuit for each logical- $Z$  constraint. In this case, the  $Z_{i+1}$  first produces  $Z_{i+1}Z_{j+1}$  before transforming itself to  $Y_{i+1}$ , which does not affect the arguments made above for stitching. Furthermore, these are identical to the CNOTs used for stitching logical- $X$  rooted circuits in Lemma 7.*

Now, we are ready to prove the main result of this section: the construction of the complete physical circuit for logical C-QSK on  $\llbracket n, n-2, 2 \rrbracket$  codes by stitching the logical- $X$  and logical- $Z$  stitched circuits, as shown in Fig. 9.

**Theorem 10.** *The logical C-QSK (i.e., Clifford Trotter) circuit can be realized on the  $\llbracket n, n-2, 2 \rrbracket$  codes by concatenating the logical- $X$  and logical- $Z$  stitched circuits from Lemmas 7 and 8, then dropping duplicate CNOT gates. If the number of Hadamards in the logical circuit is odd, then CNOTs and Phase gates can be added to preserve the stabilizer group.*

*Proof:* See Appendix V-F for the proof.  $\blacksquare$

**Remark 11.** *For a logical C-QSK circuit on the  $\llbracket n, n-2, 2 \rrbracket$  code that includes a combination of Hadamard and  $H_y$  gates, the physical construction closely resembles that of a Hadamard-only C-QSK circuit, with modifications depending on the parities of the Hadamard and  $H_y$  gates in the logical circuit; refer to Algorithm 2 for the complete procedure.*

## V. DEPTH ANALYSIS AND CIRCUIT OPTIMIZATION

In our endeavor of constructing physical circuits for realizing logical C-QSK circuits on the  $\llbracket n, n-2, 2 \rrbracket$  code family, we have successfully demonstrated the effectiveness of the idea of root qubits. However, a pertinent question arises: can we optimize the circuit to reduce the number of two-qubit gates and, consequently, minimize the circuit depth? In this section we show that this is indeed possible. First, we prove that the circuit depth grows *quadratically* with  $k$ , independent of the number of Hadamard gates in the logical circuit. To reduce the depth, we introduce a promising optimization strategy: the inclusion of “complementary” CZ gates, which together with  $P$  gates on all  $n$  qubits only realizes the logical identity on the code, thereby retaining the functionality of the physical

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**Algorithm 1** Solve-and-Stitch algorithm to realize logical C-QSK (i.e., Clifford Trotter) circuits on  $\llbracket n, n-2, 2 \rrbracket$  codes

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- 1: **Input:** Logical C-QSK circuit on an even number,  $k$ , of qubits implementing an exponentiated Pauli operator  $\exp(-i\frac{\pi}{4}E_1E_2 \cdots E_k)$ , where  $E_i \in \{X, Z\}$
  - 2: **Output:** Physical circuit on  $n = k + 2$  qubits efficiently realizing the logical C-QSK circuit on the  $\llbracket n, n-2, 2 \rrbracket$  code, as shown in Fig. 9 (optimizations from Cor. 14)
  - 3: **Initialization:**  $n := k + 2$ ,  $I_h := \{i \in [n-2] : E_i = X\}$
  - 4: **Initialization:** Set `logical_Hadamard_all` = 0
  - 5: **if**  $|I_h| > (n-2)/2$  **then**
  - 6:     Set `logical_Hadamard_all` = 1
  - 7:      $E_i \leftarrow HE_iH$ ;  $I_h \leftarrow I_h^c = [n-2] \setminus I_h$
  - 8:     Apply  $H_t$  for  $t \in [n]$ , SWAP qubits 1 and  $n$ 
    - ▷ This implements the logical Hadamard on all  $k = n - 2$  logical qubits, which will be repeated at the end of the circuit to retain the desired functionality
    - ▷ The sequence of gates below follows Fig. 9
  - 9:     Apply  $\text{CZ}_{i+1,j+1}$  gates for all pairs  $i, j \notin I_h$
  - 10:     Apply  $\text{CZ}_{s,t}, P_s$  gates for all pairs  $s, t \in [n]$  and cancel the CZ gates from above to reduce CZ count
  - 11:     ▷ These CZ and  $P$  gates together implement the logical identity on the code, so they do not affect functionality
  - 12:     ▷ Besides these cancellations, the complement in Line 7 greatly reduces the number of CZ gates in Line 25 too
  - 13:     **if**  $|I_h|$  is odd **then**
  - 14:         Apply  $\text{CZ}_{i+1,n}$  gates for  $i \notin I_h$
  - 15:         Apply  $P_{i+1}$  for each  $i \notin I_h$
  - 16:     **if**  $|I_h|$  is odd **then**
  - 17:         Apply  $P_n$            ▷ Sometimes  $P_n^\dagger$  may be appropriate
  - 18:         Apply  $\text{CNOT}_{i+1 \rightarrow j+1}$  for each  $i \notin I_h, j \in I_h$
  - 19:         **if**  $|I_h|$  is odd **then**
  - 20:             Apply  $\text{CNOT}_{i+1 \rightarrow 1}$  gates for  $i \notin I_h$
  - 21:             Apply  $\text{CNOT}_{n \rightarrow 1}$
  - 22:             Apply  $\text{CNOT}_{n \rightarrow i+1}$  gates for  $i \in I_h$
- 

circuits. This approach ensures that the circuit depth grows only *linearly* with  $k$ , which is optimal since the logical circuit itself has linear depth (see Section II-A).

Let  $h := |I_h|$  denote the number of Hadamard gates in the logical C-QSK circuit implementing  $\exp(-i\frac{\pi}{4}E_1E_2 \cdots E_k)$ , where  $E_i \in \{X, Z\}$ , i.e.,  $h = |\{i \in [n-2] : E_i = X\}|$ . We will use the sequence of gates in Fig. 9 for all arguments. The validity of this sequence to implement the logical C-QSK circuit has been established in Theorem 10. For all depth calculations, we assume that each two-qubit gate increases the depth by 1, even though this may not be the case for some hardware that can perform gates in a parallel fashion. A layer of identical single-qubit gates on multiple qubits is also considered depth-1. Hence, our expressions can safely be considered as upper bounds to the true depth in practice.

**Theorem 12.** *Consider the physical circuit constructed by the solve-and-stitch algorithm in Theorem 10 to realize a logical C-QSK circuit on the  $\llbracket n, n-2, 2 \rrbracket$  codes. The depth of this circuit is upper bounded by  $\frac{k(k-1)}{2} + 5$  when  $h$  is even and*

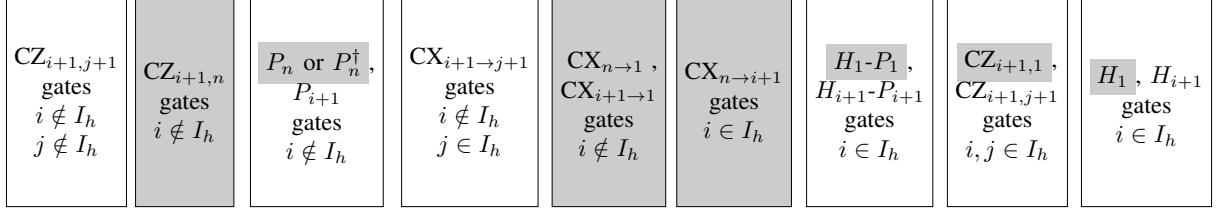


Fig. 9: The sequence of gates in the full physical circuit realizing the logical C-QSK (i.e., Clifford Trotter) circuit on the  $\llbracket n, n-2, 2 \rrbracket$  codes. The set  $I_h \subseteq [n-2]$  consists of the indices of logical qubits on which the logical circuit applies a Hadamard. The white blocks and non-highlighted gates are common to the cases of even and odd number of Hadamards, i.e.,  $|I_h|$ , but the gray blocks and the highlighted gates are needed only for the case of odd number of Hadamards. From Corollary 14, there are additional optimizations possible to reduce the gate count and circuit depth, which are described in Algorithm 1.

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23: Apply  $H_{i+1}$  followed by  $P_{i+1}$  for each  $i \in I_h$ 
24: if  $|I_h|$  is odd then
25:   Apply  $H_1$  followed by  $P_1$ 
26: Apply  $CZ_{i+1,j+1}$  gates for all pairs  $i, j \in I_h$ 
27: if  $|I_h|$  is odd then
28:   Apply  $CZ_{i+1,1}$  for each  $i \in I_h$ 
29: Apply  $H_{i+1}$  for each  $i \in I_h$ 
30: if  $|I_h|$  is odd then
31:   Apply  $H_1$ 
      ▷ This completes the sequence of gates from Fig. 9
32: Check for all the mappings in Corollary 5 ( $|I_h|$  even) or
   Corollary 6 ( $|I_h|$  odd)
33: if some signs in the mappings are not satisfied then
34:   Apply an appropriate Pauli operator to fix all the signs
      ▷ Such an operator can be found efficiently using
         the binary representation of Pauli operators, e.g., see [18]
35: if logical_Hadamard_all = 1 then
36:   Apply  $H_t$  for  $t \in [n]$ , SWAP qubits 1 and  $n$ 
37:   ▷ This complements the action of Line 8
38: Return: Physical circuit constructed by the procedure

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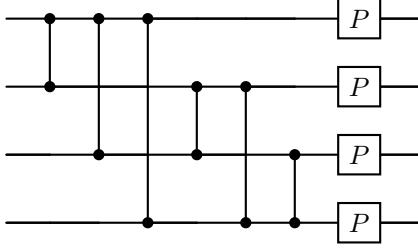


Fig. 10: Logical identity gadget for the  $\llbracket 4, 2, 2 \rrbracket$  code.

$\frac{(k+2)(k+1)}{2} + 5$  when  $h$  is odd, where  $k = n - 2$ .  
*Proof:* See Appendix V-G for the proof. ■

We have demonstrated that the depth of physical circuits grows quadratically with the dimension of the  $\llbracket n, n-2, 2 \rrbracket$  codes. To mitigate this, we propose the incorporation of “complementary” CZ gates at the beginning of the physical circuit. When combined with  $P$  gates on all  $n$  qubits, these CZ gates only implement the logical identity on the code,

**Algorithm 2** Solve-and-Stitch algorithm to realize logical C-QSK (i.e., Clifford Trotter) circuits with mixed Hadamard and  $H_y$  gates on  $\llbracket n, n-2, 2 \rrbracket$  codes

---

- 1: **Input:** Logical C-QSK circuit on an even number,  $k$ , of qubits implementing an exponentiated Pauli operator  $\exp(-i\frac{\pi}{4}E_1E_2\cdots E_k)$ , where  $E_i \in \{X, Y, Z\}$
- 2: **Output:** Physical circuit on  $n = k + 2$  qubits efficiently realizing the logical C-QSK circuit on the  $\llbracket n, n-2, 2 \rrbracket$  code
- 3: **Initialization:**  $n := k + 2$ ,  $I_h := \{i \in [n-2]: E_i = X\}$ ,  $I_{hy} := \{i \in [n-2]: E_i = Y\}$ ,  $I_e := \{i \in [n-2]: E_i = Z\}$
- 4: Replace all  $H_y$  gates into Hadamard gates, run Algorithm 1, generate physical circuit.
- 5: **if**  $|I_h|$  is even,  $|I_{hy}|$  is even **then**
  - 6: Apply  $P_{I_{hy}+1}$  at the beginning and the end of the physical circuit generated in Line 4.
- 7: **if**  $|I_h|$  is odd,  $|I_{hy}|$  is odd **then**
  - 8: Apply  $P_{I_{hy}+1}$  at the beginning and the end of the physical circuit generated in Line 4, then apply  $CZ_{n, I_e+1}$ ,  $CNOT_{n \rightarrow I_h+1}$ ,  $CNOT_{n \rightarrow I_{hy}+1}$ ,  $CZ_{n, I_{hy}+1}$  at the end.
- 9: **if**  $|I_h|$  is odd,  $|I_{hy}|$  is even **then**
  - 10: Apply  $CZ_{I_{hy}+1, I_e+1}$  at the beginning of the physical circuit generated in Line 4, then apply additional  $P_{I_{hy}+1}$  at the position of original Phase gates in the physical circuit from Line 4, and duplicate these Phase gates at the end of the circuit as well.
- 11: **if**  $|I_h|$  is even,  $|I_{hy}|$  is odd **then**
  - 12: Delete all CZ and P in logical-X component of the physical circuit generated in Line 4, then delete all gates involving in the last qubit, then apply  $CZ_{I_{hy}+1, I_e+1}$  at the beginning, then apply additional  $P_{I_{hy}+1}$  just before logical-Z component of the circuit, and duplicate these Phase gates at the end of the circuit as well.
- 13: Check for all the Pauli constraints
- 14: **if** some signs in the mappings are not satisfied **then**
  - 15: Apply an appropriate Pauli operator to fix all the signs
    - ▷ Such an operator can be found efficiently using the binary representation of Pauli operators, e.g., see [18]
- 16: **Return:** Physical circuit constructed by the procedure

---

thereby not affecting the logical functionality of the physical circuit. Figure 10 illustrates an example of this logical identity circuit for the  $\llbracket 4, 2, 2 \rrbracket$  code, which can be extended to any member of the  $\llbracket n, n - 2, 2 \rrbracket$  code family. Indeed, this CZ- $P$  gadget induces the mappings  $\overline{Z}_i = Z_{i+1}Z_n \mapsto Z_{i+1}Z_n$  and  $\overline{X}_i = X_1X_{i+1} \mapsto X_1X_{i+1}$ , which are trivial, indicating that all logical Pauli operators remain unchanged. It is easily checked that the stabilizers are also preserved.

Therefore, by implementing the logical identity at the beginning of the physical circuit in Fig. 9, we can cancel the CZ $_{i+1,n}$  gates for all  $i \notin I_h$ .

Importantly, the depth increase scales as  $\mathcal{O}(kh)$ , where  $k = n - 2$  is the number of logical qubits and  $h$  is the number of Hadamard gates in the logical Trotter circuit. In many physically motivated Hamiltonians, such as Ising or Heisenberg or Fermi-Hubbard models, the number of Hadamard gates is small compared to  $k$  and can be treated as a fixed constant. Consequently, the physical depth scales essentially linearly with  $k$ . Since the logical Clifford Trotter circuit itself has depth that grows linearly with  $k$ , we expect any reasonable fault-tolerant physical implementation to exhibit the same scaling trend. Thus, achieving a physical circuit depth of  $\mathcal{O}(k)$ —even with added gadgets for fault tolerance—can be considered optimal in scaling within this context. The following theorem provides expressions for the depth of the physical circuit incorporating these cancellations, asserting that the circuit’s depth grows only linearly with  $k$ , albeit quadratically with  $h$ .

**Theorem 13.** Consider the physical circuit constructed by the solve-and-stitch algorithm in Theorem 10 to realize a logical C-QSK circuit on the  $\llbracket n, n - 2, 2 \rrbracket$  codes. After integrating the logical identity into this circuit, the depth is at most

$$\begin{cases} (2 + 2h)k - h^2 - h + 6 & \text{for even } h, \\ (2 + 2h)k - h^2 + h + 7 & \text{for odd } h. \end{cases} \quad (19)$$

*Proof:* See Appendix V-H for the proof. ■

To illustrate the gains from the optimized circuits, in Fig. 11 we plot the relationship between  $k$  and the depth when  $h = 2$ . The depth of the optimized physical circuit is  $6k - 1$  in this illustration. Observe that for lower values of  $k$ , the original circuit from Fig. 9 has a smaller depth. However, when  $k \geq 14$ , the optimized circuit from Theorem 13 proves advantageous. It is also natural to consider the setting of fixed  $k$  and increasing  $h$ . Here, we can leverage the structure of the problem, specifically the exponentiated Pauli operator  $\exp(-i\frac{\pi}{4}E_1E_2 \cdots E_k)$ , where  $E_i \in \{X, Z\}$ . We realize that the operator can be sandwiched within transversal Hadamard gates on the  $k$  qubits to swap  $X$ s with  $Z$ s. Such a logical operation can be implemented on the code by performing physical transversal Hadamard gates and swapping qubits 1 and  $n$ . From Section I-B it is clear that this satisfies the necessary mappings on the logical Pauli operators and preserves the stabilizers. The operation itself adds depth 3, split into 2 at the beginning and 1 at the end of the sandwich, since Fig. 9 already contains a layer of Hadamards at the end. Intuitively, when  $h > k/2$ , we can use this strategy to fall back to the case of  $h < k/2$  and hence achieve a lower depth circuit. The following corollary establishes this rigorously.

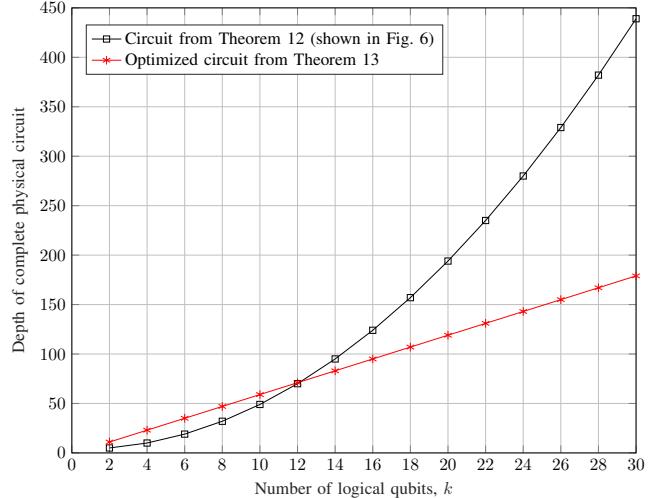


Fig. 11: Depth of original circuit from Theorem 12 and the optimized circuit from Theorem 13, where  $h = 2$  is fixed.

**Corollary 14.** When  $h > k/2$ , the logical C-QSK circuit can be realized on the  $\llbracket n, n - 2, 2 \rrbracket$  codes with depth at most

$$\begin{cases} k(k + 1) - h^2 + h + 9 & \text{for even } h, \\ k(k + 3) - h^2 - h + 10 & \text{for odd } h. \end{cases} \quad (20)$$

These are respectively smaller than the depths in Theorem 13.

*Proof:* See Appendix V-I for the proof. ■

Algorithm 1 carefully describes the complete procedure to synthesize Hadamard-only logical C-QSK circuits on the  $\llbracket n, n - 2, 2 \rrbracket$  codes, while Algorithm 2 describes the procedure to synthesize logical C-QSK circuits with mixed Hadamard and  $H_y$  gates on the  $\llbracket n, n - 2, 2 \rrbracket$  codes based on Algorithm 1. We emphasize that Algorithm 2 was not already introduced in [1].

**Remark 15.** Throughout our analysis, we have only considered logical C-QSK circuit on even number of qubits, since  $k = n - 2$  is even for the code family. To construct the logical circuit for odd number of qubits, one can transform this to the even setting as follows. Add a qubit at the top of the logical circuit, initialize it to  $|0\rangle$ , and perform CNOTs to the last qubit as always. The modification clearly doesn’t alter the functionality, but the resulting circuit has even number of qubits as necessary for our constructions. The depth overhead from this procedure is minimal in that it does not alter the linear scaling with  $k$ .

## VI. DISCUSSION ON SOLVE AND STITCH

We have systematically explored the construction of physical circuits for logical C-QSK circuits on  $\llbracket n, n - 2, 2 \rrbracket$  codes. However, it is essential to note that in certain cases, while the root qubit idea and the construction of rooted circuits still apply, some principles may vary. We contend that the root qubit idea could potentially lead to a further reduction in circuit depth compared to algorithms such as LCS, warranting further exploration and consideration. In this section, we briefly illustrate this under a few different settings.

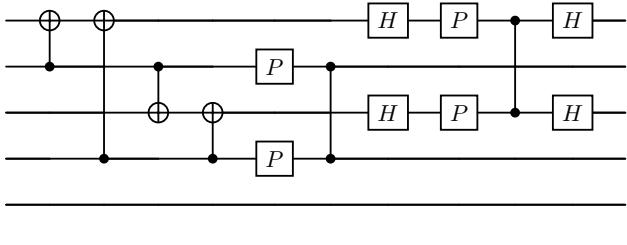


Fig. 12: Physical realization of Fig. 1 on the  $[6, 4, 2]$  code produced by the solve-and-stitch approach using root qubits.

#### A. Logical C-QSK Circuit on Odd Number of Qubits

Let us consider the 3-qubit logical C-QSK circuit in Fig. 1, which we will realize on the  $[6, 4, 2]$  code. In this context, we treat the fourth logical qubit as idle. The Pauli mapping rules in this scenario are listed below:

$$\begin{aligned} X_1X_2 &\mapsto Y_2X_3Z_4 , \quad Z_2Z_6 \mapsto Z_2Z_6 , \\ X_1X_3 &\mapsto X_1X_3 , \quad Z_3Z_6 \mapsto -X_1Z_2Y_3Z_4Z_6 , \\ X_1X_4 &\mapsto Z_2X_3Y_4 , \quad Z_4Z_6 \mapsto Z_4Z_6 , \\ X_1X_5 &\mapsto X_1X_5 , \quad Z_5Z_6 \mapsto Z_5Z_6 . \end{aligned} \quad (21)$$

For the construction of logical-X rooted circuits, the methodology is similar: selecting root qubits and avoiding the use of the same gates more than once when building the physical circuit. In contrast, for logical-Z, there is only one non-trivial rooted circuit, which reveals only half of the  $H$ - $P$ - $CZ$ - $H$  structure. However, as we construct the physical circuit, a complete and whole structure emerges, preserving the stabilizers (Fig. 12). This illustrates that even if certain patterns in the physical circuit don't explicitly appear in the rooted circuits, we can still construct the physical circuit based on previous knowledge about the circuit and the code.

#### B. Solve-and-Stitch for Single Logical Hadamard

In this example, we consider realizing a single logical Hadamard gate,  $\overline{H}_1$ , on the  $[6, 4, 2]$  code instead of an entire Trotter block. This highlights the generalizability of the solve-and-stitch approach beyond C-QSK circuits. The non-trivial physical Pauli mappings are listed below:

$$X_1X_2 \mapsto Z_2Z_6 , \quad Z_2Z_6 \mapsto X_1X_2 \quad (22)$$

Several circuits can satisfy the given Pauli constraints. In [17], they proposed the circuit in Fig. 13, which exhibits certain symmetric properties and has depth just 8. In contrast, the circuit generated by the LCS algorithm in Fig. 14 has depth 11 (assuming that the swap gate is physically implemented with a depth of 3). Notably, it lacks the symmetric structure and appears more complex than the circuit in Fig. 13. However, our root qubit idea proves effective and yields a simpler circuit with depth just 6, as shown in Fig. 16.

For the mapping  $X_1X_2 \mapsto Z_2Z_6$  in Fig. 15a, we choose the second qubit as the root. We first apply  $CZ_{2 \rightarrow 6}$  to transform  $X_2$  into  $Z_2Z_6$ , then implement  $CNOT_{2 \rightarrow 1}$  to transform  $X_1X_2$  into  $X_2$ , and finally apply a Hadamard on the second qubit to transform  $X_2$  into  $Z_2$ . For the mapping  $Z_2Z_6 \mapsto X_1X_2$ , we reverse this process, as shown in Fig. 15b.

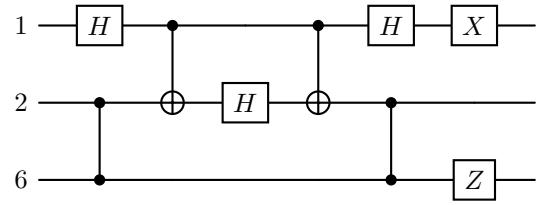


Fig. 13: Physical circuit proposed in [17] for realizing  $\overline{H}_1$ .

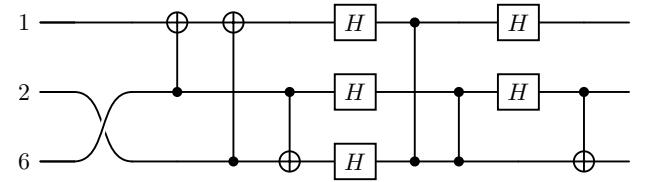
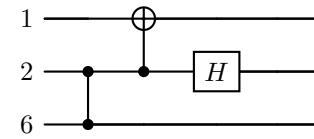


Fig. 14: Physical circuit from LCS algorithm [18] for  $\overline{H}_1$ .

In the construction of the physical circuit in Fig. 16, we leverage the symmetric property of Pauli mappings. We drop a Hadamard gate and seamlessly stitch the two rooted circuits together. This process is slightly different from other examples provided previously since  $CNOT_{2 \rightarrow 1}$  and  $CZ_{2 \rightarrow 6}$  appear twice in the physical circuit. Moreover, we add  $Z_1$  at the end to ensure that the stabilizers remain preserved exactly. The reduction in circuit depth emphasizes the efficacy of the root qubit idea in simplifying the physical circuit.



(a)  $X_1X_2 \mapsto Z_2Z_6$

Fig. 15: Rooted circuits for realizing  $\overline{H}_1$  on  $[6, 4, 2]$  code

#### C. Solve-and-Stitch on Hypergraph Product Code

To further illustrate the generalizability of the solve-and-stitch construction, we provide a concrete example using a  $[20, 4, 2]$  hypergraph product code. The logical Clifford Trotter circuit we consider corresponds to the structure depicted in Fig. 23, applied to four logical qubits.

The logical operators for this code are:

$$\begin{aligned} \bar{X}_1 &= X_1X_3, & \bar{Z}_1 &= Z_1Z_9, \\ \bar{X}_2 &= X_2X_4, & \bar{Z}_2 &= Z_2Z_{10}, \\ \bar{X}_3 &= X_5X_7, & \bar{Z}_3 &= Z_5Z_{13}, \\ \bar{X}_4 &= X_6X_8, & \bar{Z}_4 &= Z_6Z_{14}. \end{aligned} \quad (23)$$

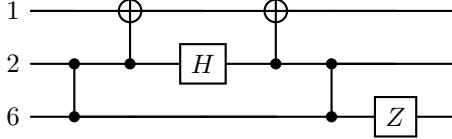


Fig. 16: Physical circuit from solve-and-stitch for  $\bar{H}_1$ .

The 16 stabilizers of the code are given by:

$$\begin{aligned}
 S_1 &= Z_1 Z_3 Z_{17}, & S_2 &= X_1 X_9 X_{17}, & S_3 &= Z_2 Z_4 Z_{18}, \\
 S_4 &= X_2 X_{10} X_{18}, & S_5 &= Z_5 Z_7 Z_{19}, & S_6 &= X_4 X_{12} X_{18}, \\
 S_7 &= Z_6 Z_8 Z_{20}, & S_8 &= X_4 X_{12} X_{18}, & S_9 &= Z_9 Z_{11} Z_{17}, \\
 S_{10} &= X_5 X_{13} X_{19}, & S_{11} &= Z_{10} Z_{12} Z_{18}, & S_{12} &= X_6 X_{14} X_{20}, \\
 S_{13} &= Z_{13} Z_{15} Z_{19}, & S_{14} &= X_7 X_{15} X_{19}, \\
 S_{15} &= Z_{14} Z_{16} Z_{20}, & S_{16} &= X_8 X_{16} X_{20}.
 \end{aligned} \tag{24}$$

Given these stabilizers and logical operators, we derive the physical circuit by solving the Pauli propagation constraints induced by the logical Trotter circuit. These constraints are expressed as follows:

$$\begin{aligned}
 X_1 X_3 &\mapsto Y_1 X_2 X_3 X_4 X_5 Z_6 X_7 Z_9 Z_{14}, \\
 Z_1 Z_9 &\mapsto Z_1 Z_9, \\
 X_2 X_4 &\mapsto X_2 X_4, \\
 Z_2 Z_{10} &\mapsto Z_1 Y_2 X_4 X_5 Z_6 X_7 Z_9 Z_{13} Z_{14}, \\
 X_5 X_7 &\mapsto X_5 X_7, \\
 Z_5 Z_{13} &\mapsto Z_1 X_2 X_4 Y_5 Z_6 X_7 Z_9 Z_{13} Z_{14}, \\
 X_6 X_8 &\mapsto Z_1 X_2 X_4 X_5 Y_6 X_7 X_8 Z_9 Z_{14}, \\
 Z_6 Z_{14} &\mapsto Z_6 Z_{14}.
 \end{aligned} \tag{25}$$

From the solution to these Pauli propagation constraints, we determine the root qubits for each logical gate gadget following the same procedure described in the main text. For the logical  $X$  component, we examine the first Pauli constraint and observe that  $X_1$  maps to  $Y_1$ ; among all outputs, qubit 1 is the only one with a  $Y$  term, which uniquely identifies it as a suitable root qubit. Similarly, for another non-trivial Pauli constraint, we select qubit 6 as the root qubit for the same reason. For the logical  $Z$  component, we choose qubits 2 and 5 as root qubits based on the corresponding propagation patterns. Using these root qubits, we construct the physical gadgets for each logical Clifford gate using the solve-and-stitch method. These small circuits are then combined to form the full physical circuit. To preserve the code stabilizers across the entire circuit, we append additional gates at the end of the circuit. The resulting physical circuit has depth 33 and preserves the modular block structure introduced by solve-and-stitch. An illustration of the complete circuit is shown in Fig. 17. This example demonstrates that the solve-and-stitch framework extends beyond the  $[n, n - 2, 2]$  family and applies to more general stabilizer codes such as hypergraph product codes. The process of propagating Pauli constraints and selecting root qubits remains consistent and modular, supporting the broader claim of generalizability.

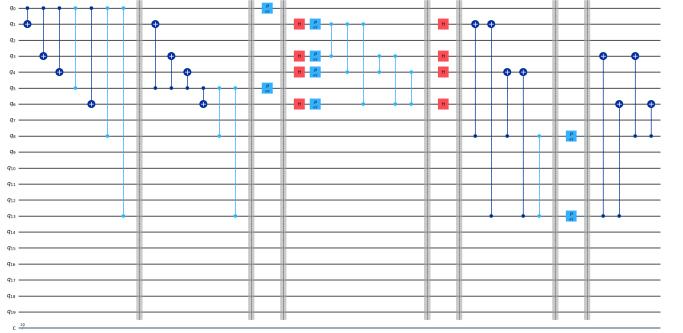


Fig. 17: Physical implementation of the four-qubit logical Clifford Trotter circuit in Fig. 23 on the  $[[20, 4, 2]]$  hypergraph product code using the solve-and-stitch framework. The circuit is constructed by stitching together physical gadgets derived from Pauli propagation constraints, based on root qubit selection as described in the main text. The final circuit includes additional layers at the end to preserve all stabilizers. Gray dashed lines indicate manually enforced ordering of gates in IBM Qiskit to follow the intended solve-and-stitch structure. These annotations override automatic gate reordering by the visualization tool, ensuring that the modular block pattern is preserved visually.

## VII. FAULT-TOLERANT QSK VIA FLAG QUBITS

The physical circuits constructed using the solve-and-stitch approach are not inherently fault-tolerant, as a single fault from a two-qubit gate can propagate to other qubits. However, by applying *flag gadgets* [17] to the physical circuits on the  $[[6, 4, 2]]$  code, we observe that two additional flag qubits make the circuit fault-tolerant, i.e., they enable the detection of correlated errors arising from a single fault in the circuit. Due to the distance-2 nature of the code, it is sufficient to show error detection for a single fault. We posit that a similar

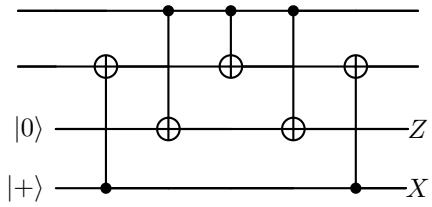


Fig. 18: Flag gadget on a CNOT to detect errors  $XI$ ,  $IZ$ ,  $XZ$ ,  $XX$ ,  $IZ$ ,  $XY$ ,  $YI$ ,  $YX$ ,  $ZZ$  from a single fault.

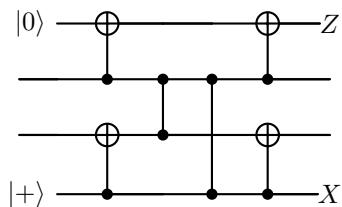


Fig. 19: Flag gadget on a CZ to detect errors  $XX$ ,  $YY$ ,  $ZZ$  from a single fault.

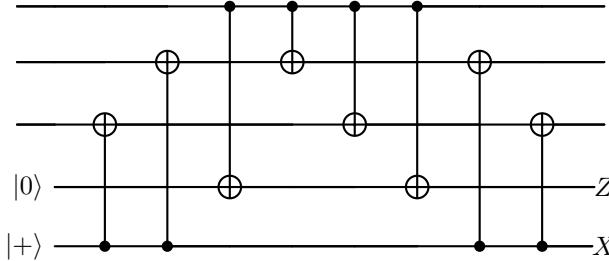


Fig. 20: Merged gadgets to catch errors arising from a single fault on multiple CNOT gates.

approach with flag qubits could be applied effectively to the  $\llbracket n, n - 2, 2 \rrbracket$  code family in general.

Table I provides a comprehensive list of output errors resulting from a single fault in two-qubit gates in Fig. 27. The “Location” in the first row denotes the position of the two-qubit gate in the quantum circuit, where “1” refers to the quantum wires at the circuit’s beginning. Each single-fault-induced error in the first row occurs at the output of the gates in the first column, where the left qubit is the control and the right qubit is the target. Such an error at the gate output results in an error at the circuit’s output, which is given as the corresponding cell entry. Output errors that commute with all stabilizers cannot be detected by syndrome measurements.

The undetectable errors caused by single faults, such as  $XI$ ,  $IZ$ ,  $XZ$  on  $\text{CNOT}_{2 \rightarrow 3}$  or  $XX$ ,  $IZ$ ,  $XY$  on  $\text{CNOT}_{2 \rightarrow 4}$  or  $YI$ ,  $XZ$ ,  $ZZ$  on  $\text{CNOT}_{5 \rightarrow 3}$  or  $YX$ ,  $XY$ ,  $ZZ$  on  $\text{CNOT}_{5 \rightarrow 4}$  are observed in Table I. To address potential undetectable errors, we employ flag gadgets for each two-qubit gate [17], necessitating the inclusion of two additional flag qubits. We introduce a gadget for each CNOT gate in Fig. 27. The gadget illustrated in Fig. 18 effectively captures all aforementioned faults. Additionally, errors such as  $XX$ ,  $YY$ ,  $ZZ$  on  $\text{CZ}_{25}$  and  $\text{CZ}_{34}$  can be detected using the gadget presented in Fig. 19. Incorporating these gadgets for each two-qubit gate in Fig. 27 results in a fault-tolerant circuit, where all errors arising from single faults can now be detected.

In fact, the gadgets can be merged to minimize the use of two-qubit gates on flag qubits, as shown in Figs. 20 and 21. By adjusting the positions of CNOT and CZ gates in Fig. 27, it is possible to group CNOT gates together and CZ gates together. The resulting circuit in Appendix II with merged gadgets achieves a fault-tolerant implementation of the logical C-QSK circuit. Crucially, this construction generalizes naturally to any member of the  $\llbracket n, n - 2, 2 \rrbracket$  family. Since the solve-and-stitch framework produces a modular and repetitive physical layout in Fig. 9, the same flag gadget templates for CNOT and CZ groups in Fig. 20 and Fig. 21 can be reused across larger codes. Therefore, combining solve-and-stitch with reusable flag gadgets yields a systematic, low-depth, and fault-tolerant realization of logical C-QSK circuits for arbitrary  $n$ . Hence, we conclude that the solve-and-stitch approach combined with flag gadgets enables a systematic, optimal-depth, fault-tolerant realization of logical C-QSK circuits on this code family.

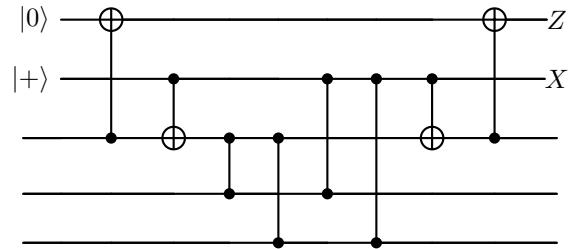


Fig. 21: Merged gadgets to catch errors arising from a single fault on multiple CZ gates.

## VIII. CONCLUSION AND FUTURE WORK

The general approach to fault-tolerance via quantum error correction is to design general-purpose codes and decoders and demonstrate fault-tolerant realizations of a universal set of logical gates on the codes. Then, in principle, any quantum algorithm on the logical qubits can be executed fault-tolerantly by composing these realizations appropriately. In this work, we were motivated by the fact that quantum computers are expected to show major advantages over classical computers only in specific algorithms and applications. Hence, we began to explore a new path where compilers for universal fault-tolerant quantum computers tailor the codes to execute a given target algorithm efficiently and fault-tolerantly. As an illustrative algorithm, we considered Trotter circuits for quantum simulation, which is a key application of quantum computers. We developed a systematic solve-and-stitch approach to synthesize optimal-depth realizations of Clifford Trotter circuits on the well-known  $\llbracket n, n - 2, 2 \rrbracket$  code family. We analyzed the approach rigorously and described the steps in Fig. 9 and Algorithm 1. We ensured fault-tolerance by embedding flag gadgets in the synthesized physical circuits. Furthermore, we discussed the potential for the approach to provide simplified circuits in a few different settings.

Obviously, this code family can only detect errors but not correct them. In future work, we will explore the generalization of the approach to better code families. We will leverage the insights developed in Theorem 10 to understand the code properties necessary to realize Clifford Trotter circuits efficiently and fault-tolerantly. This will bring us closer to truly tailoring code design for this application.

Naturally, we will investigate how these structured constructions can be used to design decoders that perform much better than structure-agnostic ones. We will also explore the extension to Trotter circuits with finer angle  $Z$ -rotations. Ultimately, we will determine the gains from the best tailored approaches and compare them with the surface code-based benchmarks for fault-tolerant quantum simulation [27].

It will also be very interesting to investigate the tailored realization of other quantum algorithms that are shown to provide a quantum advantage. In the near-term, variational quantum algorithms form one of the widely applicable use-cases of quantum computers [10], [11]. Hence, a fundamental understanding of the necessary code structure to efficiently implement error-corrected versions of these algorithms will

likely result in valuable practical gains. Instead of relying on long-term general purpose codes, this pursuit could identify small codes that still provide advantages in the near term. We anticipate that these explorations will lead to intriguing design problems for both classical and quantum coding theorists.

#### ACKNOWLEDGMENT

The work of N. R. was partially supported by the National Science Foundation under Grant no. 2106189. We thank Swayangprabha Shaw for help with IBM Qiskit and Fig. 17.

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APPENDIX I  
PRELIMINARIES (CONTINUED)

*A. Pauli Group and Stabilizer Codes*

For a single qubit, the Hermitian Pauli operators are denoted by  $I, X, Y, Z$ . For  $n \geq 1$  qubit(s), the *Pauli group* is given by

$$\mathcal{P}_n := \langle i^\kappa I, X, Y, Z ; \kappa \in \{0, 1, 2, 3\} \rangle^{\otimes n}. \quad (26)$$

We denote an  $n$ -qubit Hermitian Pauli operator as  $E(a, b)$ , where  $a, b \in \{0, 1\}^n$ . When  $a_i = 1$  (resp.  $b_i = 1$ ), the  $X$  (resp.  $Z$ ) gate is applied to qubit  $i$ , and when  $a_i = b_i = 1$ , the  $Y$  gate is applied to qubit  $i$ , where  $i \in \{1, 2, \dots, n\}$ . For example, for  $n = 3$ ,  $E([101, 011]) = X \otimes Z \otimes Y$ . The *weight* of a Pauli operator is the number of non-identity elements in its Kronecker product, e.g.,  $X \otimes Z \otimes Y$  has weight 3.

Any pair of single-qubit non-identity Pauli operators anti-commute, e.g.,  $XZ = -ZX$ . For multiple qubits, since the Kronecker product satisfies the property  $(A \otimes B)(C \otimes D) = (AC) \otimes (BD)$ , two non-identity Pauli operators can commute, e.g.,  $X \otimes X$  and  $Z \otimes Z$ . We will represent such operators using qubit subscripts for convenience, e.g.,  $E_1 E'_2 \equiv E \otimes E'$  for  $E, E' \in \{I, X, Y, Z\}$ . On  $n$  qubits, this means  $E_i \equiv I_1 I_2 \cdots I_{i-1} E_i I_{i+1} \cdots I_n = I \otimes \cdots \otimes I \otimes E \otimes I \otimes \cdots \otimes I$ .

Let  $N := 2^n$  for an  $n$ -qubit system. A *stabilizer group*,  $\mathcal{S}$ , is a group generated by commuting Hermitian Pauli operators such that  $-I_N \notin \mathcal{S}$ . The associated *stabilizer code*,  $\mathcal{Q}_{\mathcal{S}}$ , is the subspace of unit vectors in  $\mathbb{C}^N$  that are the common +1-eigenvectors of operators in  $\mathcal{S}$ . In other words, each  $|\psi\rangle \in \mathcal{Q}_{\mathcal{S}}$  satisfies  $S|\psi\rangle = |\psi\rangle$  for all  $S \in \mathcal{S}$ . The *logical Pauli operators* of a code are Hermitian Pauli operators that commute with the stabilizers but are not stabilizers themselves. If  $\mathcal{S}$  has  $r = n-k$  independent generators and the minimum weight of any logical Pauli operator is  $d$ , then the code is an  $[[n, k, d]]$  code. Such a code encodes  $k$  logical qubits into  $n$  physical qubits. It can detect up to  $(d-1)$  Pauli errors but can correct only up to  $\lfloor \frac{d-1}{2} \rfloor$  Pauli errors using a maximum-likelihood decoder. A CSS code is a stabilizer code whose stabilizer group can be generated by purely  $X$ -type and purely  $Z$ -type operators.

*B. The  $[[n, n-2, 2]]$  Code Family*

This is a family of CSS codes with exactly two stabilizer generators,  $X_1 X_2 \cdots X_n$  and  $Z_1 Z_2 \cdots Z_n$ , where  $n$  is set to be even [16], [17]. It is easily checked that these generators commute. The generators of logical- $X$  and  $Z$  operators are of the form  $\overline{X}_i = X_1 X_{i+1}$  and  $\overline{Z}_i = Z_{i+1} Z_n$ , where  $i = 1, 2, \dots, n-2$ . Hence, the distance of the codes in this family is always 2. The family is only error-detecting because it can detect up to 1 error but cannot correct any errors. As an example, for  $n = 6$ , the  $[[6, 4, 2]]$  is described by the stabilizer group  $\mathcal{S} = \langle X_1 \cdots X_6, Z_1 \cdots Z_6 \rangle$  and the following generators of the logical Pauli group:

$$\begin{aligned} \overline{X}_1 &= X_1 X_2, \quad \overline{Z}_1 = Z_2 Z_6; \\ \overline{X}_2 &= X_1 X_3, \quad \overline{Z}_2 = Z_3 Z_6; \\ \overline{X}_3 &= X_1 X_4, \quad \overline{Z}_3 = Z_4 Z_6; \\ \overline{X}_4 &= X_1 X_5, \quad \overline{Z}_4 = Z_5 Z_6. \end{aligned} \quad (27)$$

We will use this code as the running example but the results apply to the entire code family.

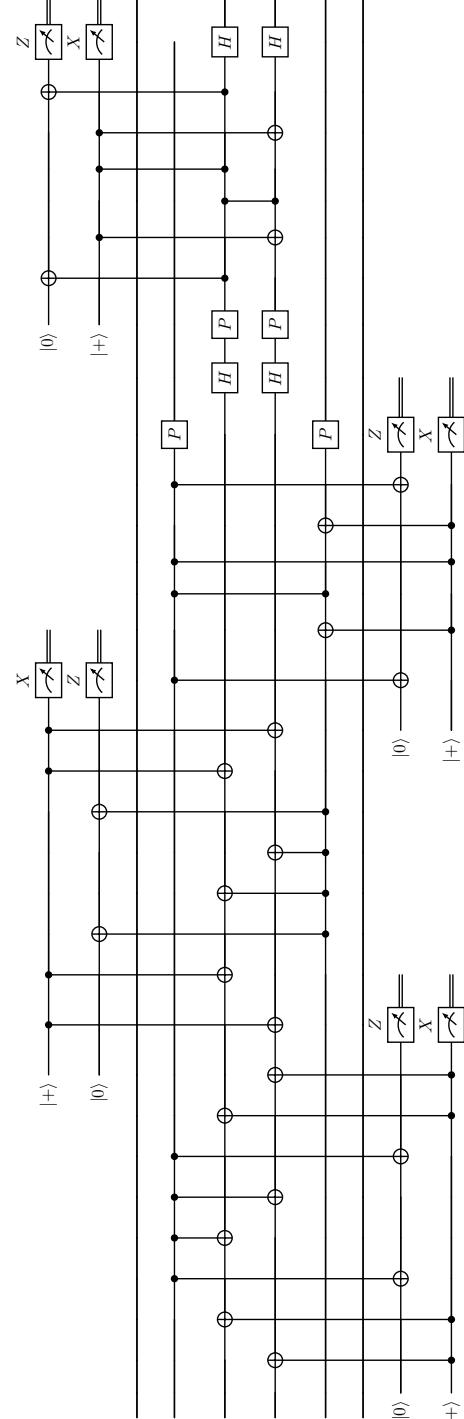


Fig. 22: Fault-tolerant execution of the physical circuit in Fig. 27 by embedding flag gadgets.

APPENDIX II  
FAULT TOLERANT LOGICAL C-QSK ON THE  $[[6, 4, 2]]$  CODE

Table I shows the errors at the output of Fig. 27 resulting from a single fault at the output of a two-qubit gate. Fig. 22 shows the fault-tolerant execution of the physical circuit in Fig. 27 by embedding flag gadgets.

TABLE I: Errors at the output of Fig. 27 resulting from a single fault at the output of a two-qubit gate.

	Location	$IY$	$IX$	$IY$	$IY$	$XY$	$XY$	$XZ$	$XZ$	$YI$	$YI$	$YY$	$YY$	$YZ$	$YZ$	$ZI$	$ZI$	$ZX$	$ZX$	$ZY$	$ZY$	$ZZ$	$ZZ$		
$ CNOT_{2 \rightarrow 3} $	2	$X_3$	$Z_3 X_4 Z_5$	$-Y_3 X_4 Z_5$	$Y_2 X_3 X_4 Z_5$	$Y_2 Z_3$	$-Y_2 Y_3$	$-X_2 X_3 X_4 Z_5$	$-X_2 X_3 X_4 Z_5$	$-X_2 Z_3$	$-X_2 Z_3$	$X_2 Y_3$	$X_2 Y_3$	$Z_2 Z_3 X_4 Z_5$	$Z_2 Z_3 X_4 Z_5$	$Z_2 Z_3 X_5$	$Z_2 Z_3 X_5$	$Z_2 Z_3 X_5$	$Z_2 Z_3 X_5$	$Z_2 Z_3 X_5$	$Z_2 Z_3 X_5$	$-Z_2 Y_3 X_4 Z_5$	$-Z_2 Y_3 X_4 Z_5$		
$ CNOT_{2 \rightarrow 4} $	3	$X_4$	$X_3$	$Z_3 Z_4 Z_5$	$-X_3 Y_4 Z_5$	$Y_2 Z_5$	$Y_2 X_4 Z_5$	$Y_2 X_5 Z_4$	$-Y_2 X_5 Y_4$	$-X_2 Z_5$	$-X_2 Z_5$	$X_2 X_3 Z_4$	$X_2 X_3 Z_4$	$Z_2 X_3 X_4 X_5$	$Z_2 X_3 X_4 X_5$	$Z_2 X_3 Y_4 X_6$	$Z_2 X_3 Y_4 X_6$	$Z_2 X_3 Y_5$	$Z_2 X_3 Y_5$	$Z_2 X_3 Z_5$	$Z_2 X_3 Z_5$	$-Z_2 X_3 Y_4 X_6$	$-Z_2 X_3 Y_4 X_6$	$Z_2 Z_4 Z_5$	$Z_2 Z_4 Z_5$
$ CZ_{2 \rightarrow 5} $	4	$X_5$	$X_4$	$X_3 X_4 Y_5$	$-X_3 X_4 X_5$	$Z_5$	$Y_2$	$Y_2 X_3 X_4 Y_5$	$-Y_2 X_3 X_4 X_5$	$Y_2 Z_5$	$-X_2$	$-X_2 X_3 X_4 Y_5$	$-X_2 X_3 X_4 X_5$	$X_2 X_3 Y_4 X_6$	$X_2 X_3 Y_4 X_6$	$-X_2 Z_5$	$-X_2 Z_5$	$Z_2 X_3 Y_4 Z_6$	$Z_2 X_3 Y_4 Z_6$	$Z_2 X_4 Z_5$	$Z_2 X_4 Z_5$	$-Y_2 X_3 Y_4 Z_6$	$-Y_2 X_3 Y_4 Z_6$	$Z_2 Z_4 Z_5$	$Z_2 Z_4 Z_5$
$ CNOT_{5 \rightarrow 3} $	5	$X_3$	$X_4$	$Z_3 X_4$	$-Y_3 X_4$	$X_5 Y_6$	$X_5 Y_6$	$X_3 X_4 Y_6$	$-X_3 X_4 Y_6$	$Z_3 Y_5$	$-Y_3 Y_6$	$-X_3 X_4 Z_5$	$-X_3 X_4 Z_5$	$-Z_3 X_5$	$-Z_3 X_5$	$Y_3 X_5$	$Y_3 X_5$	$Z_3 Z_5$	$Z_3 Z_5$	$Z_3 Z_5$	$Z_3 Z_5$	$Z_3 Z_5$	$Z_3 Z_5$	$-X_3 Y_4 Z_5$	$-X_3 Y_4 Z_5$
$ CNOT_{5 \rightarrow 4} $	6	$X_4$	$X_3$	$X_3 Z_4$	$-X_3 Y_4$	$Y_6$	$X_1 Y_6$	$X_1 Y_6$	$-X_1 Y_4 Y_5$	$-X_5$	$-Y_5$	$-X_1 Y_4 Y_5$	$-X_1 Y_4 Y_5$	$-X_5 Z_4$	$-X_5 Z_4$	$X_3 Z_4$	$X_3 Z_4$	$X_4 Z_5$	$X_4 Z_5$	$X_4 Z_5$	$X_4 Z_5$	$X_3 Z_4$	$X_3 Z_4$	$-X_3 X_4$	$-X_3 X_4$
$ CZ_{3 \rightarrow 4} $	10	$Z_4$	$Z_4$	$-Z_4$	$-Z_4$	$X_1$	$Z_3$	$Z_3$	$Z_3 Z_4$	$Z_3 Z_4$	$-Z_3 Y_4$	$-Z_3 Y_4$	$-Y_3$	$-Y_3$	$-Y_3 Z_4$	$-Y_3 Z_4$	$Y_4$	$Y_4$	$-Y_3 X_4$	$-Y_3 X_4$	$X_3$	$X_3$	$-X_3 Z_4$	$-X_3 Z_4$	

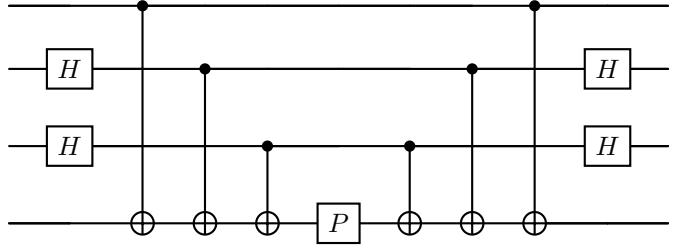


Fig. 23: C-QSK circuit with even number of Hadamard gates.

### APPENDIX III EVEN NUMBER OF HADAMARDS FOR $\llbracket 6, 4, 2 \rrbracket$ CODE

For our first scenario, we assume that the logical C-QSK circuit consists of an even number of Hadamard gates. The  $\llbracket 6, 4, 2 \rrbracket$  code serves as an excellent testbed for our exploration, in which case the logical circuit comprises 4 qubits. As an example, consider the circuit in Fig. 23, where the Hadamard gates are applied to the second and third qubits. The circuit implements the exponentiated Pauli operator  $\exp(-i\frac{\pi}{4}Z_1 X_2 X_3 Z_4)$ . A similar approach applies for Pauli operators with  $Y$  entries, where  $H$  gates are replaced with  $H_y$  gates (see Section II-A).

This C-QSK circuit dictates the following input-output mappings of logical Pauli operators:

$$\begin{aligned} \overline{X_1} &\mapsto \overline{Y_1} \overline{X_2} \overline{X_3} \overline{Z_4} , & \overline{Z_1} &\mapsto \overline{Z_1} , \\ \overline{X_2} &\mapsto \overline{X_2} , & \overline{Z_2} &\mapsto -\overline{Z_1} \overline{Y_2} \overline{X_3} \overline{Z_4} , \\ \overline{X_3} &\mapsto \overline{X_3} , & \overline{Z_3} &\mapsto -\overline{Z_1} \overline{X_2} \overline{Y_3} \overline{Z_4} , \\ \overline{X_4} &\mapsto \overline{Z_1} \overline{X_2} \overline{X_3} \overline{Y_4} , & \overline{Z_4} &\mapsto \overline{Z_4} . \end{aligned} \quad (28)$$

Substituting for the logical operators of the  $\llbracket 6, 4, 2 \rrbracket$  code, we obtain the following mappings of physical Pauli operators:

$$\begin{aligned} X_1 X_2 &\mapsto X_1 Y_2 X_3 X_4 Z_5 , & Z_2 Z_6 &\mapsto Z_2 Z_6 , \\ X_1 X_3 &\mapsto X_1 X_3 , & Z_3 Z_6 &\mapsto -Z_2 Y_3 X_4 Z_5 Z_6 , \\ X_1 X_4 &\mapsto X_1 X_4 , & Z_4 Z_6 &\mapsto -Z_2 X_3 Y_4 Z_5 Z_6 , \\ X_1 X_5 &\mapsto X_1 Z_2 X_3 X_4 Y_5 , & Z_5 Z_6 &\mapsto Z_5 Z_6 . \end{aligned} \quad (29)$$

Additionally, we require that the two stabilizer generators  $X_1 \cdots X_6$  and  $Z_1 \cdots Z_6$  are mapped to themselves, even though it is sufficient to map them to a pair of equivalent stabilizers, i.e., normalize the stabilizer group. The minimum depth solution produced by the LCS algorithm for this case is shown below in Fig. 24. This physical circuit satisfies all stipulated Pauli constraints above while preserving stabilizers. Observe that the (naïve) depth of this circuit is 10, which is comparable to the depth of the logical circuit in Fig. 23.

For the  $\llbracket n, n-2, 2 \rrbracket$  code family, we have  $r = n-k = 2$ , so the number of symplectic solutions (for a fixed set of Pauli constraints) is only  $2^{r(r+1)/2} = 8$ . Hence, it is easy to enumerate the solutions and identify the minimum depth circuit. However, this becomes impractical even for  $r=6$ . Besides, the LCS algorithm does not enable us to predict the minimum depth until we obtain all solutions and decompose each of them into elementary Clifford gates as in Fig. 24.

To address these limitations, we propose an alternative method for constructing physical circuits by identifying a *root*

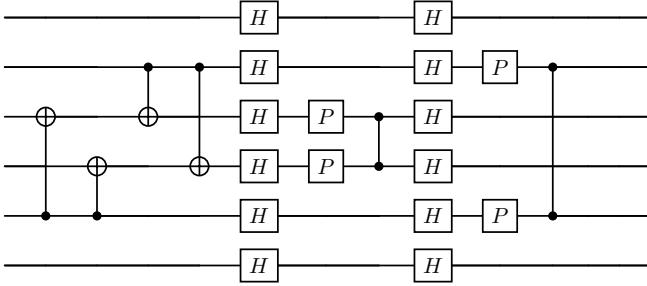


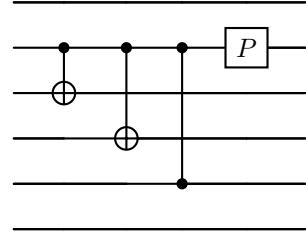
Fig. 24: The minimum depth solution of LCS algorithm for realizing the logical circuit in Fig. 23 on the  $[6, 4, 2]$  code. Note that the algorithm does not perform circuit simplification.

qubit for each (physical) Pauli constraint. For a non-trivial constraint, we identify qubits that appear in both the input and output, and then eliminate the qubits with an unchanged Pauli gate. From the remaining root qubits, we choose one as the root. For instance, consider the mapping of  $X_1X_2$  to  $X_1Y_2X_3X_4Z_5$ . In this case, we choose the second qubit as the root rather than the first qubit because  $X_1$  remains unchanged, requiring no additional gates in the circuit. For (non-root) qubits that are absent in the input Pauli but present in the output of the constraint, we introduce two-qubit gates controlled by the root qubit because single-qubit gates like  $H$  and  $P$  cannot affect the Pauli on other qubits.

Specifically, for the above example, since CNOT gate maps  $XI$  to  $XX$ , we apply  $\text{CNOT}_{2 \rightarrow 3}$  and  $\text{CNOT}_{2 \rightarrow 4}$  for the third and fourth qubits with the second qubit as the root (control). Since the CZ gate maps  $XI$  to  $XZ$ , we apply  $\text{CZ}_{25}$  for the fifth qubit to satisfy its mapping. The output term of the second qubit is a  $Y$  gate, so we directly introduce a Phase gate to achieve the desired mapping at the end. This “local” circuit construction is illustrated in Fig. 25a.

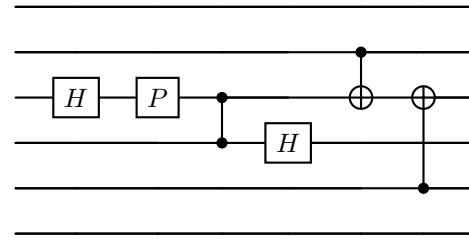
For mappings involving  $\overline{X}_2$  and  $\overline{X}_3$ , where the input gates are the same as the output gates, we have verified that these mappings remain unchanged as the gates propagate through the above rooted circuit we constructed. Consequently, there is no need to construct new rooted circuits for these trivial mappings. Additionally, for the Pauli constraint of  $\overline{X}_4$ , we choose the fifth qubit as the root and apply CNOT or CZ gates to other qubits based on the input-output Pauli relations. A Phase gate is then applied to the root qubit to complete the rooted circuit in Fig. 25b for mapping  $X_1X_5$  to  $X_1Z_2X_3X_4Y_5$ .

For the mappings corresponding to the logical- $Z$  constraints, the construction of rooted circuits has some variations. For example, consider the mapping  $Z_3Z_6 \mapsto Z_2Y_3X_4Z_5Z_6$ . Here, just as before, we designate the third qubit as the root rather than the sixth qubit because  $Z_6$  remains unchanged. However, unlike the logical- $X$  constraints, where the root’s mapping is processed at the end, here we process this qubit at the beginning. To transform  $Z_3$  to  $Y_3$  in the output, we apply  $H$  followed by  $P$  on the third qubit. Next, we observe that the output of the fourth qubit is  $X_4$ . While it might seem intuitive to apply  $\text{CNOT}_{3 \rightarrow 4}$ , which maps  $Y_3I_4$  to  $Y_3Z_4$ , we realize that the constraint  $Z_4Z_6 \mapsto Z_2X_3Y_4Z_5Z_6$  would later

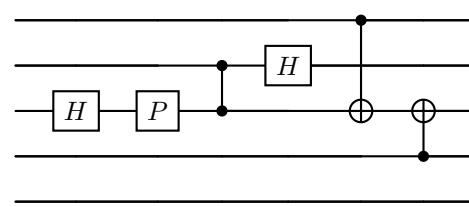


(a)  $X_1X_2 \mapsto X_1Y_2X_3X_4Z_5$

Fig. 25: Rooted circuit construction for logical- $X$  constraints.



(a)  $Z_3Z_6 \mapsto Z_2Y_3X_4Z_5Z_6$  (ignoring sign)



(b)  $Z_4Z_6 \mapsto Z_2X_3Y_4Z_5Z_6$  (ignoring sign)

Fig. 26: Rooted circuit construction for logical- $Z$  constraints.

require a reversed CNOT, i.e.,  $\text{CNOT}_{4 \rightarrow 3}$ . Since the CNOT is not symmetric with respect to swapping the control and target qubits, we apply a CZ gate on the third and fourth qubits instead, followed by  $H$  on these qubits. Subsequently, we apply CNOTs for qubits 2 and 5, with the root qubit as the target and themselves as controls. Finally, as for the logical- $X$  constraints, we verify that these rooted circuits satisfy the trivial mappings of  $\overline{Z}_1$  and  $\overline{Z}_4$  as well. The final rooted circuits for logical- $Z$  constraints are illustrated in Figs. 26a and 26b.

To consolidate the rooted circuits satisfying individual Pauli constraints into a comprehensive physical circuit that simultaneously meets all constraints, we follow a systematic “stitching” approach, initially addressing logical- $X$ s and subsequently logical- $Z$ s. We begin with the rooted circuit for  $\overline{X}_1$ , which we have verified adheres to the trivial mappings of  $\overline{X}_2$  and  $\overline{X}_3$ . Subsequently, we seamlessly append the rooted circuit for  $\overline{X}_4$  at the end. During this process, we ensure smooth integration of shared gates; for example, since  $\text{CZ}_{25}$  is already present, we incorporate it without duplication. Then we optimize the depth by consolidating all  $P$  gates into a single stage.

Upon checking all mappings of the logical- $X$  part, we confirm the circuit’s validity. Moving to the rooted circuits

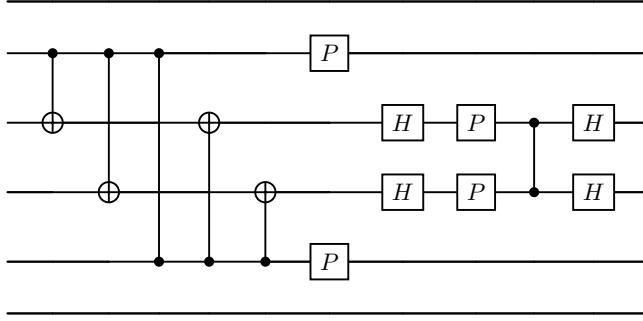


Fig. 27: Physical realization of Fig. 23 on the  $\llbracket 6, 4, 2 \rrbracket$  code produced by the solve-and-stitch approach using root qubits. Signs for  $\overline{Z}_2$  and  $\overline{Z}_3$  can be fixed with Pauli gates at the end.

for the logical- $Z$  constraints in Fig. 26, we observe that the two CNOT gates in Fig. 26a have already been incorporated in the logical- $X$  part. Consequently, we exclude them and proceed to add  $H_3$ ,  $P_3$ ,  $CZ_{34}$ , and  $H_4$  into the final circuit. At this stage, we verify that all prior Pauli constraints are still satisfied. Next, in Fig. 26b, we observe a similar  $H$ - $P$ - $CZ$ - $H$  structure, sharing the same CZ gate. This structure is consolidated into the physical circuit, as depicted in Fig. 27. Once again, the CNOT gates in Fig. 26b are already present in previous rooted circuits, so we do not duplicate them. Through this process, we validate that all Pauli constraints are satisfied simultaneously, the two stabilizer generators are preserved, and the depth aligns with the circuit generated by the LCS algorithm in Fig. 24. The notable differences lie in the repositioning of certain gates and the cancellation of some Hadamard gates. Hence, we have a bottom-up approach to derive the best output of the LCS algorithm in this case, while being able to track the structure of the circuit at each stage of the process. This directly addresses the question we posed at the beginning of Section IV.

While it may appear that we must check for past constraints when stitching each rooted circuit to the existing physical circuit, this was done for pedagogical reasons. Later, we prove rigorously that the stitching procedure always satisfies all constraints for logical C-QSK circuits on this code family. Therefore, the validity of the circuits is established analytically, and for all members of the code family.

#### APPENDIX IV

#### EVEN NUMBER OF HADAMARDS FOR $\llbracket 8, 6, 2 \rrbracket$ CODE

We have successfully implemented the solve-and-stitch approach on the  $\llbracket 6, 4, 2 \rrbracket$  code by identifying root qubits for different non-trivial constraints. Here we show that the approach extends seamlessly to a larger code size, such as the  $\llbracket 8, 6, 2 \rrbracket$  code. In this extended scenario, we incorporate Hadamard gates on multiple qubits in the logical circuit, as shown in Fig. 28. The root qubit idea continues to be effective, demonstrating its utility in tailoring circuit synthesis for this code family. The circuits are constructed similar to the  $\llbracket 6, 4, 2 \rrbracket$  code.

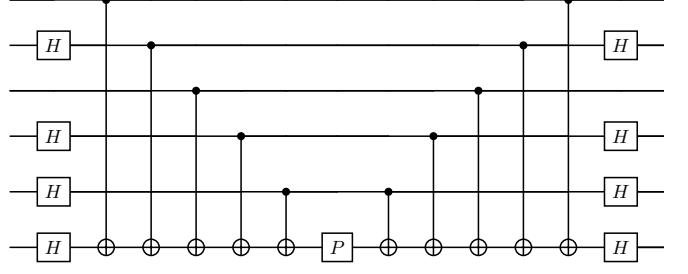
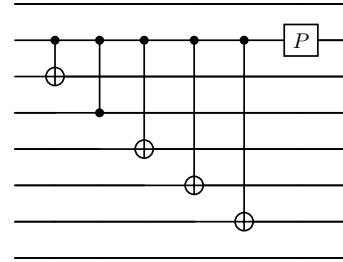


Fig. 28: C-QSK circuit with even Hadamards on many qubits.



(a)  $\overline{X}_1 \mapsto X_1 Y_2 X_3 Z_4 X_5 X_6 X_7$

Fig. 29: Rooted circuit construction for logical- $X$  constraints.

As previously discussed in the  $\llbracket 6, 4, 2 \rrbracket$  code scenario, when encountering an  $X$  gate in the output of a logical- $Z$  constraint, a CZ gate is applied followed by  $H$ , instead of implementing a single CNOT gate. It is important to note that this results in a distinctive  $H$ - $P$ - $CZ$ - $H$  “special” structure, which may include multiple CZ gates (depending upon the number of  $X$  terms in the output of the constraint). Towards the end of these rooted circuits, CNOT gates are introduced, which would have already appeared in previous logical- $X$  rooted circuits.

Fig. 31 illustrates the construction of the complete physical circuit on  $\llbracket 8, 6, 2 \rrbracket$  code using the solve-and-stitch approach. As before, when incorporating new rooted circuits, it is crucial to ensure that these circuits do not duplicate existing gates in the physical circuit. It can be readily verified that the complete circuit satisfies all logical Pauli constraints and preserves the stabilizer group. Of course, further simplifications are possible.

#### APPENDIX V

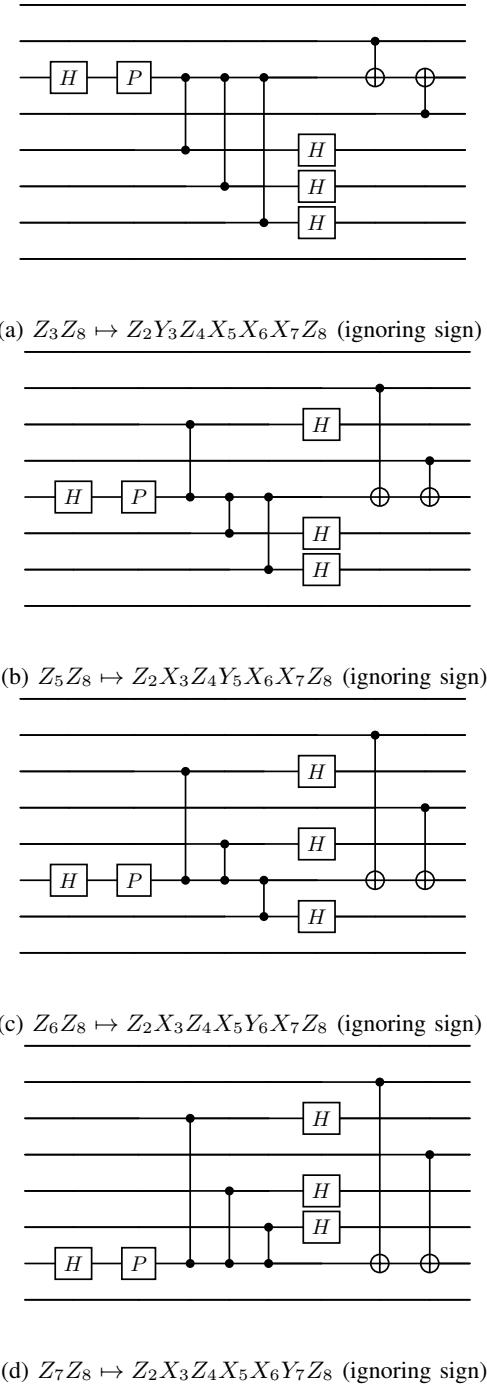
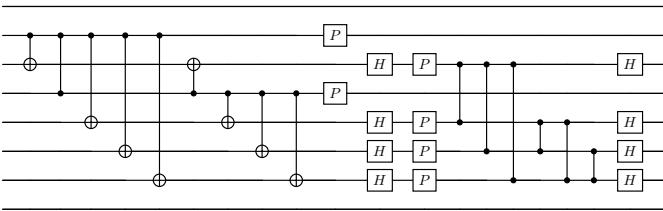
#### PROOFS FOR ALL RESULTS

##### A. Proof of Theorem 1

*Proof:* For convenience, we focus on the 3-qubit logical C-QSK circuit in Fig. 1 (with a fixed angle  $\theta = \frac{\pi}{2}$ ), but the proof strategy generalizes to C-QSK circuits comprising an arbitrary number of qubits and combinations of  $H$  and  $H_y$ . According to Section II-A, the mapping rules for Fig. 1 are:

$$\begin{aligned} \overline{X}_1 &\mapsto \overline{Y}_1 \overline{X}_2 \overline{Z}_3 , \quad \overline{Z}_1 \mapsto \overline{Z}_1 , \\ \overline{X}_2 &\mapsto \overline{X}_2 , \quad \overline{Z}_2 \mapsto -\overline{Z}_1 \overline{Y}_2 \overline{Z}_3 , \\ \overline{X}_3 &\mapsto \overline{Z}_1 \overline{X}_2 \overline{Y}_3 , \quad \overline{Z}_3 \mapsto \overline{Z}_3 . \end{aligned} \quad (30)$$

To make the analysis easier, we can represent the logical Pauli operators as binary vectors according to Section I-A.

Fig. 30: Rooted circuit construction for logical- $Z$  constraints.Fig. 31: Physical realization of Fig. 28 on the  $[[8, 6, 2]]$  code produced by the solve-and-stitch approach using root qubits. Signs for  $\overline{Z}_i$  can be fixed with Pauli gates at the end.

Let  $x_i, z_i, a_i, b_i \in \{0, 1\}^n$  for  $i = 1, 2, 3$ . Then the logical Pauli operators can be expressed as follows:

$$\begin{aligned}\overline{X}_1 &\equiv E(x_1, z_1) , \quad \overline{Z}_1 \equiv E(a_1, b_1) , \\ \overline{X}_2 &\equiv E(x_2, z_2) , \quad \overline{Z}_2 \equiv E(a_2, b_2) , \\ \overline{X}_3 &\equiv E(x_3, z_3) , \quad \overline{Z}_3 \equiv E(a_3, b_3) .\end{aligned}\quad (31)$$

The mapping rules of a single Hadamard gate are  $H X H^\dagger = Z$ ,  $H Z H^\dagger = X$ . Thus, the general mapping rule of transversal Hadamard on  $n$  qubits can be expressed as follows:

$$H^{\otimes n} E(x, z)(H^{\otimes n})^\dagger = E(z, x). \quad (32)$$

Assume that transversal Hadamard realizes the 3-qubit logical C-QSK circuit on a stabilizer code with the above logical Pauli operators. Then it must satisfy the mappings in Eq. (30):

$$\begin{aligned}H^{\otimes n} \overline{X}_1 (H^{\otimes n})^\dagger \\ = E(z_1, x_1)\end{aligned}\quad (33)$$

$$= \overline{Y}_1 \overline{X}_2 \overline{Z}_3 \quad (34)$$

$$\propto E(x_1 \oplus a_1 \oplus x_2 \oplus a_3, z_1 \oplus b_1 \oplus z_2 \oplus b_3). \quad (35)$$

Hence, we obtain the following relations from  $\overline{X}_1$ :

$$\overline{X}_1: z_1 = x_1 \oplus a_1 \oplus x_2 \oplus a_3, \quad (36)$$

$$x_1 = z_1 \oplus b_1 \oplus z_2 \oplus b_3. \quad (37)$$

Similarly, from the other constraints in Eq. (30) we obtain:

$$\overline{Z}_1: a_1 = b_1, \quad (38)$$

$$\overline{X}_2: x_2 = z_2, \quad (39)$$

$$\overline{Z}_2: b_2 = a_1 \oplus x_2 \oplus a_2 \oplus a_3, \quad (40)$$

$$a_2 = b_1 \oplus z_2 \oplus b_2 \oplus b_3, \quad (41)$$

$$\overline{X}_3: z_3 = a_1 \oplus x_2 \oplus x_3 \oplus a_3, \quad (42)$$

$$x_3 = b_1 \oplus z_2 \oplus z_3 \oplus b_3, \quad (43)$$

$$\overline{Z}_3: a_3 = b_3. \quad (44)$$

Combining the relations on  $z_1$  and  $b_2$  we get

$$a_2 \oplus b_2 = x_1 \oplus z_1. \quad (45)$$

Similarly, combining the relations on  $a_2$  and  $x_3$  we have

$$x_3 \oplus z_3 = a_2 \oplus b_2. \quad (46)$$

Thus, we have the chain of relations

$$x_1 \oplus z_1 = a_2 \oplus b_2 = x_3 \oplus z_3. \quad (47)$$

It can be shown that two Hermitian Pauli operators satisfy

$$E(a, b)E(c, d) = (-1)^{\langle [a, b], [c, d] \rangle_s} E(c, d)E(a, b), \quad (48)$$

where  $\langle [a, b], [c, d] \rangle_s := ad^T \oplus bc^T$  is called the *symplectic inner product*. Therefore, two Pauli matrices  $E(a, b)$ ,  $E(c, d)$  commute if and only if  $\langle [a, b], [c, d] \rangle_s = 0$ . We know that logical- $X$  and  $Z$  operators must anti-commute on the same logical qubit and must commute on different logical qubits, i.e.,  $\overline{X}_i \overline{Z}_j = (-1)^{\delta_{ij}} \overline{Z}_j \overline{X}_i$ , where  $\delta_{ij}$  is the Kronecker delta function. Thus, we have the following constraints:

$$x_1 b_1^T \oplus z_1 a_1^T = 1, \quad (49)$$

$$x_1 b_3^T \oplus z_1 a_3^T = 0, \quad (50)$$

$$x_1 z_2^T \oplus z_1 x_2^T = 0, \quad (51)$$

$$a_1 b_2^T \oplus b_1 a_2^T = 0. \quad (52)$$

From previously established relations we know that  $a_1 = b_1, x_2 = z_2, a_3 = b_3$ , and  $x_1 \oplus z_1 = a_2 \oplus b_2 = x_3 \oplus z_3$ . Thus, the last constraint above can be rewritten as follows:

$$a_1 b_2^T \oplus b_1 a_2^T = b_1 b_2^T \oplus b_1 a_2^T \quad (53)$$

$$= b_1 (a_2^T \oplus b_2^T) \quad (54)$$

$$= b_1 (x_1^T \oplus z_1^T) \quad (55)$$

$$= b_1 x_1^T \oplus b_1 z_1^T \quad (56)$$

$$= x_1 b_1^T \oplus z_1 a_1^T \quad (57)$$

$$= 1, \quad (58)$$

which is a contradiction. Therefore, it is impossible to implement the 3-qubit logical C-QSK circuit in Fig. 1 using a transversal Hadamard on any stabilizer code. ■

### B. Proof of Theorem 2

*Proof:* The mapping rules of a single Phase gate are  $PXP^\dagger = Y, PZP^\dagger = Z$ . Thus, the general mapping rule of transversal Phase on  $n$  qubits can be expressed as follows:

$$P^{\otimes n} E(x, z)(P^{\otimes n})^\dagger = E(x, x \oplus z). \quad (59)$$

Assume that transversal Phase realizes the 3-qubit logical C-QSK circuit in Fig. 1 on a stabilizer code with logical  $X$  (resp.  $Z$ ) operators  $E(x_i, z_i)$  (resp.  $E(a_i, b_i)$ ). Then it must satisfy:

$$\begin{aligned} \overline{X}_1 &\mapsto \overline{Y}_1 \overline{X}_2 \overline{Z}_3, & \overline{Z}_1 &\mapsto \overline{Z}_1, \\ \overline{X}_2 &\mapsto \overline{X}_2, & \overline{Z}_2 &\mapsto -\overline{Z}_1 \overline{Y}_2 \overline{Z}_3, \\ \overline{X}_3 &\mapsto \overline{Z}_1 \overline{X}_2 \overline{Y}_3, & \overline{Z}_3 &\mapsto \overline{Z}_3. \end{aligned} \quad (60)$$

For trivial mappings, we have relations such as

$$P^{\otimes n} \overline{Z}_i (P^{\otimes n})^\dagger = E(a_i, a_i \oplus b_i) = \overline{Z}_i \propto E(a_i, b_i). \quad (61)$$

Hence, we obtain the following constraints:

$$\overline{Z}_1: a_1 = \mathbf{0}, \quad \overline{X}_2: x_2 = \mathbf{0}, \quad \overline{Z}_3: a_3 = \mathbf{0}. \quad (62)$$

For non-trivial constraints such as  $\overline{X}_1$ , we have

$$P^{\otimes n} \overline{X}_1 (P^{\otimes n})^\dagger \quad (63)$$

$$= E(x_1, x_1 \oplus z_1) \quad (64)$$

$$= \overline{Y}_1 \overline{X}_2 \overline{Z}_3 \quad (65)$$

$$\propto E(x_1 \oplus a_1 \oplus x_2 \oplus a_3, z_1 \oplus b_1 \oplus z_2 \oplus b_3). \quad (66)$$

$$= E(x_1, z_1 \oplus b_1 \oplus z_2 \oplus b_3).$$

Hence, we obtain the following constraints from  $\overline{X}_1, \overline{Z}_2, \overline{X}_3$ :

$$\overline{X}_1: x_1 = b_1 \oplus z_2 \oplus b_3, \quad (67)$$

$$\overline{Z}_2: a_2 = b_1 \oplus z_2 \oplus b_3, \quad (68)$$

$$\overline{X}_3: x_3 = b_1 \oplus z_2 \oplus b_3. \quad (69)$$

Combining the relations on  $a_1, x_2$  and  $a_3$ , we get

$$a_1 = x_2 = a_3 = \mathbf{0}. \quad (70)$$

Similarly, combining the relations on  $x_1, a_2$  and  $x_3$  we have

$$x_1 = a_2 = x_3 = b_1 \oplus z_2 \oplus b_3. \quad (71)$$

Since  $\overline{X}_1, \overline{Z}_1$  anti-commute and  $\overline{Z}_1, \overline{Z}_2$  commute, we have

$$x_1 b_1^T \oplus z_1 a_1^T = x_1 b_1^T = 1, \quad (72)$$

$$a_1 b_2^T \oplus b_1 a_2^T = b_1 a_2^T = 0. \quad (73)$$

From Eqns. (71) and (73), we can rewrite Eqn. (73) as

$$b_1 a_2^T = b_1 x_1^T = x_1 b_1^T = 1, \quad (74)$$

which is a contradiction to Eqn. (73). Therefore, it is impossible to implement the 3-qubit logical C-QSK circuit in Fig. 1 using a transversal Phase on any stabilizer code. The proof can be generalized to C-QSK circuits of larger sizes. ■

### C. Proof of Lemma 4

*Proof:* Consider the general C-QSK circuit where the first and last layers have  $H_i$  gates for  $i \in I_h$ , the middle layers start with  $\text{CNOT}_{j \rightarrow k}$  gates for  $j \in [k-1]$ , then perform  $P = R_z(\frac{\pi}{2})$  on qubit  $k$ , and finally execute the prior CNOTs again but in the reverse order (see Fig. 2 for  $k = 4$  where  $I_h = \{1, 2, 3\}$ ).

Consider  $i \notin I_h$ . Then the mappings of  $\overline{Z}_i$  are trivial because  $\overline{Z}_i$  is on the control qubit of CNOT gates, except for qubit  $k$ . For the last qubit, the symmetric positioning of CNOT gates ensures that this trivial mapping still holds. However,  $\overline{X}_i$  propagates into  $\overline{X}_i \overline{X}_k$  since CNOT maps  $XI$  to  $XX$ . When  $\overline{X}_k$  encounters the Phase gate, it transforms into  $\overline{Y}_k$ , so we have the propagated operator  $\overline{X}_i \overline{Y}_k$ . Since CNOT gates map  $XY$  to  $YZ$ , the operator becomes  $\overline{Y}_i \overline{Z}_k$  after the second  $\text{CNOT}_{i \rightarrow k}$ . For the remaining qubits  $j$ , CNOT gates map  $IY$  to  $ZY$ , so  $\overline{Y}_k$  propagates into  $\overline{Z}_j \overline{Y}_k$ . At the final layer, if a qubit  $j \neq i$  contains a Hadamard gate, i.e.,  $j \in I_h$ , then the  $\overline{Z}_j$  becomes  $\overline{X}_j$ . Otherwise,  $\overline{Z}_j$  remains unchanged.

Next, consider  $i \in I_h$ . In this case, the mappings of  $\overline{X}_i$  are trivial as  $\overline{X}_i \mapsto \overline{Z}_i \mapsto \overline{X}_i$  through the two Hadamard gates at the first and last layers. In between these gates, the  $\overline{Z}_i$  does not propagate through  $\text{CNOT}_{i \rightarrow k}$ . However, for  $\overline{Z}_i$ , it first changes into  $\overline{X}_i$  through  $H$  and then propagates into the last qubit after encountering  $\text{CNOT}_{i \rightarrow k}$ . The subsequent mappings are analogous to the scenario where  $i \notin I_h$ , with the distinction that as qubit  $i \in I_h$ , the output gate of qubit  $i$  becomes  $-\overline{Y}_i$  because the final  $H$  gate maps  $Y$  to  $-Y$ . ■

### D. Proof of Lemma 7

*Proof:* The  $X$ -mappings listed in Corollary 5 and Corollary 6 identify the CNOT and CZ gates present in the rooted circuits. Recall that  $\text{CNOT}_{i+1 \rightarrow j+1}$  maps  $X_{i+1} \mapsto X_{i+1} X_{j+1}, X_{j+1} \mapsto X_{j+1}$ , and  $\text{CZ}_{i+1,j+1}$  maps  $X_{i+1} \mapsto X_{i+1} Z_{j+1}, X_{j+1} \mapsto Z_{i+1} X_{j+1}$ . For the  $i$ -th logical- $X$  constraint (rooted circuit), the root is qubit  $i+1$ . We only need to consider the case  $i \notin I_h$  because the case  $i \in I_h$  does not need a rooted circuit (the logical- $X$  mapping is trivial).

The mapping for  $X_1 X_{i+1}$  implies that the CNOT gates are  $\text{CNOT}_{i+1 \rightarrow j+1}$  for  $j \in I_h$ . Since the non-root qubits  $j+1$  are only targets, we always have  $X_1 X_{j+1} \mapsto X_1 X_{j+1}$ , so this rooted circuit satisfies the (trivial)  $X$ -mappings for  $j \in I_h$ .

Next, the mapping for  $X_1 X_{i+1}$  also implies that the CZ gates are  $\text{CZ}_{i+1,j+1}$  for  $j \notin (I_h \cup \{i\})$ . This time, these indices  $j$  also have a similar non-trivial mapping as the root  $i+1$ . Since

$j \notin I_h$ , the qubit  $j + 1$  is never involved in any CNOT with  $i + 1$ , so we only need to check that the CZ does not violate the mapping for  $X_1 X_{j+1}$ . This is indeed the case because the CZ also appears in the rooted circuit with root  $j + 1$ , since  $i \notin (I_h \cup \{j\})$  there. For the mapping in Eqn. (15), a  $\text{CZ}_{i+1,n}$  is added, but there is no constraint involving qubit  $X_n$  at the input of the mapping. As there is no other gate involving qubits  $i + 1$  and  $j + 1$  for  $j \notin I_h$ , we conclude that the rooted circuit with root  $i + 1$  does not affect other Pauli mappings.

Finally, the  $\text{CNOT}_{i+1 \rightarrow 1}$  gates (for Eqn. (15)) and the  $P_{i+1}$  gates never affect other mappings because the root qubits  $i + 1$  are unique. Hence, we can simply concatenate the individual rooted circuits for logical- $X$  constraints and drop duplicate CZ gates to satisfy all such constraints simultaneously. ■

#### E. Proof of Lemma 8

*Proof:* The proof is analogous to the above case of logical- $X$  constraints, but we will highlight some subtle differences. We only need to consider  $i \in I_h$  because  $i \notin I_h$  has trivial  $Z$ -mappings. For these rooted circuits, we first transform  $Z_{i+1}$  to  $Y_{i+1}$  through a  $H$  and  $P$  on the root  $i + 1$ . Subsequently, we perform  $\text{CZ}_{i+1,j+1}$  for  $j \in (I_h \setminus \{i\})$  rather than  $\text{CNOT}_{i+1 \rightarrow j+1}$  because the rooted circuit for this  $j$  will require  $\text{CNOT}_{j+1 \rightarrow i+1}$ , thereby doubling the number of two-qubit gates. Instead, we follow the  $\text{CZ}_{i+1,j+1}$  with  $H_{j+1}$  to produce  $X_{j+1}$  (and similarly  $H_{i+1}$  in the rooted circuit for  $j$ ). Since the other rooted circuit also transforms  $Z_{j+1} \mapsto Y_{j+1}$  before this CZ, its mapping is not violated. The  $H_{j+1}$  at the end only changes the sign of  $Y_{j+1}$  to  $-1$ , which helps satisfy the sign component of the corresponding mapping.

The  $\text{CNOT}_{n \rightarrow i+1}$  gates to cancel  $Z_n$  and the  $\text{CZ}_{i+1,1}$  followed by  $H_1$  to produce  $X_1$  in Eqn. (18) are harmless for other  $Z$ -mappings. Finally, the  $\text{CNOT}_{j+1 \rightarrow i+1}$  gates to produce  $Z_{j+1}$  for  $j \notin I_h$  (from  $Y_{i+1}$ ), which preserve the trivial mappings for  $Z_{j+1} Z_n$  as qubit  $j + 1$  is the control. ■

#### F. Proof of theorem 10

*Proof:* First, let us show that appending the logical- $X$  stitched circuit before the logical- $Z$  stitched circuit doesn't affect the logical- $Z$  Pauli mappings. In effect, we need to track  $Z_{i+1} Z_n$  through the combined circuit. From Remark 9 we know that the CNOTs at the end of the logical- $Z$  stitched circuit can be moved to its front, i.e., at the middle of the logical- $X$  and logical- $Z$  stitched circuits. But Remark 9 also shows that they already appear in the logical- $X$  stitched circuit (at the beginning). It is easily checked that these CNOTs commute with other gates in the logical- $X$  stitched circuit because their target qubits are never roots and hence are never the control qubits for any CNOT. Since the CNOTs in the middle of the two stitched circuits serve their purpose, these duplicated CNOTs can be dropped. This leaves the logical- $X$  stitched circuit with only CZ and  $P$  gates, which propagate  $Z_{i+1} Z_n$  as is into the unchanged logical- $Z$  stitched circuit. The only exception is the  $\text{CNOT}_{i+1 \rightarrow 1}$  gates when the number of Hadamards is odd, but these do not affect  $Z_{i+1} Z_n$ . Thus, the logical- $Z$  mappings are preserved by the combined circuit.

Second, let us show that the logical- $Z$  stitched circuit leaves the logical- $X$  mappings unaffected. For this argument, we will group the CNOTs in the middle of the stitched circuits with the logical- $X$  stitched circuit. This means that the remainder of the combined circuit only consists of the  $H$ - $P$ -CZ- $H$  symmetric structure. If the number of Hadamards is odd, then by Lemma 8 this structure is preceded by the set of  $\text{CNOT}_{n \rightarrow i+1}$  gates, where  $i \in I_h$ . But Corollary 6 implies that the Pauli term on qubit  $i + 1$  at the output of logical- $X$  mappings is always  $X_{i+1}$  (see Eqns. (15) and (17)). This term does not propagate through  $\text{CNOT}_{n \rightarrow i+1}$  because it belongs to the target of the CNOT, so we only need to consider the ensuing symmetric structure. However, Eqn. (14) and Lemma 8 imply that this structure also involves qubits  $i + 1$  for  $i \in I_h$ . For odd number of Hadamards, Eqn. (18) implies that qubit 1 is involved as well. Note that Lemma 8 only introduces  $\text{CZ}_{i+1,1}$  and then a  $H_1$ . But we must precede the CZ with a  $H_1$  and  $P_1$  in the combined circuit to ensure that Eqn. (17) is satisfied. In either case, by the arguments earlier, the  $X$ -mappings at the end of the logical- $X$  stitched circuit always have an  $X$  term in these qubits. This  $X_1$  or  $X_{i+1}$  comes out unchanged when propagated through the  $H$ - $P$ -CZ- $H$  structure since  $H$  maps  $X \mapsto Z$ , which commutes through  $P$  and CZ, and maps back to  $X$  after  $H$ . Hence, the combined circuit also preserves the logical- $X$  mappings.

Finally, we must ensure that the combined circuit preserves the stabilizer group of the codes. In fact, we will show the stricter result that the stabilizer generators  $X_1 X_2 \cdots X_n$  and  $Z_1 Z_2 \cdots Z_n$  commute individually through the combined circuit. Assume that the number of Hadamards is even. Then, from Eqns. (11) and (13), we observe that multiplying all the mappings for  $i \in [n - 2]$  we obtain  $X_2 X_3 \cdots X_{n-1}$  at the input. By including  $X_1$  and  $X_n$ , this produces the  $X$ -stabilizer generator. Since qubits 1 and  $n$  are not involved in the combined circuit,  $X_1$  and  $X_n$  are left unchanged. We are left to check that the result of the above multiplication also produces  $X_2 X_3 \cdots X_{n-1}$  at the output of the mapping. Since  $|I_h|$  is even, the product of Eqn. (13) for all  $i \in I_h$  results in  $\prod_{i \in I_h} X_{i+1}$ . So it suffices to show that the product of Eqn. (11) for all  $i \notin I_h$  results in  $\prod_{i \notin I_h} X_{i+1}$ . We have

$$\prod_{i \notin I_h} X_1 Y_{i+1} \left( \prod_{j \in I_h} X_{j+1} \right) \left( \prod_{j \in [n-2] \setminus (I_h \cup \{i\})} Z_{j+1} \right) \quad (75)$$

$$= \left[ X_1^{|I_h^c|} \prod_{j \in I_h} X_{j+1}^{|I_h^c|} \right] \prod_{i \notin I_h} \left[ Y_{i+1} \prod_{j \notin (I_h \cup \{i\})} Z_{j+1} \right] \quad (76)$$

$$= \prod_{i \notin I_h} \left[ Y_{i+1} \prod_{j \notin (I_h \cup \{i\})} Z_{j+1} \right], \quad (77)$$

where  $I_h^c = [n - 2] \setminus I_h$  also has  $|I_h^c|$  even. There are  $|I_h^c|$  terms in the product and each term has  $|I_h^c|$  single-qubit Pauli components in the product. Taking the product over all terms, we observe that the first Pauli component is of the form  $YZZ \cdots Z = \iota X$ , the second component is of the form  $ZYZZ \cdots Z = -\iota X$ , the third is of the form  $ZZYZZ \cdots Z = \iota X$ , and so on. Hence, each  $\iota$  pairs with a  $-\iota$

to form 1 and the final term is  $\prod_{i \notin I_h} X_{i+1}$  as required. This proves that  $X_1 \cdots X_n$  is preserved. An analogous argument shows that  $Z_1 \cdots Z_n$  is preserved too.

Next, assume that the number of Hadamards is odd. Again, multiplying Eqns. (15) and (17) with  $X_1$  and  $X_n$  produces the stabilizer  $X_1 \cdots X_n$  at the input. However, the combined circuit does involve qubits 1 and  $n$ , so we cannot ignore the propagation of  $X_1$  and  $X_n$ . For this argument, we will group the CNOTs in the middle with the logical- $X$  part of the combined circuit to form the logical- $X$  stitched circuit. At the end of this stitched circuit, all logical- $X$  mappings are satisfied, so the product of Eqns. (15) and (17) for all  $i \in [n-2]$  represents the propagation of  $X_2 X_3 \cdots X_{n-1}$ :

$$\left[ \prod_{i \in I_h} X_1 \right] \prod_{i \notin I_h} \left[ Y_{i+1} \prod_{j \in [n-2] \setminus (I_h \cup \{i\})} Z_{j+1} \right] Z_n \quad (78)$$

$$= X_1 \prod_{i \notin I_h} \left[ Y_{i+1} \prod_{j \notin (I_h \cup \{i\})} Z_{j+1} \right] Z_n. \quad (79)$$

From a similar argument as in the case of even  $|I_h|$ , the middle product has terms  $YZZ \cdots Z = Y, ZYZZ \cdots Z = -Y, ZZYZZ \cdots Z = Y$ , and so on. There will be an even number of negative signs, so the final term is  $X_1 Z_n \prod_{i \notin I_h} Y_{i+1}$ . It is easy to check that  $X_1$  commutes through the logical- $X$  stitched circuit, which together with the above calculation yields the mapping  $X_1 X_2 \cdots X_{n-1} \mapsto Z_n \prod_{i \notin I_h} Y_{i+1}$ . But  $X_n$  propagates into  $X_n Z_{i+1}$  through each  $CZ_{i+1,n}$  from Lemma 7, resulting in  $X_n \prod_{i \notin I_h} Z_{i+1}$ . Multiplying this with the above mapping produces

$$X_1 X_2 \cdots X_n \mapsto (Z_n X_n) \prod_{i \notin I_h} (Y_{i+1} Z_{i+1}) \quad (80)$$

$$= (iY_n) \left( \pm i \prod_{i \notin I_h} X_{i+1} \right) \quad (81)$$

$$= \pm Y_n \prod_{i \notin I_h} X_{i+1}. \quad (82)$$

We introduce a  $P_n$  or  $P_n^\dagger$  gate after the logical- $X$  stitching circuit to map  $\pm Y_n \mapsto X_n$ . Then we add a  $CNOT_{n \rightarrow 1}$  gate to map  $X_n \prod_{i \notin I_h} X_{i+1} \mapsto X_1 X_n \prod_{i \notin I_h} X_{i+1}$ . It is easily verified that both these gates do not affect the logical- $X$  and logical- $Z$  mappings. The remainder of the combined circuit only consists of  $CNOT_{n \rightarrow i+1}$  for  $i \in I_h$  (from Lemma 8) and the  $H$ - $P$ - $CZ$ - $H$  symmetric structure. The  $X_n$  propagates through the CNOTs to produce  $X_n \prod_{i \in I_h} X_{i+1}$ , which commutes through the structure. The  $\prod_{i \notin I_h} X_{i+1}$  term above is untouched by the CNOTs and the symmetric structure, so we have the desired mapping  $X_1 \cdots X_n \mapsto X_1 \cdots X_n$ . Thus, the  $X$ -stabilizer generator is preserved.

For the  $Z$ -stabilizer generator, we take a similar approach. The product of Eqns. (16) and (18) produces the mapping

$$Z_2 Z_3 \cdots Z_{n-1} \mapsto -X_1 Z_n \prod_{i \in I_h} \left[ Y_{i+1} \prod_{j \in I_h \setminus \{i\}} X_{j+1} \right] \quad (83)$$

$$= -X_1 Z_n \prod_{i \in I_h} Y_{i+1}. \quad (84)$$

It is easy to see that  $Z_n \mapsto Z_n$  in the combined circuit, so we can multiply this with the above to obtain  $Z_2 \cdots Z_n \mapsto -X_1 \prod_{i \in I_h} Y_{i+1}$ . We must introduce  $Z_1$  at the input to make the  $Z$ -stabilizer. The  $Z_1$  propagates into  $Z_1 \prod_{i \notin I_h} Z_{i+1}$  via the  $CNOT_{i+1 \rightarrow 1}$  gates from Lemma 7, and the product  $\prod_{i \notin I_h} Z_{i+1}$  is unaffected by the rest of the combined circuit. Then  $Z_1$  propagates into  $Z_1 Z_n$  due to the  $CNOT_{n \rightarrow 1}$  introduced above for the  $X$ -stabilizer. Finally, through the symmetric structure,  $Z_1 \mapsto Y_1$  after  $H_1$  and  $P_1$ , then maps to  $Y_1 \prod_{i \in I_h} Z_{i+1}$  after the  $CZ_{i+1,1}$  gates, and finally becomes  $-Y_1 \prod_{i \in I_h} X_{i+1}$  after the Hadamards. Combining with the  $Z_n \prod_{i \notin I_h} Z_{i+1}$  and multiplying with the mapping  $Z_2 \cdots Z_n \mapsto -X_1 \prod_{i \in I_h} Y_{i+1}$  we obtain

$$Z_1 Z_2 \cdots Z_n \mapsto (Y_1 X_1) \prod_{i \in I_h} (X_{i+1} Y_{i+1}) \prod_{i \notin I_h} (Z_{i+1}) Z_n \quad (85)$$

$$= (-iZ) \prod_{i \in I_h} (iZ) \prod_{i \notin I_h} Z_{i+1} Z_n \quad (86)$$

$$= \pm Z_1 Z_2 \cdots Z_n. \quad (87)$$

A sign discrepancy can be fixed using a layer of Pauli gates, which can be found efficiently using the binary representation of Pauli operators, e.g., see [18]. Hence, the  $Z$ -stabilizer generator is also preserved, which completes the proof. ■

#### G. Proof of Theorem 12

*Proof:* For the case of even  $h$ , we only need to consider the non-highlighted blocks and gates in Fig. 9. The  $CZ_{i+1,j+1}$  gates for all  $i, j \notin I_h$  have depth  $\binom{k-h}{2}$ . Then the layer of  $P_{i+1}$  gates for  $i \notin I_h$  increases depth by 1. The  $CNOT_{i+1 \rightarrow j+1}$  gates for  $i \notin I_h, j \in I_h$  have depth  $(k-h)h$ . The layers of  $H_{i+1}$  and  $P_{i+1}$  gates for  $i \in I_h$  increase depth by 2. The  $CZ_{i+1,j+1}$  gates for all  $i, j \in I_h$  have depth  $\binom{h}{2}$ . The final layer of  $H_{i+1}$  gates for  $i \in I_h$  adds 1 to the depth. Hence,

$$\text{Depth} = \binom{k-h}{2} + 1 + (k-h)h + 2 + \binom{h}{2} + 1 \quad (88)$$

$$= \frac{(k-h)(k-h-1) + 2h(k-h) + h(h-1)}{2} + 4 \quad (89)$$

$$= \frac{(k-h)(k+h-1) + h(h-1)}{2} + 4 \quad (90)$$

$$= \frac{k^2 + kh - k - hk - h^2 + h + h^2 - h}{2} + 4 \quad (91)$$

$$= \frac{k(k-1)}{2} + 4. \quad (92)$$

For the case of odd  $h$ , we need to include all the highlighted blocks and gates in Fig. 9. The  $CZ_{i+1,n}$  gates for all  $i \notin I_h$  add depth of  $k-h$ . The  $P_n$  or  $P_n^\dagger$  can be included in the layer of  $P_{i+1}$  gates for  $i \notin I_h$ . The  $CNOT_{n \rightarrow 1}$  and  $CNOT_{i+1 \rightarrow 1}$  gates for all  $i \notin I_h$  add depth of  $k-h+1$ . The  $CNOT_{n \rightarrow i+1}$  gates for  $i \in I_d$  add depth of  $h$ . The  $H_1$  and  $P_1$  can be included in the layers of  $H_{i+1}$  and  $P_{i+1}$  gates for  $i \in I_h$ . The  $CZ_{i+1,1}$  gates for all  $i \in I_h$  add depth of  $h$ . The final  $H_1$  can be included in the layer of  $H_{i+1}$  gates for  $i \in I_h$ . The new additions introduce a combined depth of

$$(k-h) + (k-h+1) + h + h = 2k+1. \quad (93)$$

Hence, the total depth of the complete physical circuit is

$$\frac{k(k-1)}{2} + 4 + \frac{4k+2}{2} = \frac{(k+2)(k+1)}{2} + 4. \quad (94)$$

By the proof of Theorem 10, note that a final layer of Pauli gates might be necessary to fix signs, which can increase the depth by 1. This applies to both even and odd  $h$ . ■

#### H. Proof of Theorem 13

*Proof:* Consider the case when  $h$  is even. The logical identity gadget has  $\binom{n}{2} = \binom{k+2}{2} = \frac{(k+2)(k+1)}{2}$  CZ gates. The circuit in Fig. 9 begins with  $\binom{k-h}{2} = \frac{(k-h)(k-h-1)}{2}$  CZ gates, which can now be canceled. The  $P_{i+1}$  gates are also canceled, but the remaining  $P$  gates from the gadget still contribute 1 to the depth. Hence, the number of remaining CZ gates becomes

$$\begin{aligned} & \frac{k^2 + 3k + 2}{2} - \frac{(k^2 + h^2 - 2kh) - (k-h)}{2} \\ &= \frac{4k + 2 - (1 - 2k)h - h^2}{2}. \end{aligned} \quad (95)$$

Therefore, the total depth of the optimized physical circuit is

$$\begin{aligned} & \frac{4k + 2 - (1 - 2k)h - h^2}{2} + (k-h)h + \frac{h^2 - h}{2} + 5 \\ &= \frac{2hk - 2h^2 + 4k + 2 - h + 2kh - h^2 + h^2 - h}{2} + 5 \end{aligned} \quad (96)$$

$$= \frac{4hk - 2h^2 + 4k + 2 - 2h}{2} + 5 \quad (97)$$

$$= 2hk - h^2 + 2k + 1 - h + 5 \quad (98)$$

$$= (2 + 2h)k - h^2 - h + 6. \quad (99)$$

Next, consider the case of odd  $h$ . Beyond the CZ cancellations for even  $h$ , we observe from Fig. 9 that the  $CZ_{i+1,n}$  gates for all  $i \notin I_h$  can also be cancelled. This reduces the optimized depth above for even  $h$  by  $k-h$ . Together with the remaining highlighted blocks and gates in Fig. 9 for odd  $h$ , the optimized depth can be calculated as

$$\begin{aligned} & (2 + 2h)k - h^2 - h + 6 - (k-h) + (k-h+1) + h + h \\ &= (2 + 2h)k - h^2 + h + 7. \end{aligned} \quad (100)$$

Hence, the difference in optimized depths is  $2h+1$ . ■

#### I. Proof of Corollary 14

*Proof:* Let us fix  $k$ . To understand the effect of increasing  $k$ , let us replace the set  $I_h$  with its complement  $I_h^c = [n-2] \setminus I_h$  and calculate the new depth. This corresponds to sandwiching the logical circuit between two layers of Hadamard gates on all  $k$  qubits, which can be realized on the code as discussed above. For even  $h$ , the new depth is given by

$$\begin{aligned} & (2 + 2(k-h))k - (k-h)^2 - (k-h) + 6 \\ &= k^2 + k - h^2 + h + 6. \end{aligned} \quad (101)$$

This depth is smaller than the expression in Theorem 13 when

$$k^2 + k - h^2 + h + 6 < (2 + 2h)k - h^2 - h + 6 \quad (102)$$

$$\Rightarrow k^2 - k + 2h - 2hk < 0 \quad (103)$$

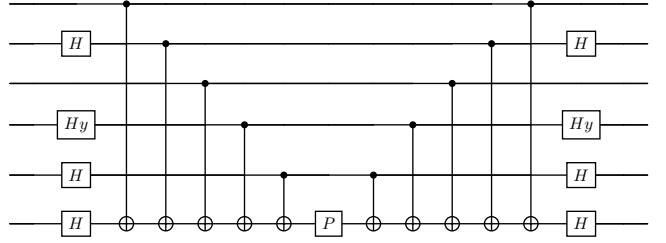


Fig. 32: C-QSK circuit with odd number of Hadamard gates and odd number of  $H_y$  gates.

$$\Rightarrow k(k-1) - 2h(k-1) < 0 \quad (104)$$

$$\Rightarrow (k-1)(k-2h) < 0 \quad (105)$$

$$\Rightarrow h > \frac{k}{2}, \quad (106)$$

as claimed. Similarly, for odd  $h$ , the new depth is

$$\begin{aligned} & (2 + 2(k-h))k - (k-h)^2 + (k-h) + 7 \\ &= k^2 + 3k - h^2 - h + 7. \end{aligned} \quad (107)$$

Once again, this depth is smaller than Theorem 13 when

$$k^2 + 3k - h^2 - h + 7 < (2 + 2h)k - h^2 + h + 7 \quad (108)$$

$$\Rightarrow k^2 + k - 2hk - 2h < 0 \quad (109)$$

$$\Rightarrow k(k+1) - 2h(k+1) < 0 \quad (110)$$

$$\Rightarrow (k+1)(k-2h) < 0 \quad (111)$$

$$\Rightarrow h > \frac{k}{2}, \quad (112)$$

leading us to the same conclusion. In both cases, the layer of physical transversal Hadamard and swap of qubits 1 and  $n$  adds 3 to the depth, 2 at the beginning of the complete physical circuit and 1 at the end due to the existing layer of Hadamards in Fig. 9. This completes the proof. ■

## APPENDIX VI EXAMPLES OF PHYSICAL IMPLEMENTATION OF LOGICAL C-QSK WITH MIXED HADAMARD AND $H_y$ GATES

This section provides examples for the physical implementation of logical C-QSK circuits with mixed Hadamard and  $H_y$  gates according to different parities of them. The complete procedure is provided in Algorithm 2.

#### A. Odd Hadamard, Odd $H_y$ on logical C-QSK

This C-QSK circuit in Fig. 32 dictates the following input-output mappings of logical Pauli operators:

$$\begin{aligned} \overline{X_1} &\mapsto \overline{Y_1} \overline{X_2} \overline{Z_3} \overline{Y_4} \overline{X_5} \overline{X_6} & , \quad \overline{Z_1} &\mapsto \overline{Z_1} , \\ \overline{X_2} &\mapsto \overline{X_2} & , \quad \overline{Z_2} &\mapsto \overline{Z_1} \overline{Y_2} \overline{Z_3} \overline{Y_4} \overline{X_5} \overline{X_6} , \\ \overline{X_3} &\mapsto \overline{Z_1} \overline{X_2} \overline{Y_3} \overline{Y_4} \overline{X_5} \overline{X_6} & , \quad \overline{Z_3} &\mapsto \overline{Z_3} , \\ \overline{X_4} &\mapsto \overline{-Z_1} \overline{X_2} \overline{Z_3} \overline{Z_4} \overline{X_5} \overline{X_6} & , \quad \overline{Z_4} &\mapsto \overline{Z_1} \overline{X_2} \overline{Z_3} \overline{Y_4} \overline{Y_5} \overline{X_6} , \\ \overline{X_5} &\mapsto \overline{X_5} & , \quad \overline{Z_5} &\mapsto \overline{Z_1} \overline{X_2} \overline{Z_3} \overline{Y_4} \overline{Y_5} \overline{X_6} , \\ \overline{X_6} &\mapsto \overline{X_6} & , \quad \overline{Z_6} &\mapsto \overline{Z_1} \overline{X_2} \overline{Z_3} \overline{Y_4} \overline{X_5} \overline{M_3} \end{aligned}$$

Substituting for the logical operators of the  $\llbracket 8, 6, 2 \rrbracket$  code, we obtain the following mappings of physical Pauli operators:

$$X_1 X_2 \mapsto X_1 Y_2 X_3 Z_4 Y_5 X_6 X_7 Z_8 , \quad Z_2 Z_8 \mapsto Z_2 Z_8 ,$$

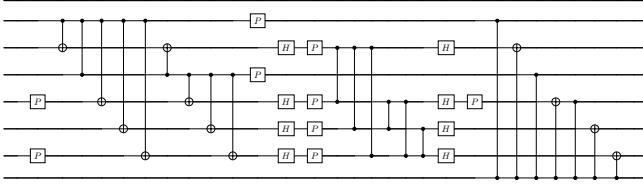


Fig. 33: Physical implementation of logical C-QSK circuit in Fig. 32.

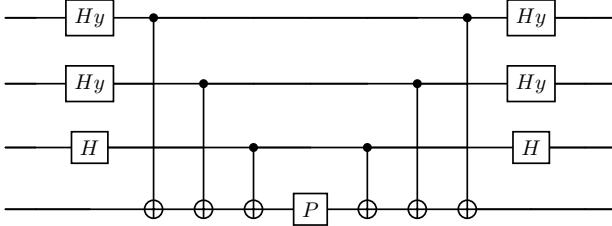


Fig. 34: C-QSK circuit with odd number of Hadamard gates and even number of  $H_y$  gates.

$$\begin{aligned}
 X_1 X_3 &\mapsto X_1 X_3 & Z_3 Z_8 &\mapsto Z_2 Y_3 Z_4 Y_5 X_6 X_7 , \\
 X_1 X_4 &\mapsto X_1 Z_2 X_3 Y_4 Y_5 X_6 X_7 Z_8 & Z_4 Z_8 &\mapsto Z_4 Z_8 , \\
 X_1 X_5 &\mapsto X_1 Z_2 X_3 Z_4 Z_5 X_6 X_7 Z_8 & Z_5 Z_8 &\mapsto Z_2 X_3 Z_4 X_5 X_6 X_7 , \\
 X_1 X_6 &\mapsto X_1 X_6 & Z_6 Z_8 &\mapsto Z_2 X_3 Z_4 Y_5 Y_6 X_7 , \\
 X_1 X_7 &\mapsto X_1 X_7 & Z_7 Z_8 &\mapsto Z_2 X_3 Z_4 Y_5 X_6 Y_7 .
 \end{aligned}$$

Similar to the even-even case in the main text, we replace all  $H_y$  gates into Hadamard gates in logical circuit, run Algorithm 1, add  $P_5$  at the beginning and the end of the physical circuit, then apply  $CZ_{8 \rightarrow 2}$ ,  $CNOT_{8 \rightarrow 3}$ ,  $CNOT_{8 \rightarrow 6}$ ,  $CNOT_{8 \rightarrow 7}$ . Finally, we apply  $CNOT_{8 \rightarrow 5}$  and  $CZ_{8 \rightarrow 5}$  simultaneously since  $H_y$  gate appears in the forth qubit in Fig. 32. The full physical circuit is displayed in Fig. 33.

#### B. Odd Hadamard, Even $H_y$ on logical C-QSK

This C-QSK circuit in Fig. 34 dictates the following input-output mappings of logical Pauli operators:

$$\begin{aligned}
 \overline{X_1} &\mapsto -\overline{Z_1} \overline{Y_2} \overline{X_3} \overline{Z_4} , & \overline{Z_1} &\mapsto \overline{X_1} \overline{Y_2} \overline{X_3} \overline{Z_4} , \\
 \overline{X_2} &\mapsto -\overline{Y_1} \overline{Z_2} \overline{X_3} \overline{Z_4} , & \overline{Z_2} &\mapsto \overline{Y_1} \overline{X_2} \overline{X_3} \overline{Z_4} , \\
 \overline{X_3} &\mapsto \overline{X_3} & \overline{Z_3} &\mapsto -\overline{Y_1} \overline{Y_2} \overline{Y_3} \overline{Z_4} , \\
 \overline{X_4} &\mapsto \overline{Y_1} \overline{Y_2} \overline{X_3} \overline{Y_4} & \overline{Z_4} &\mapsto \overline{Z_4} . \tag{114}
 \end{aligned}$$

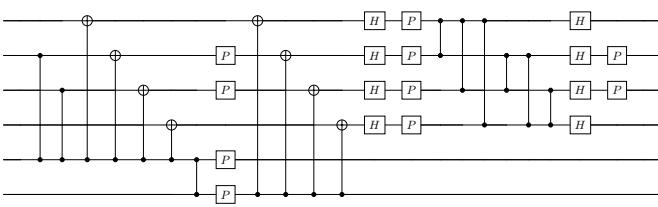


Fig. 35: Physical implementation of logical C-QSK circuit in Fig. 34.

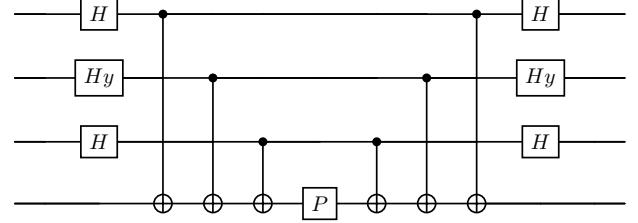


Fig. 36: C-QSK circuit with even number of Hadamard gates and odd number of  $H_y$  gates.

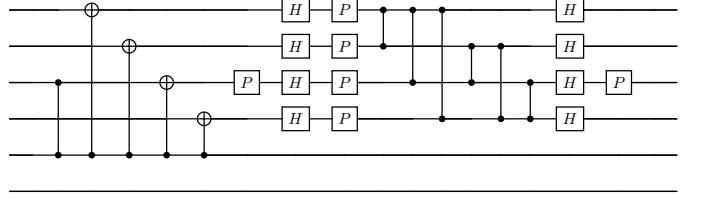


Fig. 37: Physical implementation of logical C-QSK circuit in Fig. 36.

Substituting for the logical operators of the  $\llbracket 6, 4, 2 \rrbracket$  code, we obtain the following mappings of physical Pauli operators:

$$\begin{aligned}
 X_1 X_2 &\mapsto Z_2 Y_3 X_4 Z_5 Z_6 , & Z_2 Z_6 &\mapsto -X_1 X_2 Y_3 X_4 Z_5 , \\
 X_1 X_3 &\mapsto Y_2 Z_3 X_4 Z_5 Z_6 , & Z_3 Z_6 &\mapsto -X_1 Y_2 X_3 X_4 Z_5 , \\
 X_1 X_4 &\mapsto X_1 X_4 & Z_4 Z_6 &\mapsto -X_1 Y_2 Y_3 Y_4 Z_5 , \\
 X_1 X_5 &\mapsto Y_2 Y_3 X_4 Y_5 Z_6 , & Z_5 Z_6 &\mapsto Z_5 Z_6 . \tag{115}
 \end{aligned}$$

To get the physical circuit, again we replace all  $H_y$  gates into Hadamard gates in logical circuit, run Algorithm 1. Add  $CZ_{52}$  and  $CZ_{53}$  at the beginning, then apply  $P_2$  and  $P_3$  at the position of original Phase gates in the physical circuit gained from Algorithm 1, then duplicate these  $P_2$  and  $P_3$  at the end as well. The full physical circuit is displayed in Fig. 35.

#### C. Even Hadamard, Odd $H_y$ on logical C-QSK

This C-QSK circuit in Fig. 36 dictates the following input-output mappings of logical Pauli operators:

$$\begin{aligned}
 \overline{X_1} &\mapsto \overline{X_1} & \overline{Z_1} &\mapsto -\overline{Y_1} \overline{Y_2} \overline{X_3} \overline{Z_4} , \\
 \overline{X_2} &\mapsto -\overline{X_1} \overline{Z_2} \overline{X_3} \overline{Z_4} & \overline{Z_2} &\mapsto \overline{X_1} \overline{X_2} \overline{X_3} \overline{Z_4} , \\
 \overline{X_3} &\mapsto \overline{X_3} & \overline{Z_3} &\mapsto -\overline{X_1} \overline{Y_2} \overline{Y_3} \overline{Z_4} , \\
 \overline{X_4} &\mapsto \overline{X_1} \overline{Y_2} \overline{X_3} \overline{Y_4} & \overline{Z_4} &\mapsto \overline{Z_4} . \tag{116}
 \end{aligned}$$

Substituting for the logical operators of the  $\llbracket 6, 4, 2 \rrbracket$  code, we obtain the following mappings of physical Pauli operators:

$$\begin{aligned}
 X_1 X_2 &\mapsto X_1 X_2 & Z_2 Z_6 &\mapsto X_1 Y_2 Y_3 X_4 Z_5 Z_6 , \\
 X_1 X_3 &\mapsto X_2 Z_3 X_4 Z_5 & Z_3 Z_6 &\mapsto X_1 X_2 X_3 X_4 Z_5 Z_6 , \\
 X_1 X_4 &\mapsto X_1 X_4 & Z_4 Z_6 &\mapsto X_1 X_2 Y_3 Y_4 Z_5 Z_6 , \\
 X_1 X_5 &\mapsto -X_2 Y_3 X_4 Y_5 & Z_5 Z_6 &\mapsto Z_5 Z_6 . \tag{117}
 \end{aligned}$$

For the physical circuit, after we replace all  $H_y$  gates into Hadamard gates in logical circuit and run Algorithm 1, we

delete all CZ gates and Phase gates in logical- $X$  component of this physical circuit, then delete all the gates involving in the last qubit. Then apply  $CZ_{53}$  at the beginning, then apply additional  $P_3$  just before the logical- $Z$  component of the circuit, duplicate this  $P_3$  at the end of the circuit as well. The final physical circuit in this scenario is shown in Fig. 37.