Assignment 2
CSE 311

Modüllerin neredeyse hepsinin testbenchleri yapılmıştır ve doğru çalışmaktadır. mips32_test kısmında simülasyonda herhangi bir hata yokmuş çalışıyor ama instructionlar çözemediğim bir şekilde farklı bir sırayla geliyorlar. Tam olarak çalışmadığı için tüm instructionları eklemedim. Onun dışında bir sorun yok gibi duruyor.

ModelSim ALTERA STARTER EDITION 10.1d

File Edit View Compile Simulate Add Process Tools Layout Bookmarks Window Help

sim - Default

Instance	Design unit	Design unit ty
mips	mips32	Module
inst1	instruction_...	Module
cont1	control_unit	Module
mx1	mux2to1_5bit	Module
mx2	mux2to1_5bit	Module
mr1	mips_register	Module
se	signExtend	Module
ze	zeroExtend	Module
alctr	ALUcontrol	Module
muxalu	mux2to1_3...	Module
alu1	ALU	Module
comp	comparator	Module
mxcomp	mux4to2_3...	Module
muxc	mux2to1_3...	Module
mainmem	main_memory	Module
muxmem	mux2to1_3...	Module
muxmem2	mux2to1_3...	Module
fa1	full_adder_...	Module
muxmem3	mux2to1_3...	Module
shf	leftShifter_...	Module
fa2	full_adder_...	Module
muxB	mux2to1_3...	Module
muxJ	mux2to1_3...	Module
muxJR	mux2to1_3...	Module
pc1	PC	Module
n1	mips32	Process
a1	mips32	Process

Library sim

Objects

Name	Value	Kind	Mode
clk	St0	Net	In
instruction	00000...	Net	Internal
PCout	00000...	Net	Internal
PCaddr	00000...	Net	Internal
PCplus4	00000...	Net	Internal
write_data_1	00000...	Net	Internal
signExtend_out	00000...	Net	Internal
zeroExtend_out	00000...	Net	Internal
read_data_1	00000...	Net	Internal
read_data_2	00000...	Net	Internal
ALUinput2	00000...	Net	Internal
ALUresult	00000...	Net	Internal

Processes (Active)

Name	Type (filtered)	State

Wave - Default

Msgs

Now 0.09 ns

Cursor 1 0.00 ns

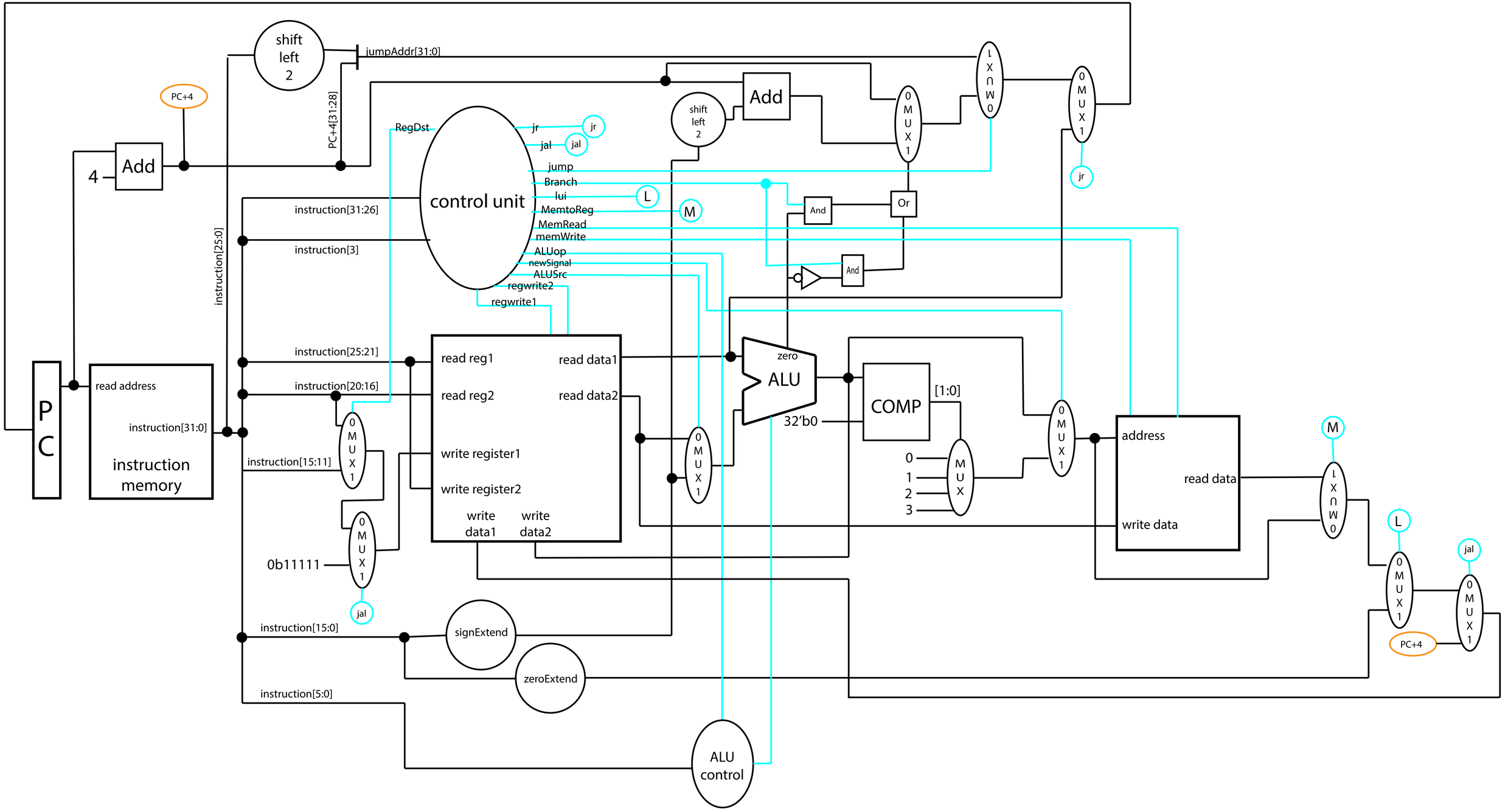
0.00 ns

0.02 ns 0.04 ns 0.06 ns 0.08 ns

Transcript

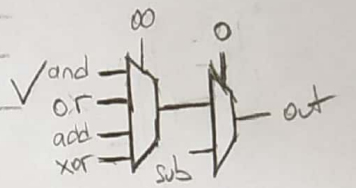
```
add wave -position end  sim:/mips32_testbench/mips/tempaddr
add wave -position end  sim:/mips32_testbench/mips/jumpAddr
add wave -position end  sim:/mips32_testbench/mips/shf1
add wave -position end  sim:/mips32_testbench/mips/branchAddr
add wave -position end  sim:/mips32_testbench/mips/trash1
add wave -position end  sim:/mips32_testbench/mips/tempMuxB
add wave -position end  sim:/mips32_testbench/mips/tempMuxJ
VSIM 53> run -all

VSIM 54>
```

Now: 90 ps Delta: 1 sim:/mips32_testbench/mips


shift left 2
jumpAddr[31:0]
PC+4
PC+4[31:28]
4
Add
RegDst
control unit
jr
jal
jump
Branch
lui
MemtoReg
MemRead
memWrite
ALUop
newSignal
ALUSrc
regwrite2
regwrite1
L
M
instruction[31:26]
instruction[3]
instruction[25:0]
instruction[25:21]
instruction[20:16]
instruction[15:11]
instruction[15:0]
instruction[5:0]
shift left 2
Add
And
Or
And
0 M U X 1
L X N W 0
jr
P C
read address
instruction[31:0]
instruction memory
read reg1
read reg2
write register1
write register2
write data1
write data2
read data1
read data2
0b11111
jal
signExtend
zeroExtend
ALU control
zero
ALU
32'b0
COMP
[1:0]
0
1
2
3
M U X
address
read data
write data
M
L
jal
PC+4

		ALUopcode	Func Field	ALU action	ALU control
lw	I	00	X	add	010
sw	I	00	X	add	010
j	j	X	X	X	X
jal	j	X	X	X	X
jr	R	10 (X)	001000	X	X
beq	I	01	X	sub	110
bne	I	01	X	sub	110
addn	R	10	100000	add	010
subn	R	10	100010	sub	110
xorn	R	10	100110	xor	011
andn	R	10	100100	and	000
orn	R	10	100101	or	001
ori	I	11	X	or	001
lui	I	X	X	X	X

000 → and
001 → or
010 → add
110 → sub
011 → xor



	RegDst	ALUSrc	MemtoReg	RegWr1	RegWr2	MemRead	MemWr	Bne/Branch	ALUOP	Jump	jr	jal	lui	newIns
lw	0	1	1	1	0	1	0	0	00	0	0	0	0	0
sw	X	1	X	0	0	0	1	0	00	0	0	0	X	0
j	X	X	X	0	0	0	0	0	X	1	0	0	X	X
jal	X	X	X	1	0	0	0	0	X	1	0	1	X	X
jr	X	X	X	0	0	0	0	0	X	0	1	0	X	X
beq	X	0	X	0	0	0	0	1	01	0	0	0	X	X
bne	X	0	X	0	0	0	0	1	01	0	0	0	X	X
addn	1	0	0	1	1	0	0	0	10	0	0	0	0	1
subn	1	0	0	1	1	0	0	0	10	0	0	0	0	1
xorn	1	0	0	1	1	0	0	0	10	0	0	0	0	1
andn	1	0	0	1	1	0	0	0	10	0	0	0	0	1
orn	1	0	0	1	1	0	0	0	10	0	0	0	0	1
ori	0	1	0	1	0	0	0	0	11	0	0	0	0	0
lui	0	X	X	1	0	0	0	0	XX	0	0	0	1	X

R-Type (jr) = 000000
lw = 100011
sw = 101011
beq = 000100
bne = 000101

j = 000010
jal = 000011
ori = 001101
lui = 001111

ALUSrc = lw + sw + ori
RegWr1 = (lw + jal + R + lui) · $\overline{jr}$
RegWr2 = R · $\overline{jr}$
MemRead = lw