CSE 331/503

Computer Organization

Homework 4

Due Date 15/01/2021 Friday 23:59

In this project, you will use Altera Quartus II with Verilog. You will implement a different version of 32-bit MIPS processor. The block that you will design will get no inputs from outside. You will have two memories: Data Memory and Instruction Memory. The instructions must be loaded to the instruction memory and the data must be put in data memory. You will support **lw, sw, j, jal, jr, beq**, **bne**, **addn, subn, xorn, andn, orn, ori** and **lui** instructions.

But the R-type instructions will execute different than the conventional MIPS we have seen. This is why they have '**n**' at the end (representing **n**ew). The new instructions have the same opcode and function fields as the conventional R-type instructions. For instance the opcode and function field of **orn** is same as **or**.

But the execution is different. For instance:

```
addn $rd, $rs, $rt
```

RTL Representation

```
$rs <= $rs + $rt
if($rs + $rt == 0)
$rd <= 1
else if($rs + $rt < 0)
$rd <= 2
else
$rd <= 3
```

In order to implement that, you must be able to write two different register addresses in one cycle Design your register accordingly.

You will write test bench and simulate your design for verification. You will write the register and memory contents before and after the execution of instructions using **writememh** in your test bench verilog code. You will initialize memory contents using **readmemh**.

The data memory size will be 256KB whereas the instruction memory size will be 16KB. Remember that addressing for a 256KB memory only requires 18 bits instead of 32 bits in regular MIPS. Update your design accordingly.

 (Bonus) There is no BONUS and we do not want you to implement any other instruction than specified above. Otherwise you get 0 due to cheating.
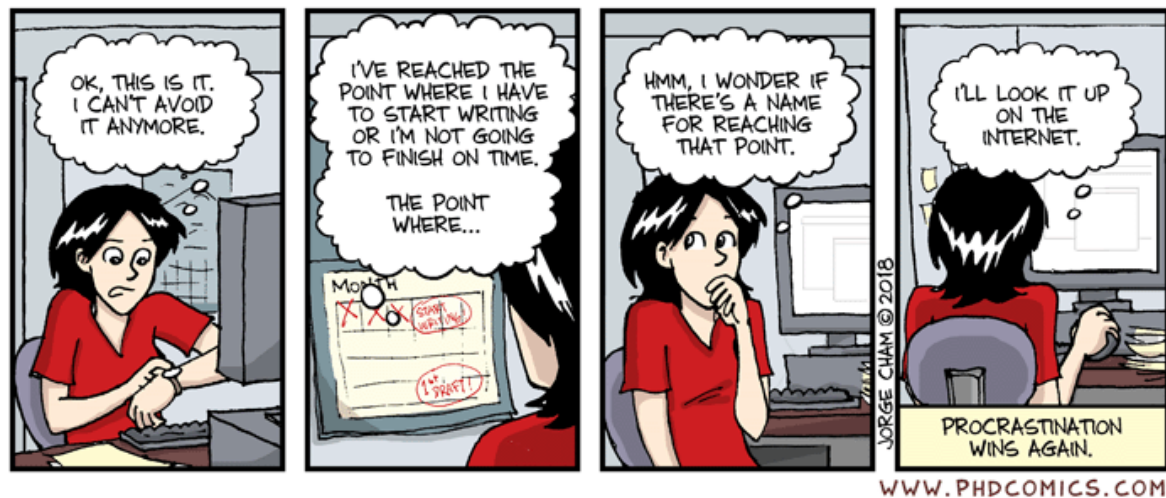
Other than registers and memory only structural Verilog is allowed. This means behavioral statements like always, if, etc are not allowed.

Please be sure that your design simulates correctly. Designs that are not even simulating can get at most 20 points.

Submit your Altera Project folder as a zip file to Moodle. We will simulate your design using not only your testbench but also our testbench to see whether all instructions are executing correctly or not.

No late submissions even if it is 1 minute. No medical reports. No excuses. No cry. So start early.

Any cheating attempt with the previous years' projects or with your friends or Internet will result in at least -100. No matter you gave or take the code. Protect your code. Do it yourself for your own good.

https://www.youtube.com/watch?v=arj7oStGLkU

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