CSE 331 Computer Organization

Project 3 – MIPS Load-Store

Due date: Dec 11, Wed. 17:00 (Moodle)

In this project you will design a processor that can only support below instructions.

NAME	MNE-MON-IC	FOR-MAT	OPERATION (in Verilog)		OPCODE/ FUNCT (Hex)
Load Byte	lb	I	R[rt]={24'b0, M[R[rs]+ZeroExtImm](7:0)}	(3)	20
Load Byte Unsigned	lbu	I	R[rt]={24'b0, M[R[rs]+SignExtImm](7:0)}	(2)	24
Load Halfword	lh	I	R[rt]={16'b0, M[R[rs]+ZeroExtImm](15:0)}	(3)	21
Load Halfword Unsigned	lhu	I	R[rt]={16'b0, M[R[rs]+SignExtImm](15:0)}	(2)	25
Load Upper Imm.	lui	I	R[rt]={imm,16'b0}		f
Load Word	lw	I	R[rt]=M[R[rs]+SignExtImm]	(2)	23
Store Byte	sb	I	M[R[rs]+SignExtImm] (7:0)=R[rt](7:0)	(2)	28
Store Halfword	sh	I	M[R[rs]+SignExtImm] (15:0)=R[rt](15:0)	(2)	29
Store Word	sw	I	M[R[rs]+SignExtImm]=R[rt]	(2)	2b

You have to implement instruction and data memory and register modules. Use your 1-bit ALU in your previous design as a module.

You have to write your own testbench on Verilog and show that the project is working right. Learn how to initialize and read a memory in PS.

Write a report that explains your Verilog modules and the testbench results. You should test all operations that ALU allows. Also report how many logic gates you used for the ALU.

RULES!!!

1. **Other than register and memory, you cannot use any other logic gates than AND, OR and NOT. (For instance XOR is not allowed.)**
2. **You can only use structural Verilog. No dataflow, no assign statement no behavioral Verilog.**
3. **ONLY THE INSTRUCTIONS IN THE TABLE WILL BE SUPPORTED. OTHERWISE 0pts.**
4. **Any not simulating Verilog project gets at most 20pts.**
5. **Any cheating means -100pts whether giving or taking the design.**
6. **You have to use hierarchy and different modules as described here.**
7. **The project will be explained in PS. So attend the PS.**
8. **If you can show your design working on actual FPGA board than you get 20pts.**