CSE 331 Computer Organization

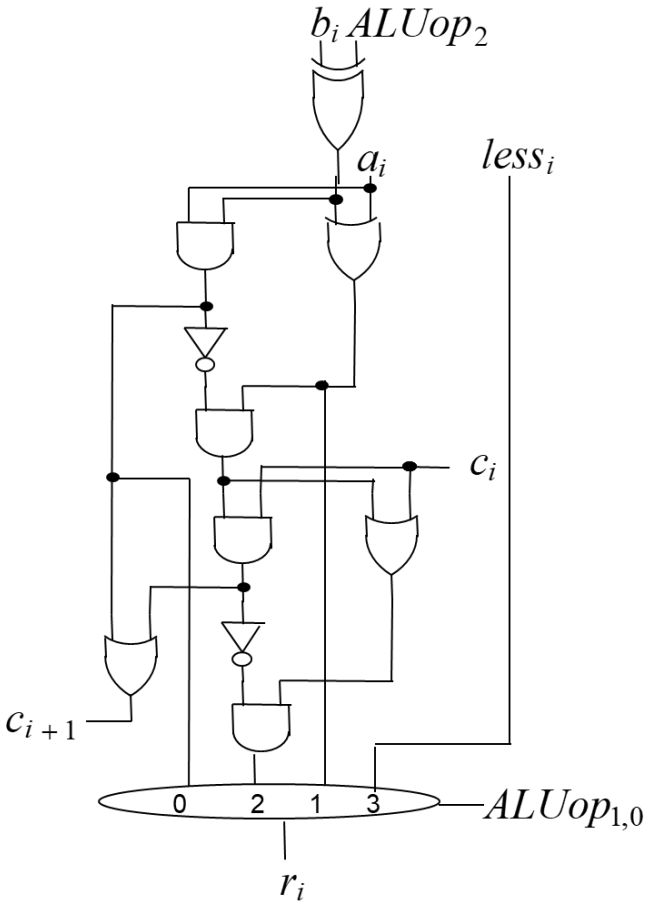
Project 2 – MIPS ALU

Due date: November 15, Fri. 17:00 (Moodle)

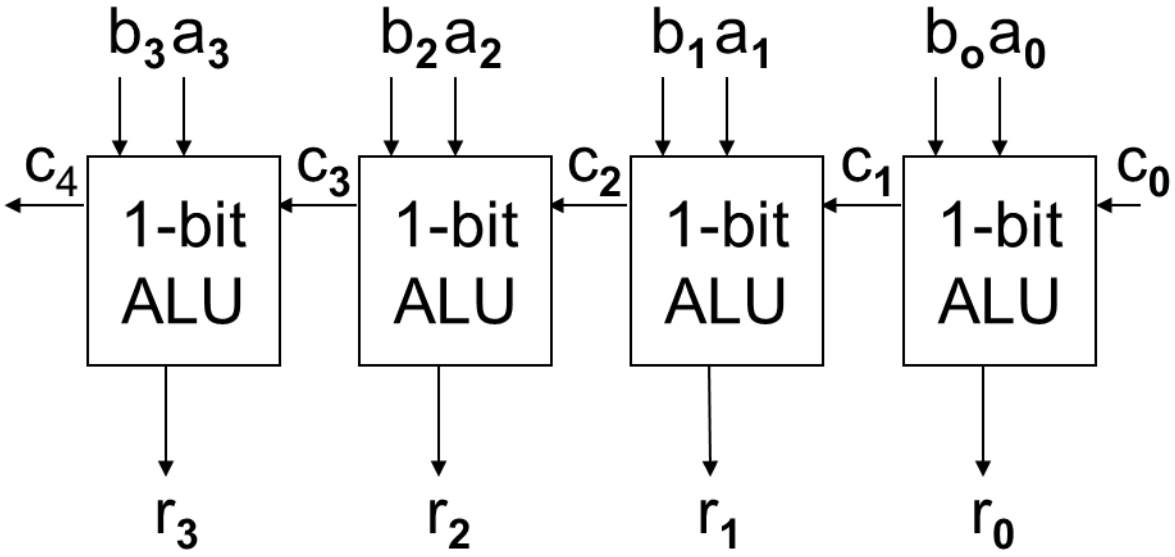
In this project you will design the exact same ALU as in the lecture notes. Your design will include:

1. 4x1 MUX module
2. 1-bit ALU
3. 32-bit ALU module

1-bit ALU module will be designed same as shown below:



32-bit ALU module will be constructed using 1-bit ALU modules as shown below:



You have to write your own testbench on Verilog and show that the project is working right.

The ALU must support AND, OR, ADD, SUBTRACT and SET ON LESS THAN operations.

Write a report that explains your Verilog modules and the testbench results. You should test all operations that ALU allows. Also report how many logic gates you used for the ALU.

RULES!!!

1. **You cannot use any other logic gates than AND, OR and NOT. (For instance XOR is not allowed.)**
2. **You can only use structural Verilog. No dataflow, no assign statement no behavioral Verilog.**
3. **<u>Any other ALU design</u> than explained above will not be accepted and means 0pts.**
4. **Any not simulating Verilog project gets at most 20pts.**
5. **Any cheating means -100pts whether giving or taking the design.**
6. **You have to use hierarchy and different modules as described here.**
7. **The project will be explained in PS. So attend the PS.**
8. **If you can show your design working on actual FPGA board than you get 30 extra pts.**