FH | JOANNEUM
System Test Engineering

STE – Digital Electronics
Lecture 12 – Lab 9

Version 1v0

DI Klaus Strohmayer – Digital Design and Verification Expert

ADC_AVG_DAC-System – Part 1

FH | JOANNEUM
System Test Engineering

Setup Vivado Project using provided constraint file

- FPGA - toplevel (basys3_top.sv)
- Constraint file (basys3_top.xdc)

Add SPI for ADC from Lab07

Add averaging filter from Lab06

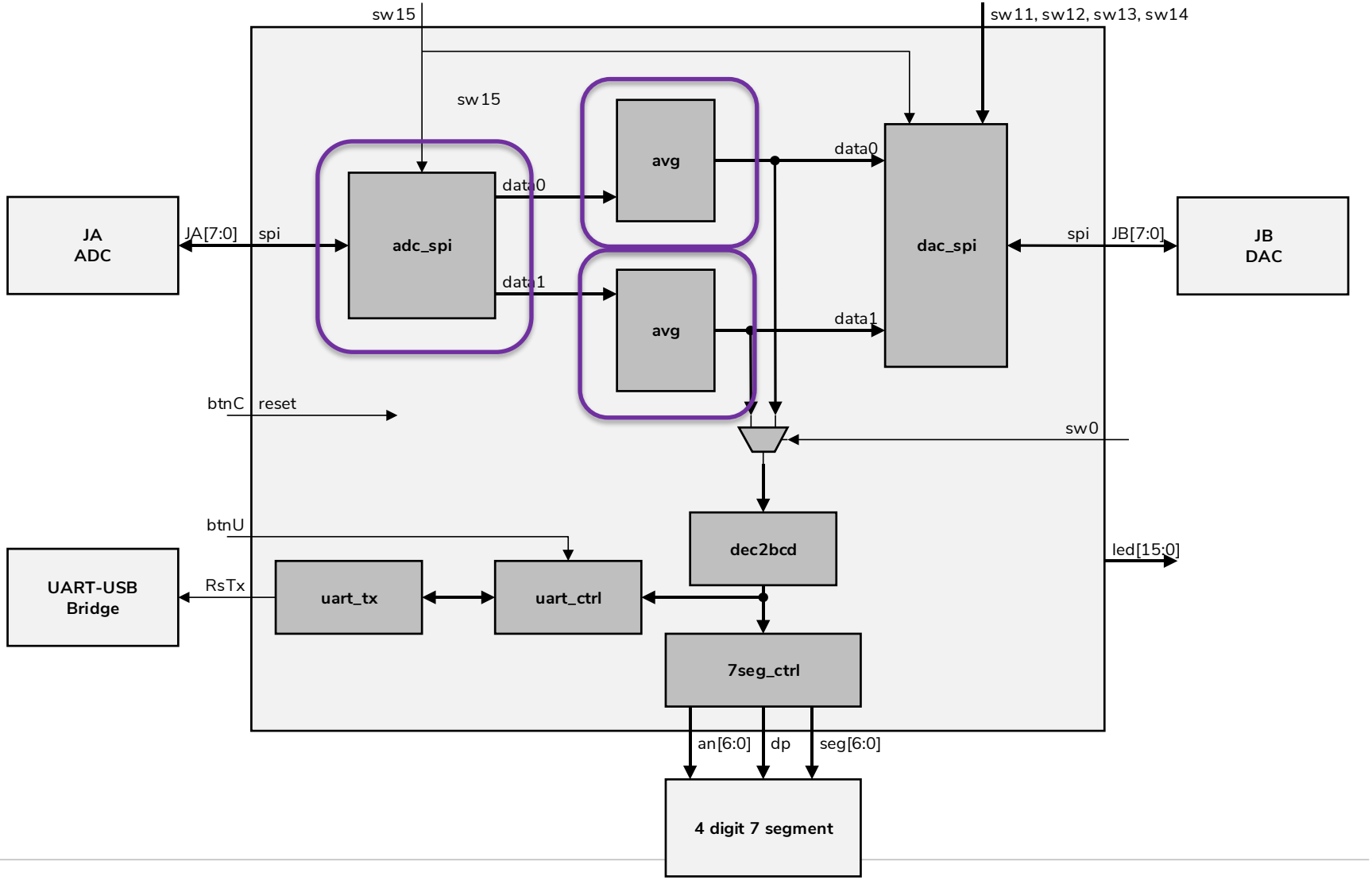
- Channel 0: IIR based
- Channel 1: FIR based

Add general functionality

- The system is reset with the center button (BTNC)
- Include ADC SPI master into the FPGA and connect it to the PmodAD1 extension board via Jumper JA.
- Enable the ADC conversion via switch SW0

ADC_AVG_DAC-System – Part 1

FH | JOANNEUM
System Test Engineering



ADC_AVG_DAC-System – Part 1

FH | JOANNEUM
System Test Engineering

Build a simple testbench capable to generate clock, reset, ADC data

Perform Synthesis and Implementation

Setup debug and trace signals

- SPI ADC data output
- Average filter data output