FH | JOANNEUM
System Test Engineering

Laboratory Report 5

Digital Electronics

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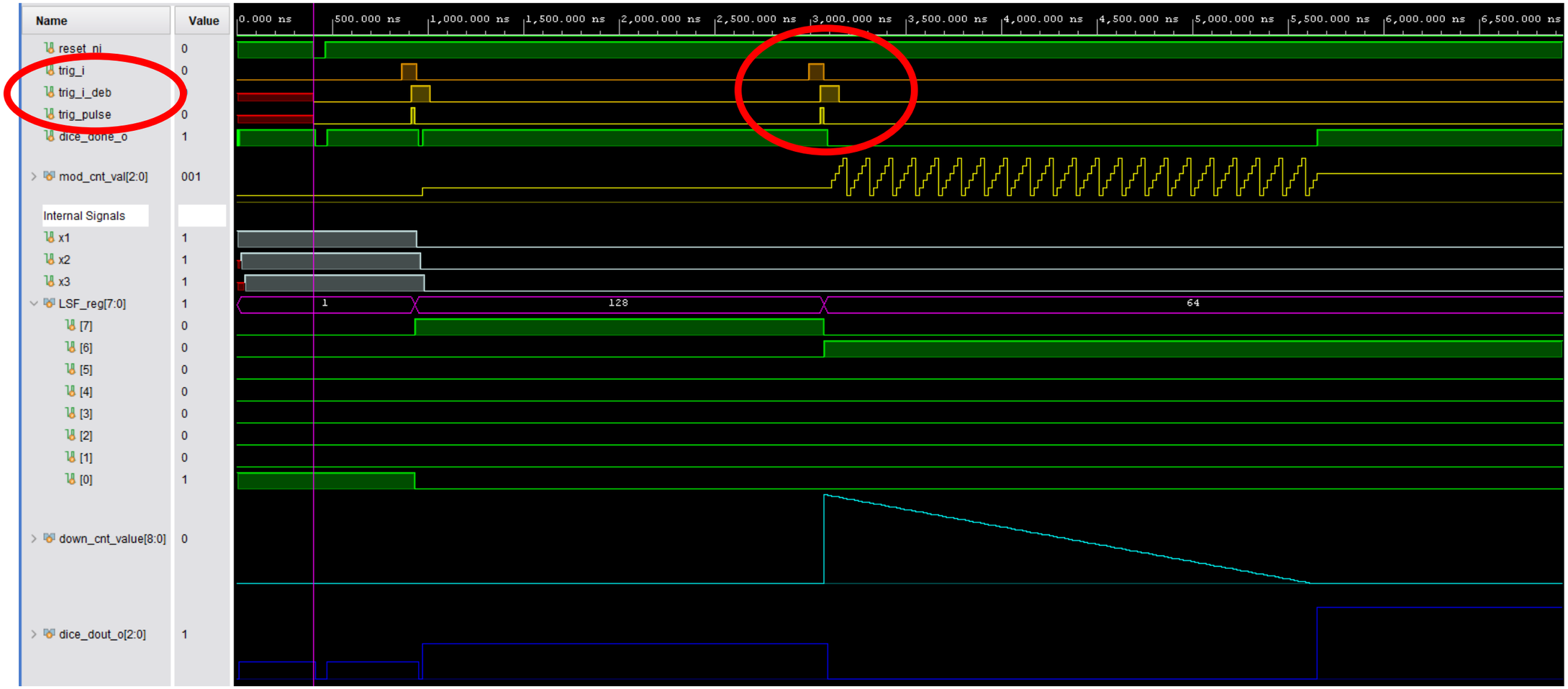
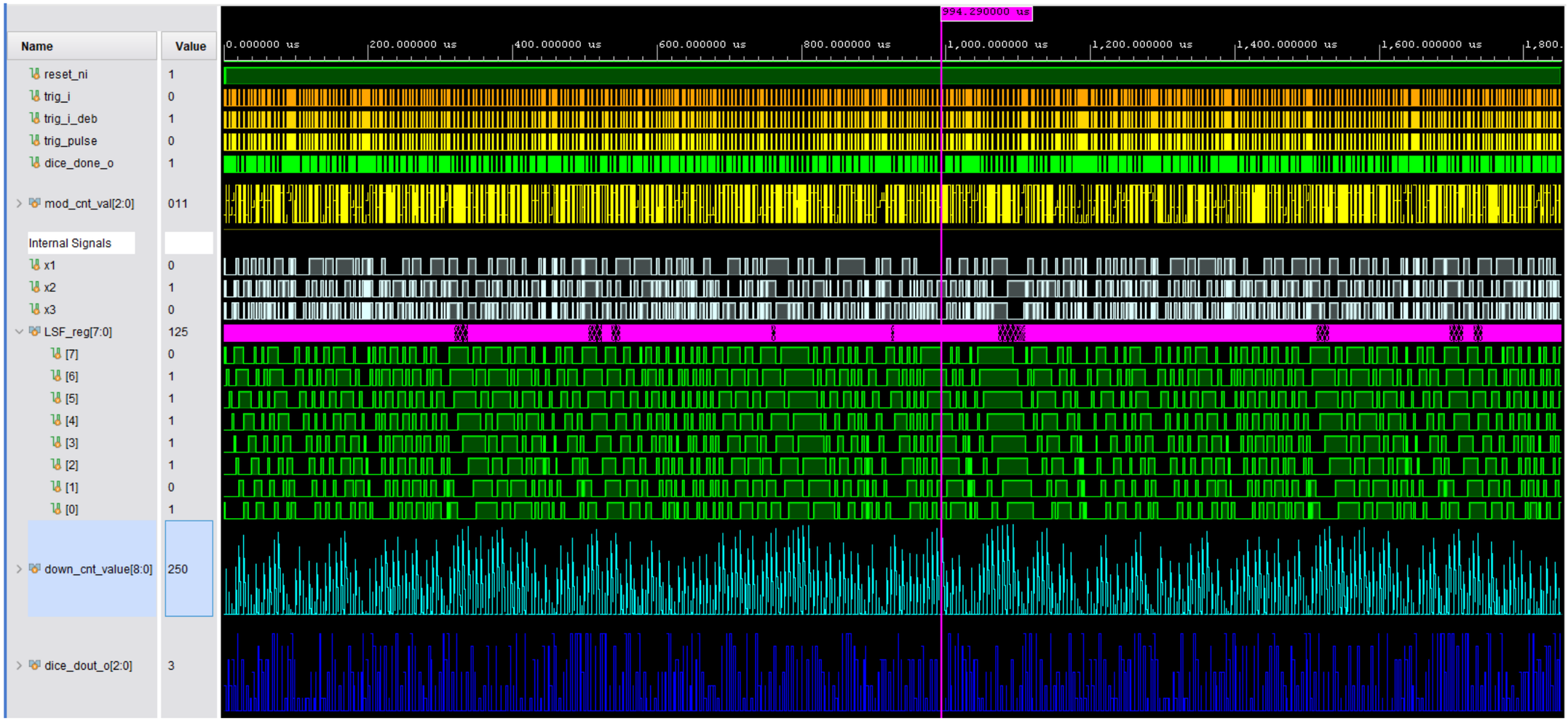
1 Debouncing *trig_i* signal and detecting its rising edge



This Figure shows the time-delay between the “analog” input signal *trig_i* and the debounced *trig_i_deb* signal. There is also a pulse which represents the rising edge-detection of the debounced trigger signal.

2 Triggering 400 times

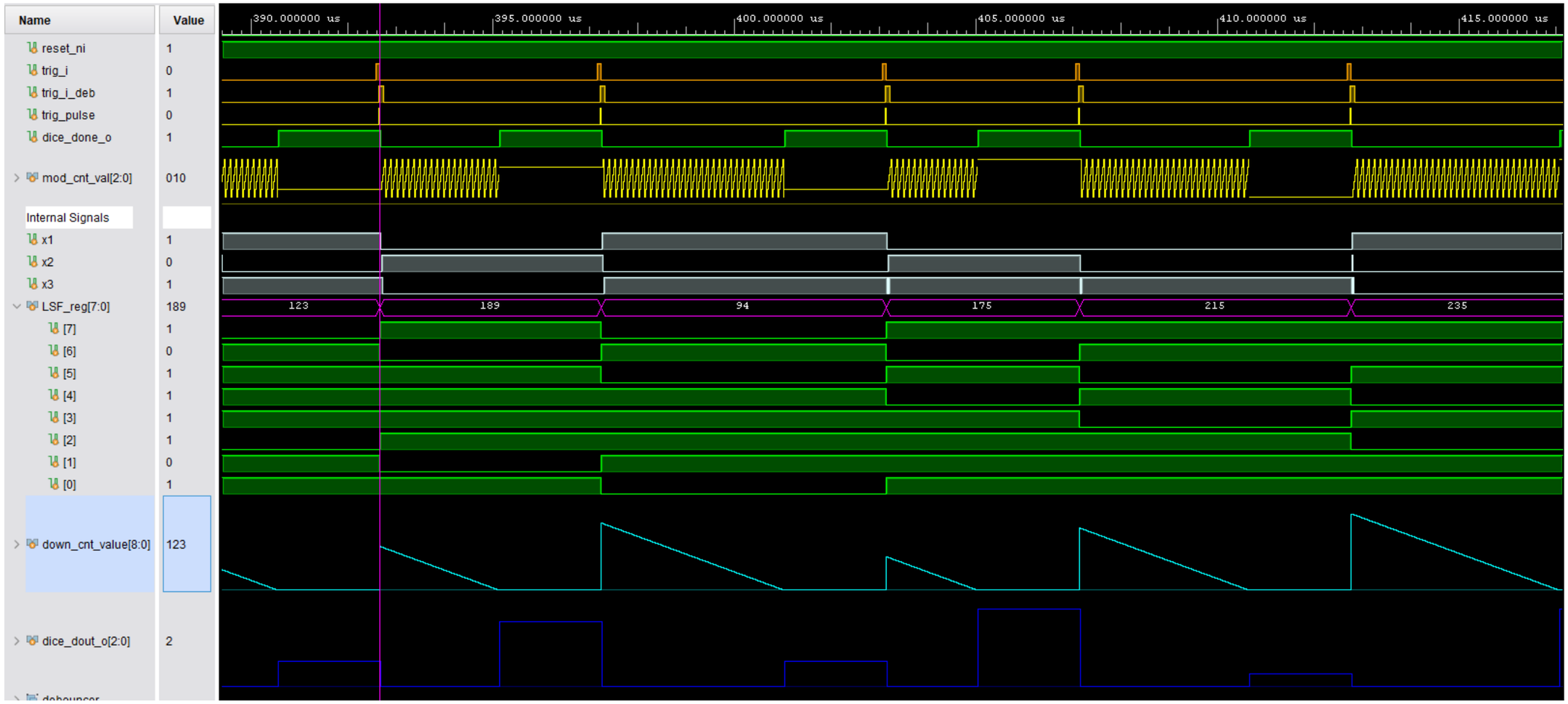


This figure shows all 400 iterations. The blue signal called *dice_dout_o* shows the random selected values between 1 and 6. The turquoise signal called *down_cnt_value* shows the output of the LSF register which is the starting value for the down counter. These values are between 1 (the init value of the LSFR) and 256 (the max value achievable with 8 bits.

The shifting of the LSF register bits is also visible in this figure.

Next figure shows a closer look at the details.

3 Closer look at the values of the counters

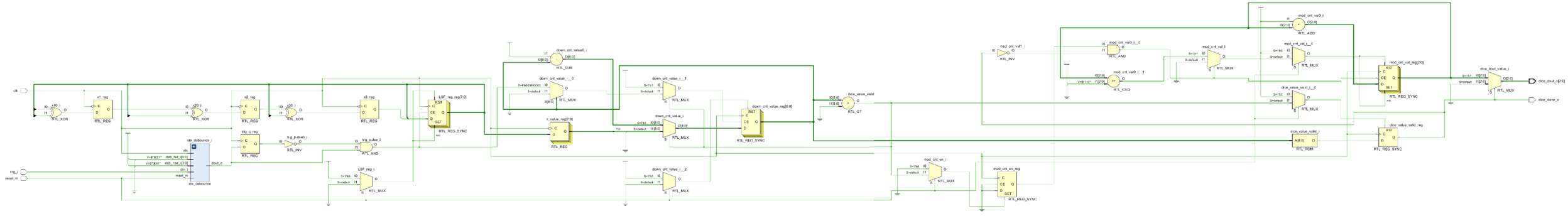


In this screenshot we observe some random generated values of the LSF register. These values are then used for the DOWN counter (see the *down_cnt_value*, turquoise*).*

The value of the modulo counter (the yellow signal called *mod_cnt_val*) is shown in the top of the screenshot. While the output value of the dice is valid (*dice_done_o* is asserted), the value of the modulo counter is frozen. The last value remains constant and it's assigned to the output signal *dice_dout_o (blue)*.

Aa soon as the *dice_done_o* signal de-asserts, the modulo counter starts again.

4 Design Schematic (Elaborated before synthesis)



4 Design Schematic (Elaborated before synthesis)

5

6

7

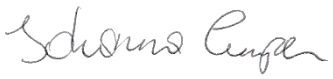
8 Configurable PWM Circuit

The files of both projects, the **Vending Machine Model** as well as the **PWM Circuit**, can be found in the following GitHub repository:

https://github.com/muresant18/LAB4_DE_STM21

29.10.2021

Muresan Timotei



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