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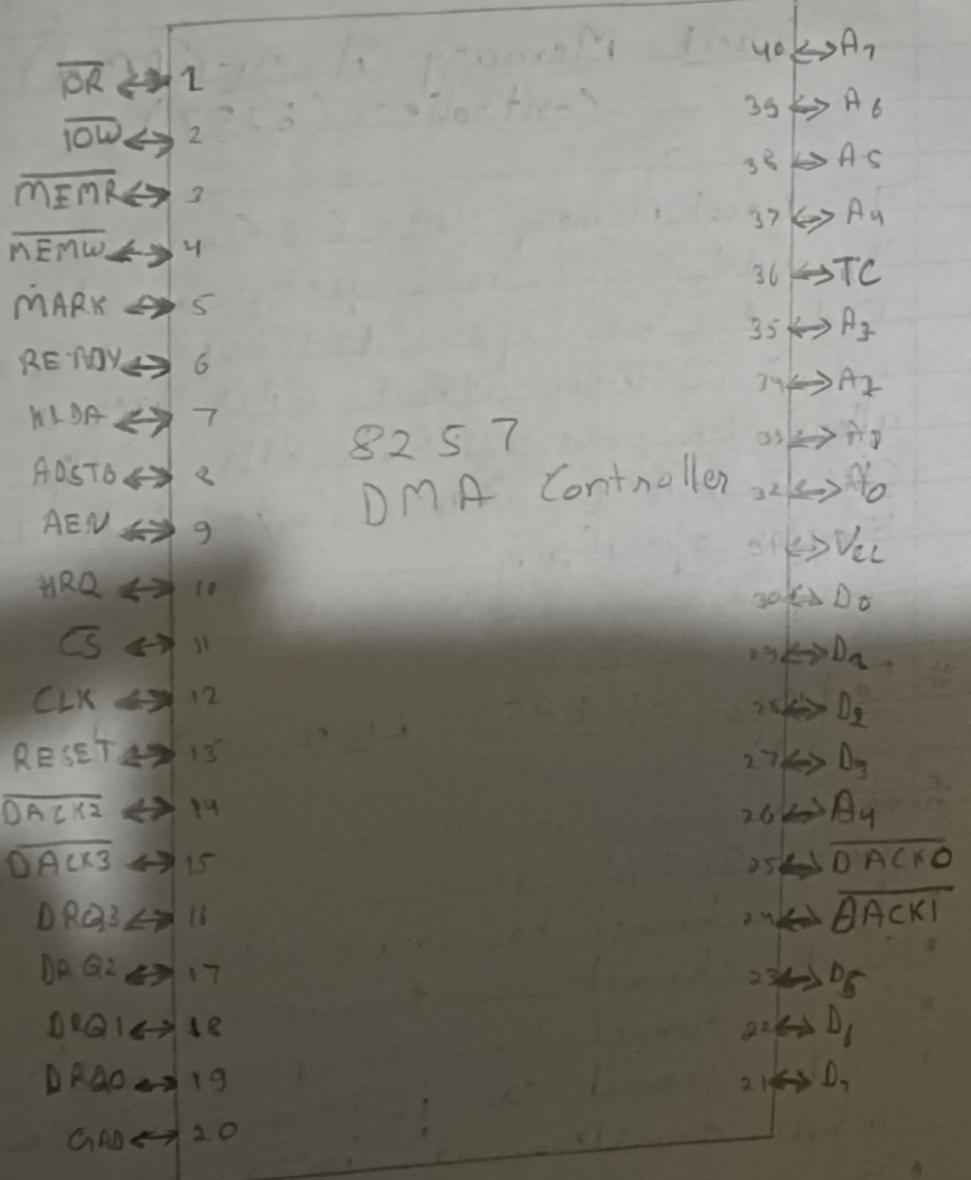
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## Direct Memory Access (DMA) Controller (8257)

The Direct Memory Access (DMA) controller, specifically the Intel 8257, is a programmable device used to manage data transfers between memory and I/O device without CPU intervention. This allows for more efficient data handling as the CPU is free to perform other tasks during data transfer operation.

### # Features of 8257 DMA controller

- It has four channels that can be used over four I/O devices.
- Each channel has 16-bit address and 14-bit counter.
- Each channel can transfer data up to 64KB.
- Each channel can be programmed independently.
- Each channel can perform read transfer, write transfer and verify transfer operations.
- It operates in 2 modes, i.e. Master mode and Slave mode



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## # Pin Description

- Data Bus (D0 - D7): These are bi-directional lines used to transfer data between the DMA controller and the microprocessor.
- Address Bus (A0-A8): These pins select one of the 16 I/O devices.
- Control and status Signals
- CS (chip select): This input is used to select the DMA controller. When low, it enables communication with the CPU.
- RD, WR :- Read/Write
- RESET :- This input is used to reset the DMA controller. When asserted, it clears all control registers and initializes the device.
- HLDA (Hold Acknowledge):- This output is used to indicate that the CPU has relinquished control of the



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System bus to the DMA controller.

- READY:- This input is used to indicate that insert wait states into the DMA controller cycles. It indicates that the peripheral is ready for data transfer.
- Memory and I/O Control Signals.
- MEMR (Memory Read): This is an active low signal used to read data from memory during a DMA cycle.
- MEMW (Memory <sup>write</sup> Read): This is an active low signal used to write data to memory during a DMA cycle.
- IOR (I/O Read):- This is an active low signal used to read data from an I/O port during a DMA cycle.
- IOW (I/O Write): This is an active low signal used to write data to an I/O port during a DMA cycle.
- Channel Control Signals.

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- DRQ0 - DRQ3 (DMA request 0-3): These inputs are used by peripheral devices to request DMA service. Each channel has its own request line.
- DACK0 - DACK3 (DMA Acknowledge 0-3): These outputs are used to acknowledge the DMA request and indicate which channel is active.
- Power Supply
- Vcc :- This pin is connected to the power supply.
- GND : This pin is connected to the ground.
- CLK : It is clock frequency signal which is required for the internal ~~for the~~ operation of 8257.
- H.RQ :- This signal is used to ~~receive~~ the hold request signal at the output. In the Slave mode, it is connected with a DRQ input line 8257. In Master mode, it is connected with



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HOLD input of the CPU.

- ADSTB :- It is a control output line used to split data and address line through Latches.
- ABN:- This signal is used to disable the address bus / data bus.
- TC :- It stands for 'Terminal Count' which indicates the present DMA cycle to the present peripheral devices.
- MARK :- The mark will be activated after each 128 cycles or integral multiples of it from the beginning. It indicates the current DMA cycle is the 128 th cycle since the previous MARK output to the selected peripheral device.



## Internal Architecture of 8257

# Functional blocks of 8257:

- (a) Data bus buffer
- (b) Control logic
- (c) Read / write logic
- (d) Priority Resolvers
- (e) DMA channels.
- (f) Interrupt logic
- (g) Mode Set Register
- (h) Status Register
- (i) Temporary Registers
- (j) Address Register
- (k) word count Register.

(a) Data bus 'buffer': 8-bit Tri-state, bidirectional buffer interface the internal bus of 8257 with the external system bus under the control of various control signals.

(b) Control logic: The control logic controls the sequences of operations and generates the required control signals like AEN, AD STB, MEMR, MEMW, TC and MARK along with the address



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Lines A4 - A7 in master mode.

(c) Read / write logic :- In the slave mode, the read / write logic accepts the I/O read or I/O write signals, decodes the A0 - A3 lines and either writes the contents of the data bus to the addressed internal registers or reads the selected register depending upon whether TOW or TOR signal is activated. In master mode, the read / write logic generates the TOR and TOW signals to control to or from the selected peripheral.

(d) Priority Resolver :- Resolver priority among the four DMA channels using either fixed or no rotating priority.

(e) DMA channels:-

(f) Interrupt logic :- Handling the generation of interrupt signals to the CPU after the completion of DMA transfer.



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- (g) **Mode Set Register** :- Configures the operating modes of the DMA controller. It stores settings for transfer mode, channel priorities, and other operational parameters.
- (h) **Status Register** :- provides the status of DMA channels, indicating whether they are active, pending, or completed. The CPU can read this register to monitor DMA operations.
- (i) **Temporary Register** :- Temporarily holds data during DMA transfers.
- (j) **Address Register** :- Stores the address of the memory location for the DMA transfer.
- (k) **Word count Register** :- keeps track of the number of words (data units) to be transferred.