Jonghyun Kim

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EDUCATION

Carnegie Mellon University

Pittsburgh, PA, USA

2024 - Present

Ph.D in Electrical and Computer Engineering
• Advisor: Professor Vanessa Chen

Konkuk University

Seoul, South Korea

B.S. & M.S. in Electrical Engineering(Admission with top-honors)

2016 - 2023

- B.S GPA: 4.05/4.5, B.S Major GPA: 4.22/4.5, M.S GPA: 4.37/4.5
- Thesis: "A High-Performance True Random Number Generator for Next-Generation Secure Systems"
- Advisor: Professor Hyungil Chae

Publications

Journal Papers(SCI/SCIE)

- [j3] Jonghyun Kim and Hyungil Chae, "A 10-Gb/s True Random Number Generator Using ML-Resistant Middle Square Method", IEEE Journal of Solid-State Circuits(JSSC), July. 2024.
- [j2] **Jonghyun Kim**, Younggyun Oh and Hyungil Chae, "An IF Reconfigurable Bandpass Noise-Shaping SAR ADC for IoT and Mobile Application", Electronics Letters(EL), Sep. 2022.
- [j1] Kihyun Kim, Jihyun Baek, **Jonghyun Kim** and Hyungil Chae, "Time-interleaved Noise-shaping SAR ADC based on CIFF Architecture with Redundancy Error Correction Technique", Journal of Semiconductor Technology and Science(JSTS), Oct. 2021.

International Conference Proceedings

- [c2] **Jonghyun Kim** and Hyungil Chae, "A 10-Gbps, 0.121-pJ/bit, All-Digital True Random-Number Generator Using Middle Square Method", in Proceedings of IEEE Asian Solid-State Circuits Conference(ASSCC), Nov. 6-9, 2022.
- [c1] Jihyun Baek, **Jonghyun Kim**, Gyuchan Cho, Jintae Kim, and Hyungil Chae, "A 7-Bit 4-GS/s Quad-Channel Time-Interleaved SAR ADC With 2-Then-1-Bit Cycle Conversion," in Proceedings of IEEE Asian Solid-State Circuits Conference(ASSCC), Nov. 6-9, 2022.

Research Experience

Energy-Efficient Circuits and Systems Lab

Pittsburgh, PA

Research Assistant

Present

- Hardware security.
- Mixed-signal domain high-efficieny machine learning accelerator.
- In sensor computable image sensor.

Circuit and System Design Laboratory

Seoul, South Korea

Jan 2020 – Dec 2023

Student Researcher

- Chip-lead tape-out project on 2.5-GS/s pipelined SAR ADC in Jun 2022.
- Chip-lead tape-out project on 40-GS/s, 32-Channel TI-SAR ADC for PAM-4 SerDes Rx in Dec 2022.
- Chip-lead tape-out project on full-custom SRAM for high-speed analog-to-digital converter (ADC) in Sep 2020.
- Chip-lead tape-out project on high-performance true random number generator(TRNG) in Sep 2021.

ARTEC IT Solutions APAC

Seoul, South Korea Oct 2018 – June 2020

Part-time R $\ensuremath{\mathcal{C}} D$ Intern

- Developed applications using C#(.NET) in a Windows WPF(xaml) environment.
- Managed an secure E-Mail archiving system.
- Built an secure unstructured data archiving system for SAP, based on SAP Archive Link.
- Experience in Debian-based Linux server management.

ARTEC IT Solutions AG

Frankfurt am Main, Hessen, Germany

Fulltime R & D Intern Nov 2018 — Mar 2019

- C#(.NET) development based on Windows WPF(xaml) application development environment.
- SAP unstructured data archiving system build based on SAP Archive Link.
- Microsoft Exchange and Hyper-V based server management.

FELLOWSHIPS

Carnegie Mellon University, Carnegie Institute of Technology Dean's Fellowship (2024): Ph.D program fellowship from electrical and computer engineering department of Carnegie Mellon University.

Konkuk University, Graduate Fellowship (2022-2023): This fellowship is granted for excellent undergraduate students. Tuition is granted for 2-year full semesters.

Konkuk University, Sang-Huh Undergraduate Fellowship (2016, 2019-2021): Admission with top-honors in engineering department. Tuition is granted for 4-year full semesters.

PROJECTS

- PIM(Process-In-Memory) Semiconductor Design Research Center, Ministry of Science and ICT, South Korea, 2022 – 2023
- Ultra-high Speed Analog-Digital Converter with Configurable Passband for Low Power/Small Beyond-5G Wireless Receiver, Ministry of Science and ICT, South Korea, 2020 2023
- Multi-band Receiver Architecture using Bandpass ADC for Low-power and Small-size 5G Mobile Applications, Samsung Research Funding & Incubation Center for Future Technology, 2020 – 2022

SKILLS

Programming Languages: Python, Linux, C#, C, C++, MATLAB, Tcl, IATEX, Skill, Tensorflow, Rust Hardware Description Languages: Verilog, System Verilog

EDA Tools: Cadence Virtuoso ADE-L, Cadence Virtuoso ADE-XL, Cadence Virtuoso Maestro, Cadence Virtuoso Layout Editor, Synopsys VCS, Synopsys Design Compiler, Synopsys IC Compiler, Synopsys IC Compiler, Synopsys Formality, Mentor Calibre DRC, Mentor Calibre LVS, Mentor Calibre xRC

Languages: Korean(Native), English(Professional, TOEFL:103), German(Elementary)

Hobbies

French Horn, Violin, Trombone, Baseball