

2006-03-16

31 bit	30 bit	29 bit	28 bit	27 bit	26 bit	25 bit	24 bit	23 bit	22 bit	21 bit	20 bit	19 bit	18 bit	17 bit	16 bit	15 bit	14 bit	13 bit	12 bit	11 bit	10 bit	09 bit	08 bit	07 bit	06 bit	05 bit	04 bit	03 bit	02 bit	01 bit	00 bit
-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------

[illegible]

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	31 bit	30 bit	29 bit	28 bit	27 bit	26 bit	25 bit	24 bit
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

=> 0xF

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	31 bit	30 bit	29 bit	28 bit	27 bit	26 bit	25 bit	24 bit	23 bit	22 bit	21 bit	20 bit	19 bit
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

=> 0x1F

Diagram illustrating the state of three modules (module 0, module 1, module 2) and their connection to the variable `tdc_num`. Each module contains two nodes (0 and 1) with values 2 and 3 respectively. Arrows indicate that the values from these nodes are being assigned to `tdc_num`.