CS303 | Assignment-4 | Due 6/Nov/2021 11:59 PM | 100 points

- Important instructions for code submissions are here: https://goo.gl/IMWvdF
- Grading scheme to be followed is available here: https://goo.gl/52D82g
- Assignment description may be underspecified to allow some room for exploration and creativity.
- Your submission should be packaged as a zip file named **exactly** in this format: CS303-[your entry no.]-[assignment no.].zip.

We need to develop a simulation program in C on linux that implements the following:

a)
Simulate the read, write and seek operations of a disk. These operations can be simulated by functions that just return the time (in ms) required to service each request. Various parameters of the disk such as:

1. Rotational speed of disk, `r` revolutions per minute.
2. Average seek time, T_s in ms.
3. Sector size, `N` in bytes.

should be taken as command-line arguments. Further, assume that the disk contains four surfaces, four read-write heads, 25 cylinders and 20 sectors per track. The disk keeps track of the current position of the read-write heads.

b)
A disk scheduler module which provides functions for implementing the following scheduling policies: Random, FIFO, SSTF, SCAN, C-SCAN

c)
Generates a uniform distribution of requests such that each request specifies:
1. The read/write address as <platter, cylinder, sector> number.
2. The number of requested sectors.

These requests should be sent to your disk scheduler, which then appropriately orders them and sends them to the disk for service by calling its read, write and seek functions. Use the values returned by the disk to determine each scheduling algorithm's throughput, response time and variance of response times.

You should report the results for the following scenarios:

Parameters: r, N , T_s	Scheduling policy	Requests	Throughput (requests/s)	<Avg., Min., Max., StdDev.> of response time (ms)
7500, 512,	Random	Sequence of randomly		

4ms		generated addresses: <platter, cylinder, sector>		
15000, 512, 4ms	Random	Sequence of randomly generated addresses: <platter, cylinder, sector>		
7500, 512, 4ms	FIFO	Sequence of randomly generated addresses: <platter, cylinder, sector>		
15000, 512, 4ms	FIFO	Sequence of randomly generated addresses: <platter, cylinder, sector>		
7500, 512, 4ms	SSTF	Sequence of randomly generated addresses: <platter, cylinder, sector>		
15000, 512, 4ms	SSTF	Sequence of randomly generated addresses: <platter, cylinder, sector>		
7500, 512, 4ms	SCAN	Sequence of randomly generated addresses: <platter, cylinder, sector>		
15000, 512, 4ms	SCAN	Sequence of randomly generated addresses: <platter, cylinder, sector>		
7500, 512, 4ms	C-SCAN	Sequence of randomly generated addresses: <platter, cylinder, sector>		
15000, 512, 4ms	C-SCAN	Sequence of randomly generated addresses: <platter, cylinder, sector>		