1. Chip Modelling (O1)

The design process begins with a high-level abstraction of the chip's functionality. This stage is focused on defining the chip's specifications and behavior.

Specs (C model): The chip's specifications are defined and modeled in a high-level programming language, such as C. This model serves as the golden reference for the design.

Testbench: A testbench, also written in C, is created to verify the functionality of the C model. It simulates the chip's environment and checks if the model behaves as expected.

2. RTL Architecture (O2)

This phase translates the high-level C model into a detailed hardware description.

Soft copy of the Hardware using RTL (Verilog): The C model is converted into Register Transfer Level (RTL) code, typically using a Hardware Description Language (HDL) like Verilog.

This RTL code describes the flow of data between hardware registers and the logical operations performed on that data.

SoC Design Flow: At this stage, the design is broken down into its core components:

Processor: The central processing unit of the SoC.

Peripherals/IPs: Pre-designed, reusable blocks of logic (Intellectual Property) that provide specific functions, such as USB controllers, memory interfaces, or graphics processors.

3. Synthesis and RTL2GDSII (O3)

In this final stage, the RTL code is synthesized and integrated to create a physical layout ready for fabrication.

Synthesis: The RTL code is converted into a physical representation, called a Gate Level Netlist. This netlist describes the design using a library of standard logic gates.

Gate Level Netlist (synth p1): A list of logic gates and their interconnections.

Macros (synth RTL): These are pre-designed hard blocks, often including memory or other complex functions, which are synthesized separately.

Analog IPs (func RTL): These are analog components, like phase-locked loops (PLLs) or data converters, which are not synthesized from RTL and are integrated as pre-designed functional blocks.

SoC Integration: The various components—the gate-level netlist, macros, and analog IPs—are assembled into a complete SoC. The General Purpose Input/Outputs (GPIOs) are also integrated at this stage.

Physical Design: The final physical layout is created. This includes:

Floorplanning: Arranging the major functional blocks on the chip's surface.

Placement: Placing the individual logic gates and components.

CTS (Clock Tree Synthesis): Creating a network to distribute the clock signal evenly across the chip.

Routing: Drawing the physical wires that connect the components.

DRC/LVS checks: Before fabrication, the final layout, in GDSII format, undergoes rigorous checks to ensure it complies with the foundry's design rules (Design Rule Check) and that the layout matches the original schematic (Layout Versus Schematic).